Contents

1 Electrical data

1.1 Maximum rating

Table 1. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{DS}	Continuous Drain-Source Voltage (T_J = 25 to 125°C)	–0.3 to 700	V
I_D	Maximum Current	Internally limited	A
V_{DD}	Supply Voltage	0 to 15	V
V_{OSC}	Voltage Range Input	0 to V_{DD}	V
V_{COMP}	Voltage Range Input	0 to 5	V
I_{COMP}	Maximum Continuous Current	±2	mA
V_{ESD}	Electrostatic Discharge (R = 1.5kΩ; C = 100pF)	4000	V
$I_{D(AR)}$	Avalanche Drain-Source Current, Repetitive or Not Repetitive (T_C = 100°C; Pulse width limited by T_J max; δ < 1%)	0.4	A
P_{TOT}	Power Dissipation at T_C= 25ºC	57	W
T_J	Junction Operating Temperature	Internally limited	°C
T_{STG}	Storage Temperature	-65 to 150	°C

1.2 Electrical characteristics

T_J = 25°C; V_{DD} = 13V, unless otherwise specified

Table 2. Power section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
BV_{DS}	Drain-Source Voltage	I_D = 1mA; V_{COMP} = 0V	700			V
I_{DSS}	Off-State Drain Current	V_{COMP} = 0V; T_j = 125°C V_{DS} = 700V			1.0	mA
$R_{DS(on)}$	Static Drain-Source On Resistance	I_D = 0.4A I_D = 0.4A; T_J= 100°C		15.5	18 32	Ω Ω
t_f	Fall Time	I_D = 0.2A; V_{IN} =300V (1) *Figure 7*		100		ns
t_r	Rise Time	I_D = 0.4A; V_{IN} = 300V (1) *Figure 7*		50		ns
C_{oss}	Output Capacitance	V_{DS} = 25V		90		pF

(1) On Inductive Load, Clamped.

Table 3. Supply section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{DDch}	Start-Up Charging Current	V_{DD} = 5V; V_{DS} = 35V *Figure 6*, *Figure 11*		-2		mA
I_{DD0}	Operating Supply Current	V_{DD} = 12V; F_{SW} = 0kHz *Figure 6*		12	16	mA
I_{DD1}	Operating Supply Current	V_{DD} = 12V; F_{sw} = 100kHz		13		mA
I_{DD2}	Operating Supply Current	V_{DD} = 12V; F_{sw} = 200kHz		14		mA
V_{DDoff}	Undervoltage Shutdown	*Figure 6*	7.5	8	9	V
V_{DDon}	Undervoltage Reset	*Figure 6*		11	12	V
V_{DDhyst}	Hysteresis Start-up	*Figure 6*	2.4	3		V

Table 4. Oscillator section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{SW}	Oscillator Frequency Total Variation	R_T=8.2KΩ; C_T=2.4nF V_{DD}=9 to 15V; with R_T± 1%; C_T± 5% (see Figure)(see Figure 14)	90	100	110	KHz
V_{OSCIH}	Oscillator Peak Voltage			7.1		V
V_{OSCIL}	Oscillator Valley Voltage			3.7		V

Table 5. Error amplifier section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DDREG}	V_{DD} Regulation Point	I_{COMP}=0mA (see Figure 5)	12.6	13	13.4	V
ΔV_{DDreg}	Total Variation	T_J = 0 to 100°C		2		%
G_{BW}	Unity Gain Bandwidth	From Input =V_{DD} to Output = V_{COMP} COMP pin is open *Figure 15*		150		KHz
A_{VOL}	Open Loop Voltage Gain	COMP pin is open *Figure 15*	45	52		dB
G_m	DC Transconductance	V_{COMP}=2.5V(see Figure 5)	1.1	1.5	1.9	mA/V
V_{COMPLO}	Output Low Level	I_{COMP}=-400µA; V_{DD}=14V		0.2		V
V_{COMPHI}	Output High Level	I_{COMP}=400µA; V_{DD}=12V		4.5		V
I_{COMPLO}	Output Low Current Capability	V_{COMP}=2.5V; V_{DD}=14V		-600		µA
I_{COMPHI}	Output High Current Capability	V_{COMP}=2.5V; V_{DD}=12V		600		µA

Table 6. PWM comparator section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
H_{ID}	ΔV_{COMP} / ΔI_{DPEAK}	V_{COMP} = 1 to 3 V	4.2	6	7.8	V/A
$V_{COMPoff}$	V_{COMP} Offset	I_{DPEAK} = 10mA		0.5		V
I_{Dpeak}	Peak Current Limitation	V_{DD} = 12V; COMP pin open	0.5	0.67	0.9	A
t_d	Current Sense Delay to Turn-Off	I_D = 1A		250		ns
t_b	Blanking Time			250	360	ns
$t_{on(min)}$	Minimum On Time			350	1200	ns

Table 7. Shutdown and overtemperature section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{COMPth}	Restart Threshold	(see Figure 8)		0.5		V
t_{DISsu}	Disable Set Up Time	(see Figure 8)		1.7	5	µs
T_{tsd}	Thermal Shutdown Temperature	(see Figure 8)	140	170	190	°C
T_{hyst}	Thermal Shutdown Hysteresis	(see Figure 8)		40		°C

2 Thermal data

Table 8. Thermal data

Symbol	Parameter		PENTAWATT	PowerSO-10™(1)	DIP-8	Unit
R_{thJA}	Thermal Resistance Junction-pin	Max			20	°C/W
R_{thJC}	Thermal Resistance Junction-case	Max	2.0	2.0		°C/W
R_{thJC}	Thermal Resistance Ambient-case	Max	70	60	35 (2)	°C/W

1. When mounted using the minimum recommended pad size on FR-4 board.
2. On multylayer PCB.

3 Pin description

3.1 Drain pin (Integrated Power MOSFET drain):

Integrated Power MOSFET drain pin. It provides internal bias current during start-up via an integrated high voltage current source which is switched off during normal operation. The device is able to handle an unclamped current during its normal operation, assuring self protection against voltage surges, PCB stray inductance, and allowing a snubberless operation for low output power.

3.2 Source pin:

Power MOSFET source pin. Primary side circuit common ground connection.

3.3 V_{DD} pin (power supply):

This pin provides two functions :

- It corresponds to the low voltage supply of the control part of the circuit. If V_{DD} goes below 8V, the start-up current source is activated and the output power MOSFET is switched off until the V_{DD} voltage reaches 11V. During this phase, the internal current consumption is reduced, the V_{DD} pin is sourcing a current of about 2mA and the COMP pin is shorted to ground. After that, the current source is shut down, and the device tries to start up by switching again.
- This pin is also connected to the error amplifier, in order to allow primary as well as secondary regulation configurations. In case of primary regulation, an internal 13V trimmed reference voltage is used to maintain V_{DD} at 13V. For secondary regulation, a voltage between 8.5V and 12.5V will be put on V_{DD} pin by transformer design, in order to stuck the output of the transconductance amplifier to the high state. The COMP pin behaves as a constant current source, and can easily be connected to the output of an optocoupler. Note that any overvoltage due to regulation loop failure is still detected by the error amplifier through the V_{DD} voltage, which cannot overpass 13V. The output voltage will be somewhat higher than the nominal one, but still under control.

3.4 Compensation pin

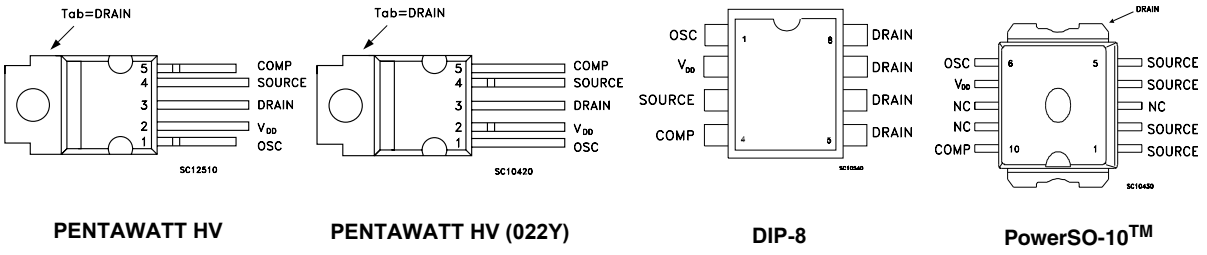
This pin provides two functions :

- It is the output of the error transconductance amplifier, and allows for the connection of a compensation network to provide the desired transfer function of the regulation loop. Its bandwidth can be easily adjusted to the needed value with usual components value. As stated above, secondary regulation configurations are also implemented through the COMP pin.
- When the COMP voltage is going below 0.5V, the shut-down of the circuit occurs, with a zero duty cycle for the power MOSFET. This feature can be used to switch off the converter, and is automatically activated by the regulation loop (no matter what the configuration is) to provide a burst mode operation in case of negligible output power or open load condition.

3.5 OSC pin (oscillator frequency):

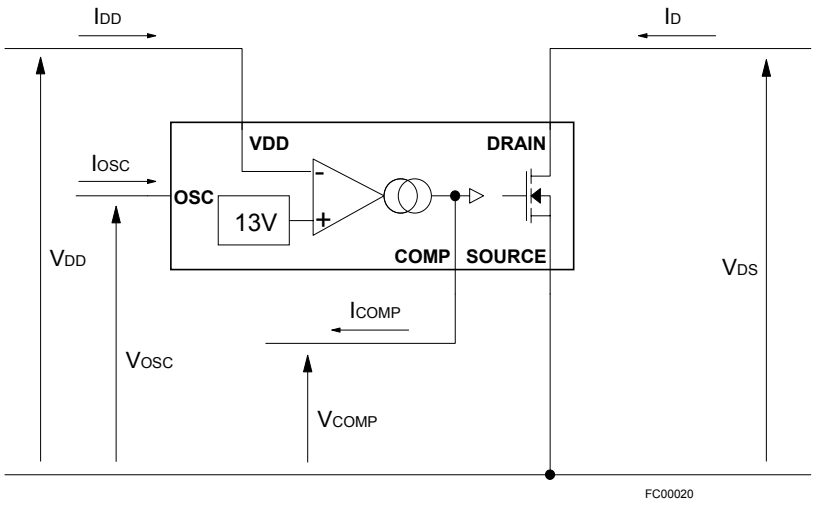
An R_t-C_t network must be connected on that to define the switching frequency. Note that despite the connection of R_t to V_{DD}, no significant frequency change occurs for V_{DD} varying from 8V to 15V. It provides also a synchronisation capability, when connected to an external frequency source.

Figure 1. Connection diagrams (top view)



PENTAWATT HV | PENTAWATT HV (022Y) | DIP-8 | PowerSO-10™

Figure 2. Current and voltage convention



4 Typical circuit

Figure 3. Offline power supply with auxiliary supply feedback

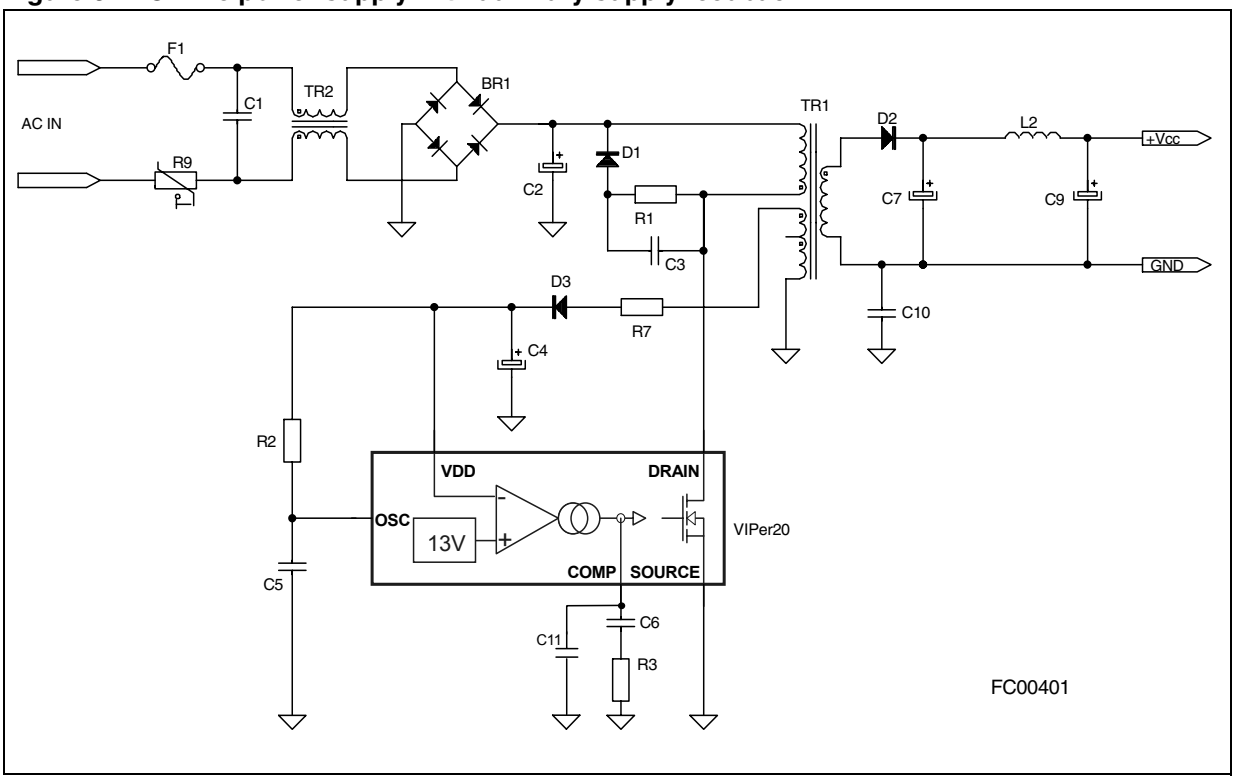
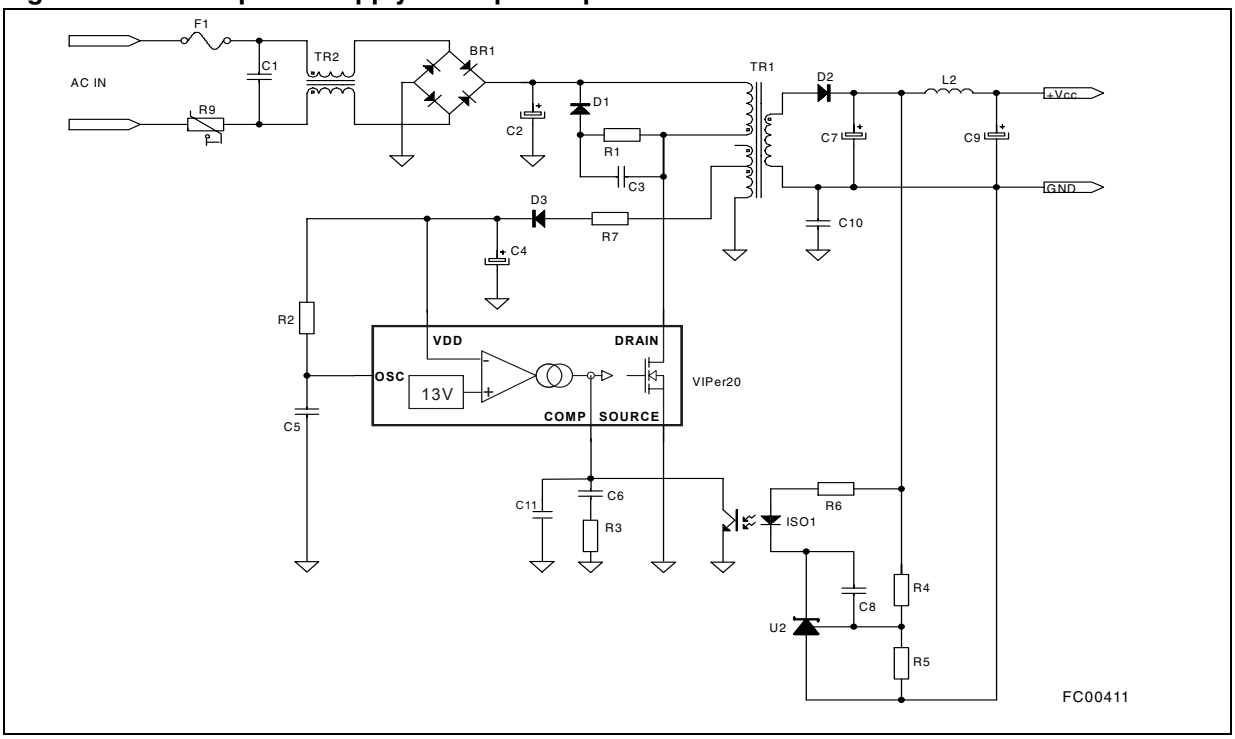


Figure 4. Offline power supply with optocoupler feedback



5 Operation description

5.1 Current mode topology:

The current mode control method, like the one integrated in the devices, uses two control loops - an inner current control loop and an outer loop for voltage control. When the Power MOSFET output transistor is on, the inductor current (primary side of the transformer) is monitored with a SenseFET technique and converted into a voltage V_S proportional to this current. When V_S reaches V_{COMP} (the amplified output voltage error) the power switch is switched off. Thus, the outer voltage control loop defines the level at which the inner loop regulates peak current through the power switch and the primary winding of the transformer.

Excellent open loop D.C. and dynamic line regulation is ensured due to the inherent input voltage feedforward characteristic of the current mode control. This results in improved line regulation, instantaneous correction to line changes, and better stability for the voltage regulation loop.

Current mode topology also ensures good limitation in case there is a short circuit. During the first phase the output current increases slowly following the dynamic of the regulation loop. Then it reaches the maximum limitation current internally set and finally stops because the power supply on V_{DD} is no longer correct. For specific applications the maximum peak current internally set can be overridden by externally limiting the voltage excursion on the COMP pin. An integrated blanking filter inhibits the PWM comparator output for a short time after the integrated Power MOSFET is switched on. This function prevents anomalous or premature termination of the switching pulse in case there are current spikes caused by primary side capacitance or secondary side rectifier reverse recovery time.

5.2 Stand-by mode

Stand-by operation in nearly open load conditions automatically leads to a burst mode operation allowing voltage regulation on the secondary side. The transition from normal operation to burst mode operation happens for a power P_{STBY} given by :

Where: $$P_{STBY} = \frac{1}{2} L_P I^2 STBY F_{SW}$$

L_P is the primary inductance of the transformer. F_{SW} is the normal switching frequency.

I_{STBY} is the minimum controllable current, corresponding to the minimum on time that the device is able to provide in normal operation. This current can be computed as :

$$I_{STBY} = \frac{(t_b + t_d) V_{IN}}{L_p}$$

$t_b + t_d$ is the sum of the blanking time and of the propagation time of the internal current sense and comparator, and represents roughly the minimum on time of the device. Note: that P_{STBY} may be affected by the efficiency of the converter at low load, and must include the power drawn on the primary auxiliary voltage.

As soon as the power goes below this limit, the auxiliary secondary voltage starts to increase above the 13V regulation level, forcing the output voltage of the transconductance amplifier to low state ($V_{COMP} < V_{COMPth}$). This situation leads to the shutdown mode where the power switch is maintained in the Off state, resulting in missing cycles and zero duty cycle. As soon as V_{DD} gets back to the regulation level and the V_{COMPth} threshold is reached, the device operates again. The above cycle repeats indefinitely, providing a burst mode of which the effective duty cycle is much lower than the minimum one when in normal operation. The equivalent switching frequency is also lower than the normal one, leading to a reduced consumption on the input main supply lines. This mode of operation allows the VIPer20A-E to meet the new German "Blue Angel" Norm with less than 1W total power consumption for the system when working in stand-by mode. The output voltage remains regulated around the normal level, with a low frequency ripple corresponding to the burst mode. The amplitude of this ripple is low, because of the output capacitors and low output current drawn in such conditions.The normal operation resumes automatically when the power gets back to higher levels than P_{STBY}.

5.3 High voltage start-up current suorce

An integrated high voltage current source provides a bias current from the DRAIN pin during the start-up phase. This current is partially absorbed by internal control circuits which are placed into a standby mode with reduced consumption and also provided to the external capacitor connected to the V_{DD} pin. As soon as the voltage on this pin reaches the high voltage threshold V_{DDon} of the UVLO logic, the device becomes active mode and starts switching. The start-up current generator is switched off, and the converter should normally provide the needed current on the V_{DD} pin through the auxiliary winding of the transformer, as shown on (see Figure 11).

In case there are abnormal conditions where the auxiliary winding is unable to provide the low voltage supply current to the V_{DD} pin (i.e. short circuit on the output of the converter), the external capacitor discharges to the low threshold voltage V_{DDoff} of the UVLO logic, and the device goes back to the inactive state where the internal circuits are in standby mode and the start-up current source is activated. The converter enters a endless start-up cycle, with a start-up duty cycle defined by the ratio of charging current towards discharging when the VIPer20-E tries to start. This ratio is fixed by design to 2A to 15A, which gives a 12% start-up duty cycle while the power dissipation at start-up is approximately 0.6W, for a 230Vrms input voltage.

This low value start-up duty cycle prevents the application of stress to the output rectifiers as well as the transformer when a short circuit occurs.

The external capacitor C_{VDD} on the V_{DD} pin must be sized according to the time needed by the converter to start up, when the device starts switching. This time t_{SS} depends on many parameters, among which transformer design, output capacitors, soft start feature, and compensation network implemented on the COMP pin. The following formula can be used for defining the minimum capacitor needed:

where: $$C_{VDD} > \frac{I_{DD} t_{SS}}{V_{DDhyst}}$$

I_{DD} is the consumption current on the V_{DD} pin when switching. Refer to specified I_{DD1} and $I_{DD}2$ values.

t_{SS} is the start up time of the converter when the device begins to switch. Worst case is generally at full load.

V_{DDhyst} is the voltage hysteresis of the UVLO logic (refer to the minimum specified value).

The soft start feature can be implemented on the COMP pin through a simple capacitor which will be also used as the compensation network. In this case, the regulation loop bandwidth is rather low, because of the large value of this capacitor. In case a large regulation loop bandwidth is mandatory, the schematics of (see Figure 17) can be used. It mixes a high performance compensation network together with a separate high value soft start capacitor. Both soft start time and regulation loop bandwidth can be adjusted separately.

If the device is intentionally shut down by tying the COMP pin to ground, the device is also performing start-up cycles, and the V_{DD} voltage is oscillating between V_{DDon} and V_{DDoff}.

This voltage can be used for supplying external functions, provided that their consumption does not exceed 0.5mA. (see Figure 18) shows a typical application of this function, with a latched shutdown. Once the "Shutdown" signal has been activated, the device remains in the Off state until the input voltage is removed.

5.4 Transconductance error amplifier

The VIPer20A-E includes a transconductance error amplifier. Transconductance Gm is the change in output current (I_{COMP}) versus change in input voltage (V_{DD}). Thus:

$$G_m = \frac{\partial I_{COMP}}{\partial V_{DD}}$$

The output impedance Z_{COMP} at the output of this amplifier (COMP pin) can be defined as:

$$Z_{COMP} = \frac{\partial V_{COMP}}{\partial I_{COMP}} = \frac{1}{G_m} \times \frac{\partial V_{COMP}}{\partial V_{DD}}$$

This last equation shows that the open loop gain A_{VOL} can be related to G_m and Z_{COMP}:

$A_{VOL} = G_m \times Z_{COMP}$

where G_m value for VIPer20A-E is 1.5 mA/V typically.

G_m is defined by specification, but Z_{COMP} and therefore A_{VOL} are subject to large tolerances. An impedance Z can be connected between the COMP pin and ground in order to define the transfer function F of the error amplifier more accurately, according to the following equation (very similar to the one above):

$F_{(S)} = Gm \times Z(S)$

The error amplifier frequency response is reported in for different values of a simple resistance connected on the COMP pin. The unloaded transconductance error amplifier shows an internal Z_{COMP} of about 330KΩ More complex impedance can be connected on the COMP pin to achieve different compensation level. A capacitor will provide an integrator function, thus eliminating the DC static error, and a resistance in series leads to a flat gain at higher frequency, insuring a correct phase margin. This configuration is illustrated in *Figure 20*

As shown in *Figure 19* an additional noise filtering capacitor of 2.2nF is generally needed to avoid any high frequency interference.

Is also possible to implement a slope compensation when working in continuous mode with duty cycle higher than 50%. *Figure 21* shows such a configuration. Note: R1 and C2 build the classical compensation network, and Q1 is injecting the slope compensation with the correct polarity from the oscillator sawtooth.

5.5 External clock synchronization:

The OSC pin provides a synchronisation capability when connected to an external frequency source. *Figure 21* shows one possible schematic to be adapted, depending the specific needs. If the proposed schematic is used, the pulse duration must be kept at a low value (500ns is sufficient) for minimizing consumption. The optocoupler must be able to provide 20mA through the optotransistor.

5.6 Primary peak current limitation

The primary I_{DPEAK} current and, consequently, the output power can be limited using the simple circuit shown in *Figure 22* . The circuit based on Q1, R_1 and R_2 clamps the voltage on the COMP pin in order to limit the primary peak current of the device to a value:

$$I_{DPEAK} = \frac{V_{COMP} - 0.5}{H_{ID}}$$

where:

$$V_{COMP} = 0.6 \times \frac{R_1 + R_2}{R_2}$$

The suggested value for R_1+R_2 is in the range of 220KΩ

5.7 Over-temperature protection

Over-temperature protection is based on chip temperature sensing. The minimum junction temperature at which over-temperature cut-out occurs is 140ºC, while the typical value is 170ºC. The device is automatically restarted when the junction temperature decreases to the restart temperature threshold that is typically 40ºC below the shutdown value (see Figure 13)

5.8 Operation pictures

Figure 5. V_{DD} Regulation point

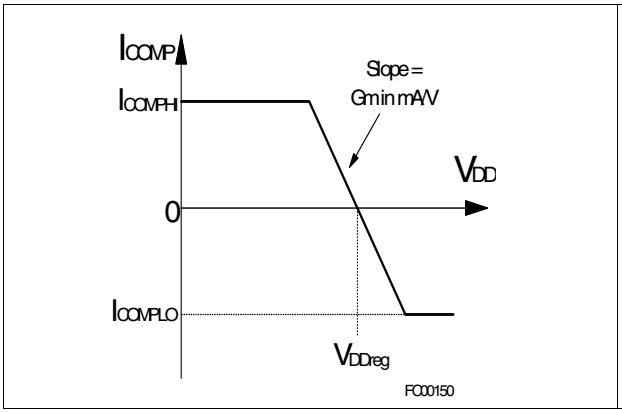


Figure 6. Undervoltage lockout

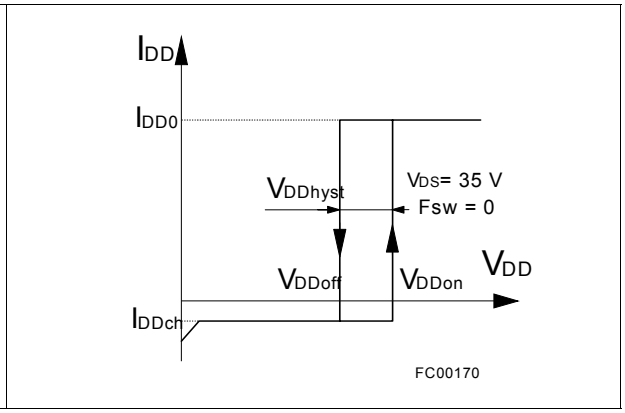


Figure 7. Transition time

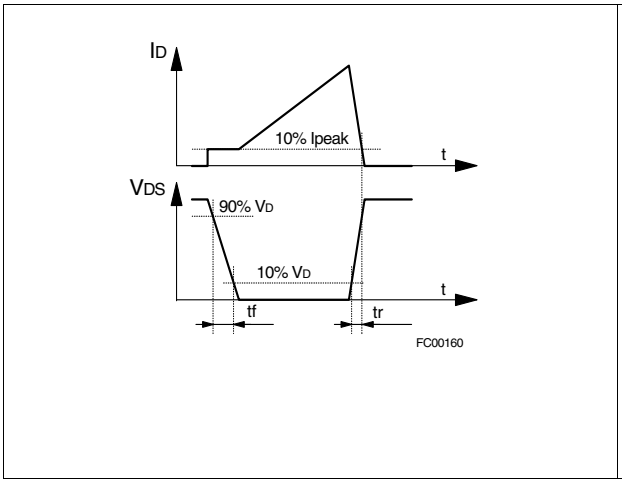


Figure 8. Shutdown action

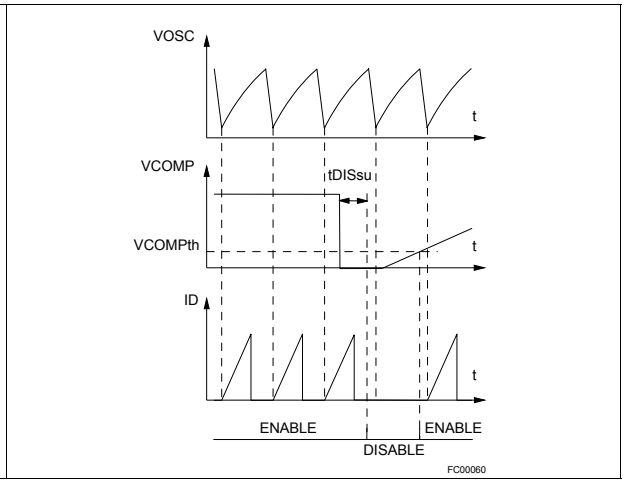


Figure 9. Breakdown voltage vs temperature

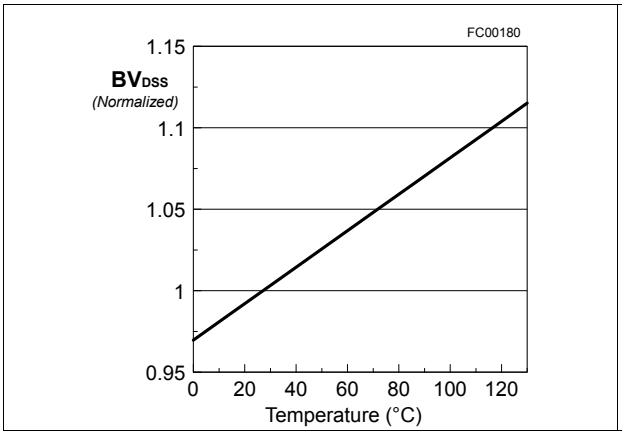


Figure 10. Typical frequency variation

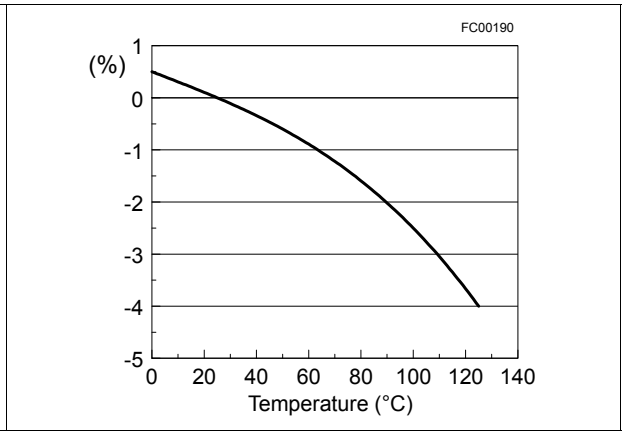


Figure 11. Behaviour of the high voltage current source at start-up

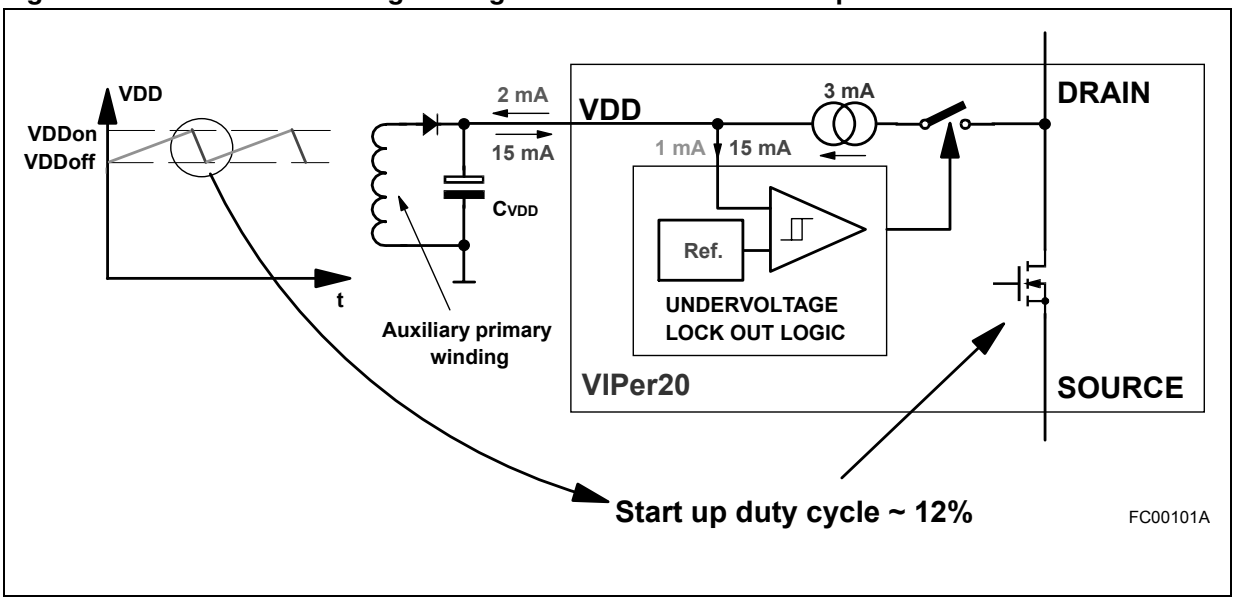


Figure 12. Start-up waveforms

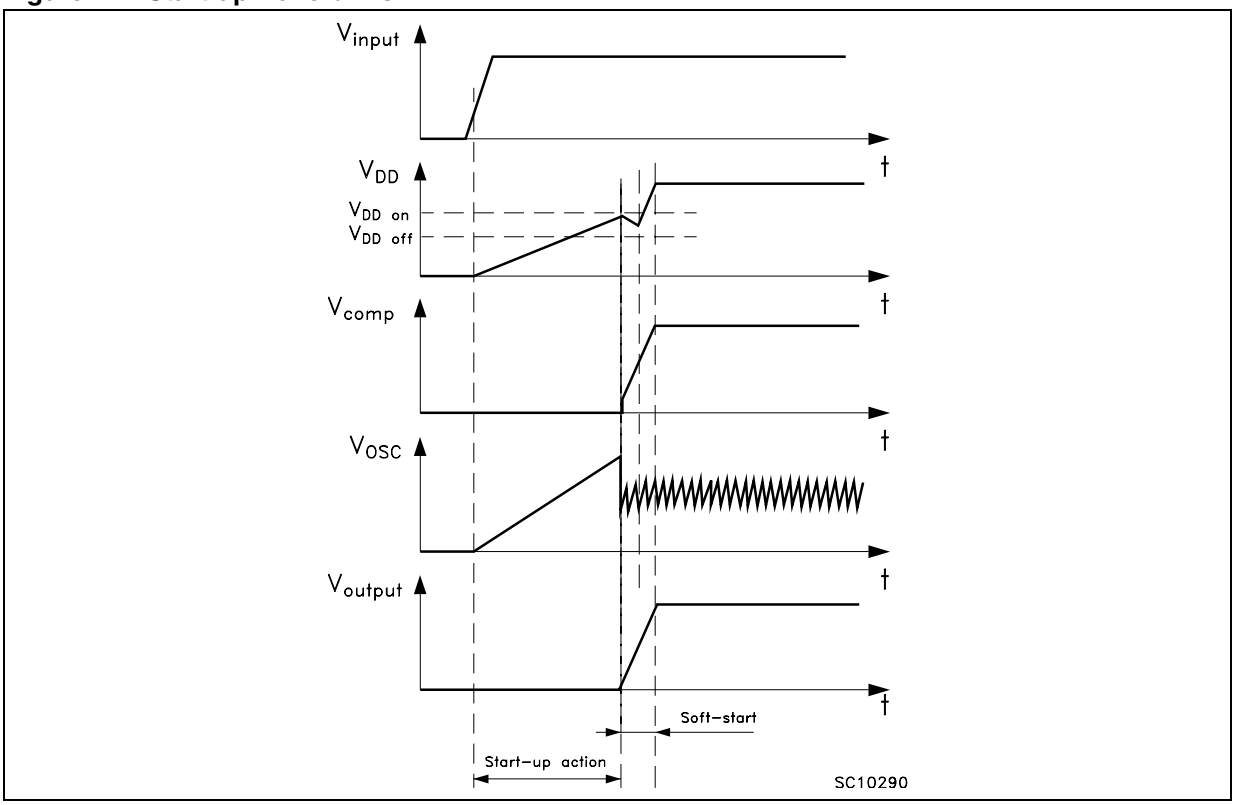


Figure 13. Over-temperature protection

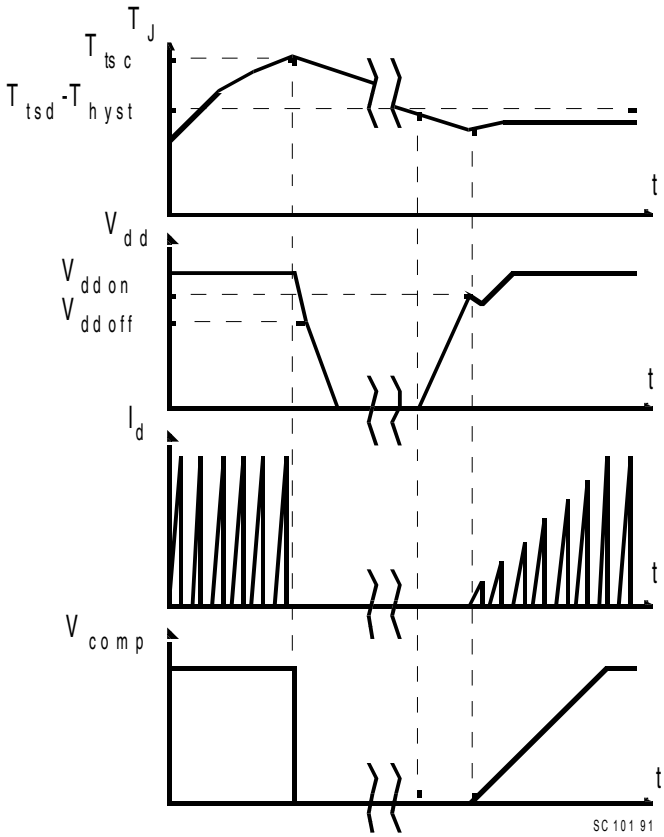
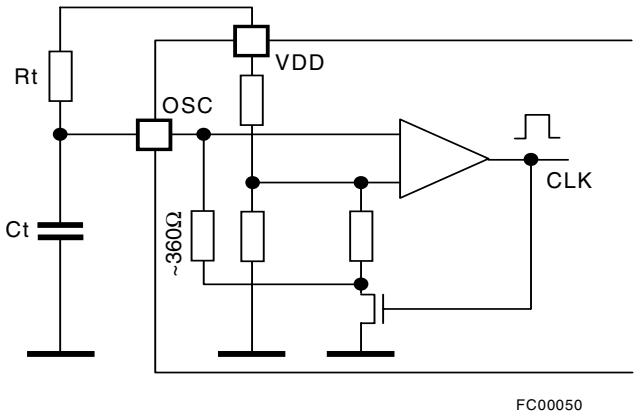
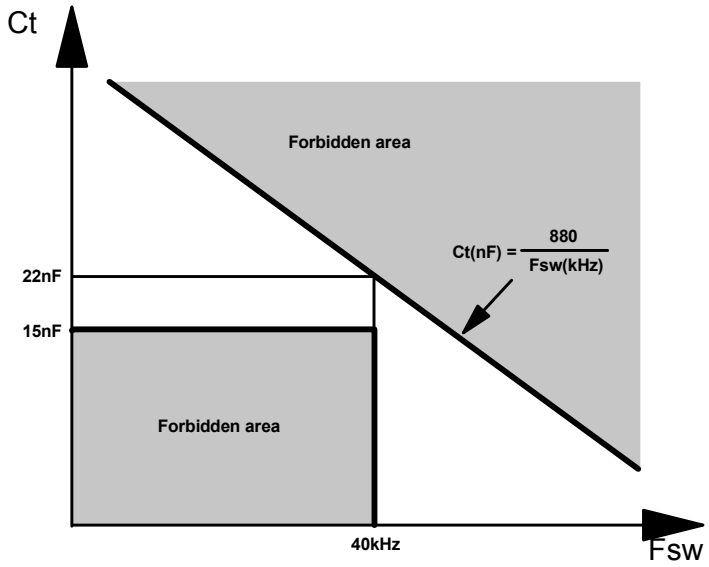


Figure 14. Oscillator



For $R_t > 1.2k\Omega$ and $C_t \leq 40KHz$

$$Fsw = \frac{2.3}{R_t \cdot C_t} \times \left(1 - \frac{550}{R_t - 150}\right)$$



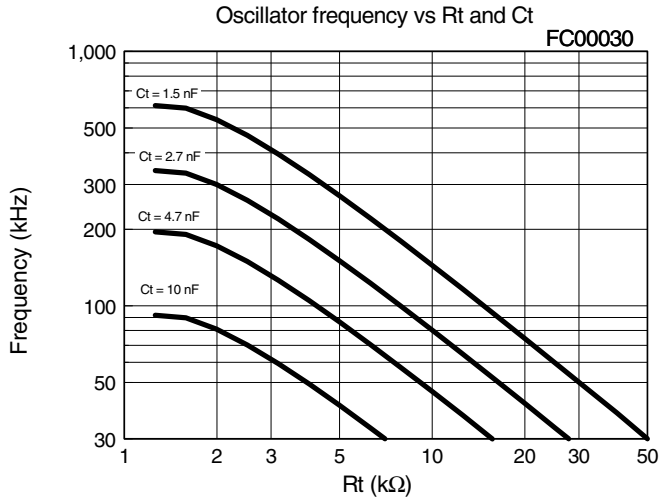


Figure 15. Error amplifier frequency response

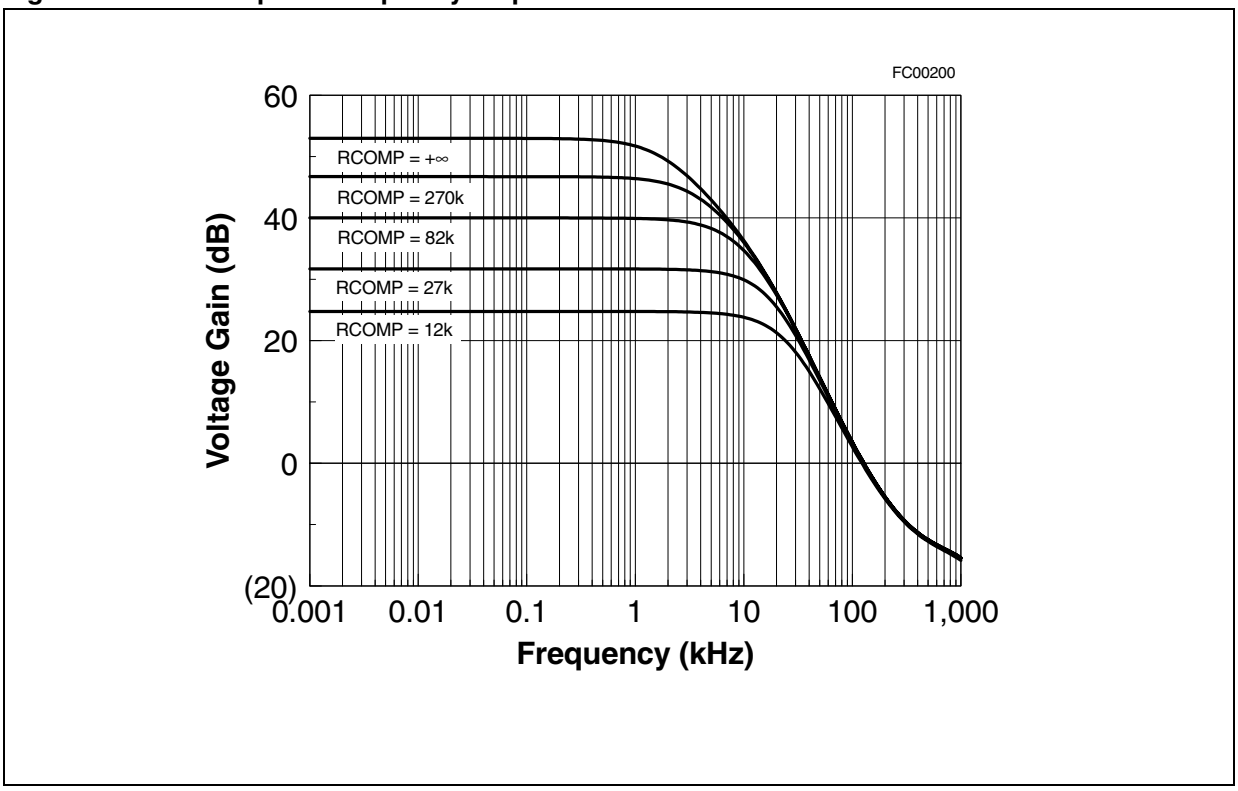


Figure 16. Error amplifier phase response

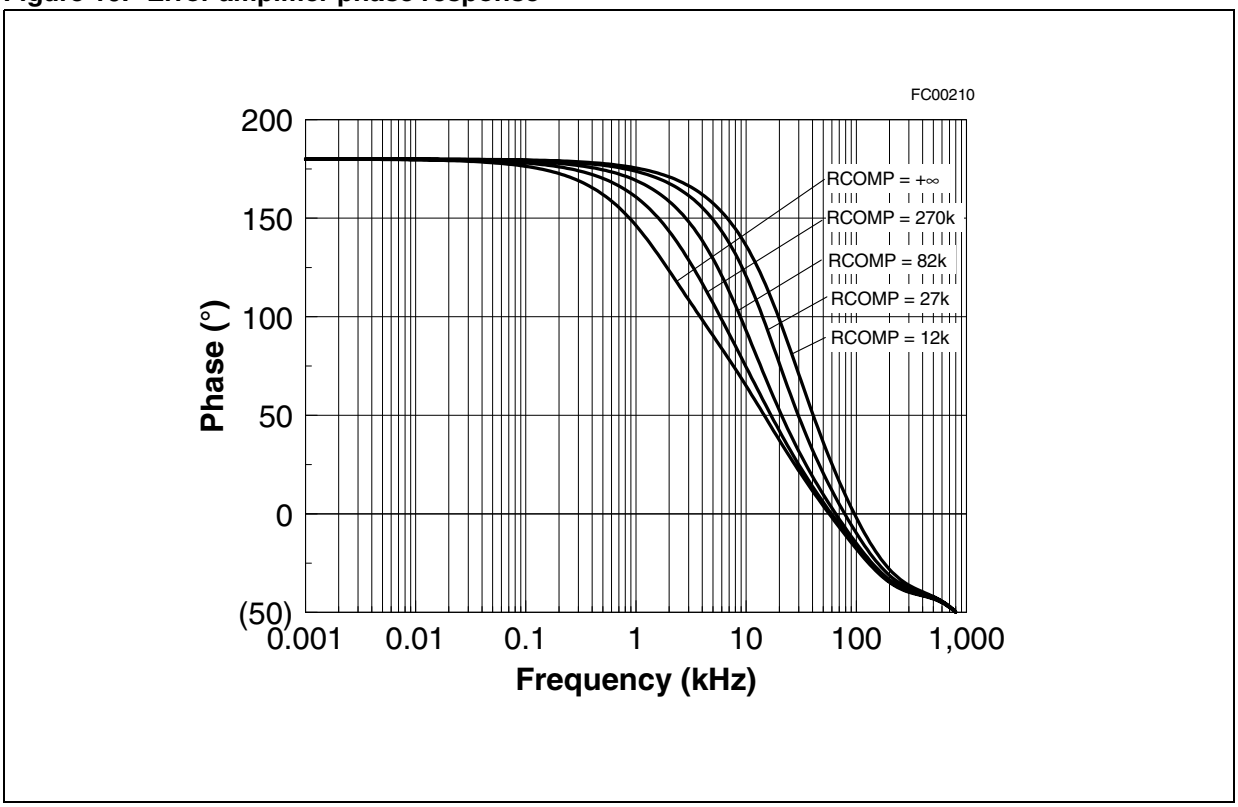


Figure 17. Mixed soft start and compensation

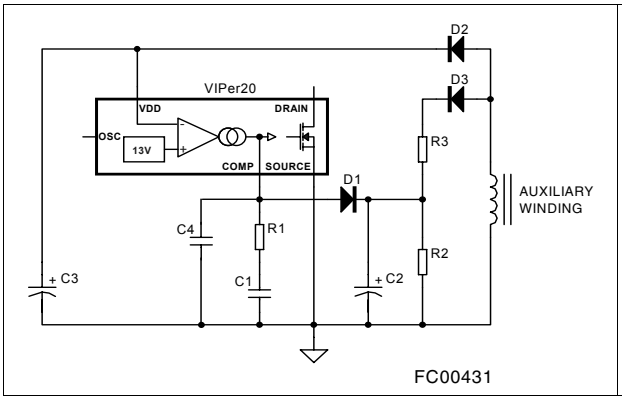


Figure 18. Latched shut down

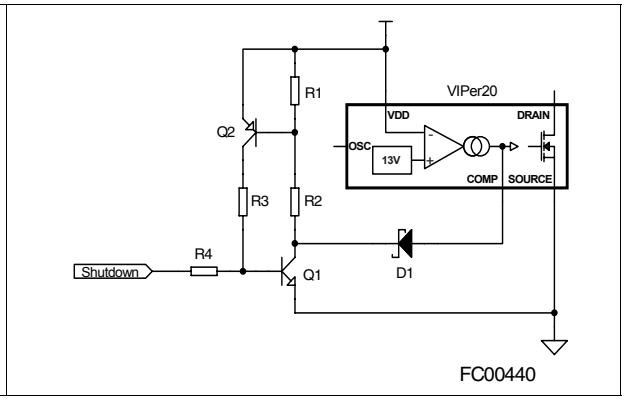


Figure 19. Typical compensation network

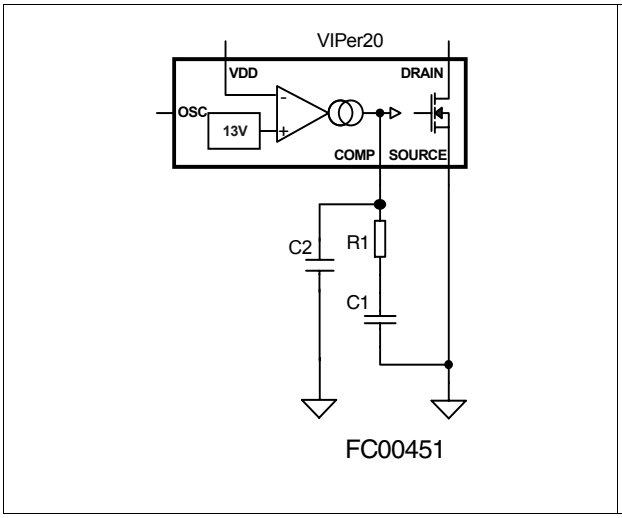


Figure 20. Slope compensation

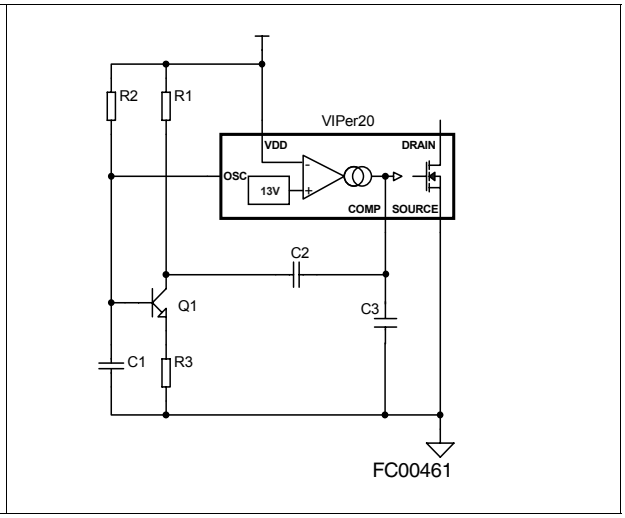


Figure 21. External clock sinchronisation

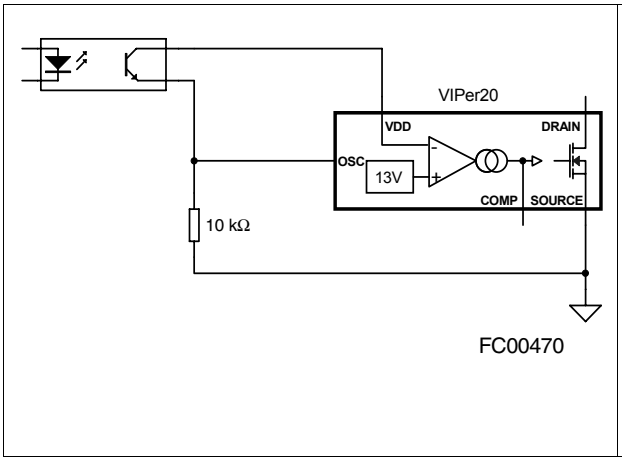
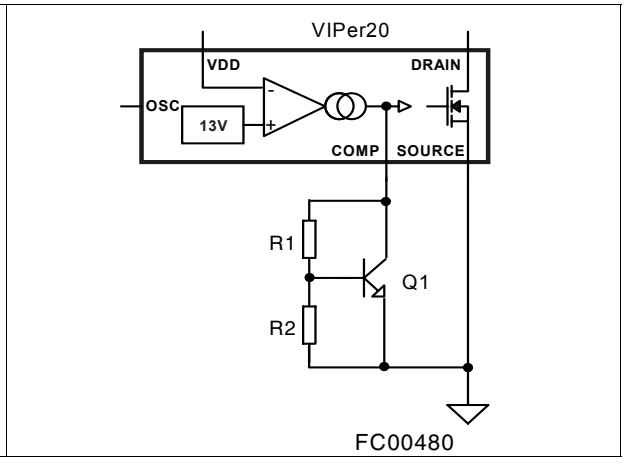


Figure 22. Current limitation circuit example

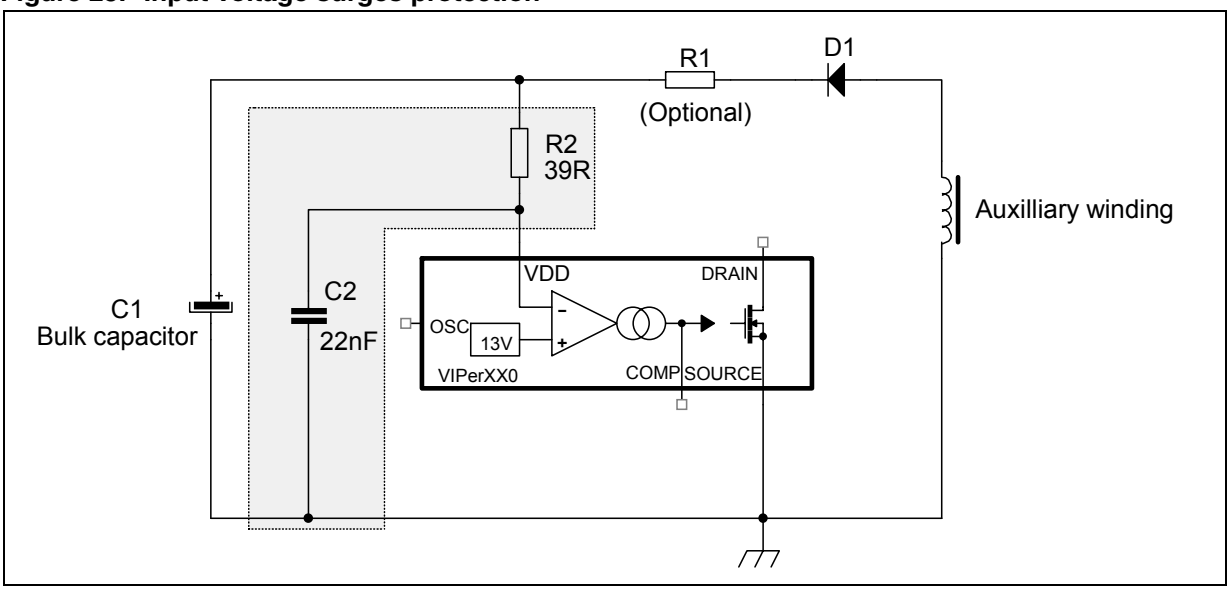


6 Electrical over stress

6.1 Electrical over stress ruggedness

The VIPer may be submitted to electrical over-stress, caused by violent input voltage surges or lightning. Following the Layout Considerations is sufficient to prevent catastrophic damages most of the time. However in some cases, the voltage surges coupled through the transformer auxiliary winding can exceed the V_{DD} pin absolute maximum rating voltage value. Such events may trigger the V_{DD} internal protection circuitry which could be damaged by the strong discharge current of the V_{DD} bulk capacitor. The simple RC filter shown in *Figure 23* can be implemented to improve the application immunity to such surges.

Figure 23. Input voltage surges protection



7 Layout

7.1 Layout considerations

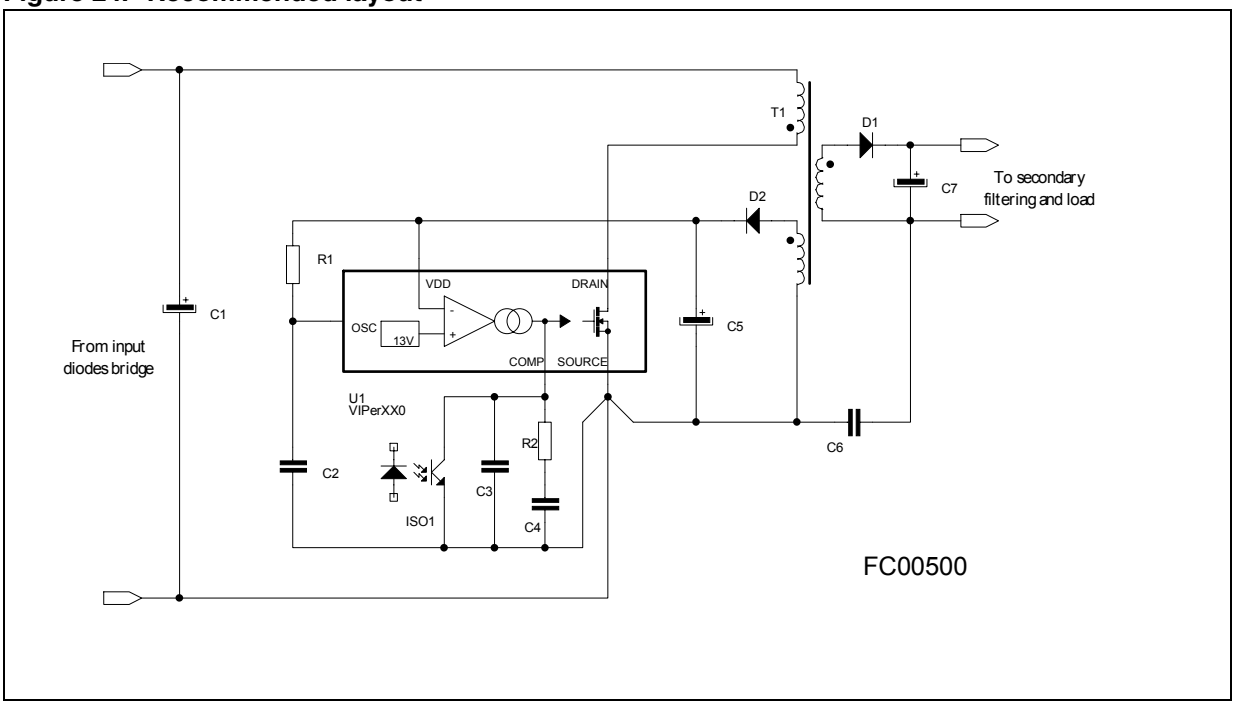
Some simple rules insure a correct running of switching power supplies. They may be classified into two categories:

- Minimizing power loops: The switched power current must be carefully analysed and the corresponding paths must be as small an inner loop area as possible. This avoids radiated EMC noises, conducted EMC noises by magnetic coupling, and provides a better efficiency by eliminating parasitic inductances, especially on secondary side.
- Using different tracks for low level and power signals: Interference due to mixing of signal and power may result in instabilities and/or anomalous behaviour of the device in case of violent power surge (Input overvoltages, output short circuits...).

In case of VIPer, these rules apply as shown on (see Figure 24).

- Loops C1-T1-U1, C5-D2-T1, and C7-D1-T1 must be minimized.
- C6 must be as close as possible to T1.
- Signal components C2, ISO1, C3, and C4 are using a dedicated track connected directly to the power source of the device.

Figure 24. Recommended layout



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 9. Pentawatt HV Mechanical data

Dim	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.30		4.80	0.169		0.189
C	1.17		1.37	0.046		0.054
D	2.40		2.80	0.094		0.11
E	0.35		0.55	0.014		0.022
F	0.60		0.80	0.024		0.031
G1	4.91		5.21	0.193		0.205
G2	7.49		7.80	0.295		0.307
H1	9.30		9.70	0.366		0.382
H2			10.40			0.409
H3	10.05		10.40		0.396	0.409
L	15.60		17.30	6.14		0.681
L1	14.60		15.22	0.575		0.599
L2	21.20		21.85	0.835		0.860
L3	22.20		22.82	0.874		0.898
L5	2.60		3	0.102		0.118
L6	15.10		15.80	0.594		0.622
L7	6		6.60	0.236		0.260
M	2.50		3.10	0.098		0.122
M1	4.50		5.60	0.177		0.220
R	0.50			0.02		
V4	90°					
Diam	3.65		3.85	0.144		0.152

Figure 25. Package dimension

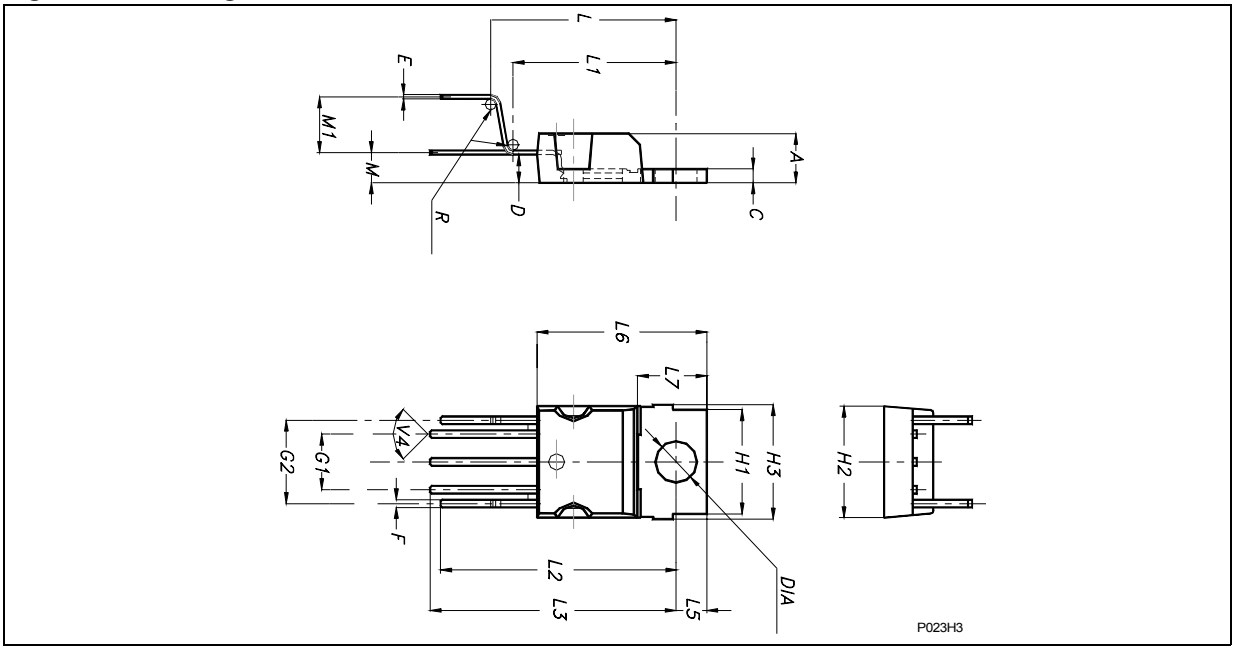


Table 10. Pentawatt HV 022Y (Vertical High Pitch) Mechanical data

Dim	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.30		4.80	0.169		0.189
C	1.17		1.37	0.046		0.054
D	2.40		2.80	0.094		0.110
E	0.35		0.55	0.014		0.022
F	0.60		0.80	0.024		0.031
G1	4.91		5.21	0.193		0.205
G2	7.49		7.80	0.295		0.307
H1	9.30		9.70	0.366		0.382
H2			10.40			0.409
H3	10.05		10.40	0.396		0.409
L	16.42		17.42	0.646		0.686
L1	14.60		15.22	0.575		0.599
L3	20.52		21.52	0.808		0.847
L5	2.60		3.00	0.102		0.118
L6	15.10		15.80	0.594		0.622
L7	6.00		6.60	0.236		0.260
M	2.50		3.10	0.098		0.122
M1	5.00		5.70	0.197		0.224
R		0.50		0.02	0.020	
V4		90°			90°	
Diam	3.65		3.85	0.144		0.154

Figure 26. Package dimension

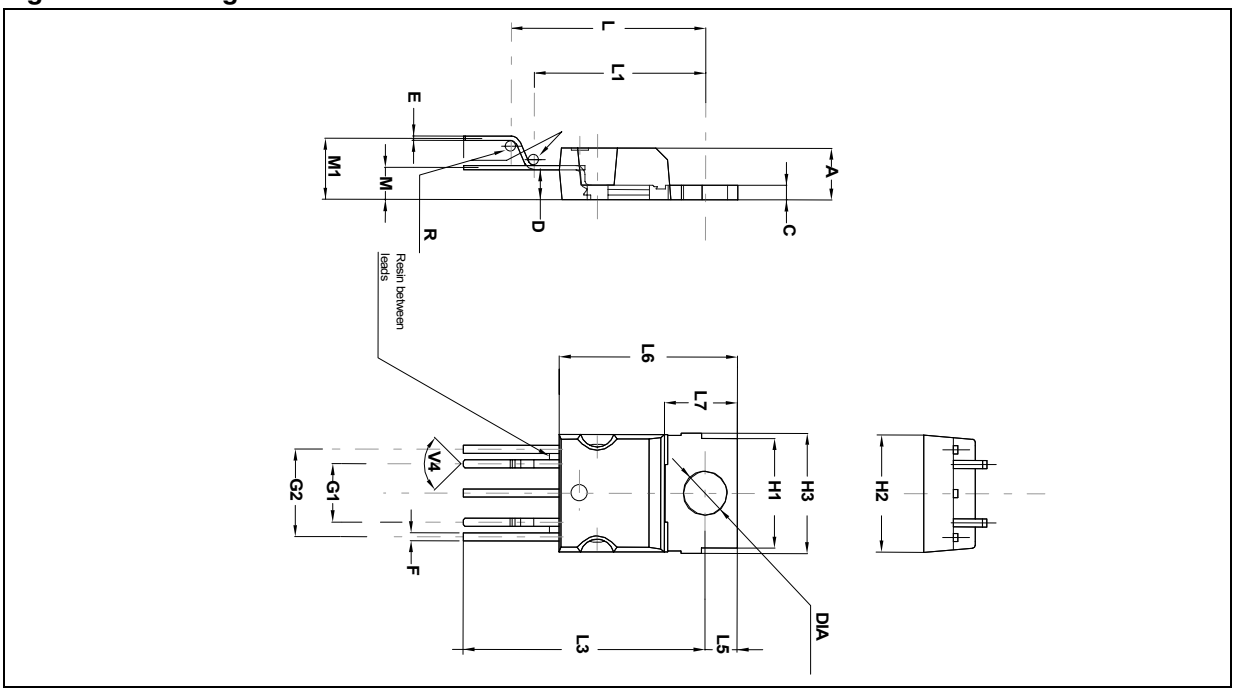


Table 11. DIP-8 Mechanical data

Dim.	mm			Inch		
	Min	Typ	Max	Min	Typ	Max
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

Figure 27. Package dimensions

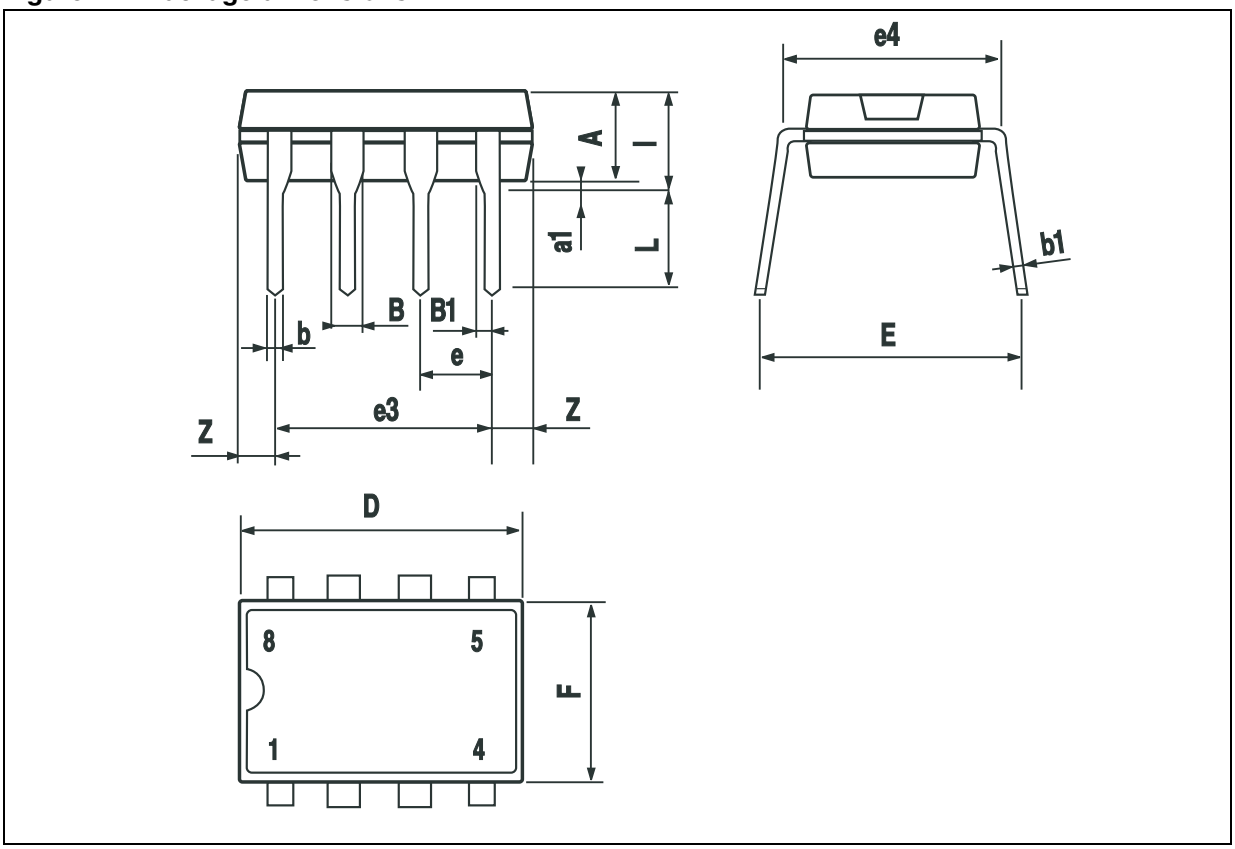


Table 12. PowerSO-10 mechanical data

Dim.	mm			Inch		
	Min	Typ	Max	Min	Typ	Max
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
C	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
e		1.27			0.050	
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
F	1.25		1.35	0.049		0.053
h		0.50			0.002	
H	13.80		14.40	0.543		0.567
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
α	0°		8°			

Figure 28. Package dimension

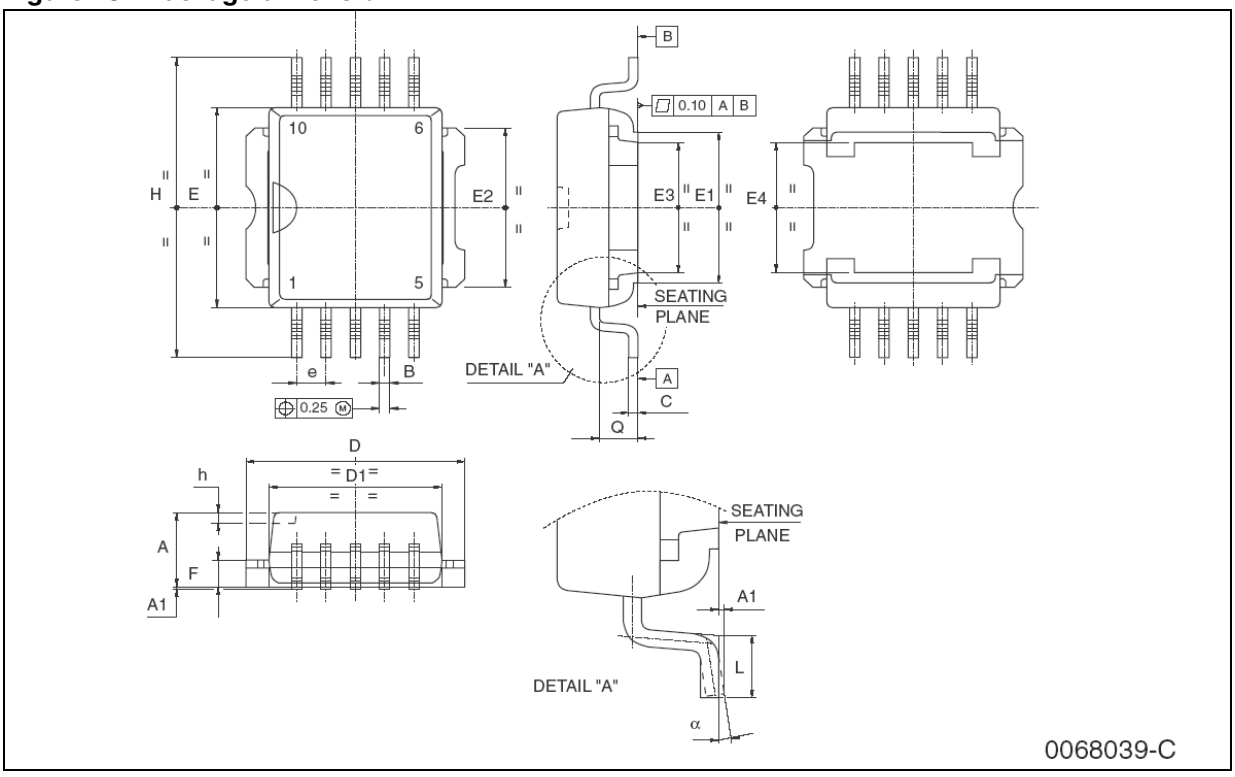


Figure 29. Power Pad layout

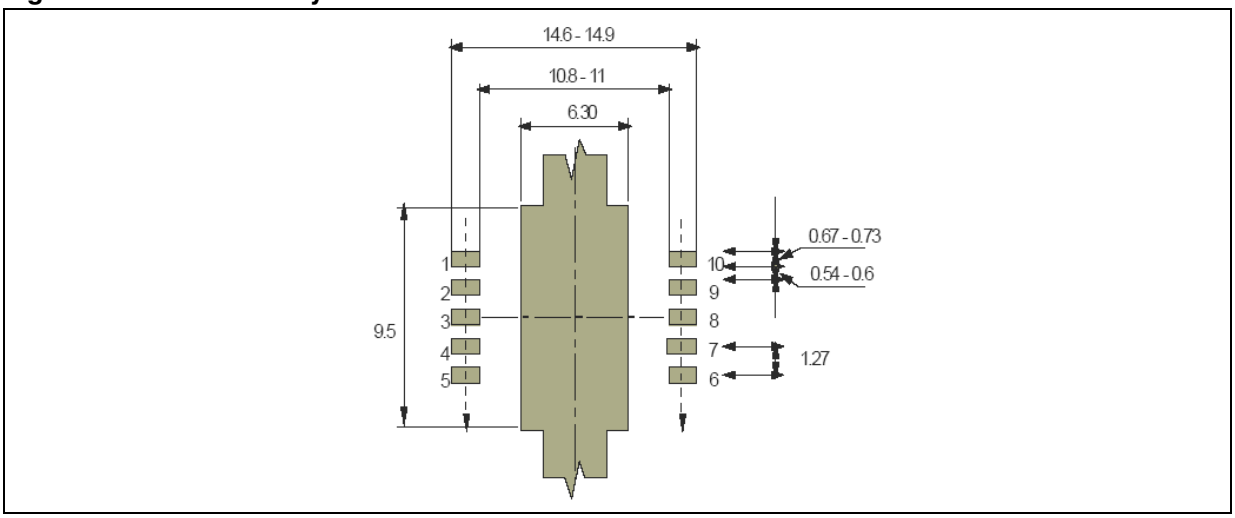


Figure 30. Tube shipment

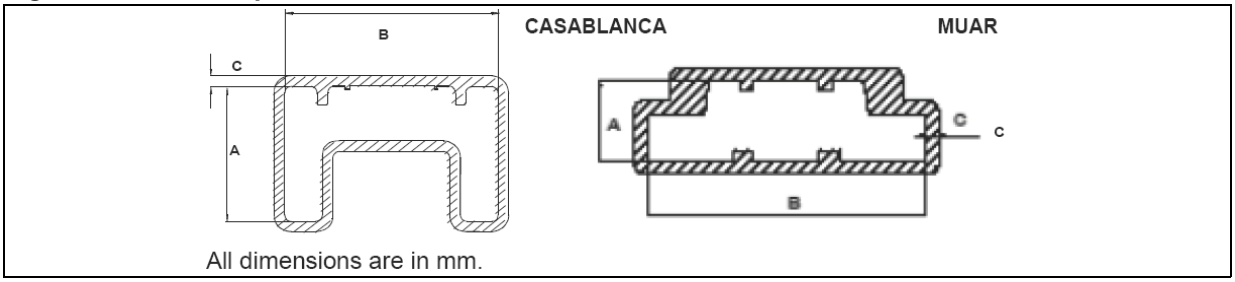


Table 13. Tube shipment

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

Figure 31. Reel shipment

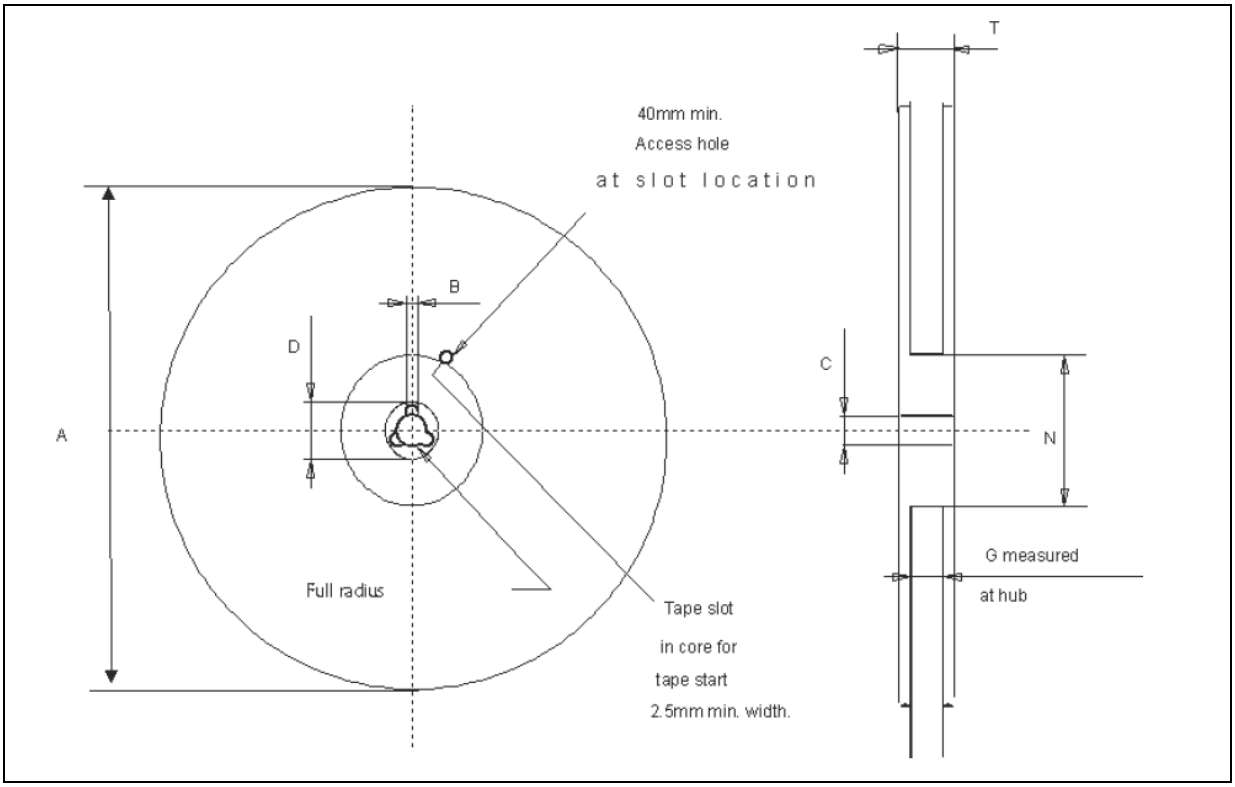


Table 14. Reel dimension

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (± 0.2)	24.4
N (min)	60
T (max)	30.4

Note: All dimensoin are in mm.

Figure 32. Tape shipment

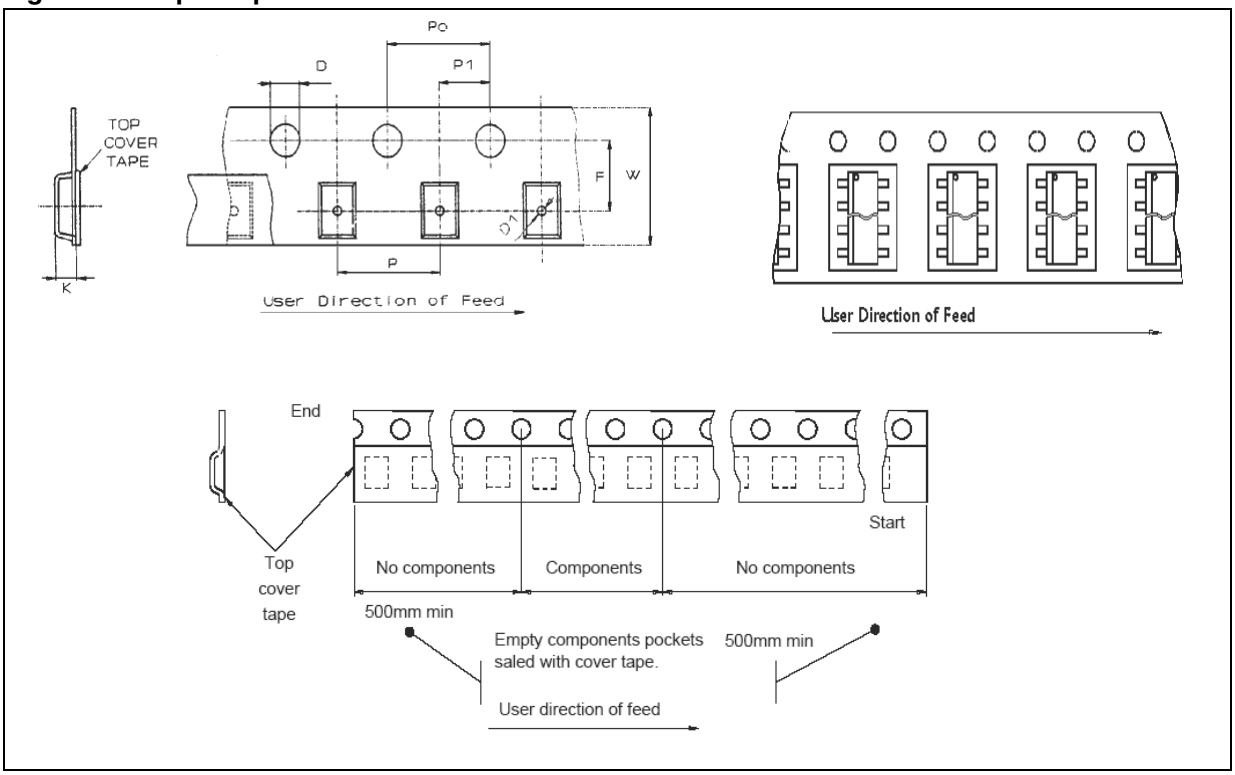


Table 15. Tape dimension

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

Note: All dimensions are in mm.

Figure 33. Pentawatt HV tube shipment (no suffix)

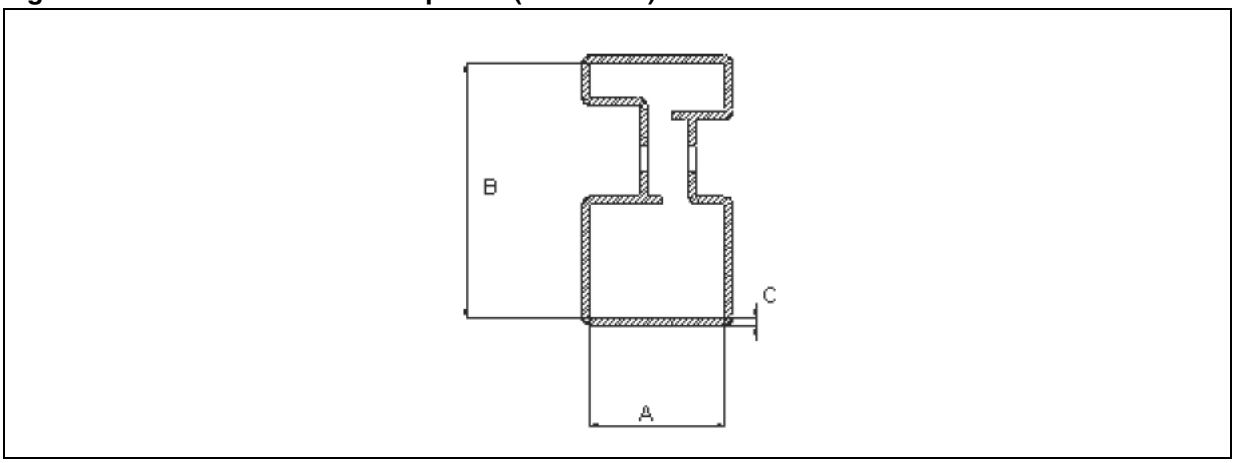


Table 16. Tube dimension

Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	18
B	33.1
C (± 0.1)	1

Note: All dimensions are in mm.

Figure 34. Dip-8 Tube shipment (no suffix)

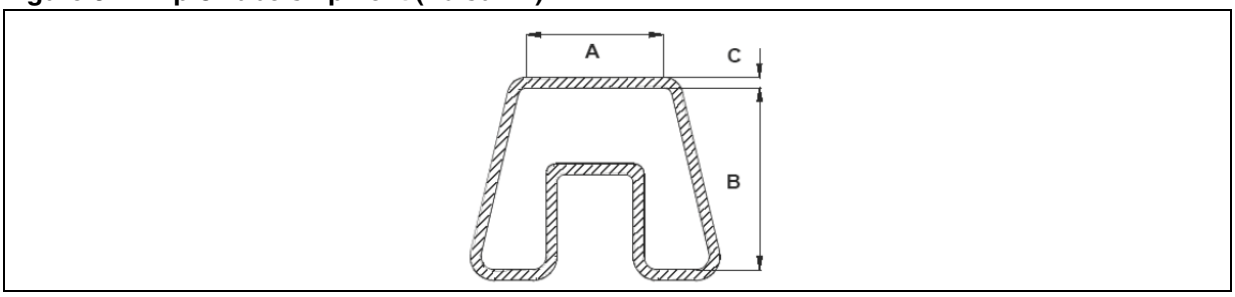


Table 17. Tube dimension

Base Q.ty	20
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	8.4
B	11.2
C (± 0.1)	0.8

Note: All dimensions are in mm.

9 Order code

Table 18. Order code

Part number	Package
VIPer20A-E	PENTAWATT HV
VIPer20A-22-E	PENTAWATT HV (022Y)
VIPer20ADIP-E	DIP-8
VIPer20ASP-E	PowerSO-10

10 Revision history

Table 19. Revision history

Date	Revision	Changes
28-Sep-2005	1	Initial release.
21-Jun-2006	2	New template, few updates

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