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# USB82514

## 1.0 INTRODUCTION

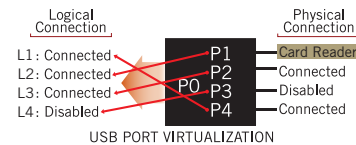
The Microchip Automotive Grade USB 2.0 4-Port Hub is a low-power, OEM configurable, MTT (Multi-Transaction Translator) hub controller IC with 4 downstream ports for embedded USB solutions. It is designed, fabricated, tested, characterized and qualified for automotive applications. The 4-port hub is fully compliant with the USB 2.0 Specification. The USB82514 will attach to an upstream port as a full-speed hub or as a full-/hi-speed hub. The 4-port hub supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D- pins and all required pull-down and pull-up resistors on D+ and D- pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

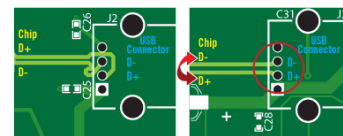
The USB82514 includes over 30 programmable features including:

**MultiTRAK™ Technology** which utilizes a dedicated TT per port to maintain consistent full-speed data throughput regardless of the number of active downstream connections. MultiTRAK outperforms conventional USB 2.0 hubs with a single TT in USB full-speed data transfers.

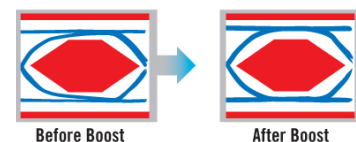
**PortMap** which provides flexible port mapping and disable sequences. The downstream ports of a USB82514 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB82514 automatically reorders the remaining ports to match the USB host controller's port numbering scheme.



**PortSwap** which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors avoiding uneven trace length or crossing of the USB differential signals on the PCB.



**PHYBoost** which enables four programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost attempts to restore USB signal integrity that has been compromised by system level variables such as poor PCB layout, long cables, etc. The boost graphic shows an example of hi-speed USB eye diagrams before (PHYBoost at 0%) and after (PHYBoost at 12%) signal integrity restoration in a compromised system environment.



The USB82514 is specifically tailored for use in automotive applications requiring automotive grade robustness starting with the comprehension of proprietary design for reliability techniques within the silicon IC itself as well as for the package design. Automotive qualified technologies and processes are used to fabricate the products with enhanced monitors to continuously drive improvements in accordance with our zero-dpm methodology. Product qualification is focused on customer expectations and exceeds many of the automotive reliability standards including AEC-Q100.

Microchip automotive services are provided during the life of the product from a dedicated organization composed of operations, quality, and product support personnel specialized in meeting the requirements of the automotive customer.

## 1.1 OEM Selectable Features

A default configuration is available in the USB82514 following a reset. This configuration may be sufficient for some applications. Strapping option pins make it possible to modify a limited sub-set of the configuration options.

The USB82514 may also be configured by an external EEPROM or a microcontroller. When using the microcontroller interface, the hub appears as an SMBus slave device. If the hub is pin-strapped for external EEPROM configuration but no external EEPROM is present, then a value of '0' will be written to all configuration data bit fields (the hub will attach to the host with all '0' values).

The USB82514 supports several OEM selectable features:

- Optional OEM configuration via I<sup>2</sup>C EEPROM or via the industry standard SMBus interface from an external SMBus host or microcontroller, see [Table 7-1, "Hub Configuration Options"](#) to configure the serial port interface behavior via the CFG\_SEL1 and CFG\_SEL0 pins.
- Compound device support (port is permanently hardwired to a downstream USB peripheral device), on a port-by-port basis, see ["Register 07h: Configuration Data Byte 2"](#), bit COMPOUND.
- Select Single-Transaction Translator (STT) or Multi-Transaction Translator (MTT), see ["Register 06h: Configuration Data Byte 1"](#), bit MTT\_ENABLE.
- Select over-current sensing and port power control on an individual (port-by-port) or ganged (all ports together) basis to match the OEM's choice of circuit board component selection, see ["Register 06h: Configuration Data Byte 1"](#), bits CURRENT\_SNS and PORT\_PWR.
- Customize vendor ID, product ID, and device ID, see ["Register 00h: Vendor ID \(LSB\)"](#), ["Register 01h: Vendor ID \(MSB\)"](#), ["Register 02h: Product ID \(LSB\)"](#), ["Register 03h: Product ID \(MSB\)"](#), ["Register 04h: Device ID \(LSB\)"](#) and ["Register 05h: Device ID \(MSB\)"](#).
- Easily configure as a 2, 3 or 4-Port Hub in common PCB layout, see ["Register 0Ah: Port Disable for Self-Powered Operation"](#) and ["Register 0Bh: Port Disable for Bus-Powered Operation"](#).
- PortMap: Flexible port mapping and disable sequence. Ports can be disabled/reordered in any sequence to support multiple platforms with a single design. The hub will automatically reorder the remaining ports to match the host controller's numbering scheme, see ["Register FBh: PortMap ID 12"](#) and ["Register FCh: PortMap 34"](#).
- PortSwap: Programmable USB differential-pair pin location.
  - Eases PCB layout by aligning USB signal lines directly to connectors, see ["Register FAh: PortSwap"](#).
- PhyBoost: Programmable USB signal drive strength. Recover USB signal integrity due to compromised system environments using 4 levels of signal drive strength, see ["Register F6h: Boost\\_Up"](#) and ["Register F8h: Boost\\_4:0"](#).
- Configure the delay time for filtering the over-current sense inputs, see ["Register 07h: Configuration Data Byte 2"](#), bit OC\_TIMER.
- Configure the downstream port power-on time reported to the host, see ["Register 10h: Power-On Time"](#).
- Indicate the maximum current that the 4-port hub consumes from the USB upstream port, see ["Register 0Eh: Hub Controller Max Current for Self-Powered Operation"](#) and ["Register 0Fh: Hub Controller Max Current for Bus-Powered Operation"](#).
- Indicate the maximum current required for the hub controller, see ["Register 0Ch: Max Power for Self-Powered Operation"](#) and ["Register 0Dh: Max Power for Bus-Powered Operation"](#).
- Support custom string descriptor up to 31 characters in length for:
  - Manufacturer string, see ["Register 16h-53h: Manufacturer String"](#).
  - Product string, see ["Register 54h-91h: Product String"](#).
  - Serial number string, see ["Register 92h-CFh: Serial String"](#).
- Pin selectable options for default configuration:
  - Downstream ports as non-removable ports, see ["Register 09h: Non-Removable Device"](#).
  - Downstream ports as disabled ports, see ["Register 0Ah: Port Disable for Self-Powered Operation"](#) and ["Register 0Bh: Port Disable for Bus-Powered Operation"](#).

## 2.0 ACRONYMS

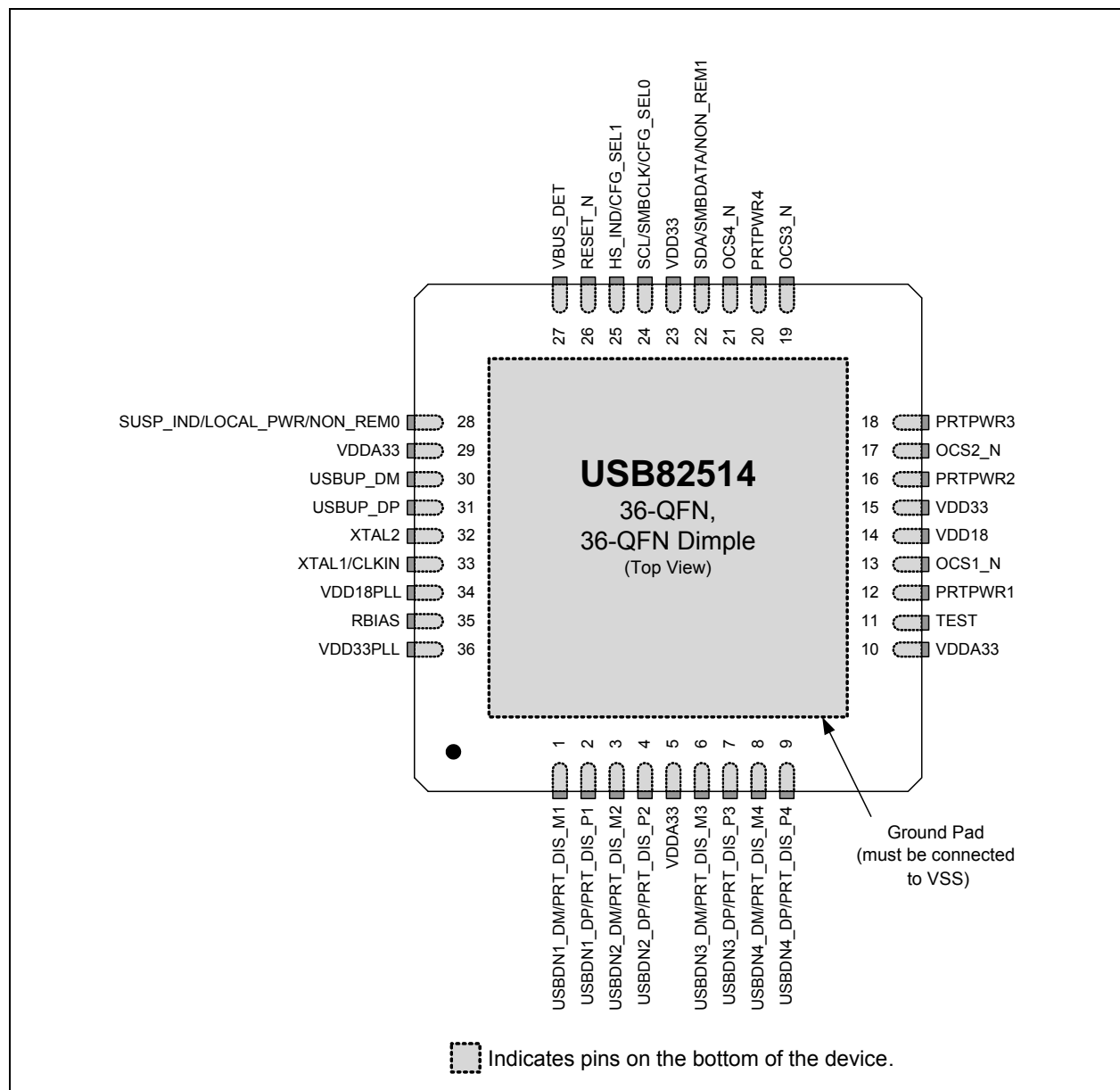
The following is a list of the general terms used throughout this document:

**TABLE 2-1: ACRONYMS**

| Acronym          | Description   |
|------------------|---|
| ACK              | Handshake packet indicating a positive acknowledgment |
| EOF              | End of (micro) Frame                                  |
| EOP              | End of Packet   |
| I <sup>2</sup> C | Inter-Integrated Circuit                              |
| MTT              | Multi-Transaction Translator                          |
| OCS              | Over-current Sense                                    |
| PCB              | Printed Circuit Board                                 |
| PHY              | Physical Layer  |
| PLL              | Phase-Locked Loop                                     |
| QFN              | Quad Flat No Leads                                    |
| RoHS             | Restriction of Hazardous Substances directive         |
| SMBus            | System Management Bus                                 |
| STT              | Single-Transaction Translator                         |
| TT               | Transaction Translator                                |

## 3.0 PIN CONFIGURATION

FIGURE 3-1: USB82514 36-PIN QFN (TOP VIEW)



# USB82514

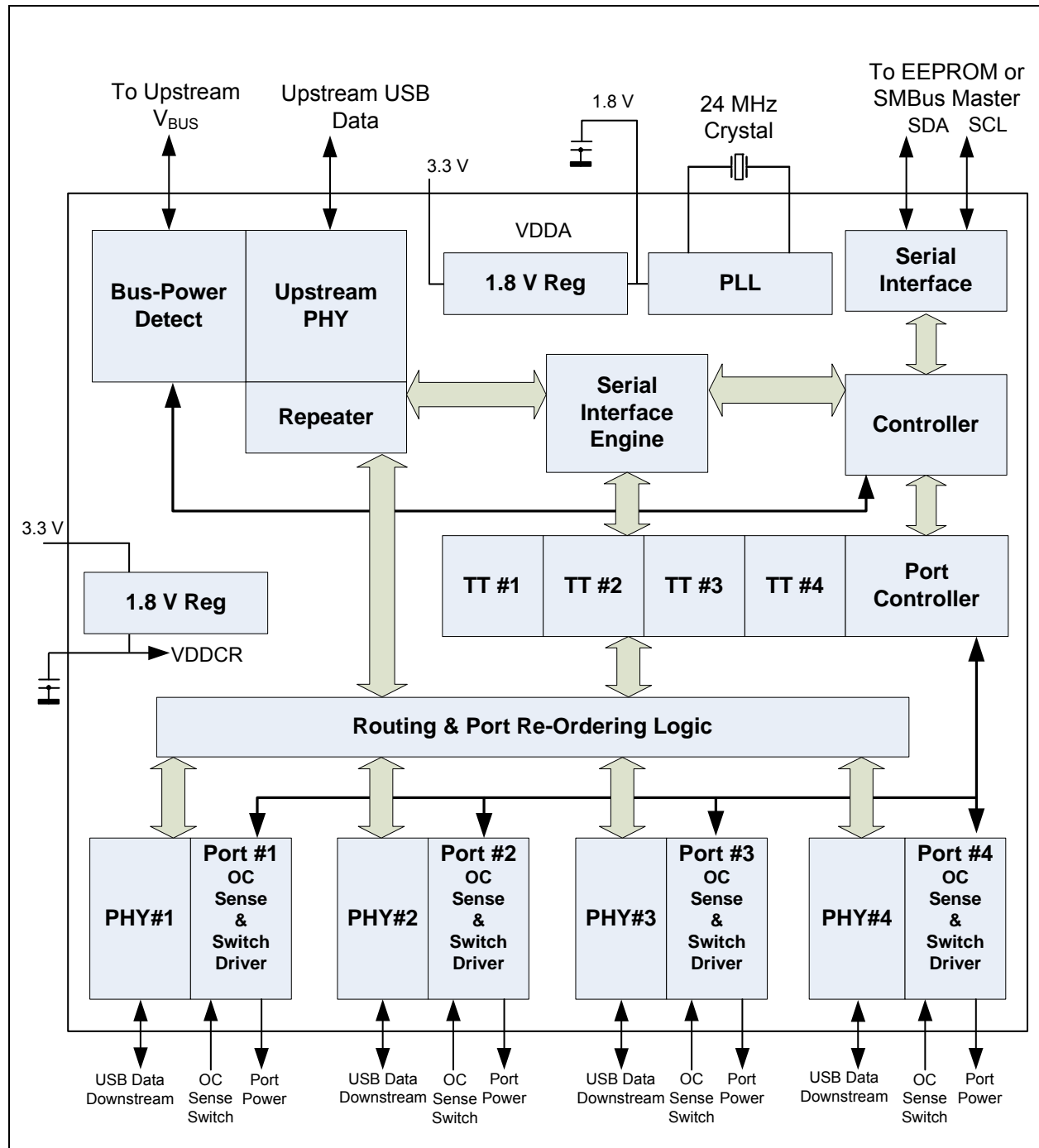
## 4.0 PIN TABLE

TABLE 4-1: USB82514 36-PIN TABLE

| Upstream USB Interfaces (3 Pins)        |                             |                          |                                     |
|---|-----------------------------|--------------------------|-------------------------------------|
| USBUP_DP                                | USBUP_DM                    | VBUS_DET                 |                                     |
| Downstream USB 2.0 Interfaces (17 Pins) |                             |                          |                                     |
| USBDN1_DP/<br>PRT_DIS_P1                | USBDN2_DP/<br>PRT_DIS_P2    | USBDN3_DP/<br>PRT_DIS_P3 | USBDN4_DP/<br>PRT_DIS_P4            |
| USBDN1_DM/<br>PRT_DIS_M1                | USBDN2_DM/<br>PRT_DIS_M2    | USBDN3_DM/<br>PRT_DIS_M3 | USBDN4_DM/<br>PRT_DIS_M4            |
| PRT_PWR1                                | PRT_PWR2                    | PRT_PWR3                 | PRT_PWR4                            |
| OCS1_N                                  | OCS2_N                      | OCS3_N                   | OCS4_N                              |
| RBIAS                                   |                             |                          |                                     |
| Serial Port Interfaces (3 Pins)         |                             |                          |                                     |
| SDA/<br>SMBDATA/<br>NON_REM1            | SCL/<br>SMBCLK/<br>CFG_SEL0 | HS_IND/<br>CFG_SEL1      |                                     |
| Misc (5 Pins)                           |                             |                          |                                     |
| XTAL1/CLKIN                             | XTAL2                       | RESET_N                  | SUSP_IND/<br>LOCAL_PWR/<br>NON_REM0 |
| TEST                                    |                             |                          |                                     |
| Analog / Digital Power (8 Pins)         |                             |                          |                                     |
| (2) VDD33                               | (3) VDDA33                  | VDD18                    | VDD18PLL                            |
| VDD33PLL                                |                             |                          |                                     |
| Total 36 Pins                           |                             |                          |                                     |

## 5.0 BLOCK DIAGRAM

FIGURE 5-1: USB82514 BLOCK DIAGRAM





# USB82514

## 6.0 PIN DESCRIPTIONS

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “N” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “N” is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

**TABLE 6-1: USB82514 PIN DESCRIPTIONS**

| Symbol                                    | 36 QFN               | Buffer Type | Description   |
|---|----------------------|-------------|---|
| <b>UPSTREAM USB INTERFACES</b>            |                      |             |   |
| USBUP_DP<br>USBUP_DM                      | 31<br>30             | IO-U        | USB Bus Data<br><br>These pins connect to the upstream USB bus data signals (host port or upstream hub).  |
| VBUS_DET                                  | 27                   | I           | Detect Upstream VBUS Power<br><br>Detects state of upstream VBUS power. The Microchip hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor (signaling a connect event).<br><br>When designing a detachable hub, this pin must be connected to the VBUS on the upstream port via a 2 to 1 voltage divider.<br><br>For self-powered applications with a permanently attached host, this pin must be connected to 3.3 V (typically VDD33). |
| <b>DOWNSTREAM USB 2.0 INTERFACE</b>       |                      |             |   |
| USBDN[4:1]_DP/<br>PRT_DIS_P[4:1]<br><br>& | 9<br>7<br>4<br>2     | IO-U        | Hi-Speed USB Data<br><br>These pins connect to the downstream USB peripheral devices attached to the hub's port.  |
| USBDN[4:1]_DM/<br>PRT_DIS_M[4:1]          | 8<br>6<br>3<br>1     |             | Downstream Port Disable Strap Option<br><br>If this strap is enabled by package and configuration settings (see <a href="#">Table 7-1, "Hub Configuration Options"</a> ), this pin will be sampled at RESET_N negation to determine if the port is disabled.<br><br>Both USB data pins for the corresponding port must be tied to the VDDA33 to disable the associated downstream port.   |
| PRT_PWR[4:1]                              | 20<br>18<br>16<br>12 | O12         | USB Port Power Enable<br><br>Enables power to downstream USB peripheral devices.<br><br><b>Note:</b> The hub will only support active high power controllers.   |

**TABLE 6-1: USB82514 PIN DESCRIPTIONS (CONTINUED)**

| Symbol                       | 36 QFN               | Buffer Type | Description  |
|------------------------------|----------------------|-------------|--|
| OCS_N[4:1]                   | 21<br>19<br>17<br>13 | IPU         | Over-current Sense<br><br>Input from external current monitor indicating an over-current condition.  |
| RBIAS                        | 35                   | I-R         | USB Transceiver Bias<br><br>A 12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.   |
| <b>SERIAL PORT INTERFACE</b> |                      |             |  |
| SDA/<br>SMBDATA/<br>NON_REM1 | 22                   | I/OSD12     | Serial Data<br><br>SMB Data<br><br>NON_REM1: Non-removable port strap option.<br><br>If this strap is enabled by package and configuration settings (see <a href="#">Table 7-1, "Hub Configuration Options"</a> ), this pin will be sampled (in conjunction with SUSP_IND/LOCAL_PWR/NON_REM0) at RESET_N negation to determine if ports [4:1] contain permanently attached (non-removable) devices:<br><br>NON_REM[1:0] = '00', All ports are removable,<br><br>NON_REM[1:0] = '01', Port 1 is non-removable,<br><br>NON_REM[1:0] = '10', Ports 1 & 2 are non-removable,<br><br>NON_REM[1:0] = '11', Ports 1, 2 & 3 are non-removable. |
| SCL/<br>SMBCLK/<br>CFG_SEL0  | 24                   | I/OSD12     | Serial Clock (SCL)<br><br>SMBus Clock (SMBCLK)<br><br>Configuration Select_SEL0: The logic state of this multifunction pin is internally latched on the rising edge of RESET_N (RESET_N negation) and will determine the hub configuration method as described in <a href="#">Table 7-1, "Hub Configuration Options"</a> .   |

# USB82514

**TABLE 6-1: USB82514 PIN DESCRIPTIONS (CONTINUED)**

| Symbol                  | 36 QFN | Buffer Type | Description  |
|-------------------------|--------|-------------|--|
| HS_IND/<br><br>CFG_SEL1 | 25     | I/O12       | <p>Hi-Speed Upstream Port Indicator Configuration Programming Select</p> <p>HS_IND: Hi-Speed Indicator for upstream port connection speed.</p> <p>The active state of HS_IND will be determined as follows:</p> <p>CFG_SEL1 = '0', Configuration Programming Select</p> <p>HS_IND is active high,</p> <p>CFG_SEL1 = '1',<br/>HS_IND is active low,</p> <p>'Asserted' = Hub is connected at HS<br/>'Negated' = Hub is connected at FS</p> <p><b>Note:</b> An LED can be attached to this signal for visual indication.</p> <p>CFG_SEL1: The logic state of this pin is internally latched on the rising edge of RESET_N (RESET_N negation), and will determine the hub configuration method as described in <a href="#">Table 7-1, "Hub Configuration Options"</a>.</p> |
| <b>MISC</b>             |        |             |  |
| XTAL1/<br>CLKIN         | 33     | ICLKx       | <p>Crystal Input/External Clock Input</p> <p>This pin connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used. When used with an external clock, the signal level must comply with the ICLK buffer levels.</p>  |
| XTAL2                   | 32     | OCLKx       | <p>Crystal Output</p> <p>24 MHz Crystal</p> <p>This is the other terminal of the crystal, or it is left disconnected when an external clock source is used to drive XTAL1/CLKIN.</p> <p><b>Note:</b> This output must not be used to drive any external circuitry other than the crystal circuit.</p>  |
| RESET_N                 | 26     | IS          | <p>RESET Input</p> <p>The system can reset the chip by driving this input low. The minimum active low pulse is 1 <math>\mu</math>s after all power supply voltages are at nominal levels.</p>  |

**TABLE 6-1: USB82514 PIN DESCRIPTIONS (CONTINUED)**

| Symbol                                      | 36 QFN | Buffer Type | Description   |
|---|--------|-------------|---|
| SUSP_IND/<br><br>LOCAL_PWR/<br><br>NON_REM0 | 28     | I/O12       | <p>Active/Suspend Status Signal Indicator or Local-Power &amp; Non-Removable Strap Option</p> <p>Suspend Indicator: Indicates USB state of the hub.<br/>'negated' = Unconfigured, or configured and in USB suspend<br/><br/>'asserted' = Hub is configured, and is active (i.e., not in suspend)</p> <p><b>Note:</b> An LED can be attached to this signal for visual indication.</p> <p>Local Power: Detects availability of local self-power source</p> <p>Low = Self/local power source is NOT available (i.e., hub gets all power from Upstream USB VBus).</p> <p>High = Self/local power source is available.</p> <p>NON_REM0 Strap Option:</p> <p>If this strap is enabled by package and configuration settings (see <a href="#">Table 7-1, "Hub Configuration Options"</a>), this pin will be sampled (in conjunction with NON_REM1) at RESET_N negation to determine if ports [4:1] contain permanently attached (non-removable) devices. Also, the active state of the signal will be determined as follows:</p> <p>NON_REM[1:0] = '00', All ports are removable, and the SUSP_IND signal is active high,</p> <p>NON_REM[1:0] = '01', Port 1 is non-removable, and the SUSP_IND signal is active low,</p> <p>NON_REM[1:0] = '10', Ports 1 &amp; 2 are non-removable, and the SUSP_IND signal is active high,</p> <p>NON_REM[1:0] = '11', Ports 1, 2 &amp; 3 are non-removable, and the SUSP_IND signal is active low.</p> |
| TEST  | 11     | IPD         | <p>TEST pin</p> <p>Tie this pin to ground for normal operation.</p>   |
| <b>POWER / GROUND</b>                       |        |             |   |
| VDD18                                       | 14     |             | <p>VDD Core</p> <p>+1.8 V core power. This pin must have a 1.0 <math>\mu</math>F (or greater) <math>\pm</math>20% (ESR &lt;0.1 <math>\Omega</math>) capacitor to VSS.</p>   |
| VDD33PLL                                    | 36     |             | <p>VDD 3.3 PLL Regulator Reference</p> <p>+3.3 V power supply for the PLL.</p>  |

# USB82514

**TABLE 6-1: USB82514 PIN DESCRIPTIONS (CONTINUED)**

| Symbol   | 36 QFN        | Buffer Type | Description  |
|----------|---------------|-------------|--|
| VDD18PLL | 34            |             | VDD PLL<br><br>+1.8 V Filtered analog power for internal PLL. This pin must have a 1.0 $\mu$ F (or greater) $\pm 20\%$ (ESR $< 0.1 \Omega$ ) capacitor to VSS. |
| VDDA33   | 5<br>10<br>29 |             | VDD Analog I/O<br><br>+3.3 V Filtered analog PHY power, shared between adjacent ports.   |
| VDD33    | 23<br>15      |             | VDDIO/VDD 3.3 Core Regulator Reference<br><br>+3.3 V power supply for the digital I/O. VDD33 acts as the regulator input.                                      |
| VSS      |               |             | VSS<br><br>Ground (The thermal slug must be connected to VSS.)   |

**TABLE 6-2: USB82514 BUFFER TYPE DESCRIPTIONS**

| Buffer  | Description   |
|---------|---|
| I       | Input   |
| IPD     | Input with internal weak pull-down resistor   |
| IPU     | Input with internal weak pull-up resistor   |
| IS      | Input with Schmitt trigger  |
| O12     | Output 12 mA  |
| I/O12   | Input/Output buffer with 12 mA sink and 12 mA source  |
| I/OSD12 | Open drain with Schmitt trigger 12 mA sink. Meets I <sup>2</sup> C-Bus specification version 2.1 requirements |
| ICLKx   | XTAL clock input  |
| OCLKx   | XTAL clock output   |
| I-R     | RBIAS   |
| IO-U    | Analog input/output as defined in USB specification   |

## 7.0 CONFIGURATION OPTIONS

### 7.1 4-Port Hub

Microchip's Automotive Grade USB 2.0 4-Port Hub is fully compliant to the Universal Serial Bus Specification available from the USB Implementer's Forum found at <http://www.usb.org/developers/docs/> (Revision 2.0 from April 27, 2000 and the 12/7/2000 and 5/28/2002 Errata). Please refer to Chapter 11 (Hub Specification) for general details regarding hub operation and functionality.

For performance reasons, the 4-Port Hub provides 1 Transaction Translator (TT) per port (defined as Multi-TT configuration), and each TT has 1512 bytes of periodic buffer space and 272 bytes of non-periodic buffer space (divided into 4 non-periodic buffers per TT), for a total of 1784 bytes of buffer space for each Transaction Translator.

#### 7.1.1 HUB CONFIGURATION OPTIONS

The Microchip hub supports a large number of features (some are mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. There are three principal ways to configure the hub: SMBus, EEPROM, or by internal default settings (with or without pin strapping option overrides). In all cases, the configuration method will be determined by the CFG\_SEL1 and CFG\_SEL0 pins immediately after RESET\_N negation.

If the SMBus or EEPROM is selected using the CFG\_SEL pins, then the data read in from the EEPROM/SMBus will take precedence over the pin strapping options. If the internal default setting is selected, the options come from the internal ROM. These values can be selectively overridden using the pin strapping options.

#### 7.1.2 SMBus OR EEPROM INTERFACE

**TABLE 7-1: HUB CONFIGURATION OPTIONS**

| CFG_SEL1 | CFG_SEL0 | SMBUS OR EEPROM INTERFACE BEHAVIOR  |
|----------|----------|---|
| 0        | 0        | Internal default configuration <ul style="list-style-type: none"> <li>• Strap options enabled</li> <li>• Self-powered operation enabled</li> </ul>  |
| 0        | 1        | Configured as an SMBus slave for external download of user-defined descriptors. <ul style="list-style-type: none"> <li>• SMBus slave address 58 (0101100x)</li> <li>• Strap options disabled</li> <li>• All settings controlled by registers</li> </ul> |
| 1        | 0        | Internal default configuration <ul style="list-style-type: none"> <li>• Strap options enabled</li> <li>• Bus power operation</li> </ul>   |
| 1        | 1        | 2-Wire I <sup>2</sup> C EEPROMS are supported <ul style="list-style-type: none"> <li>• Strap options disabled</li> <li>• All settings controlled by registers</li> </ul>  |

##### 7.1.2.1 Power Switching Polarity

The hub will only support active high power controllers.

##### 7.1.3 VBus DETECT

According to section 7.2.1 of the USB 2.0 Specification, a downstream port can never provide power to its D+ or D- pull up resistors unless the upstream port's VBUS is in the asserted (powered) state. The VBUS\_DET pin on the hub monitors the state of the upstream VBUS signal and will not pull up the D+ resistor if VBUS is not active. If VBUS goes from an active to an inactive state (not powered), the hub will remove power from the D+ pull-up resistor within 10 seconds.

# USB82514

## 7.2 EEPROM Interface

The Microchip hub can be configured via a 2-wire (I<sup>2</sup>C) EEPROM (256x8). (Please see [Table 7-1, "Hub Configuration Options"](#) for specific details on how to enable configuration via an I<sup>2</sup>C EEPROM).

When configured for EEPROM support, the internal state machine will read the external EEPROM for configuration data. The hub will then "attach" to the upstream USB host.

**Note:** The hub does not have the capacity to write, or "Program," an external EEPROM. The hub only has the capability to read external EEPROMs. The external EEPROM will be read (even if it is blank or non-populated), and the hub will be "configured" with the values that are read.

Each register has R/W capability. SMBUS and EEPROM Reset Values are 0x00. Reserved registers should be written to '0' unless otherwise specified.

### 7.2.1 INTERNAL REGISTER SET (COMMON TO EEPROM AND SMBus)

| Reg Addr | Register Name   | Internal Default ROM |
|----------|---|----------------------|
| 00h      | Vendor ID (LSB)                                       | 24h                  |
| 01h      | Vendor ID (MSB)                                       | 04h                  |
| 02h      | Product ID (LSB)                                      | 14h                  |
| 03h      | Product ID (MSB)                                      | 25h                  |
| 04h      | Device ID (LSB)                                       | A0h                  |
| 05h      | Device ID (MSB)                                       | 80h                  |
| 06h      | Configuration Data Byte 1                             | 9Bh                  |
| 07h      | Configuration Data Byte 2                             | 20h                  |
| 08h      | Configuration Data Byte 3                             | 02h                  |
| 09h      | Non-Removable Device                                  | 00h                  |
| 0Ah      | Port Disable for Self-Powered Operation               | 00h                  |
| 0Bh      | Port Disable for Bus-Powered Operation                | 00h                  |
| 0Ch      | Max Power for Self-Powered Operation                  | 01h                  |
| 0Dh      | Max Power for Bus-Powered Operation                   | 32h                  |
| 0Eh      | Hub Controller Max Current for Self-Powered Operation | 01h                  |
| 0Fh      | Hub Controller Max Current for Bus-Powered Operation  | 32h                  |
| 10h      | Power-on Time   | 32h                  |
| 11h      | Language ID High                                      | 00h                  |
| 12h      | Language ID Low                                       | 00h                  |
| 13h      | Manufacturer String Length                            | 00h                  |
| 14h      | Product String Length                                 | 00h                  |
| 15h      | Serial String Length                                  | 00h                  |
| 16h-53h  | Manufacturer String                                   | 00h                  |
| 54h-91h  | Product String  | 00h                  |

| Reg Addr | Register Name                                      | Internal Default ROM |
|----------|--|----------------------|
| 92h-Cfh  | Serial String                                      | 00h                  |
| D0h-F5h  | Reserved   | 00h                  |
| F6h      | Boost_Up   | 00h                  |
| F7h      | Reserved   | 00h                  |
| F8h      | Boost_4:0  | 00h                  |
| F9h      | Reserved   | 00h                  |
| FAh      | PortSwap   | 00h                  |
| FBh      | PortMap 12   | 00h                  |
| FCh      | PortMap 34   | 00h                  |
| FDh      | Reserved   | 00h                  |
| FFh      | Status/Command<br><b>Note:</b> SMBus register only | 00h                  |

## 7.2.1.1 Register 00h: Vendor ID (LSB)

| Bit Number | Bit Name | Description  |
|------------|----------|--|
| 7:0        | VID_LSB  | Least Significant Byte of the Vendor ID: This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the OEM using either the SMBus or EEPROM interface options. |

## 7.2.1.2 Register 01h: Vendor ID (MSB)

| Bit Number | Bit Name | Description   |
|------------|----------|---|
| 7:0        | VID_MSB  | Most Significant Byte of the Vendor ID: This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the OEM using either the SMBus or EEPROM interface options. |

## 7.2.1.3 Register 02h: Product ID (LSB)

| Bit Number | Bit Name | Description  |
|------------|----------|--|
| 7:0        | PID_LSB  | Least Significant Byte of the Product ID: This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options. |



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## 7.2.1.4 Register 03h: Product ID (MSB)

| Bit Number | Bit Name | Description   |
|------------|----------|---|
| 7:0        | PID_MSB  | Most Significant Byte of the Product ID: This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options. |

## 7.2.1.5 Register 04h: Device ID (LSB)

| Bit Number | Bit Name | Description   |
|------------|----------|---|
| 7:0        | DID_LSB  | Least Significant Byte of the Device ID: This is a 16-bit device release number in BCD format (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options. |

## 7.2.1.6 Register 05h: Device ID (MSB)

| Bit Number | Bit Name | Description  |
|------------|----------|--|
| 7:0        | DID_MSB  | Most Significant Byte of the Device ID: This is a 16-bit device release number in BCD format (assigned by OEM). This field is set by the OEM using either the SMBus or EEPROM interface options. |

## 7.2.1.7 Register 06h: Configuration Data Byte 1

| Bit Number | Bit Name     | Description  |
|------------|--------------|--|
| 7          | SELF_BUS_PWR | <p>Self or Bus-Power: Selects between self and bus-powered operation.</p> <p>The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller).</p> <p>When configured as a bus-powered device, the Microchip hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered Microchip hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 specifications are not violated.</p> <p>When configured as a self-powered device, &lt;1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current.</p> <p>This field is set by the OEM using either the SMBus or EEPROM interface options.</p> <p>See description of the DYNAMIC bit (reg 07h, bit 7) for the self-/bus-power functionality when dynamic power switching is enabled.</p> <p>'0' = Bus-powered operation<br/>'1' = Self-powered operation</p> <p><b>Note:</b> If dynamic power switching is enabled, this bit is ignored and the LOCAL_PWR pin is used to determine if the hub is operating from self or bus power.</p> |
| 6          | Reserved     | Reserved   |
| 5          | HS_DISABLE   | <p>Hi-Speed Disable: Disables the capability to attach as either a Hi-/Full-speed device, and forces attachment as Full-speed only (i.e., no Hi-Speed support).</p> <p>'0' = Hi-/Full-Speed<br/>'1' = Full-Speed-Only (Hi-Speed is disabled!)</p>  |
| 4          | MTT_ENABLE   | <p>Multi-TT enable: Enables one Transaction Translator per port operation.</p> <p>Selects between a mode where only one Transaction Translator is available for all ports (Single-TT), or each port gets a dedicated Transaction Translator (Multi-TT) {Note: The host may force Single-TT mode only}.</p> <p>'0' = Single TT for all ports<br/>'1' = One TT per port (multiple TT's supported)</p>  |

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| Bit Number | Bit Name    | Description   |
|------------|-------------|---|
| 3          | EOP_DISABLE | <p>EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the USB 2.0 Specification for additional details. Note: generation of an EOP at the EOF1 point may prevent a host controller (operating in FS mode) from placing the USB bus in suspend.</p> <p>'0' = EOP generation is normal<br/>'1' = EOP generation is disabled</p> |
| 2:1        | CURRENT_SNS | <p>Over-current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a port or ganged basis is hardware implementation dependent.</p> <p>'00' = Ganged sensing (all ports together)<br/>'01' = Individual port-by-port<br/>'1x' = Over-current sensing not supported (must only be used with bus-powered configurations!)</p>   |
| 0          | PORT_PWR    | <p>Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port-by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent.</p> <p>'0' = Ganged switching (all ports together)<br/>'1' = Individual port-by-port switching</p>   |

## 7.2.1.8 Register 07h: Configuration Data Byte 2

| Bit Number | Bit Name | Description  |
|------------|----------|--|
| 7          | DYNAMIC  | <p>Dynamic Power Switching Enable: Controls the ability of the hub to automatically change from self-powered operation to bus-powered operation if the local power source is removed or is unavailable (and from bus-powered to self-powered if the local power source is restored). {Note: If the local power source is available, the hub will always switch to self-powered operation.}</p> <p>When dynamic power switching is enabled, the hub detects the availability of a local power source by monitoring the external LOCAL_PWR pin. If the hub detects a change in power source availability, the hub immediately disconnects and removes power from all downstream devices and disconnects the upstream port. The hub will then re-attach to the upstream port as either a bus-powered hub (if local-power is unavailable) or a self-powered hub (if local power is available).</p> <p>'0' = No dynamic auto-switching<br/>'1' = Dynamic auto-switching capable</p> |
| 6          | Reserved | Reserved   |

| Bit Number | Bit Name | Description  |
|------------|----------|--|
| 5:4        | OC_TIMER | Over-Current Timer: Over-current timer delay<br><br>'00' = 0.1 ms<br>'01' = 4.0 ms<br>'10' = 8.0 ms<br>'11' = 16.0 ms  |
| 3          | COMPOUND | Compound Device: Allows the OEM to indicate that the hub is part of a compound device (see the USB Specification for definition) . The applicable port(s) must also be defined as having a "non-removable device".<br><br><b>Note:</b> When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device.<br><br>'0' = No<br>'1' = Yes, the hub is part of a compound device |
| 2:0        | Reserved | Reserved   |

## 7.2.1.9 Register 08h: Configuration Data Byte 3

| Bit Number | Bit Name  | Description   |
|------------|-----------|---|
| 7:4        | Reserved  | Reserved  |
| 3          | PRTMAP_EN | Port Re-mapping Enable: Selects the method used by the hub to assign port numbers and disable ports.<br><br>'0' = Standard mode<br>'1' = Port re-map mode |
| 2:1        | Reserved  | Reserved  |
| 0          | STRING_EN | Enables string descriptor support<br><br>'0' = String support disabled<br>'1' = String support enabled  |

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## 7.2.1.10 Register 09h: Non-Removable Device

| Bit Number | Bit Name  | Description   |
|------------|-----------|---|
| 7:0        | NR_DEVICE | <p>Non-Removable Device: Indicates which port(s) include non-removable devices.</p> <p>'0' = port is removable<br/>'1' = port is non-removable</p> <p>Informs the host if one of the active ports has a permanent device that is undetachable from the hub. (Note: The device must provide its own descriptor data.)</p> <p>When using the internal default option, the NON_REM[1:0] pins will designate the appropriate ports as being non-removable.</p> <p>Bit 7 = Reserved<br/>Bit 6 = Reserved<br/>Bit 5 = Reserved<br/>Bit 4 = Controls physical port 4<br/>Bit 3 = Controls physical port 3<br/>Bit 2 = Controls physical port 2<br/>Bit 1 = Controls physical port 1<br/>Bit 0 = Reserved</p> |

## 7.2.1.11 Register 0Ah: Port Disable for Self-Powered Operation

| Bit Number | Bit Name    | Description   |
|------------|-------------|---|
| 7:0        | PORT_DIS_SP | <p>Port Disable Self-Powered: Disables 1 or more contiguous ports.</p> <p>'0' = port is available<br/>'1' = port is disabled</p> <p>During self-powered operation when remapping mode is disabled (PRT_MAP_EN = '0'), this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a host controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host, and will reorder the active ports in order to ensure proper function.</p> <p>Bit 7 = Reserved<br/>Bit 6 = Reserved<br/>Bit 5 = Reserved<br/>Bit 4 = Controls physical port 4<br/>Bit 3 = Controls physical port 3<br/>Bit 2 = Controls physical port 2<br/>Bit 1 = Controls physical port 1<br/>Bit 0 = Reserved</p> |

## 7.2.1.12 Register 0Bh: Port Disable for Bus-Powered Operation

| Bit Number | Bit Name    | Description  |
|------------|-------------|--|
| 7:0        | PORT_DIS_BP | <p>Port Disable Bus-Powered: Disables 1 or more contiguous ports.</p> <p>'0' = port is available<br/>'1' = port is disabled</p> <p>During self-Powered operation when remapping mode is disabled (PRT-MAP_EN = '0'), this selects the ports which will be permanently disabled, and are not available to be enabled or enumerated by a host controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host, and will reorder the active ports in order to ensure proper function.</p> <p>When using the internal default option, the PRT_DIS_P[4:1] and PRT_DIS_M[4:1] pins will disable the appropriate ports.</p> <p>Bit 7 = Reserved<br/>Bit 6 = Reserved<br/>Bit 5 = Reserved<br/>Bit 4 = Controls physical port 4<br/>Bit 3 = Controls physical port 3<br/>Bit 2 = Controls physical port 2<br/>Bit 1 = Controls physical port 1<br/>Bit 0 = Reserved</p> |

## 7.2.1.13 Register 0Ch: Max Power for Self-Powered Operation

| Bit Number | Bit Name   | Description   |
|------------|------------|---|
| 7:0        | MAX_PWR_SP | <p>Max Power Self_Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors.</p> <p><b>Note:</b> The USB 2.0 Specification does not permit this value to exceed 100 mA.</p> |

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## 7.2.1.14 Register 0Dh: Max Power for Bus-Powered Operation

| Bit Number | Bit Name   | Description   |
|------------|------------|---|
| 7:0        | MAX_PWR_BP | <p>Max Power Bus_Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors.</p> <p>A value of 50 (decimal) indicates 100 mA, which is the default value.</p> |

## 7.2.1.15 Register 0Eh: Hub Controller Max Current for Self-Powered Operation

| Bit Number | Bit Name    | Description  |
|------------|-------------|--|
| 7:0        | HC_MAX_C_SP | <p>Hub Controller Max Current Self-Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.</p> <p><b>Note:</b> The USB 2.0 Specification does not permit this value to exceed 100 mA.</p> |

## 7.2.1.16 Register 0Fh: Hub Controller Max Current for Bus-Powered Operation

| Bit Number | Bit Name    | Description   |
|------------|-------------|---|
| 7:0        | HC_MAX_C_BP | <p>Hub Controller Max Current Bus-Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.</p> <p>A value of 50 (decimal) would indicate 100 mA, which is the default value.</p> |

## 7.2.1.17 Register 10h: Power-On Time

| Bit Number | Bit Name      | Description  |
|------------|---------------|--|
| 7:0        | POWER_ON_TIME | <p>Power-On Time: The length of time that it takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is stable on that port.</p> |

## 7.2.1.18 Register 11h: Language ID High

| Bit Number | Bit Name  | Description   |
|------------|-----------|---|
| 7:0        | LANG_ID_H | USB LANGUAGE ID (Upper 8 bits of a 16-bit ID field) |

## 7.2.1.19 Register 12h: Language ID Low

| Bit Number | Bit Name  | Description   |
|------------|-----------|---|
| 7:0        | LANG_ID_L | USB LANGUAGE ID (Lower 8 bits of a 16-bit ID field) |

## 7.2.1.20 Register 13h: Manufacturer String Length

| Bit Number | Bit Name    | Description   |
|------------|-------------|---|
| 7:0        | MFR_STR_LEN | Manufacturer String Length<br>Maximum string length is 31 characters. |

## 7.2.1.21 Register 14h: Product String Length

| Bit Number | Bit Name    | Description  |
|------------|-------------|--|
| 7:0        | PRD_STR_LEN | Product String Length<br>Maximum string length is 31 characters. |

## 7.2.1.22 Register 15h: Serial String Length

| Bit Number | Bit Name    | Description   |
|------------|-------------|---|
| 7:0        | SER_STR_LEN | Serial String Length<br>Maximum string length is 31 characters. |



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## 7.2.1.23 Register 16h-53h: Manufacturer String

| Bit Number | Bit Name | Description  |
|------------|----------|--|
| 7:0        | MFR_STR  | <p>Manufacturer String, UNICODE UTF-16LE per USB 2.0 Specification</p> <p>Maximum string length is 31 characters (62 bytes).</p> <p><b>Note:</b> The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Some EEPROM programmers may transpose the MSB and LSB, thus reversing the byte order. Please pay careful attention to the byte ordering for your selected programming tools.</p> |

## 7.2.1.24 Register 54h-91h: Product String

| Bit Number | Bit Name | Description   |
|------------|----------|---|
| 7:0        | PRD_STR  | <p>Product String, UNICODE UTF-16LE per USB 2.0 Specification</p> <p>Maximum string length is 31 characters (62 bytes).</p> <p><b>Note:</b> The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Some EEPROM programmers may transpose the MSB and LSB, thus reversing the byte order. Please pay careful attention to the byte ordering for your selected programming tools.</p> |

## 7.2.1.25 Register 92h-CFh: Serial String

| Bit Number | Bit Name | Description   |
|------------|----------|---|
| 7:0        | SER_STR  | <p>Serial String, UNICODE UTF16LE per USB 2.0 Specification</p> <p>Maximum string length is 31 characters (62 bytes).</p> <p><b>Note:</b> The string consists of individual 16-bit UNICODE UTF-16LE characters. The characters will be stored starting with the LSB at the least significant address and the MSB at the next 8-bit location (subsequent characters must be stored in sequential contiguous address in the same LSB, MSB manner). Some EEPROM programmers may transpose the MSB and LSB, thus reversing the byte order. Please pay careful attention to the byte ordering for your selected programming tools.</p> |

## 7.2.1.26 Register F6h: Boost\_Up

| Bit Number | Bit Name   | Description   |
|------------|------------|---|
| 7:2        | Reserved   | Reserved  |
| 1:0        | BOOST_IOUT | <p>USB electrical signaling drive strength Boost Bit for Upstream Port.</p> <p>'00' = Normal electrical drive strength = No boost<br/>           '01' = Elevated electrical drive strength = Low (approximately 4% boost)<br/>           '10' = Elevated electrical drive strength = Medium (approximately 8% boost)<br/>           '11' = Elevated electrical drive strength = High (approximately 12% boost)</p> <p><b>Note:</b> "Boost" could result in non-USB Compliant parameters, the OEM should use a '00' value unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels.</p> |

## 7.2.1.27 Register F8h: Boost\_4:0

| Bit Number | Bit Name     | Description  |
|------------|--------------|--|
| 7:6        | BOOST_IOUT_4 | <p>Upstream USB electrical signaling drive strength Boost Bit for Downstream Port '4'.</p> <p>'00' = Normal electrical drive strength = No boost<br/>           '01' = Elevated electrical drive strength = Low (approximately 4% boost)<br/>           '10' = Elevated electrical drive strength = Medium (approximately 8% boost)<br/>           '11' = Elevated electrical drive strength = High (approximately 12% boost)</p> <p><b>Note:</b> "Boost" could result in non-USB Compliant parameters, the OEM should use a '00' value unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels.</p> |
| 5:4        | BOOST_IOUT_3 | <p>USB electrical signaling drive strength Boost Bit for Downstream Port '3'.</p> <p>'00' = Normal electrical drive strength = No boost<br/>           '01' = Elevated electrical drive strength = Low (approximately 4% boost)<br/>           '10' = Elevated electrical drive strength = Medium (approximately 8% boost)<br/>           '11' = Elevated electrical drive strength = High (approximately 12% boost)</p> <p><b>Note:</b> "Boost" could result in non-USB Compliant parameters, the OEM should use a '00' value unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels.</p>          |

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| Bit Number | Bit Name     | Description  |
|------------|--------------|--|
| 3:2        | BOOST_IOUT_2 | USB electrical signaling drive strength Boost Bit for Downstream Port '2'.<br><br>'00' = Normal electrical drive strength = No boost<br>'01' = Elevated electrical drive strength = Low (approximately 4% boost)<br>'10' = Elevated electrical drive strength = Medium (approximately 8% boost)<br>'11' = Elevated electrical drive strength = High (approximately 12% boost)<br><br><b>Note:</b> "Boost" could result in non-USB Compliant parameters, the OEM should use a '00' value unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels. |
| 1:0        | BOOST_IOUT_1 | USB electrical signaling drive strength Boost Bit for Downstream Port '1'.<br><br>'00' = Normal electrical drive strength = No boost<br>'01' = Elevated electrical drive strength = Low (approximately 4% boost)<br>'10' = Elevated electrical drive strength = Medium (approximately 8% boost)<br>'11' = Elevated electrical drive strength = High (approximately 12% boost)<br><br><b>Note:</b> "Boost" could result in non-USB Compliant parameters, the OEM should use a '00' value unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels. |

## 7.2.1.28 Register FAh: PortSwap

| Bit Number | Bit Name | Description   |
|------------|----------|---|
| 7:0        | PRTSP    | PortSwap: Swaps the upstream and downstream USB DP and DM Pins for ease of board routing to devices and connectors.<br><br>'0' = USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin.<br><br>'1' = USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin.<br><br>Bit 7 = Reserved<br>Bit 6 = Reserved<br>Bit 5 = Reserved<br>Bit 4 = '1'; Port 4 DP/DM is swapped.<br>Bit 3 = '1'; Port 3 DP/DM is swapped.<br>Bit 2 = '1'; Port 2 DP/DM is swapped.<br>Bit 1 = '1'; Port 1 DP/DM is swapped.<br>Bit 0 = '1'; Upstream Port DP/DM is swapped. |

## 7.2.1.29 Register FBh: PortMap 12

| Bit Number   | Bit Name               | Description   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
|--|------------------------|---|-----------|--------|-----------------------------|--|--------|---|--|--------|---|--|--------|---|--|--------|---|--|------------------------|---------------------|-----------|--------|-----------------------------|--|--------|---|--|--------|---|--|--------|---|--|--------|---|--|------------------------|---------------------|
| 7:0  | PRTR12                 | <p>PortMap register for ports 1 &amp; 2</p> <p>When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number '1' up to the number of ports that the hub recognizes.</p> <p>The host's port number is referred to as "logical port number" and the physical port on the hub is the "physical port number". When the remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).</p> <p><b>Note:</b> The OEM must ensure that contiguous logical port numbers are used, starting from #1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.</p> |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
| <p><b>TABLE 7-2: PORTMAP REGISTER FOR PORTS 1 &amp; 2</b></p> <table> <tr> <td>Bit [7:4]</td><td>'0000'</td><td>Physical Port 2 is disabled</td></tr> <tr> <td></td><td>'0001'</td><td>Physical Port 2 is mapped to Logical Port 1</td></tr> <tr> <td></td><td>'0010'</td><td>Physical Port 2 is mapped to Logical Port 2</td></tr> <tr> <td></td><td>'0011'</td><td>Physical Port 2 is mapped to Logical Port 3</td></tr> <tr> <td></td><td>'0100'</td><td>Physical Port 2 is mapped to Logical Port 4</td></tr> <tr> <td></td><td>'0101'<br/>to<br/>'1111'</td><td>Illegal; Do Not Use</td></tr> <tr> <td>Bit [3:0]</td><td>'0000'</td><td>Physical Port 1 is disabled</td></tr> <tr> <td></td><td>'0001'</td><td>Physical Port 1 is mapped to Logical Port 1</td></tr> <tr> <td></td><td>'0010'</td><td>Physical Port 1 is mapped to Logical Port 2</td></tr> <tr> <td></td><td>'0011'</td><td>Physical Port 1 is mapped to Logical Port 3</td></tr> <tr> <td></td><td>'0100'</td><td>Physical Port 1 is mapped to Logical Port 4</td></tr> <tr> <td></td><td>'0101'<br/>to<br/>'1111'</td><td>Illegal; Do Not Use</td></tr> </table> |                        |   | Bit [7:4] | '0000' | Physical Port 2 is disabled |  | '0001' | Physical Port 2 is mapped to Logical Port 1 |  | '0010' | Physical Port 2 is mapped to Logical Port 2 |  | '0011' | Physical Port 2 is mapped to Logical Port 3 |  | '0100' | Physical Port 2 is mapped to Logical Port 4 |  | '0101'<br>to<br>'1111' | Illegal; Do Not Use | Bit [3:0] | '0000' | Physical Port 1 is disabled |  | '0001' | Physical Port 1 is mapped to Logical Port 1 |  | '0010' | Physical Port 1 is mapped to Logical Port 2 |  | '0011' | Physical Port 1 is mapped to Logical Port 3 |  | '0100' | Physical Port 1 is mapped to Logical Port 4 |  | '0101'<br>to<br>'1111' | Illegal; Do Not Use |
| Bit [7:4]  | '0000'                 | Physical Port 2 is disabled   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
|  | '0001'                 | Physical Port 2 is mapped to Logical Port 1   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
|  | '0010'                 | Physical Port 2 is mapped to Logical Port 2   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
|  | '0011'                 | Physical Port 2 is mapped to Logical Port 3   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
|  | '0100'                 | Physical Port 2 is mapped to Logical Port 4   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
|  | '0101'<br>to<br>'1111' | Illegal; Do Not Use   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
| Bit [3:0]  | '0000'                 | Physical Port 1 is disabled   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
|  | '0001'                 | Physical Port 1 is mapped to Logical Port 1   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
|  | '0010'                 | Physical Port 1 is mapped to Logical Port 2   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
|  | '0011'                 | Physical Port 1 is mapped to Logical Port 3   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
|  | '0100'                 | Physical Port 1 is mapped to Logical Port 4   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |
|  | '0101'<br>to<br>'1111' | Illegal; Do Not Use   |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |           |        |                             |  |        |   |  |        |   |  |        |   |  |        |   |  |                        |                     |

## 7.2.1.30 Register FCh: PortMap 34

| Bit Number   | Bit Name        | Description   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
|--|-----------------|---|-----------|--------|-----------------------------|--------|---|--------|---|--------|---|--------|---|-----------------|---------------------|-----------|--------|-----------------------------|--------|---|--------|---|--------|---|--------|---|-----------------|---------------------|
| 7:0  | PRTR34          | <p>PortMap register for ports 3 &amp; 4</p> <p>When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number '1' up to the number of ports that the hub recognizes.</p> <p>The host's port number is referred to as "logical port number" and the physical port on the hub is the "physical port number". When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).</p> <p><b>Note:</b> The OEM must ensure that contiguous logical port numbers are used, starting from #1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.</p> |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
| <b>TABLE 7-3: PORTMAP REGISTER FOR PORTS 3 &amp; 4</b>   |                 |   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
| <table> <tr> <td rowspan="6">Bit [7:4]</td><td>'0000'</td><td>Physical Port 4 is disabled</td></tr> <tr> <td>'0001'</td><td>Physical Port 4 is mapped to Logical Port 1</td></tr> <tr> <td>'0010'</td><td>Physical Port 4 is mapped to Logical Port 2</td></tr> <tr> <td>'0011'</td><td>Physical Port 4 is mapped to Logical Port 3</td></tr> <tr> <td>'0100'</td><td>Physical Port 4 is mapped to Logical Port 4</td></tr> <tr> <td>'0101 to '1111'</td><td>Illegal: Do Not Use</td></tr> <tr> <td rowspan="6">Bit [3:0]</td><td>'0000'</td><td>Physical Port 3 is disabled</td></tr> <tr> <td>'0001'</td><td>Physical Port 3 is mapped to Logical Port 1</td></tr> <tr> <td>'0010'</td><td>Physical Port 3 is mapped to Logical Port 2</td></tr> <tr> <td>'0011'</td><td>Physical Port 3 is mapped to Logical Port 3</td></tr> <tr> <td>'0100'</td><td>Physical Port 3 is mapped to Logical Port 4</td></tr> <tr> <td>'0101 to '1111'</td><td>Illegal; Do Not Use</td></tr> </table> |                 |   | Bit [7:4] | '0000' | Physical Port 4 is disabled | '0001' | Physical Port 4 is mapped to Logical Port 1 | '0010' | Physical Port 4 is mapped to Logical Port 2 | '0011' | Physical Port 4 is mapped to Logical Port 3 | '0100' | Physical Port 4 is mapped to Logical Port 4 | '0101 to '1111' | Illegal: Do Not Use | Bit [3:0] | '0000' | Physical Port 3 is disabled | '0001' | Physical Port 3 is mapped to Logical Port 1 | '0010' | Physical Port 3 is mapped to Logical Port 2 | '0011' | Physical Port 3 is mapped to Logical Port 3 | '0100' | Physical Port 3 is mapped to Logical Port 4 | '0101 to '1111' | Illegal; Do Not Use |
| Bit [7:4]  | '0000'          | Physical Port 4 is disabled   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
|  | '0001'          | Physical Port 4 is mapped to Logical Port 1   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
|  | '0010'          | Physical Port 4 is mapped to Logical Port 2   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
|  | '0011'          | Physical Port 4 is mapped to Logical Port 3   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
|  | '0100'          | Physical Port 4 is mapped to Logical Port 4   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
|  | '0101 to '1111' | Illegal: Do Not Use   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
| Bit [3:0]  | '0000'          | Physical Port 3 is disabled   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
|  | '0001'          | Physical Port 3 is mapped to Logical Port 1   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
|  | '0010'          | Physical Port 3 is mapped to Logical Port 2   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
|  | '0011'          | Physical Port 3 is mapped to Logical Port 3   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
|  | '0100'          | Physical Port 3 is mapped to Logical Port 4   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |
|  | '0101 to '1111' | Illegal; Do Not Use   |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |           |        |                             |        |   |        |   |        |   |        |   |                 |                     |

## 7.2.1.31 Register FFh: Status/Command

| Bit Number | Bit Name   | Description   |
|------------|------------|---|
| 7:3        | Reserved   | Reserved  |
| 2          | INTF_PW_DN | SMBus Interface Power Down<br><br>'0' = Interface is active<br>'1' = Interface power down after ACK has completed   |
| 1          | RESET      | Reset the SMBus Interface and internal memory back to RESET_N assertion default settings.<br><br>'0' = Normal Run/Idle State<br>'1' = Force a reset of registers to their default state   |
| 0          | USB_ATTACH | USB Attach (and write protect)<br><br>'0' = SMBus slave interface is active<br>'1' = Hub will signal a USB attach event to an upstream device. The internal memory (address range 00h-FEh) is "write-protected" to prevent unintentional data corruption. |

## 7.2.2 I<sup>2</sup>C EEPROM

The I<sup>2</sup>C EEPROM interface implements a subset of the I<sup>2</sup>C Master Specification (Please refer to the Philips Semiconductor Standard I<sup>2</sup>C-Bus Specification for details on I<sup>2</sup>C bus protocols). The hub's I<sup>2</sup>C EEPROM interface is designed to attach to a single "dedicated" I<sup>2</sup>C EEPROM, and conforms to the Standard-mode I<sup>2</sup>C Specification (100 kbit/s transfer rate and 7-bit addressing) for protocol and electrical compatibility.

**Note:** Extensions to the I<sup>2</sup>C Specification are not supported. The hub acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions.

### 7.2.2.1 Implementation Characteristics

The hub will only access an EEPROM using the sequential read protocol.

### 7.2.2.2 Pull-Up Resistor

The circuit board designer is required to place external pull-up resistors (10 kΩ recommended) on the SDA/SMBDATA/ NON\_REM1 and SCL/SMBCLK/CFG\_SEL0 lines (per SMBus 1.0 Specification, and EEPROM manufacturer guidelines) to VDD in order to assure proper operation.

### 7.2.2.3 I<sup>2</sup>C EEPROM Slave Address

Slave address is 1010000.

**Note:** 10-bit addressing is NOT supported.

## 7.2.3 IN-CIRCUIT EEPROM PROGRAMMING

The EEPROM can be programmed via ATE (Automatic Test Equipment) by pulling RESET\_N low (which tri-states the hub's EEPROM interface and allows an external source to program the EEPROM).

7.3 SMBus Slave Interface

Instead of loading user-defined descriptor data from an external EEPROM, the Microchip hub can be configured to receive a code load from an external processor via an SMBus interface. The SMBus interface shares the same pins as the EEPROM interface; if CFG\_SEL1 & CFG\_SEL0 activates the SMBus interface, external EEPROM support is no longer available (and the user-defined descriptor data must be downloaded via the SMBus). The Microchip hub waits indefinitely for the SMBus code load to complete and only “appears” as a newly connected device on USB after the code load is completed.

The hub’s SMBus implementation is a *slave-only* SMBus device. The implementation only supports read block and write block protocols. The hub responds to other protocols as described in [Section 7.3.2, “Invalid Protocol Response Behavior,” on page 33](#). Reference to the System Management Bus Specification, Rev 1.0.

The SMBus interface is used to read and write the registers in the device. The register set is shown in [Section 7.2.1, “Internal Register Set \(Common to EEPROM and SMBus\),” on page 16](#).

7.3.1 BUS PROTOCOLS

Typical write block and read block protocols are shown below. Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading indicates the hub driving data on the SMBDATA line; otherwise, host data is on the SDA/SMBDATA/NON\_REM1 line.

The slave address is the unique SMBus Interface Address for the hub that identifies it on SMBus. The register address field is the internal address of the register to be accessed. The register data field is the data that the host is attempting to write to the register or the contents of the register that the host is attempting to read.

**Note:** Data bytes are transferred MSB first.

7.3.1.1 Block Read/Write

The block write begins with a slave address and a write condition. After the command code, the host issues a byte count, which describes how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block read or write is allowed to transfer a maximum of 32 data bytes.

**Note:** For the following SMBus tables:

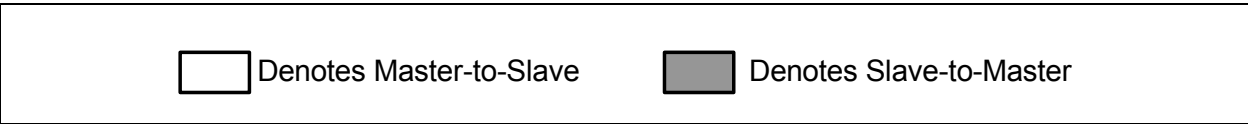
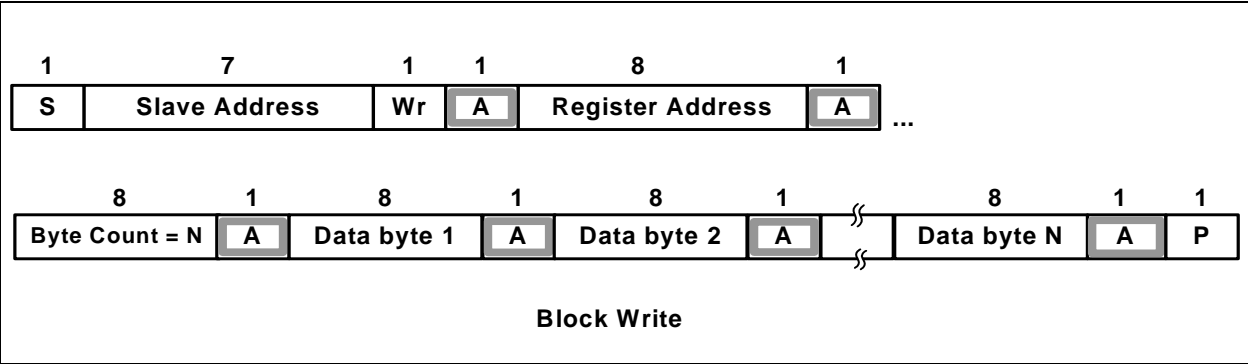


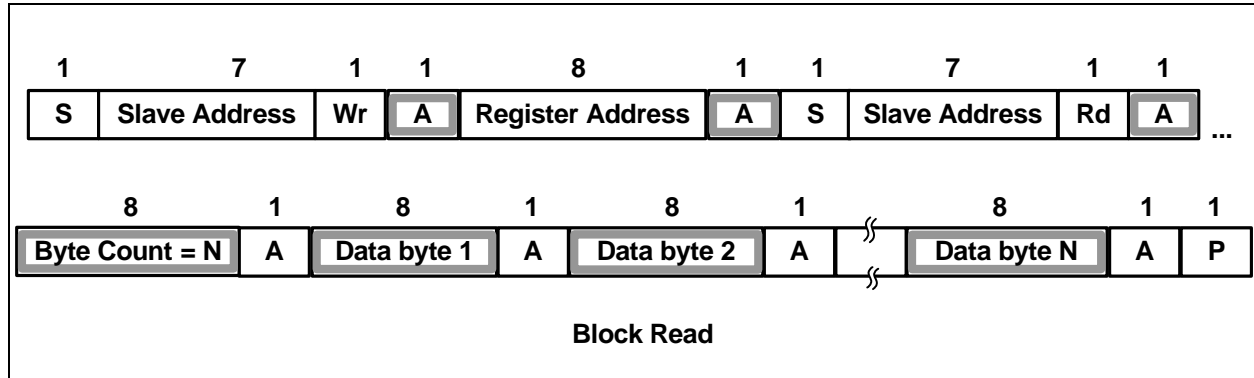
FIGURE 7-1: BLOCK WRITE



## 7.3.1.2 Block Read

A block read differs from a block write in that the repeated start condition exists to satisfy the I<sup>2</sup>C specification's requirement for a change in the transfer direction.

**FIGURE 7-2: BLOCK READ**



## 7.3.2 INVALID PROTOCOL RESPONSE BEHAVIOR

Registers accessed with an invalid protocol are not updated. A register is only updated following a valid protocol. The only valid protocols are write block and read block, which are described above.

The hub only responds to the hardware selected Slave Address (0101100x).

Attempting to communicate with the hub over SMBus with an invalid slave address or invalid protocol results in no response, and the SMBus Slave Interface returns to the idle state.

The only valid registers that are accessible by the SMBus slave address are the registers defined in the Registers Section. The hub does not respond to undefined registers.

## 7.3.3 GENERAL CALL ADDRESS RESPONSE

The hub does not respond to a general call address of 0000\_000b.

## 7.3.4 SLAVE DEVICE TIME-OUT

According to the SMBus Specification, version 1.0 devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25 ms ( $T_{\text{TIMEOUT, MIN}}$ ). Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than 35 ms ( $T_{\text{TIMEOUT, MAX}}$ ).

**Note:** Some simple devices do not contain a clock low drive circuit; this simple kind of device typically resets its communications port after a start or stop condition. The slave device time-out must be implemented.

## 7.3.5 STRETCHING THE SCLK SIGNAL

The hub supports stretching of the SCLK by other devices on the SMBus. The hub does not stretch the SCLK.

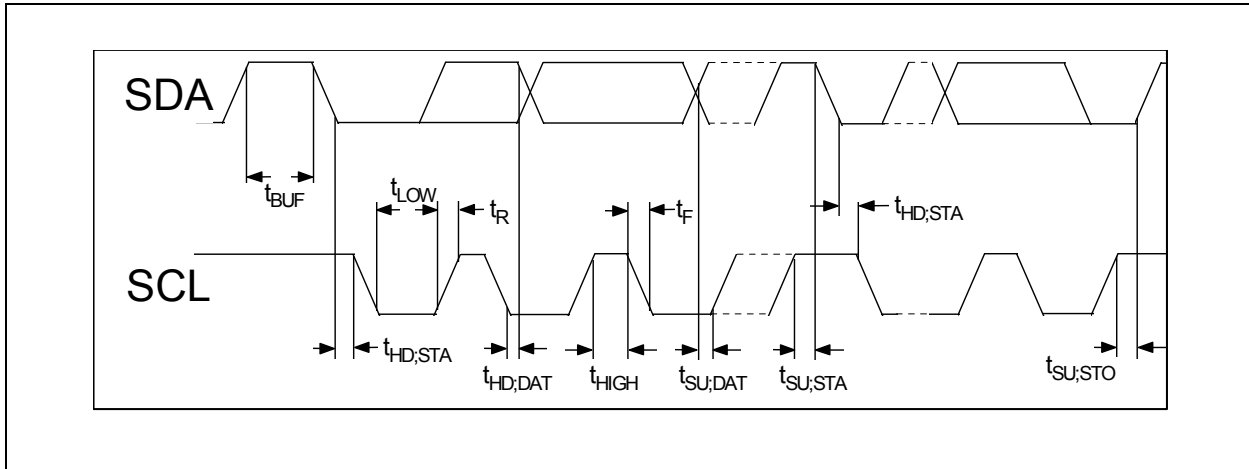


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## 7.3.6 SMBus/I<sup>2</sup>C TIMING

The SMBus slave interface complies with the SMBus AC Timing Specification.

**FIGURE 7-3: SMBus/I<sup>2</sup>C TIMING PARAMETERS**



| Symbol              | Parameter                   | Min  | Typ | Max | Unit |
|---------------------|-----------------------------|------|-----|-----|------|
| fSCL                | SCL Clock Frequency         | -    | -   | 100 | kHz  |
| t <sub>BUF</sub>    | Bus Free Time               | 4.7  | -   | -   | μs   |
| t <sub>SU;STA</sub> | START Condition Set-Up Time | 4.7  | -   | -   | μs   |
| t <sub>HD;STA</sub> | START Condition Hold Time   | 4.0  | -   | -   | μs   |
| t <sub>LOW</sub>    | SCL LOW Time                | 4.7  | -   | -   | μs   |
| t <sub>HIGH</sub>   | SCL HIGH Time               | 4.0  | -   | -   | μs   |
| t <sub>R</sub>      | SCL and SDA Rise Time       | -    | -   | 1.0 | μs   |
| t <sub>F</sub>      | SCL and SDA Fall Time       | -    | -   | 0.3 | μs   |
| t <sub>SU;DAT</sub> | Data Set-Up Time            | 0.25 | -   | -   | μs   |
| t <sub>HD;DAT</sub> | Data Hold Time              | 0.25 | -   | -   | μs   |
| t <sub>SU;STO</sub> | STOP Condition Set-Up Time  | 4.0  | -   | -   | μs   |

## 7.3.7 BUS RESET SEQUENCE

The SMBus slave interface resets and returns to the idle state upon a START field followed immediately by a STOP field.

### 7.3.7.1 Undefined Registers

The registers shown in Table 7-2 are the defined registers in the hub. Reads to undefined registers return to 00h. Writes to undefined registers have no effect and do not return an error.

### 7.3.7.2 Reserved Registers

Only a '0' should be written to all reserved registers or bits.

## 7.4 Default Configuration Option

To configure the hub in its default configuration, strap the CFG\_SEL1 to 0 and CFG\_SEL0 to 0. This configures the hub to the internal defaults and enables the strapping options. (Please see [Section 7.2.1, "Internal Register Set \(Common to EEPROM and SMBus\)"](#) for the list of the default values.) For specific pin strapping options, please see [Chapter 6.0, Pin Descriptions](#) for instructions on how to modify the default values. Options include port disable and non-removable pin strapping.

## 7.5 Reset

There are two different resets that the hub experiences. One is a hardware reset via the external RESET\_N pin and the second is via the USB Bus Reset.

### 7.5.1 EXTERNAL HARDWARE RESET\_N

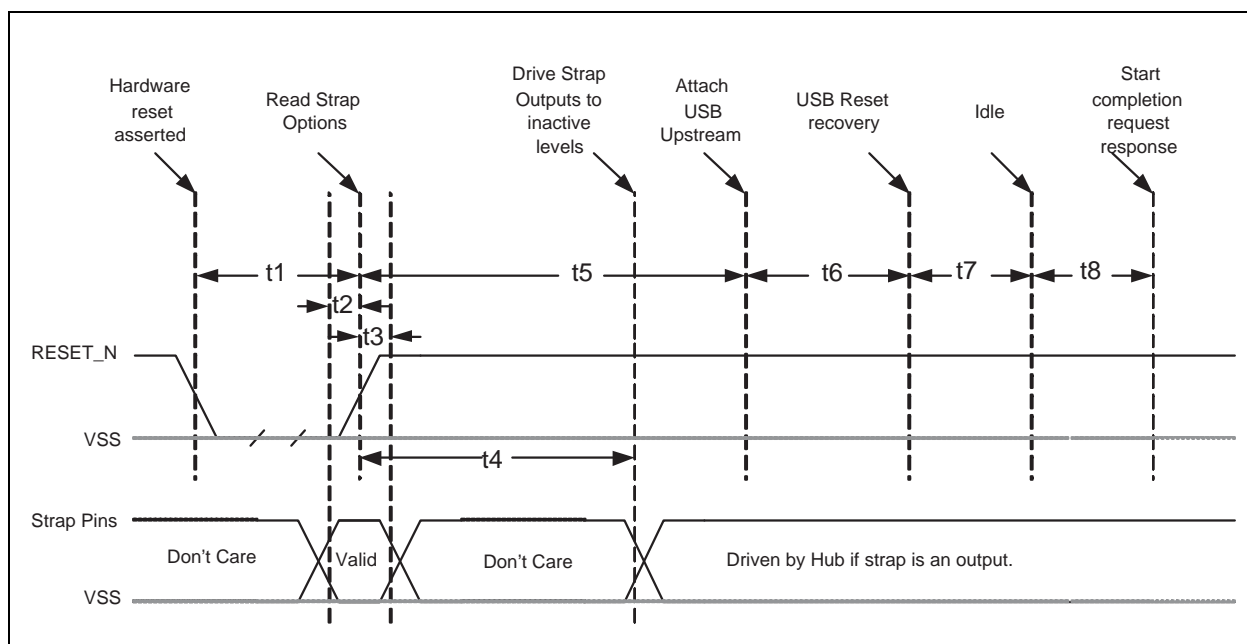
A valid hardware reset is defined as assertion of RESET\_N for a minimum of 1 $\mu$ s after all power supplies are within operating range. While reset is asserted, the hub (and its associated external circuitry) consumes less than 500  $\mu$ A of current from the upstream USB power source.

Assertion of RESET\_N (external pin) causes the following:

1. All downstream ports are disabled, and PRTPOWER to downstream devices is removed.
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00(h)).
5. The external crystal oscillator is halted.
6. The PLL is halted.

The hub is "operational" 500  $\mu$ s after RESET\_N is negated. Once operational, the hub configures itself based on the settings of pins CFG\_SEL[1:0]. See [Table 7-1, "Hub Configuration Options,"](#) on page 15.

**FIGURE 7-4: RESET\_N TIMING FOR DEFAULT/STRAP OPTION MODE**



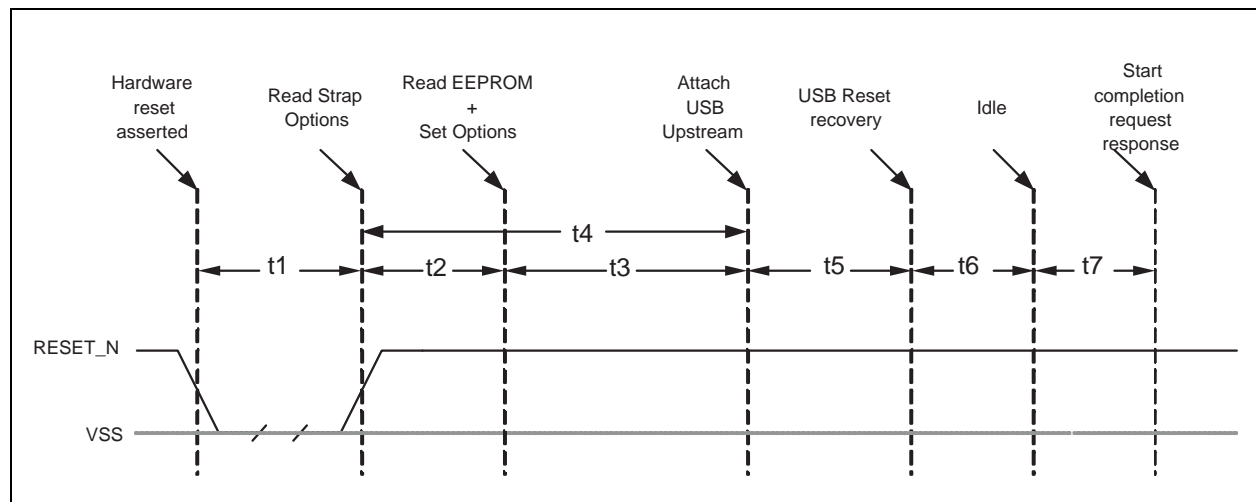
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| Name | Description  | Min  | Typ       | Max  | Unit |
|------|--|------|-----------|------|------|
| t1   | RESET_N Asserted   | 1    | -         | -    | μsec |
| t2   | Strap Setup Time   | 16.7 | -         | -    | nsec |
| t3   | Strap Hold Time  | 16.7 | -         | 1400 | nsec |
| t4   | Hub outputs driven to inactive logic states                      | -    | 1.5       | 2    | μsec |
| t5   | USB Attach (see <a href="#">Note 1:</a> and <a href="#">2:</a> ) | -    | -         | 100  | msec |
| t6   | Host acknowledges attach and signals USB Reset                   | 100  | -         | -    | msec |
| t7   | USB Idle   | -    | undefined | -    | msec |
| t8   | Completion time for requests (with or without data stage)        | -    | -         | 5    | msec |

- Note 1:** In bus-powered mode, the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t1+t5.
- 2:** All power supplies must have reached the operating levels mandated in Chapter [8.0, DC Parameters](#) prior to (or coincident with) the assertion of RESET\_N.

## 7.5.1.1 RESET\_N for EEPROM Configuration

**FIGURE 7-5: RESET\_N TIMING FOR EEPROM MODE**



| Name | Description  | Min | Typ       | Max  | Units |
|------|--|-----|-----------|------|-------|
| t1   | RESET_N Asserted   | 1   | -         | -    | μsec  |
| t2   | Hub Recovery/Stabilization                                       | -   | -         | 500  | μsec  |
| t3   | EEPROM Read / Hub Config   | -   | 2.0       | 99.5 | msec  |
| t4   | USB Attach (see <a href="#">Note 1:</a> and <a href="#">2:</a> ) | -   | -         | 100  | msec  |
| t5   | Host acknowledges attach and signals USB Reset                   | 100 | -         | -    | msec  |
| t6   | USB Idle   | -   | undefined | -    | msec  |
| t7   | Completion time for requests (with or without data stage)        | -   | -         | 5    | msec  |

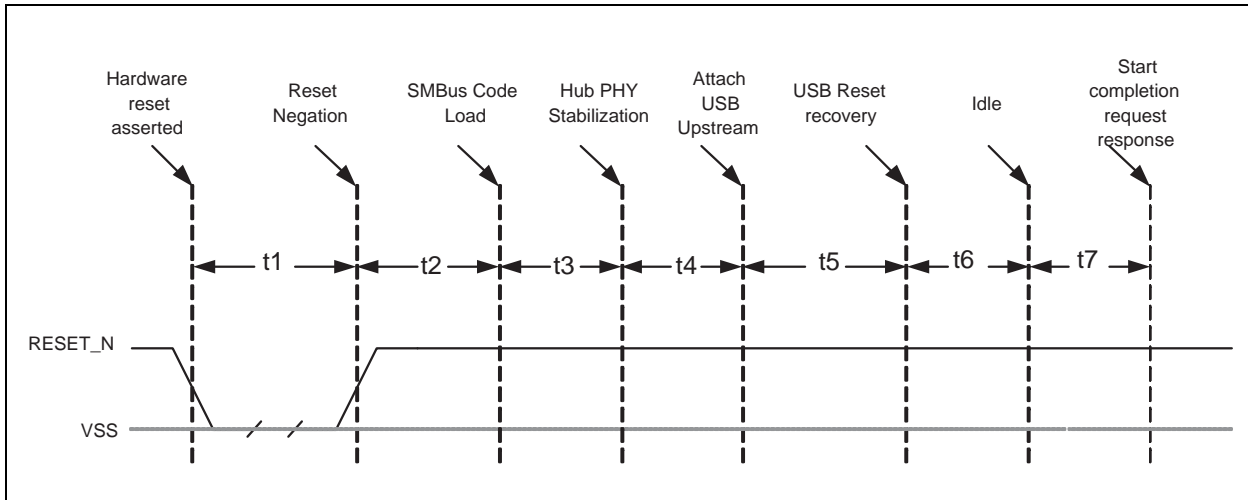
**Note 1:** When in bus-powered mode, the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t4+t5+t6+t7.

**2:** All power supplies must have reached the operating levels mandated in Chapter 8.0, [DC Parameters](#), prior to (or coincident with) the assertion of RESET\_N.

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## 7.5.1.2 RESET\_N for SMBus Slave Configuration

**FIGURE 7-6: RESET\_N TIMING FOR SMBUS MODE**



| Name | Description  | Min | Typ       | Max | Units |
|------|--|-----|-----------|-----|-------|
| t1   | RESET_N Asserted   | 1   | -         | -   | μsec  |
| t2   | Hub Recovery/Stabilization   | -   | -         | 500 | μsec  |
| t3   | SMBus Code Load  | -   | 250       | 300 | msec  |
| t4   | Hub Configuration and USB Attach (see <a href="#">Note 1:</a> and <a href="#">2:</a> ) | -   | -         | 100 | msec  |
| t5   | Host acknowledges attach and signals USB Reset   | 100 | -         | -   | msec  |
| t6   | USB Idle   | -   | Undefined | -   | msec  |
| t7   | Completion time for requests (with or without data stage)                              | -   | -         | 5   | msec  |

**Note 1:** For bus-powered configurations the maximum time is 99.5 ms, and the hub and its associated circuitry must not consume more than 100 mA from the upstream USB power source during t2+t3+t4+t5+t6+t7. For Self-Powered configurations, t3 MAX is not applicable and the time to load the configuration is determined by the external SMBus host.

**2:** All power supplies must have reached the operating levels mandated in [Chapter 8.0, DC Parameters](#), prior to (or coincident with) the assertion of RESET\_N.

## 7.5.2 USB BUS RESET

In response to the upstream port signaling a reset to the hub, the hub does the following:

1. Sets default bus address to '0'.
2. Sets configuration to: Unconfigured.
3. Negates PRTPWR[4:1] to all downstream ports.
4. Clears all TT buffers.
5. Moves device from suspended to active (if suspended).
6. Complies with Section 11.10 of the USB 2.0 Specification for behavior after completion of the reset sequence. The host then configures the hub and the hub's downstream port devices in accordance with the USB Specification.

**Note:** The hub does not propagate the upstream USB reset to downstream devices.

## 8.0 DC PARAMETERS

### 8.1 Maximum Guaranteed Ratings

| Parameter              | Symbol  | Min  | Max                     | Units | Comments |
|------------------------|---|------|-------------------------|-------|----------|
| Storage Temperature    | $T_{\text{STOR}}$   | -55  | 150                     | °C    | -        |
| 3.3 V supply voltage   | $V_{\text{DDA33}}$ ,<br>$V_{\text{DD33PLL}}$ ,<br>$V_{\text{DD33}}$ | -0.5 | 4.0                     | V     | -        |
| Voltage on any I/O pin | -   | -0.5 | $V_{\text{DD33}} + 0.3$ | V     | -        |
| Voltage on XTAL1       | -   | -0.5 | 3.6                     | V     | -        |
| Voltage on XTAL2       | -   | -0.5 | 2.0                     | V     | -        |

**Note 1:** Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

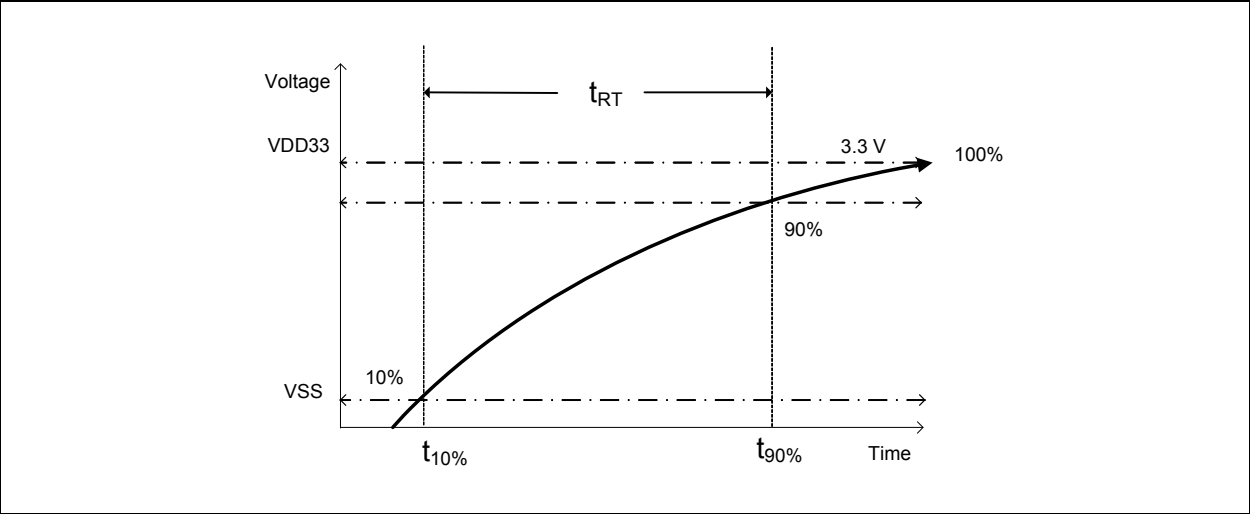
**2:** When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested to use a clamp circuit.

8.2 Operating Conditions

| Parameter                               | Symbol                                     | Min  | Max | Units | Comments   |
|---|--|------|-----|-------|--|
| 36-pin package<br>Operating Temperature | $T_A$                                      | -40  | 85  | °C    | Ambient temperature in still air.<br>(See <a href="#">Note 1:</a> )                                    |
| 3.3 V supply voltage                    | $V_{DDA33}$<br>$V_{DD33PLL}$<br>$V_{DD33}$ | 3.0  | 3.6 | V     | -  |
| 3.3 V supply rise time                  | $t_{RT}$                                   | -    | 400 | μs    | (See <a href="#">Figure 8-1</a> , "Supply Rise Time Models")<br>(See <a href="#">2:</a> )              |
| Voltage on any I/O pin                  | -  | -0.3 | 3.6 | V     | If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes:<br>(3.3 V supply voltage) + 0.5 V |
| Voltage on XTAL1                        | -  | -0.3 | 2.0 | V     | -  |
| Voltage on XTAL2                        | -  | -0.3 | 2.0 | V     | -  |

- Note 1:** The  $T_j$  (junction temperature) must not exceed 125°C.
- 2:** The rise time for the 3.3 V supply can be extended to 500 ms max if RESET\_N is actively driven low, typically by another IC, until 1 μs after all supplies are within operating range.

FIGURE 8-1: SUPPLY RISE TIME MODELS



## 8.3 Package Thermal Specifications

**TABLE 8-1: 36-PIN QFN PACKAGE THERMAL PARAMETERS**

| Parameter                  | Symbol        | Value | Unit | Comments                                  |
|----------------------------|---------------|-------|------|---|
| Thermal Resistance         | $\Theta_{JA}$ | 39    | °C/W | Measured from the die to the ambient air. |
| Junction-to-Top-of-Package | $\Psi_{JT}$   | 0.3   | °C/W | -   |

**Note:** Thermal parameters are measured or estimated for devices with the exposed pad soldered to thermal vias in a multilayer 2S2P PCB per JESD51.

## 8.4 DC Electrical Characteristics

**TABLE 8-2: DC ELECTRICAL CHARACTERISTICS**

| Parameter                                | Symbol     | Min | Typ | Max  | Units | Comments                                       |
|--|------------|-----|-----|------|-------|--|
| <b>I, IS Type Input Buffer</b>           | -          | -   | -   | -    | -     |  |
| Low Input Level                          | $V_{ILI}$  | -   | -   | 0.8  | V     | TTL Levels                                     |
| High Input Level                         | $V_{IHI}$  | 2.0 | -   | -    | V     |  |
| Input Leakage                            | $I_{IL}$   | -10 | -   | +10  | μA    | $V_{IN} = 0$ to $V_{DD33}$                     |
| Hysteresis ('IS' Only)                   | $V_{HYSI}$ | 250 | -   | 600  | mV    |  |
| <b>Input Buffer with Pull-Up (IPU)</b>   |            |     |     |      |       |  |
| Low Input Level                          | $V_{ILI}$  | -   | -   | 0.8  | V     | TTL Levels                                     |
| High Input Level                         | $V_{IHI}$  | 2.0 | -   | -    | V     | -  |
| Low Input Leakage                        | $I_{ILL}$  | +20 | -   | +110 | μA    | $V_{IN} = 0$                                   |
| High Input Leakage                       | $I_{IHL}$  | -10 | -   | +10  | μA    | $V_{IN} = V_{DD33}$                            |
| IPU Buffer Float Voltage                 | $V_{IPUF}$ |     | 2.0 |      | V     | Voltage at the IPU pin when floated. (Note 3:) |
| <b>Input Buffer with Pull-Down (IPD)</b> |            |     |     |      |       |  |
| Low Input Level                          | $V_{ILI}$  | -   | -   | 0.8  | V     | TTL Levels                                     |
| High Input Level                         | $V_{IHI}$  | 2.0 | -   |      | V     | -  |
| Low Input Leakage                        | $I_{ILL}$  | +10 | -   | -10  | μA    | $V_{IN} = 0$                                   |
| High Input Leakage                       | $I_{IHL}$  | -20 | -   | -100 | μA    | $V_{IN} = V_{DD33}$                            |



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**TABLE 8-2: DC ELECTRICAL CHARACTERISTICS (CONTINUED)**

| Parameter                                   | Symbol        | Min | Typ | Max | Units   | Comments                                |
|---|---------------|-----|-----|-----|---------|---|
| <b>ICLK Input Buffer</b>                    |               |     |     |     |         |   |
| Low Input Level                             | $V_{ILCK}$    | -   | -   | 0.5 | V       | -                                       |
| High Input Level                            | $V_{IHCK}$    | 1.4 | -   | -   | V       | -                                       |
| Input Leakage                               | $I_{IL}$      | -10 | -   | +10 | $\mu A$ | $V_{IN} = 0$ to $V_{DD33}$              |
| <b>O12, I/O12 &amp; I/OSD12 Type Buffer</b> |               |     |     |     |         |   |
| Low Output Level                            | $V_{OL}$      | -   | -   | 0.4 | V       | $I_{OL} = 12$ mA @ $V_{DD33} = 3.3$ V   |
| High Output Level                           | $V_{OH}$      | 2.4 | -   | -   | V       | $I_{OH} = -12$ mA @ $V_{DD33} = 3.3$ V  |
| Output Leakage                              | $I_{OL}$      | -10 | -   | +10 | $\mu A$ | $V_{IN} = 0$ to $V_{DD33}$<br>(Note 1:) |
| Hysteresis ('SD' pad only)                  | $V_{HYSC}$    | 250 | -   | 600 | mV      |   |
| <b>IO-U</b><br>(Note 2:)                    | -             | -   | -   | -   | -       | -                                       |
| <b>USB82514</b>                             |               |     |     |     |         |   |
| Supply Current Unconfigured                 |               |     |     |     |         |   |
| Hi-Speed Host                               | $I_{CCINTHS}$ | -   | 85  | 100 | mA      | No device connected                     |
| Full-Speed Host                             | $I_{CCINTFS}$ | -   | 72  | -   | mA      |   |
| Supply Current Configured (Hi-Speed Host)   |               |     |     |     |         | All supplies combined                   |
| 1 Port @ HS                                 | $I_{HCH1}$    | -   | 225 | -   | mA      | Device connected                        |
| 2 Ports @ HS                                | $I_{HCH2}$    | -   | 255 | -   | mA      |   |
| 3 Ports @ HS                                | $I_{HCH3}$    | -   | 260 | -   | mA      |   |
| 4 Ports @ HS                                | $I_{HCH4}$    | -   | 260 | 300 | mA      |   |
| Supply Current Configured (Full-Speed Host) |               |     |     |     |         | All supplies combined                   |
| 1 Port @ FS                                 | $I_{HCH1}$    | -   | 150 | -   | mA      |   |
| 2 Ports @ FS                                | $I_{HCH2}$    | -   | 160 | -   | mA      |   |
| 3 Ports @ FS                                | $I_{HCH3}$    | -   | 160 | -   | mA      |   |
| 4 Ports @ FS                                | $I_{HCH4}$    | -   | 160 | -   | mA      |   |
| Supply Current Suspend                      | $I_{CSBY}$    | -   | 325 | -   | $\mu A$ | All supplies combined                   |
| Supply Current Reset                        | $I_{CRST}$    | -   | 115 | -   | $\mu A$ | All supplies combined                   |

**Note 1:** Output leakage is measured with the current pins in high impedance.

**2:** See USB 2.0 Specification for USB DC Electrical Characteristics.

**3:** When the IPU type pin is floated, the internal logic will interpret this as logic high. IPU buffer pins include an internal pull up and level shifter. IPU pins float to ~2.0 V with external loads less than 10  $\mu A$ . This ensures the internal level shifted voltage is above the high level threshold for the internal logic.

## 8.5 Capacitance

TA = 25°C; fc = 1 MHz; VDD33 = 3.3 V

**TABLE 8-3: PIN CAPACITANCE**

| Parameter               | Symbol            | Limits |     |     | Unit | Test Condition   |
|-------------------------|-------------------|--------|-----|-----|------|--|
|                         |                   | Min    | Typ | Max |      |  |
| Clock Input Capacitance | C <sub>XTAL</sub> | -      | -   | 2   | pF   | All pins except USB pins (and pins under test tied to AC ground) |
| Input Capacitance       | C <sub>IN</sub>   | -      | -   | 10  | pF   |  |
| Output Capacitance      | C <sub>OUT</sub>  | -      | -   | 20  | pF   |  |

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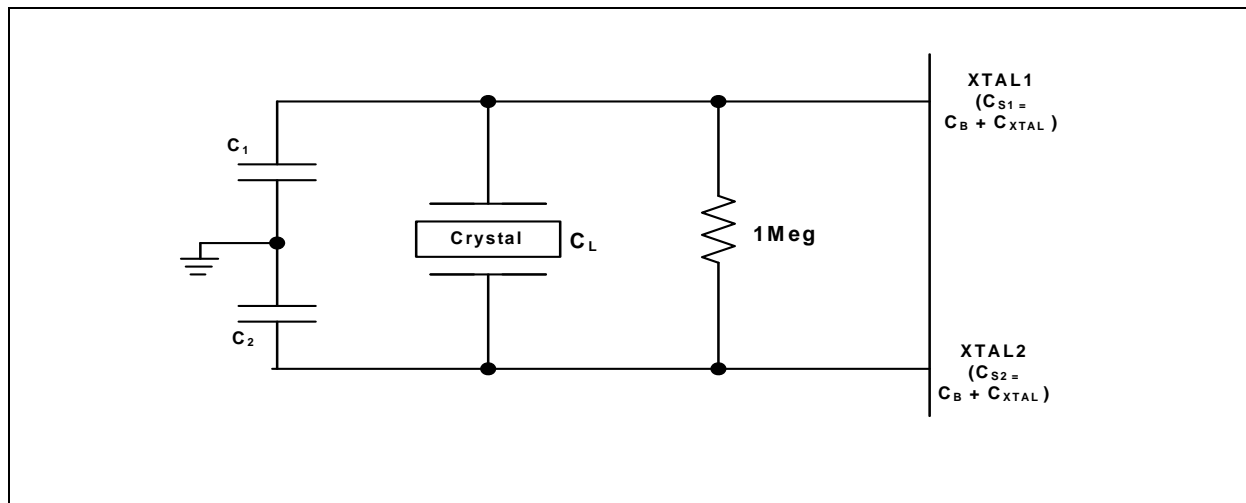
## 9.0 AC SPECIFICATIONS

### 9.1 Oscillator/Clock

Crystal: Parallel Resonant, Fundamental Mode, 24 MHz  $\pm$  350 ppm.

External Clock: 50% Duty cycle  $\pm$  10%, 24 MHz  $\pm$  350 ppm, Jitter < 100 ps rms.

**FIGURE 9-1: TYPICAL CRYSTAL CIRCUIT**



**Note:** C<sub>B</sub> equals total board/trace capacitance.

**FIGURE 9-2: FORMULA TO FIND VALUE OF C<sub>1</sub> AND C<sub>2</sub>**

$$C_L = \frac{(C_1 + C_{S1}) \times (C_2 + C_{S2})}{(C_1 + C_{S1} + C_2 + C_{S2})}$$

#### 9.1.1 SMBus INTERFACE

The Microchip hub is designed to meet the specifications as set forth in the SMBus 1.0 Specification for Slave-Only devices (except as noted in [Section 7.3, "SMBus Slave Interface"](#)).

#### 9.1.2 I<sup>2</sup>C EEPROM

Frequency is fixed at 60 kHz  $\pm$  20%.


#### 9.1.3 USB 2.0

The Microchip hub is designed to comply with the USB 2.0 Specification (Revision 2.0 from April 27, 2000 and the 12/7/2000 and 5/28/2002 Errata). Please refer to the USB 2.0 Specification for more information.

## 10.0 PACKAGE INFORMATION

### 10.1 Package Marking Information

36-QFN (6x6 mm),  
36-QFN Dimple (6x6 mm)



PIN 1

|                |  |
|----------------|--|
| <b>Legend:</b> | <div style="display: flex; align-items: flex-start;"> <div style="margin-right: 10px;">x</div> <div>Kind of package (refer to Product Identification System)</div> </div> <div style="margin-top: 5px;"> <div style="display: flex; align-items: flex-start;"> <div style="margin-right: 10px;">lll</div> <div>Lot Sequence Code</div> </div> <div style="margin-top: 5px;"> <div style="display: flex; align-items: flex-start;"> <div style="margin-right: 10px;">r</div> <div>Chip Revision Number</div> </div> <div style="margin-top: 5px;"> <div style="display: flex; align-items: flex-start;"> <div style="margin-right: 10px;">yy</div> <div>last two digits of Assembly Year</div> </div> <div style="margin-top: 5px;"> <div style="display: flex; align-items: flex-start;"> <div style="margin-right: 10px;">ww</div> <div>Assembly Work Week</div> </div> <div style="margin-top: 5px;"> <div style="display: flex; align-items: flex-start;"> <div style="margin-right: 10px;">tttttttttt</div> <div>Tracking Number (up to 12 characters)</div> </div> <div style="margin-top: 5px;"> <div style="display: flex; align-items: flex-start;"> <div style="margin-right: 10px;">cc</div> <div>Country of Original Abbreviation (Optional - up to 2 characters)</div> </div> </div> </div> </div> </div> </div></div> |
| <b>Note:</b>   | <p>In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.</p>   |

\* Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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## 10.2 Package Drawings

**Note:** For the most current package drawings, see the Microchip Packaging Specification at:  
<http://www.microchip.com/packaging>.

**FIGURE 10-1: 36-PIN QFN, 6X6 mm<sup>2</sup> BODY, 0.5 mm PITCH (DIMPLE PACKAGE)**

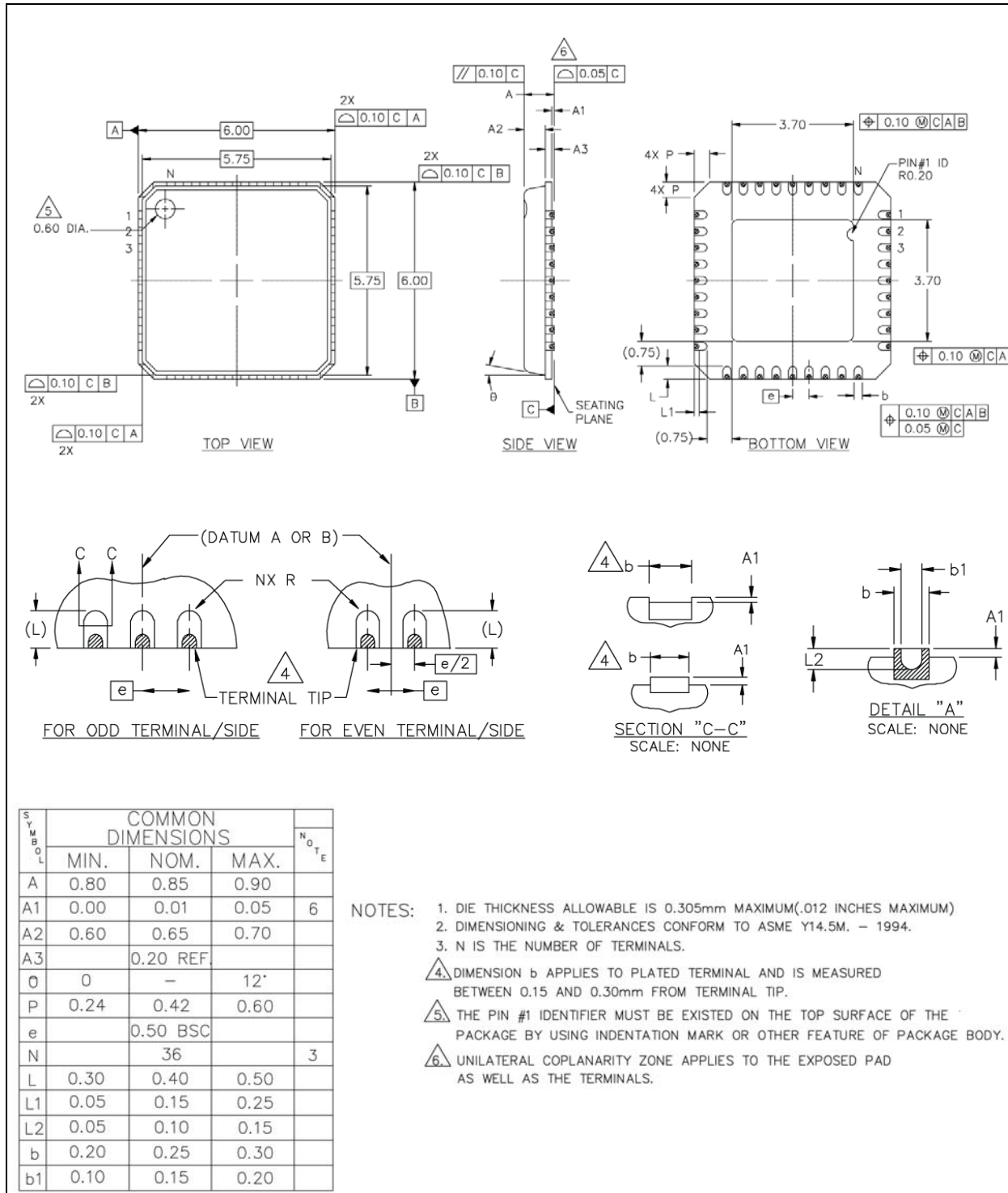
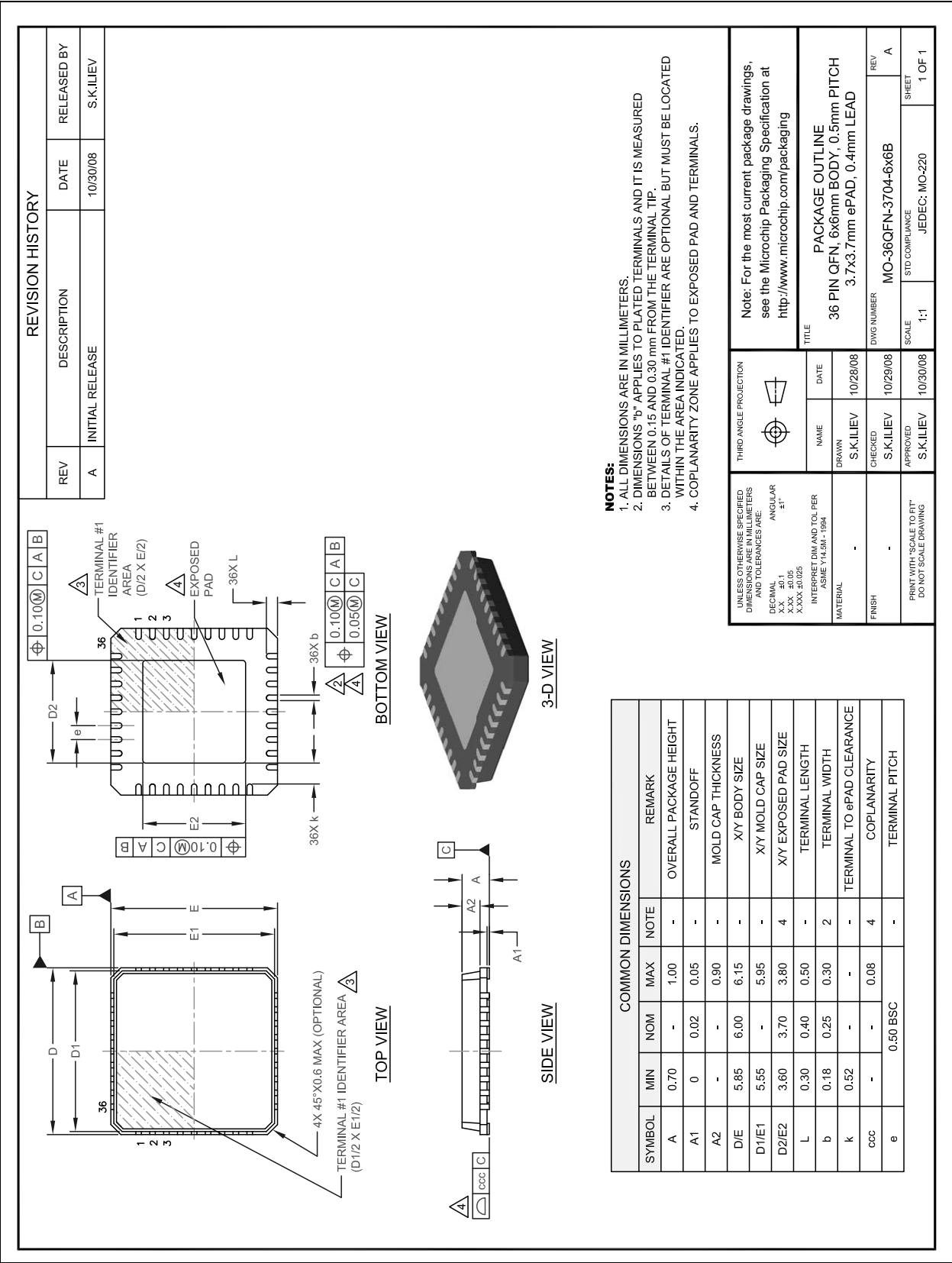


FIGURE 10-2: 36-PIN QFN, 6X6 mm<sup>2</sup> BODY, 0.5 mm PITCH



## APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: CUSTOMER REVISION HISTORY

| REVISION LEVEL & DATE  | SECTION/FIGURE/ENTRY  | CORRECTION   |
|------------------------|---|--|
| DS60001234C (02-01-17) | Product Identification System   | Adopted according to new system.   |
|                        | Chapter 3.0, Pin Configuration  | Package marking information (legend) moved to Chapter 10.0, Package Information  |
|                        | Chapter 10.0, Package Information   | New section Section 10.1, "Package Marking Information"  |
| DS60001234B (06-04-14) | All   | Version migrated to Microchip template   |
|                        | Cover Sheet   | Trueauto remark removed, dimple package added  |
|                        | Chapter 3.0, Pin Configuration  | Figure 3-1 improved: USB82514AM -> USB82514Ax (generalized description), added in legend   |
|                        | Chapter 10.0, Package Information   | Normal QFN package (no dimple) corrected (56 pins -> 36 pins)  |
| DS60001234A (10-04-13) | All   | Microchip DS number inserted.<br>Revision A replaces the previous SMSC version Rev. 1.4<br>Trademark and last page according to Microchip guidelines.<br>SMSC branding removed |
|                        | Page 2  | Order numbers added for both packages  |
|                        | Chapter 3.0, Pin Configuration  | PB free information removed in Figure 3-1.   |
|                        | Chapter 10.0, Package Information   | New version includes both packages   |
| Rev. 1.4 (08-14-13)    | Chapter 10.0, Package Information   | New package added  |
| Rev. 1.3 (06-10-13)    | All   | Order numbers modified according to Microchip guideline.   |
|                        | All   | 'Lead-free' remark removed in the document   |
| Rev. 1.3 (04-04-13)    | Section 7.2.1.14, "Register 0Dh: Max Power for Bus-Powered Operation"                   | Added sentence:<br>A value of 50 (decimal) indicates 100 mA, which is the default value.   |
|                        | Section 7.2.1.15, "Register 0Eh: Hub Controller Max Current for Self-Powered Operation" | Removed sentence:<br>A value of 50 (decimal) indicates 100 mA, which is the default value.   |
|                        | Section 8.1, "Maximum Guaranteed Ratings"   | Row 3.3 V supply voltage: Min value added: -0.5 V  |
| Rev. 1.2 (09-26-12)    | All   | Microchip style implemented (logo and legend).   |
|                        | Section 7.5.1, "External Hardware RESET_N"  | CFG_SEL[2:0] -> CFG_SEL[1:0]   |

**TABLE A-1: CUSTOMER REVISION HISTORY (CONTINUED)**

| REVISION LEVEL & DATE  | SECTION/FIGURE/ENTRY  | CORRECTION   |
|------------------------|---|--|
| Rev. 1.1<br>(11-18-11) | <a href="#">Section 8.4, "DC Electrical Characteristics"</a>  | $V_{IPUF}$ (IPU Buffer Float Voltage) added in <a href="#">Table 8-3</a> .   |
| Rev. 1.1<br>(11-17-11) | <a href="#">Chapter 3.0, Pin Configuration</a>                | <a href="#">Figure 3-1</a> improved:   |
| Rev. 1.1<br>(11-09-11) | <a href="#">Chapter 3.0, Pin Configuration</a>                | Topmark information added in <a href="#">Figure 3-1</a> . Package designators described.                                       |
|                        | <a href="#">Section 8.2, "Operating Conditions"</a>           | Max value corrected for 'voltage on any I/O pin': 3.6 V  |
|                        | <a href="#">Section 8.5, "Capacitance"</a>                    | VDD18, VDDPLL 0 1.8 V replaced by VDD33 = 3.3 V  |
| Rev. 1.1<br>(07-19-11) | <a href="#">Section 8.2, "Operating Conditions"</a>           | In the table: Added Note 8.4 under Note 8.3. Added reference to Note 8.4 in the comments column for 3.3 V rise time parameter. |
| Rev. 1.1<br>(05-30-11) | <a href="#">Chapter 6.0, Pin Descriptions</a>                 | VBUS_DET is an input. Buffer type changed from "I/O12" to "I".   |
| Rev. 1.1<br>(05-04-11) | <a href="#">Section 8.2, "Operating Conditions"</a>           | Max value corrected for XTAL1 and XTAL2: 2.0 V   |
| Rev. 1.1<br>(03-21-11) | <a href="#">Chapter 6.0, Pin Descriptions</a>                 | The internal regulator cannot be turned off.   |
|                        | <a href="#">Section 8.1, "Maximum Guaranteed Ratings"</a>     | The chip does not have an external 1.8 V supply. Max value of 3.3 V supply voltages changed from 4.6 V to 4.0 V.               |
|                        | <a href="#">Section 8.2, "Operating Conditions"</a>           | The chip does not have an external 1.8 V supply.   |
| Rev. 1.0<br>(10-19-10) | <a href="#">Section 8.1, "Maximum Guaranteed Ratings"</a>     | Max value corrected for 'voltage on any I/O pin': 5.5 -> $V_{DD33} + 0.3$  |
| Rev. 1.0<br>(10-12-10) | Page 2  | Order information completed.   |
| Rev. 1.0<br>(09-02-09) | <a href="#">Section 8.3, "Package Thermal Specifications"</a> | TBD values have been specified.  |
| Rev. 0.8<br>(08-28-09) | <a href="#">Section 8.4, "DC Electrical Characteristics"</a>  | TBD values have been specified.  |
| Rev. 0.7<br>(03-13-09) | All   | Confidential designation removed from document.  |
| Rev. 0.7<br>(12-01-08) | Initial Release   |  |



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| <u>PART NO.</u>       | <u>[X]</u>        | <u>X</u>                       | <u>[X]<sup>(1)</sup></u> | <u>-</u> | <u>X</u> | <u>-<sup>(2)</sup></u> | <u>Vxx</u> |
|-----------------------|-------------------|--------------------------------|--------------------------|----------|----------|------------------------|------------|
| Device                | Temperature Range | Package                        | Tape and Reel Option     |          | Pattern  |                        | Designator |
| Device:               | USB82514          |                                |                          |          |          |                        |            |
| Temperature Range:    | A                 | = -40°C to +85°C               |                          |          |          |                        |            |
| Package:              | M                 | = QFN (36-pin)                 |                          |          |          |                        |            |
|                       | F                 | = QFN Dimple Package (36-pin)  |                          |          |          |                        |            |
| Tape and Reel Option: | Blank             | = Standard packaging (tray)    |                          |          |          |                        |            |
|                       | R                 | = Tape and Reel <sup>(1)</sup> |                          |          |          |                        |            |
| Pattern:              | A                 | = Product Version              |                          |          |          |                        |            |
|                       | B                 | = Product Version              |                          |          |          |                        |            |
| Designator:           | Vxx               | = Automotive Designator        |                          |          |          |                        |            |

**Examples:**

a) USB82514AMR-A-V03  
-40°C to + 85°C,  
QFN (36-pin),  
Tape & Reel,  
A,  
V03

b) USB82514AF-B-V06  
-40°C to + 85°C,  
QFN dimple package (36-pin),  
Tray,  
B,  
V06

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**Note 2:** “-” is optional. Check with your Microchip Sales Office for exact ordering part number.

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