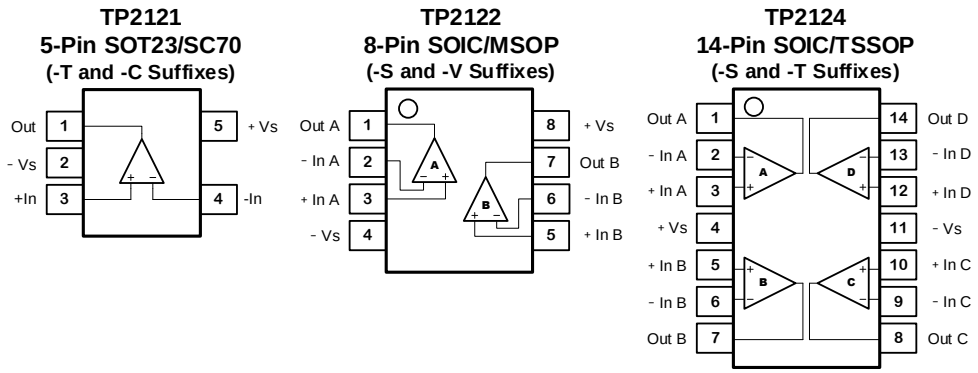
1.8V, 600nA Nanopower, Rail-to-Rail Input/Output Op-amps

Pin Configuration (Top View)



Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP2121	TP2121-TR	5-Pin SOT23	Tape and Reel, 3,000	B2TYW (1)
	TP2121-CR	5-Pin SC70	Tape and Reel, 3,000	B2CYW (1)
TP2122	TP2122-SR	8-Pin SOIC	Tape and Reel, 4,000	B22S
	TP2122-VR	8-Pin MSOP	Tape and Reel, 3,000	B22V
TP2124	TP2124-SR	14-Pin SOIC	Tape and Reel, 2,500	B24S
	TP2124-TR	14-Pin TSSOP	Tape and Reel, 3,000	B24T

Note (1): 'YW' is date coding scheme. 'Y' stands for calendar year, and 'W' stands for single workweek coding scheme.

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ – V^–$.....6.0V
Input Voltage..... $V^–$ – 0.3 to V^+ + 0.3
Input Current: +IN, –IN, SHDN Note 2..... ±10mA
SHDN Pin Voltage……$V^–$ to V^+
Output Current: OUT..... ±20mA

Output Short-Circuit Duration Note 3..... Indefinite
Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	6	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1.5	kV

5V Electrical Characteristics

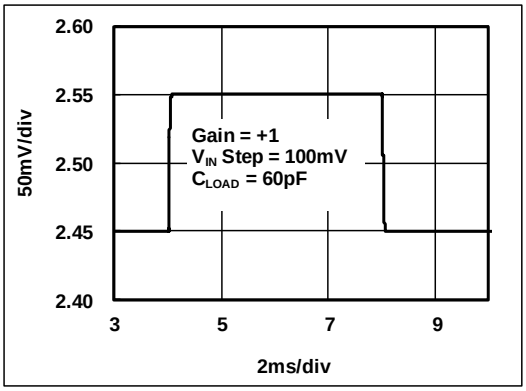
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 27°C. V_{SUPPLY} = 5V, V_{CM} = V_{OUT} = V_{SUPPLY}/2, R_L = 100kΩ, C_L =60pF, V_{SHDN} is unconnected.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V_{DD}/2 and V_{CM} = GND	●	-1.5	±0.1	+1.5	mV
V_{OS} TC	Input Offset Voltage Drift				0.5		μV/°C
I_B	Input Bias Current	T_A=27 °C			1		fA
		T_A=85 °C			700		fA
		T_A=125 °C			45		pA
I_{OS}	Input Offset Current				1		fA
V_n	Input Voltage Noise	f = 0.1Hz to 10Hz			6.5		μV_{P-P}
e_n	Input Voltage Noise Density	f = 1kHz			170		nV/√Hz
R_{IN}	Input Resistance				> 1		TΩ
C_{IN}	Input Capacitance	Differential Common Mode			2.9 5		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = 0.1V to 4.9V	●	80	130		dB
V_{CM}	Common-mode Input Voltage Range		●	V^-–0.3		V^++0.3	V
PSRR	Power Supply Rejection Ratio		●	60	92		dB
A_{VOL}	Open-Loop Large Signal Gain	V_{OUT} = 2.5V, R_{LOAD} = 100kΩ	●	80	120		dB
		V_{OUT} = 0.1V to 4.9V, R_{LOAD} = 100kΩ	●	80	120		dB
V_{OL}, V_{OH}	Output Swing from Supply Rail	R_{LOAD} = 100kΩ			5		mV
R_{OUT}	Closed-Loop Output Impedance	G = 1, f = 1kHz, I_{OUT} = 0			0.4		Ω
R_O	Open-Loop Output Impedance	f = 1kHz, I_{OUT} = 0			2.6		Ω
I_{SC}	Output Short-Circuit Current	Sink or source current			20		mA
V_{DD}	Supply Voltage			1.8		6.0	V
I_Q	Quiescent Current per Amplifier		●		600	950	nA
PM	Phase Margin	R_{LOAD} = 100kΩ, C_{LOAD} = 60pF			61		°
GM	Gain Margin	R_{LOAD} = 100kΩ, C_{LOAD} = 60pF			-10		dB
GBWP	Gain-Bandwidth Product	f = 1kHz			18		kHz
t_S	Settling Time, 1.5V to 3.5V, Unity Gain Settling Time, 2.45V to 2.55V, Unity Gain	0.1% 0.01% 0.1% 0.01%			0.25 0.253 0.035 0.038		ms
SR	Slew Rate	A_V = 1, V_{OUT} = 1.5V to 3.5V, C_{LOAD} = 60pF, R_{LOAD} = 100kΩ			10		mV/μs
FPBW	Full Power Bandwidth Note 1	$2V_{P-P}$			600		Hz

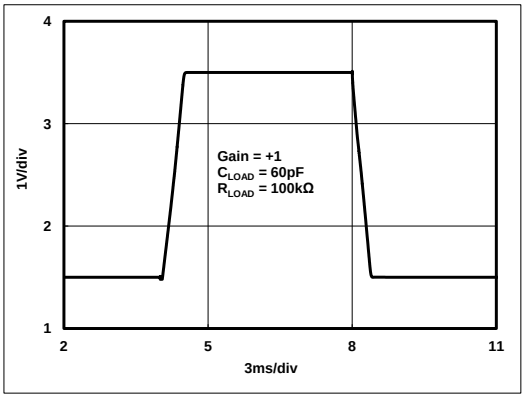
Note 1: Full power bandwidth is calculated from the slew rate FPBW = SR/π • V_{P-P}.

Typical Performance Characteristics

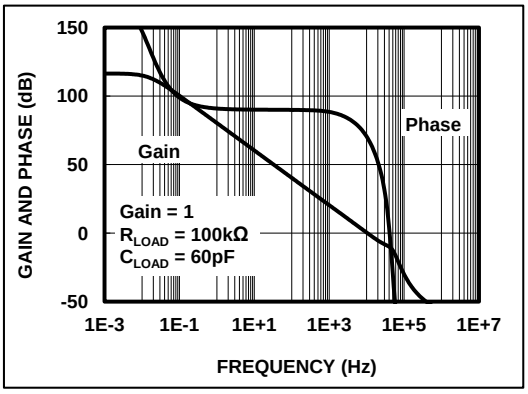
Small-Signal Step Response, 100mV Step



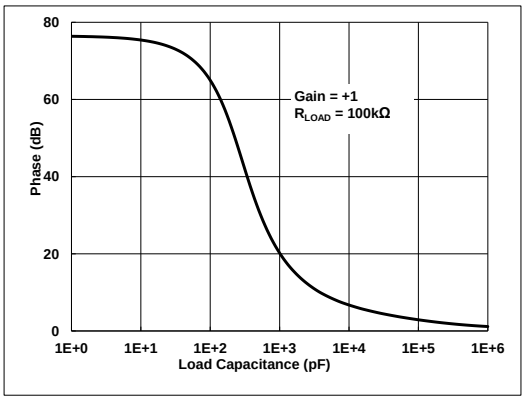
Large-Signal Step Response, 2V Step



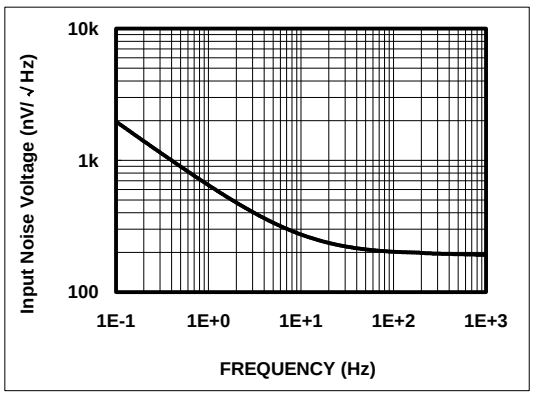
Open-Loop Gain and Phase



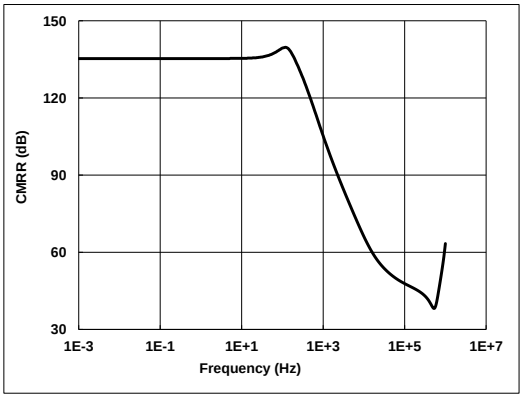
Phase Margin vs. C_{LOAD} (Stable for Any C_{LOAD})



Input Voltage Noise Spectral Density

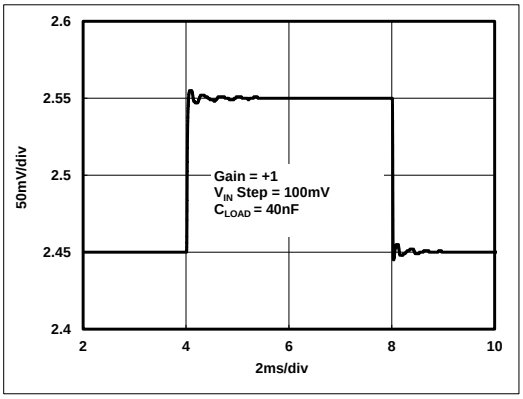


Common-Mode Rejection Ratio

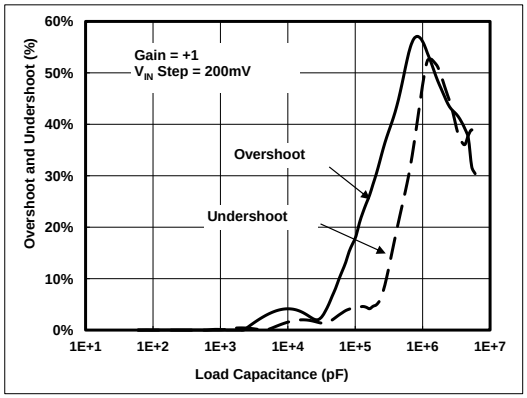


Typical Performance Characteristics

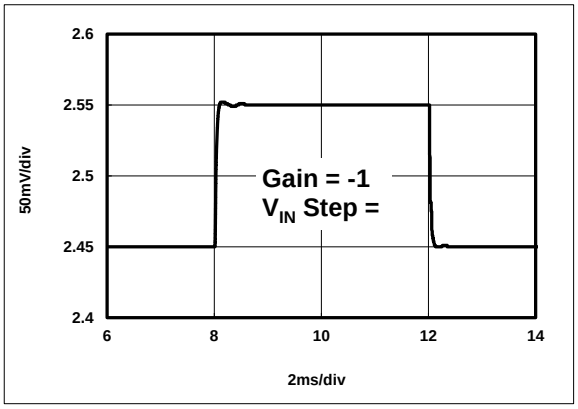
Over-Shoot Voltage, C_{LOAD} = 40nF, Gain = +1, R_{FB}=100kΩ



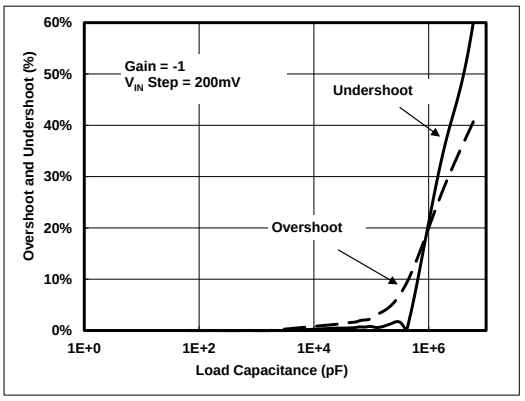
Over-Shoot % vs. C_{LOAD}, Gain = +1, R_{FB} = 1MΩ



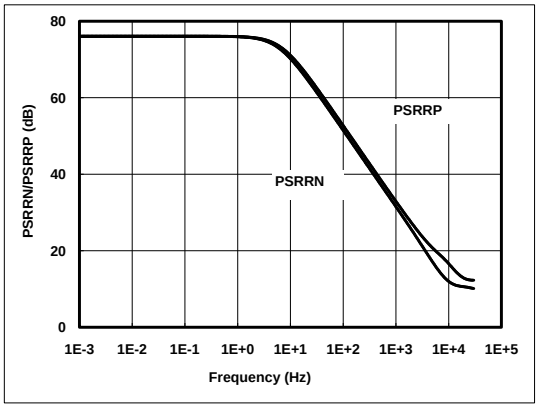
Over-Shoot Voltage, C_{LOAD}=40nF, Gain= -1, R_{FB}=100kΩ



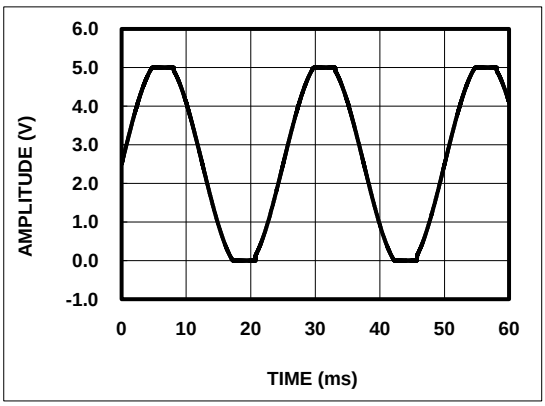
Over-Shoot % vs. C_{LOAD}, Gain = -1, R_{FB} = 1MΩ



Power-Supply Rejection Ratio

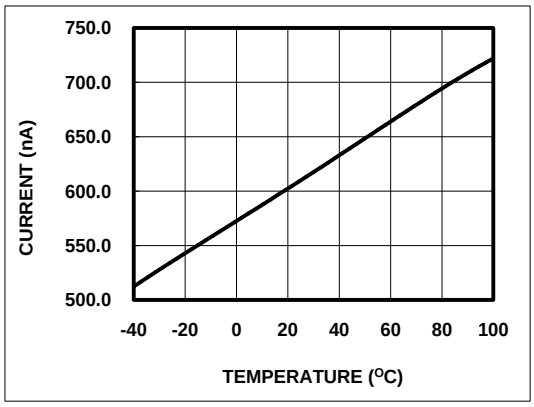


V_{IN} = -0.2V to 5.7V, No Phase Reversal

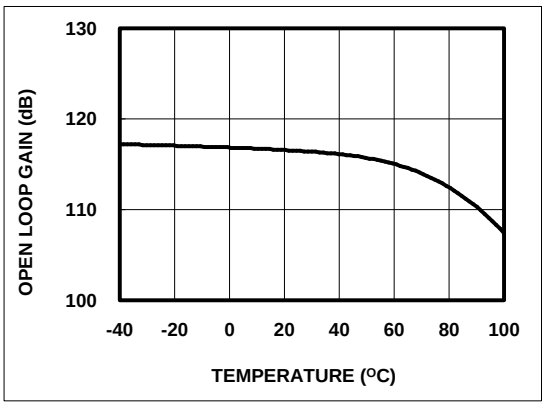


Typical Performance Characteristics

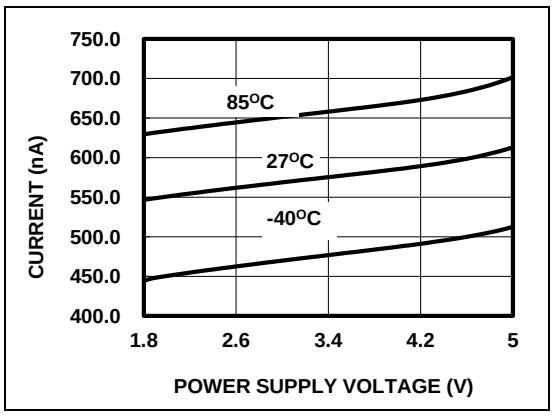
Quiescent Supply Current vs. Temperature



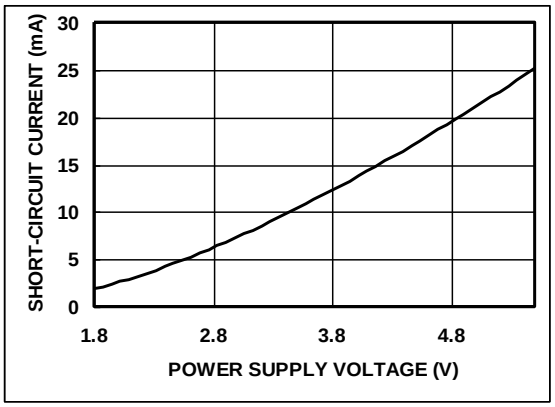
Open-Loop Gain vs. Temperature



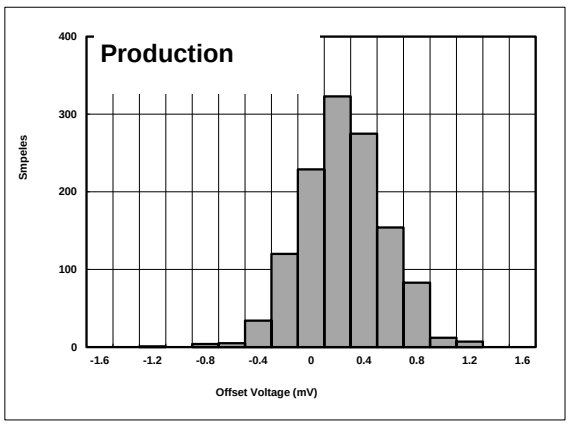
Quiescent Supply Current vs. Supply Voltage



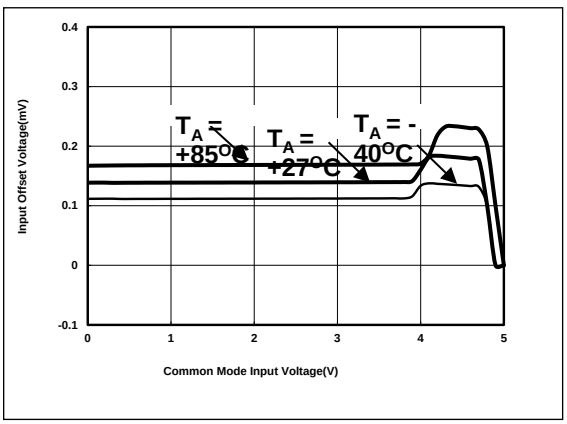
Short-Circuit Current vs. Supply Voltage



Input Offset Voltage Distribution

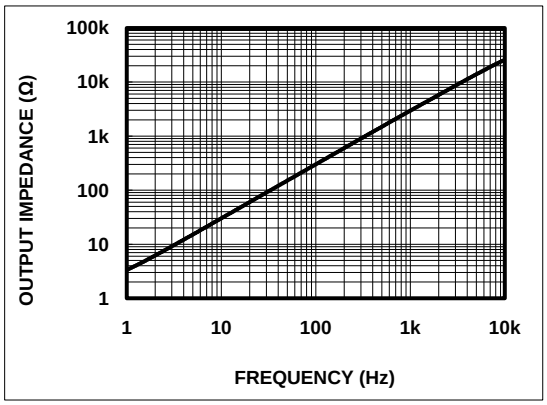


Input Offset Voltage vs. Common Mode Input Voltage

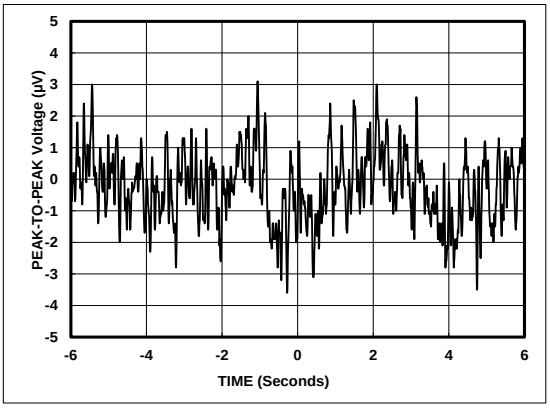


Typical Performance Characteristics

Closed-Loop Output Impedance vs. Frequency



0.1Hz to 10Hz Time Domain Output Voltage Noise



Pin Functions

–IN: Inverting Input of the Amplifier. Voltage range of this pin can go from V^- – 0.3V to V^+ + 0.3V.

+IN: Non-Inverting Input of Amplifier. This pin has the same voltage range as –IN.

V+ or $+V_S$: Positive Power Supply. Typically the voltage is from 1.8V to 5.5V. Split supplies are possible as long as the voltage between V+ and V– is between 1.8V and 5.5V. A bypass capacitor of 0.1μF as close to the part as possible should be used between power supply pins or between supply pins and ground.

N/C: No Connection.

V^- or ^-V_S: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 1.8V to 5.5V. If it is not connected to ground, bypass it with a capacitor of 0.1μF as close to the part as possible.

OUT: Amplifier Output. The voltage range extends to within milli-volts of each supply rail.

Operation

The TP212x family input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply. The input stage is comprised of two CMOS differential amplifiers, a PMOS stage and NMOS stage that are active over different ranges of common mode input voltage. The Class-AB control buffer and output bias stage uses a proprietary compensation technique to take full advantage of the process technology to drive very high capacitive loads. This is evident from the transient over shoot measurement plots in the Typical Performance Characteristics.

Applications Information

Low Supply Voltage and Low Power Consumption

The TP212x family of operational amplifiers can operate with power supply voltages from 1.8V to 6.0V. Each amplifier draws only 600nA quiescent current. The low supply voltage capability and low supply current are ideal for portable applications demanding HIGH CAPACITIVE LOAD DRIVING CAPABILITY and CONSTANT WIDE BANDWIDTH. The TP212x family is optimized for wide bandwidth low power applications. They have an industry leading high GBWP to power ratio and are unity gain stable for 1,000nF capacitive load. When the load capacitance increases, the increased capacitance at the output pushed the non-dominant pole to lower frequency in the open loop frequency response, lowering the phase and gain margin. Higher gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence higher phase margin.

Low Input Referred Noise

The TP212x family provides a low input referred noise density of 170nV/ √ Hz at 1kHz. The voltage noise will grow slowly with the frequency in wideband range, and the input voltage noise is typically 6.5μV_{P-P} at the frequency of 0.1Hz to 10Hz.

Low Input Offset Voltage

The TP212x family has a low offset voltage of 1.5mV maximum which is essential for precision applications. The offset voltage is trimmed with a proprietary trim algorithm to ensure low offset voltage for precision signal processing requirement.

Low Input Bias Current

The TP212x family is a CMOS OPA family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on “PCB Surface Leakage” for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the TP212x OPA’s input bias current at +27°C (±1fA, typical). It is recommended to use multi-layer PCB layout and route the OPA’s -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 1 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common Mode input voltage.
2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op-amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

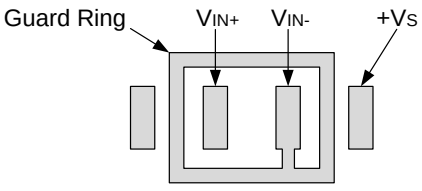


Figure 1

Ground Sensing and Rail to Rail Output

The TP212x family has excellent output drive capability, delivering over 10mA of output drive current. The output stage is a rail-to-rail topology that is capable of swinging to within 5mV of either rail. Since the inputs can go 300mV beyond either rail, the op-amp can easily perform ‘true ground’ sensing.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

ESD

The TP212x family has reverse-biased ESD protection diodes on all inputs and output. Input and out pins can not be biased more than 300mV beyond either supply rail.

Driving Large Capacitive Load

The TP212x family of OPA is designed to drive large capacitive loads. Refer to Typical Performance Characteristics for "Phase Margin vs. Load Capacitance". As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer (G = +1V/V) is the most sensitive to large capacitive loads.

When driving large capacitive loads with the TP212x OPA family (e.g., > 200 pF when G = +1V/V), a small series resistor at the output (R_{ISO} in Figure 2) improves the feedback loop's phase margin and stability by making the output load resistive at higher frequencies.

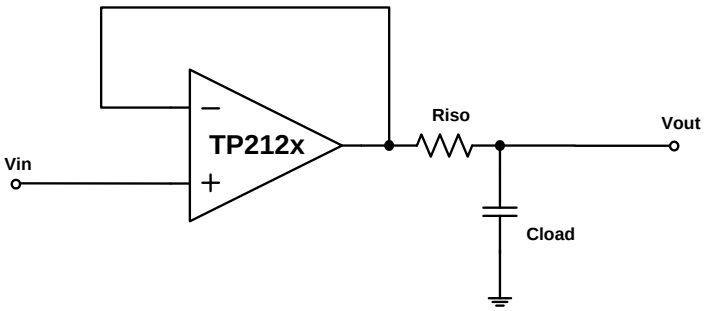


Figure 2

Power Supply Layout and Bypass

The TP212x OPA's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

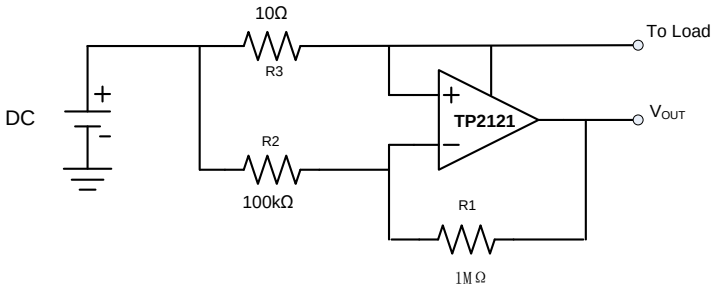
A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

BATTERY CURRENT SENSING

The Common Mode Input voltage Range of TP212x OPA series, which goes 0.3V beyond both supply rails, supports their use in high-side and low-side battery current sensing applications. The low quiescent current (600nA, typical) helps prolong battery life, and the rail-to-rail output supports detection of low currents.

The battery current (I_{DD}) through the 10Ω resistor causes its top terminal to be more negative than the bottom terminal. This keeps the Common Mode Input voltage below V_{DD}, which is within its allowed range. The output of the OPA will also be blow V_{DD}, within its Maximum Output Voltage Swing specification.



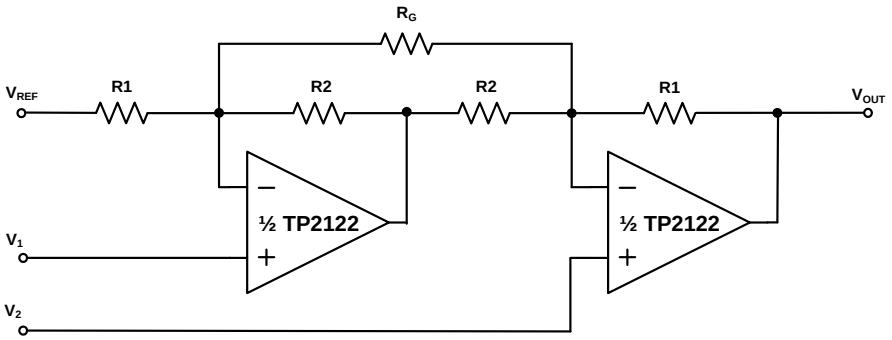
$$I_{DD} = \frac{V_{DD} - V_{OUT}}{\frac{R1}{R2} \cdot R3}$$

Figure 3

Instrumentation Amplifier

The TP212x OPA series is well suited for conditioning sensor signals in battery-powered applications. Figure 4 shows a two op-amp instrumentation amplifier, using the TP212x OPA.

The circuit works well for applications requiring rejection of Common Mode noise at higher gains. The reference voltage (V_{REF}) is supplied by a low-impedance source. In single voltage supply applications, V_{REF} is typically $V_{DD}/2$.



$$V_{OUT} = (V_1 - V_2)(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}) + V_{REF}$$

Figure 4

Buffered Chemical Sensor (pH) Probe

The TP212x OPA has input bias current in the pA range. This is ideal in buffering high impedance chemical sensors such as pH probe. As an example, the circuit in Figure 5 eliminates expansive low-leakage cables that that is required to connect pH probe to metering ICs such as ADC, AFE and/or MCU. A TP212x OPA and a lithium battery are housed in the probe assembly. A conventional low-cost coaxial cable can be used to carry OPA's output signal to subsequent ICs for pH reading.

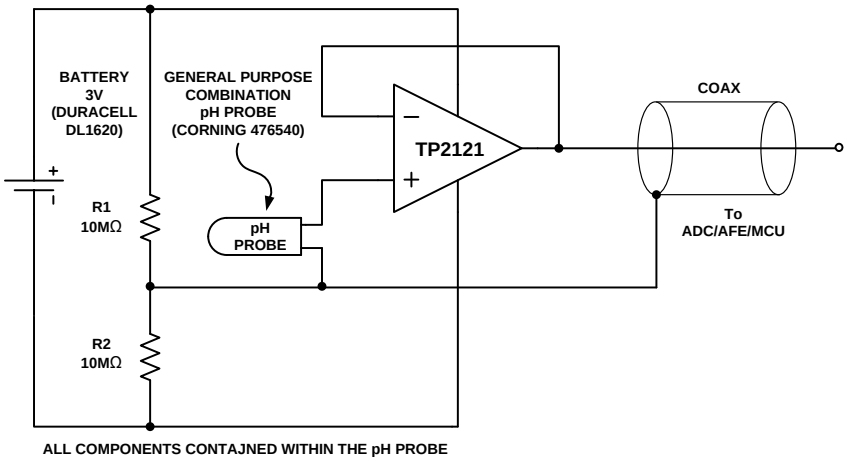


Figure 5: Buffer pH Probe

Portable Gas Sensor Amplifier

Gas sensors are used in many different industrial and medical applications. Gas sensors generate a current that is proportional to the percentage of a particular gas concentration sensed in an air sample. This output current flows through a load resistor and the resultant voltage drop is amplified. Depending on the sensed gas and sensitivity of the sensor, the output current can be in the range of tens of microamperes to a few milli-amperes. Gas sensor datasheets often specify a recommended load resistor value or a range of load resistors from which to choose.

There are two main applications for oxygen sensors – applications which sense oxygen when it is abundantly present (that is, in air or near an oxygen tank) and those which detect traces of oxygen in parts-per-million concentration. In medical applications, oxygen sensors are used when air quality or oxygen delivered to a patient needs to be monitored. In fresh air, the concentration of oxygen is 20.9% and air samples containing less than 18% oxygen are considered dangerous. In industrial applications, oxygen sensors are used to detect the absence of oxygen; for example, vacuum-packaging of food products.

The circuit in Figure 6 illustrates a typical implementation used to amplify the output of an oxygen detector. With the components shown in the figure, the circuit consumes less than 600nA of supply current ensuring that small form-factor single- or button-cell batteries (exhibiting low mAh charge ratings) could last beyond the operating life of the oxygen sensor. The precision specifications of these amplifiers, such as their low offset voltage, low V_{OS} TC, low input bias current, high CMRR, and high PSRR are other factors which make these amplifiers excellent choices for this application.

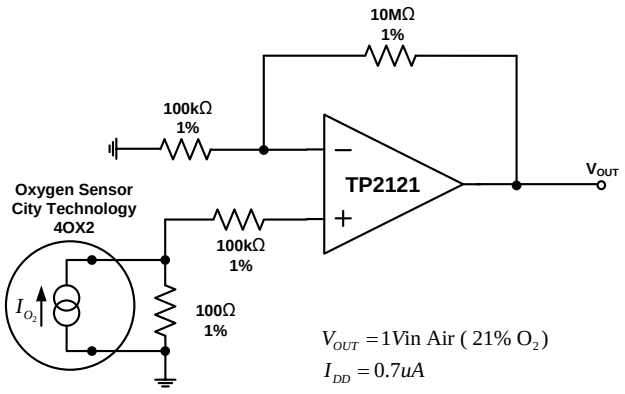
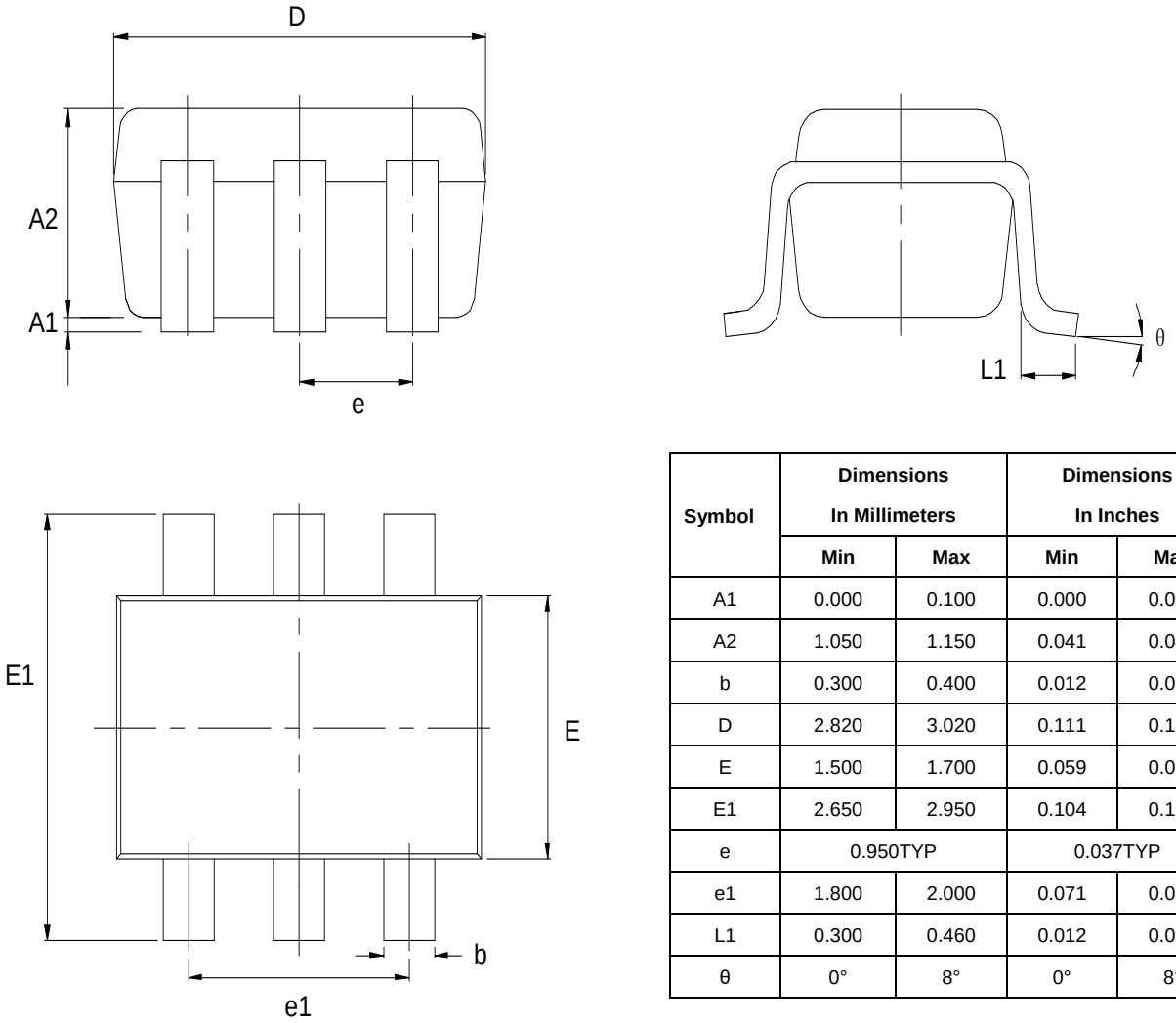


Figure 6

Package Outline Dimensions

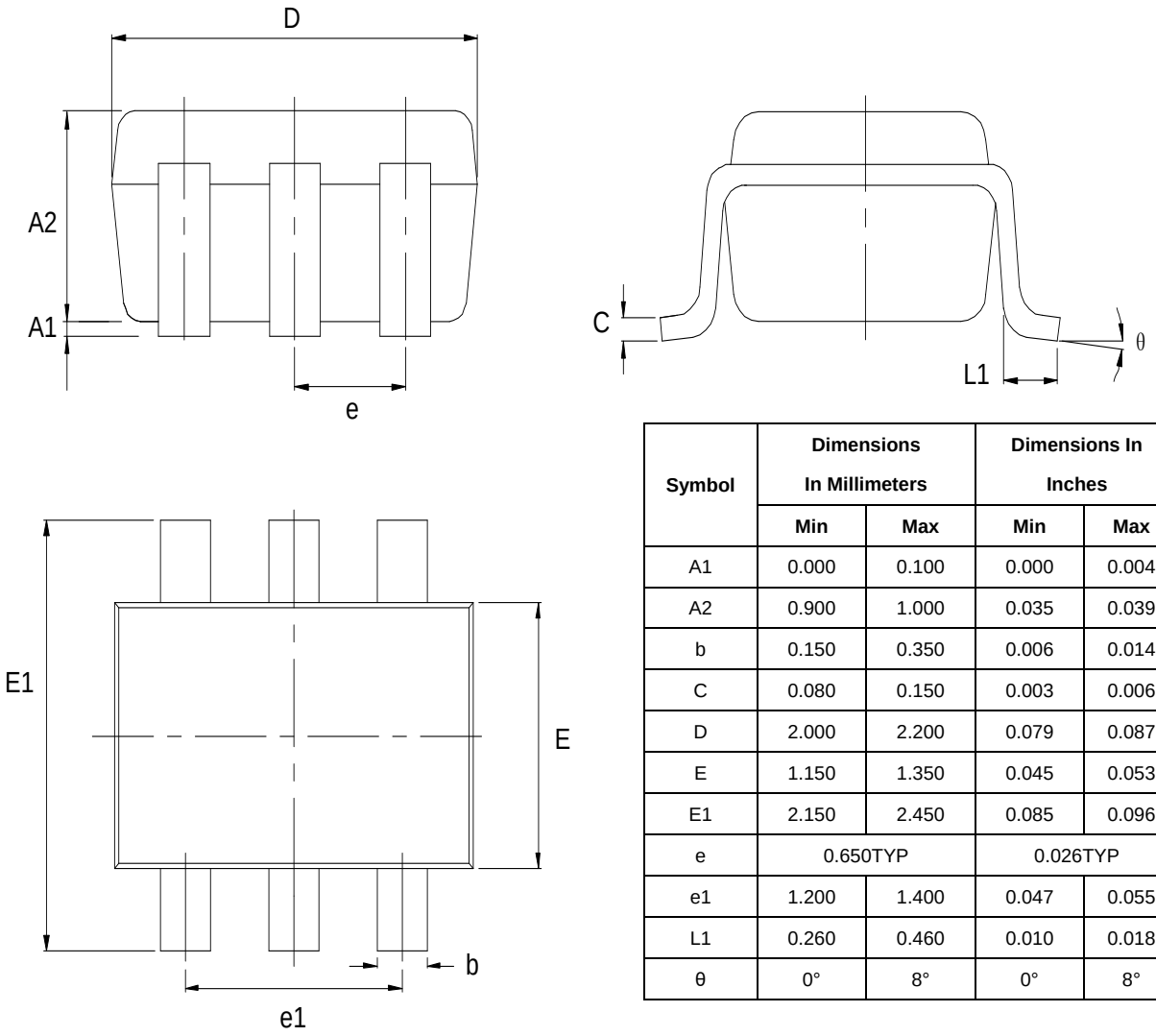
SOT23-5 / SOT23-6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L1	0.300	0.460	0.012	0.024
θ	0°	8°	0°	8°

Package Outline Dimensions

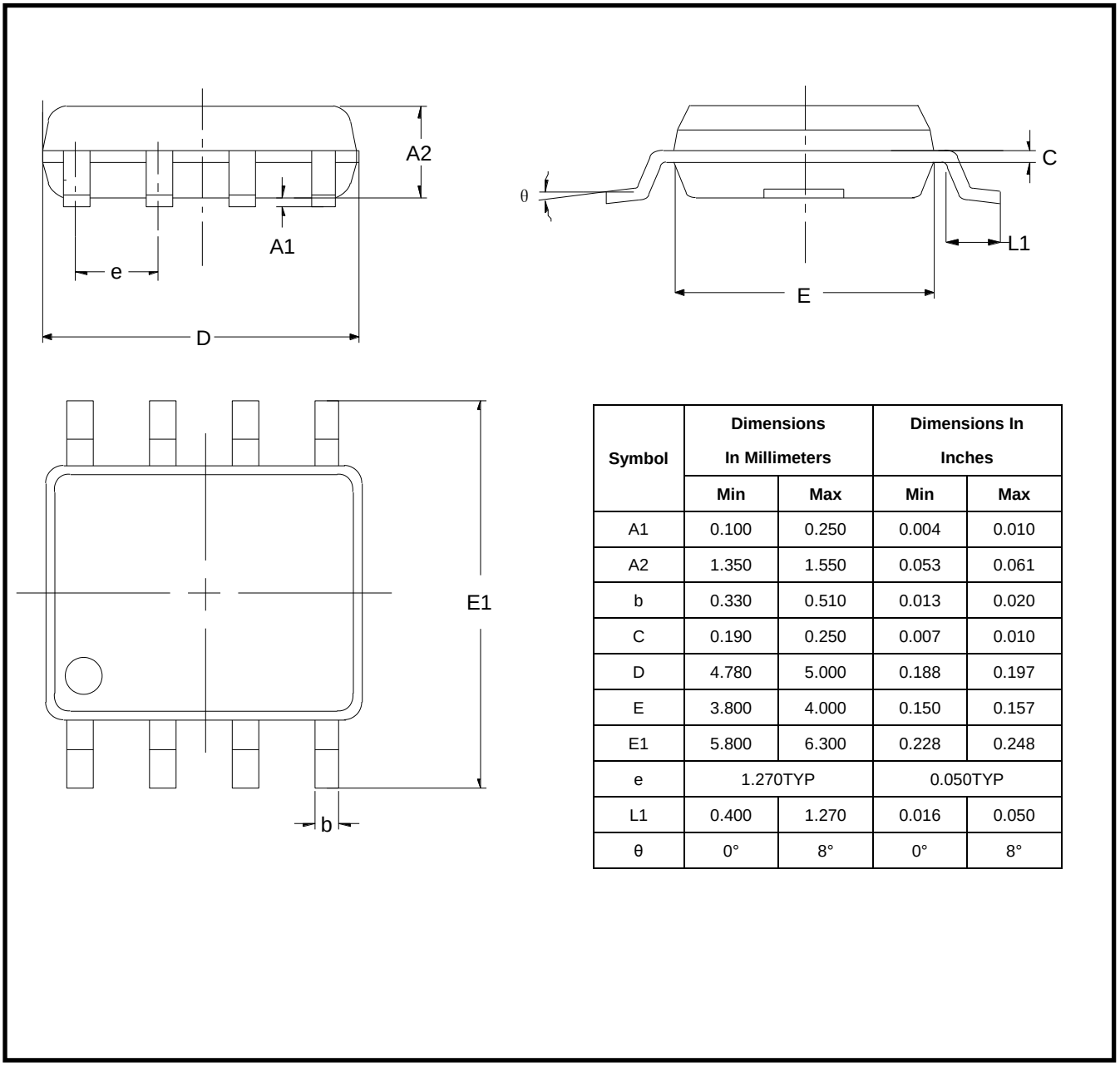
SC-70-5 / SC-70-6 (SOT353 / SOT363)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650TYP		0.026TYP	
e1	1.200	1.400	0.047	0.055
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

Package Outline Dimensions

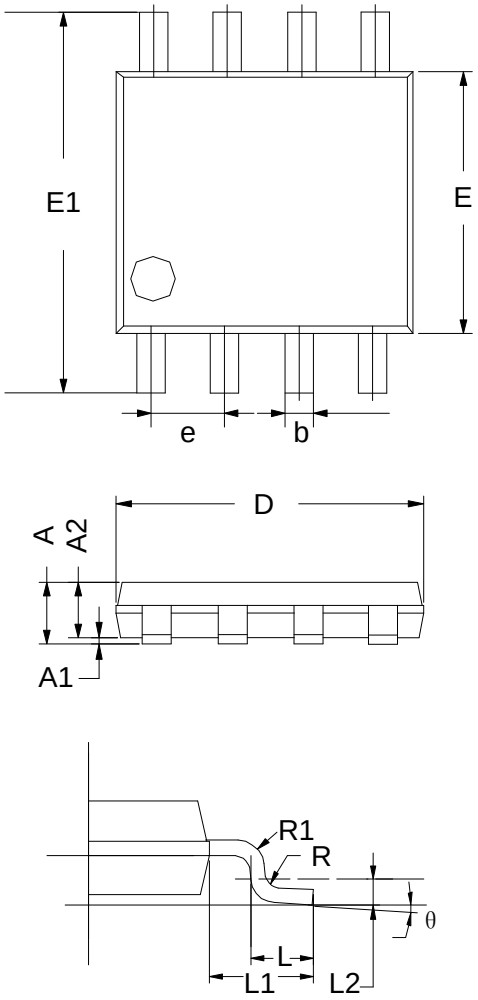
SO-8 (SOIC-8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Outline Dimensions

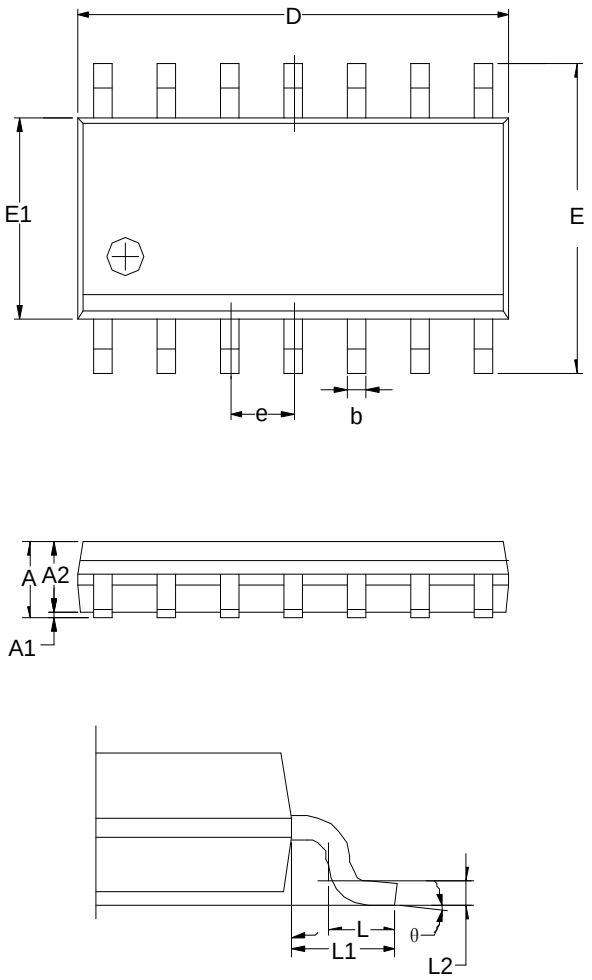
MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Package Outline Dimensions

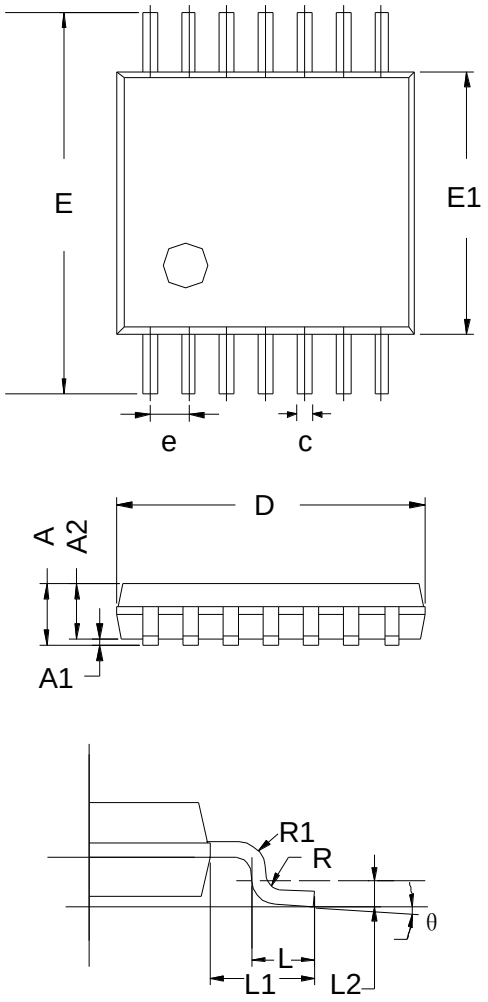
SO-14 (SOIC-14)



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.36		0.49
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
θ	0°		8°

Package Outline Dimensions

TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.20	-	0.28
c	0.10	-	0.19
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°