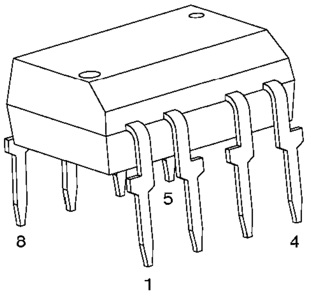
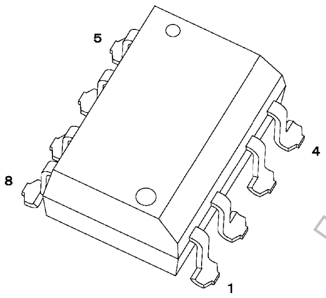
4. Packaging (Note)

TLP350



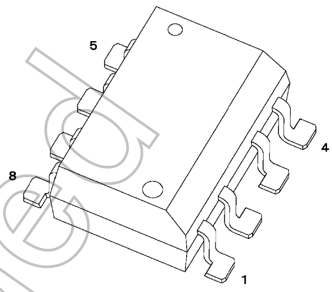
11-10C4S

TLP350(LF1,TP1)



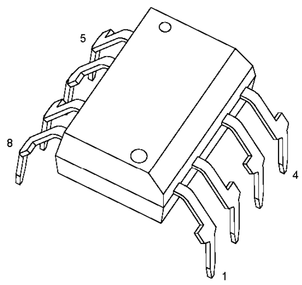
11-10C401S

TLP350(LF5,TP5)



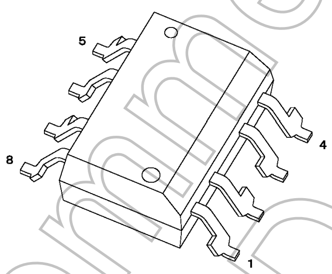
11-10C405S

TLP350F



11-10C402S

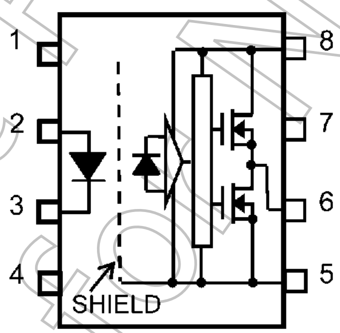
TLP350F(LF4,TP4)



11-10C404S

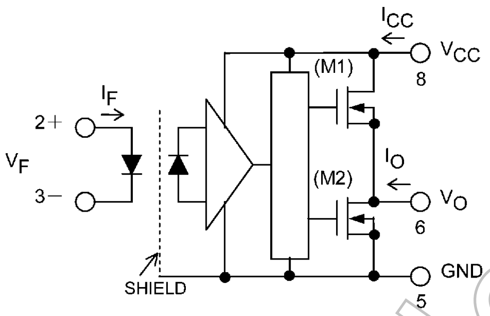
Note: Through-hole type: TLP350, TLP350F
Lead forming option: (LF1), (LF4), (LF5)
Taping option: (TP1), (TP4), (TP5)

5. Pin Assignment



1: N.C.
2: Anode
3: Cathode
4: N.C.
5: GND
6: V_O (Output)
7: N.C.
8: V_{CC}

6. Internal Circuit (Note)



Note: A 0.1-μF bypass capacitor must be connected between pin 8 and pin 5.

7. Principle of Operation

7.1. Truth Table

Input	LED	M1	M2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

7.2. Mechanical Parameters

Characteristics	7.62 mm Pitch TLP350	10.16 mm Pitch TLP350F	Unit
Creepage distances	7.0 (min)	8.0 (min)	mm
Clearance distances	7.0 (min)	8.0 (min)	
Internal isolation thickness	0.4 (min)	0.4 (min)	

8. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

	Characteristics	Symbol	Note	Rating	Unit
LED	Input forward current	I_F		20	mA
	Input forward current derating ($T_a \geq 85$ °C)	$\Delta I_F/\Delta T_a$		-0.54	mA/°C
	Peak transient input forward current	I_{FPT}	(Note 1)	1	A
	Peak transient input forward current derating ($T_a \geq 85$ °C)	$\Delta I_{FPT}/\Delta T_a$		-25	mA/°C
	Input reverse voltage	V_R		5	V
	Input power dissipation	P_D		40	mW
	Input power dissipation derating ($T_a \geq 85$ °C)	$\Delta P_D/\Delta T_a$		-1.0	mW/°C
	Junction temperature	T_j		125	°C
Detector	Peak high-level output current (T_a = -40 to 100 °C)	I_{OPH}	(Note 2)	-2.5	A
	Peak low-level output current (T_a = -40 to 100 °C)	I_{OPL}	(Note 2)	+2.5	
	Output voltage	V_O		35	V
	Supply voltage (T_a < 95 °C)	V_{CC}		35	
	Supply voltage derating ($T_a \geq 95$ °C)	$\Delta V_{CC}/\Delta T_a$		-1.0	V/°C
	Output power dissipation	P_O		260	mW
	Output power dissipation derating ($T_a \geq 110$ °C)	$\Delta P_O/\Delta T_a$		-6.5	mW/°C
	Junction temperature	T_j		125	°C
Common	Operating frequency	f	(Note 3)	50	kHz
	Operating temperature	T_{opr}		-40 to 100	°C
	Storage temperature	T_{stg}		-55 to 125	
	Lead soldering temperature (10 s)	T_{sol}	(Note 4)	260	
	Isolation voltage (AC, 60 s, R.H. $\leq$ 60 %)	BV_S	(Note 5)	3750	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note: A ceramic capacitor (0.1 μF) should be connected between pin 8 and pin 5 to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: Pulse width (P_W) $\leq$ 1 μs, 300 pps

Note 2: Exponential waveform. Pulse width $\leq$ 0.3 μs, f $\leq$ 15 kHz

Note 3: If the rising slope of the supply voltage (V_{CC}) for the detector is steep, stable operation of the internal circuits cannot be guaranteed.
Be sure to set 3.0 V/μs or less for a rising slope of the V_{CC}.

Note 4: $\geq$ 2 mm below seating plane.

Note 5: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

9. Recommended Operating Conditions (Note)

Characteristics	Symbol	Note	Min	Typ.	Max	Unit
Input on-state current	$I_{F(ON)}$	(Note 1)	7.5	—	10	mA
Input off-state voltage	$V_{F(OFF)}$		0	—	0.8	V
Supply voltage	V_{CC}	(Note 2)	15	—	30	
Peak high-level output current	I_{OPH}	(Note 3)	—	—	-2.0	A
Peak low-level output current	I_{OPL}	(Note 3)	—	—	+2.0	
Operating temperature	T_{opr}		-40	—	100	℃

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note 1: The rise and fall times of the input on-current should be less than 0.5 μs.

Note 2: Denotes the operating range, not the recommended operating condition.

Note 3: Exponential waveform. $I_{OPH} \geq$ -2.0 A ($\leq$ 0.3 μs), $I_{OPL} \leq$ 2.0 A ($\leq$ 0.3 μs), T_a = 100 ℃

10. Electrical Characteristics (Note) (Unless otherwise specified, T_a = -40 to 100 ℃)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	V_F		—	I_F = 10 mA, T_a = 25 ℃	—	1.6	1.8	V
Input forward voltage temperature coefficient	$\Delta V_F/\Delta T_a$		—	I_F = 10 mA	—	-2.4	—	mV/℃
Input reverse current	I_R		—	V_R = 5 V, T_a = 25 ℃	—	—	10	μA
Input capacitance	C_t		—	V = 0 V, f = 1 MHz, T_a = 25 ℃	—	45	250	pF
Peak high-level output current	I_{OPH}	(Note 1)	Fig. 13.1.1	V_{CC} = 30 V, I_F = 5 mA, V_{8-6} = 3.5 V	—	-2.5	-1.0	A
				V_{CC} = 15 V, I_F = 5 mA, V_{8-6} = 7.0 V	—	—	-2.0	
Peak low-level output current	I_{OPL}	(Note 1)	Fig. 13.1.2	V_{CC} = 30 V, I_F = 0 mA, V_{6-5} = 2.5 V	1.0	2.5	—	
				V_{CC} = 15 V, I_F = 0 mA, V_{6-5} = 7.0 V	2.0	—	—	
High-level output voltage	V_{OH}		Fig. 13.1.3	V_{CC1} = +15 V, V_{EE1} = -15 V, R_L = 200 Ω, I_F = 5 mA	11.0	13.9	—	V
Low-level output voltage	V_{OL}		Fig. 13.1.4	V_{CC1} = +15 V, V_{EE1} = -15 V, R_L = 200 Ω, V_F = 0.8 V	—	-14.9	-12.5	
High-level supply current	I_{CCH}		Fig. 13.1.5	V_{CC} = 30 V, I_F = 10 mA, V_O = Open	—	1.5	2.0	mA
Low-level supply current	I_{CCL}		Fig. 13.1.6	V_{CC} = 30 V, I_F = 0 mA, V_O = Open	—	1.5	2.0	
Threshold input current (L/H)	I_{FLH}		—	V_{CC} = 15 V, V_O > 1 V, I_O = 0 mA	—	1.2	5	
Threshold input voltage (H/L)	V_{FHL}		—	V_{CC} = 15 V, V_O < 1 V, I_O = 0 mA	0.8	—	—	V
Supply voltage	V_{CC}		—		15	—	30	V
UVLO threshold voltage	V_{UVLO+}		Fig. 13.1.9	I_F = 5 mA, V_O > 2.5 V	11.0	12.5	13.5	
	V_{UVLO-}		Fig. 13.1.9	I_F = 5 mA, V_O < 2.5 V	9.5	11.0	12.0	
UVLO hysteresis	$UVLO_{HYS}$		Fig. 13.1.9		—	1.5	—	

Note: All typical values are at T_a = 25 ℃.

Note : This device is designed for low power consumption, making it more sensitive to ESD than its predecessors. Extra care should be taken in the design of circuitry and pc board implementation to avoid ESD problems.

Note 1: I_O application time $\leq$ 50 μs; single pulse.

11. Isolation Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Note	Test Conditions	Min	Typ.	Max	Unit
Total capacitance (input to output)	C_S	(Note 1)	V_S = 0 V, f = 1 MHz	—	1.0	—	pF
Isolation resistance	R_S	(Note 1)	V_S = 500 V, R.H. ≤ 60 %	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	(Note 1)	AC, 60 s	3750	—	—	Vrms
			AC, 1 s in oil	—	10000	—	
			DC, 60 s in oil	—	10000	—	Vdc

Note 1: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

12. Switching Characteristics (Note) (Unless otherwise specified, T_a = -40 to 100 °C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (L/H)	t_{pLH}	(Note 1)	Fig. 13.1.7	I_F = 0 → 5 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	50	150	500	ns
Propagation delay time (H/L)	t_{pHL}	(Note 1)		I_F = 5 → 0 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	50	150	500	
Pulse width distortion	$\lvert t_{pHL}-t_{pLH} \rvert$	(Note 1)		I_F = 0 ←→ 5 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	—	—	350	
Rise time	t_r	(Note 1)		I_F = 0 → 5 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	—	15	—	
Fall time	t_f	(Note 1)		I_F = 5 → 0 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	—	8	—	
Common-mode transient immunity at output high	CM_H	(Note 2)	Fig. 13.1.8	V_{CM} = 1000 V_{p-p}, I_F = 5 mA, V_{CC} = 30 V, T_a = 25 °C, $V_{O(min)}$ = 26 V	-15	—	—	kV/μs
Common-mode transient immunity at output low	CM_L	(Note 3)		V_{CM} = 1000 V_{p-p}, I_F = 0 mA, V_{CC} = 30 V, T_a = 25 °C, $V_{O(max)}$ = 1 V	15	—	—	

Note: All typical values are at T_a = 25 °C.

Note 1: f = 25 kHz, duty = 50 %, input current t_r = t_f = 5 ns, C_L is approximately 15 pF which includes probe and stray wiring capacitance.

Note 2: CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 26 V).

Note 3: CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 1 V).

13. Test Circuits and Characteristics Curves

13.1. Test Circuits

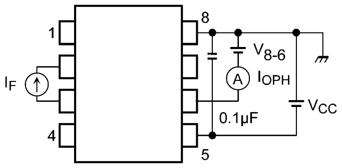


Fig. 13.1.1 I_{OPH} Test Circuit

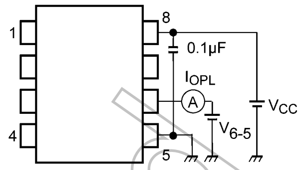


Fig. 13.1.2 I_{OPL} Test Circuit

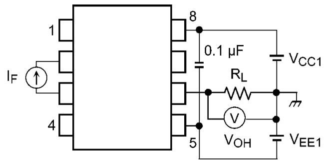


Fig. 13.1.3 V_{OH} Test Circuit

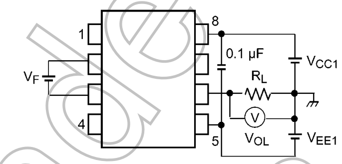


Fig. 13.1.4 V_{OL} Test Circuit

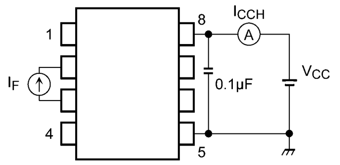


Fig. 13.1.5 I_{CCH} Test Circuit

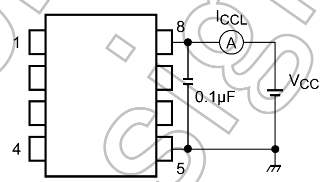


Fig. 13.1.6 I_{CCL} Test Circuit

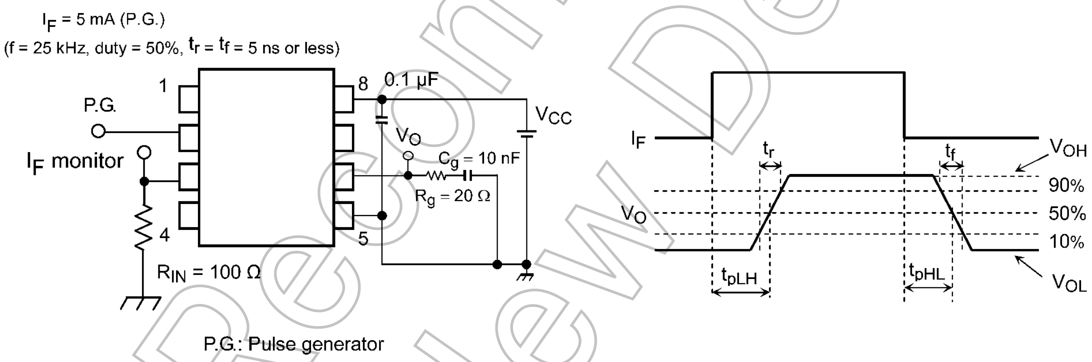
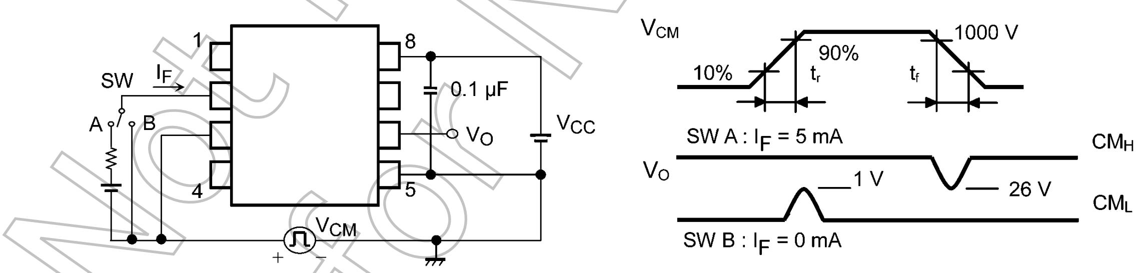


Fig. 13.1.7 Switching Time Test Circuit and Waveform



$$CM_L = \frac{800(V)}{t_r(\mu s)} \qquad CM_H = -\frac{800(V)}{t_f(\mu s)}$$

CM_L (CM_H) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

Fig. 13.1.8 Common-Mode Transient Immunity Test Circuit and Waveform

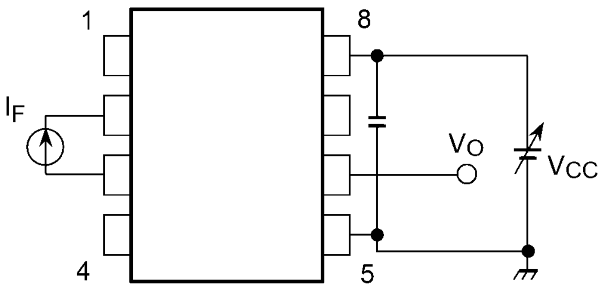


Fig. 13.1.9 V_{CC}-$V_{O(VUVLO)}$ Test Circuit

13.2. Characteristics Curves (Note)

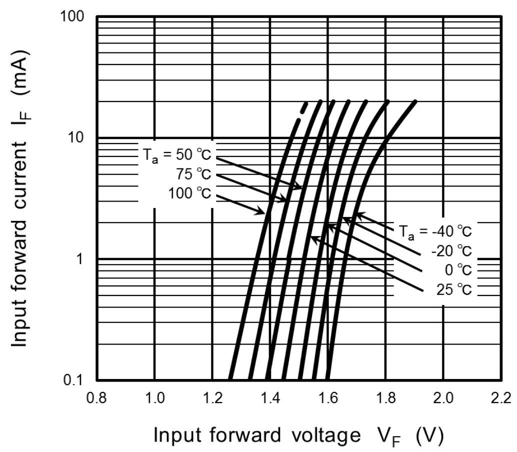


Fig. 13.2.1 I_F - V_F

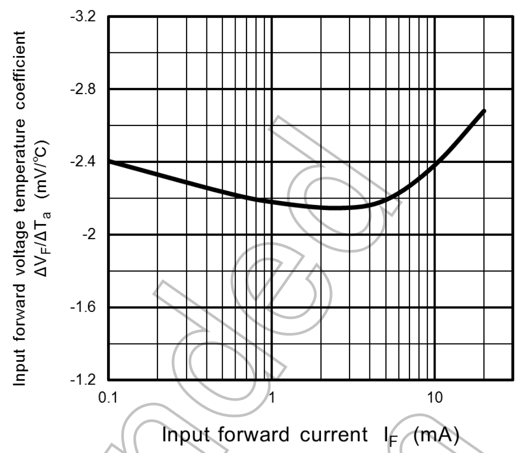


Fig. 13.2.2 $\Delta V_F/\Delta T_a$ - I_F

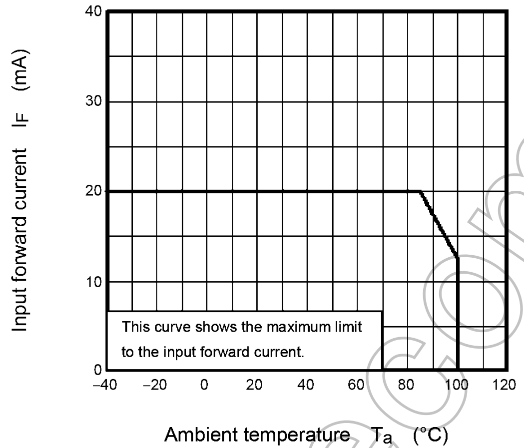


Fig. 13.2.3 I_F - T_a

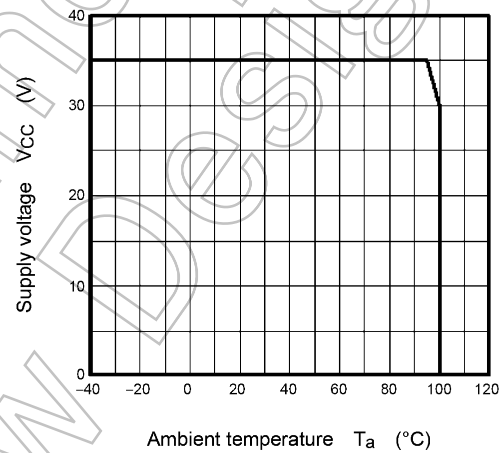


Fig. 13.2.4 V_{CC} - T_a

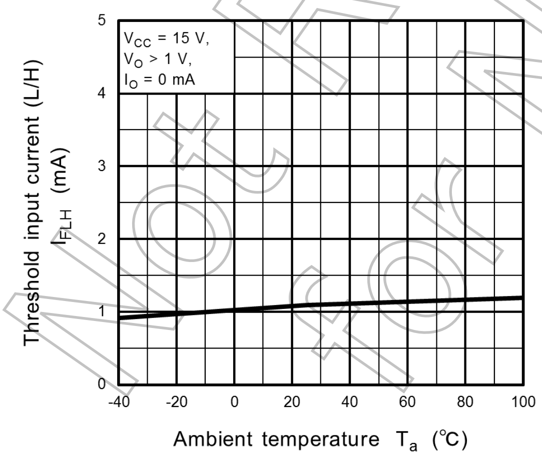


Fig. 13.2.5 I_{FLH} - T_a

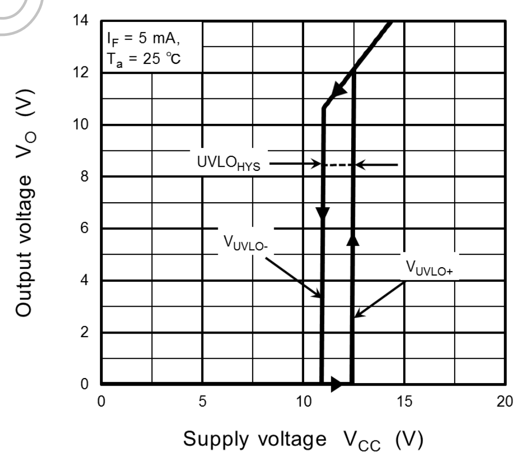


Fig. 13.2.6 $V_O(V_{UVLO})$ - V_{CC}

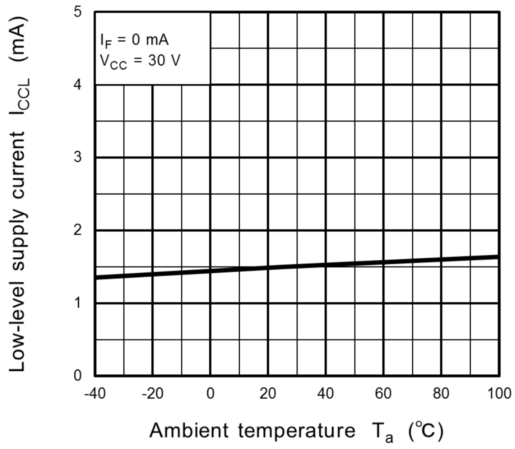


Fig. 13.2.7 I_{CCL} - T_a

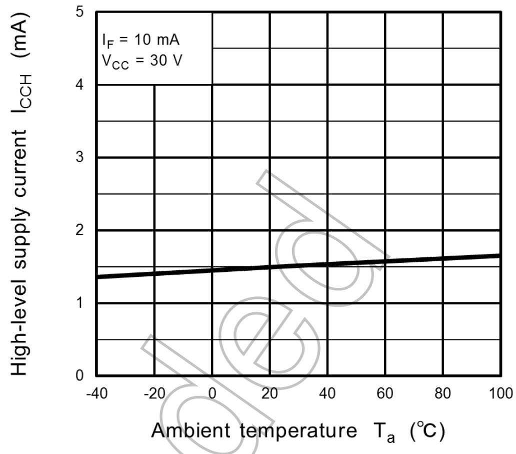


Fig. 13.2.8 I_{CCH} - T_a

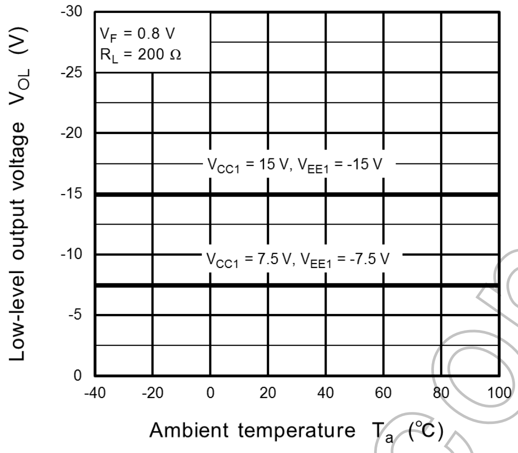


Fig. 13.2.9 V_{OL} - T_a

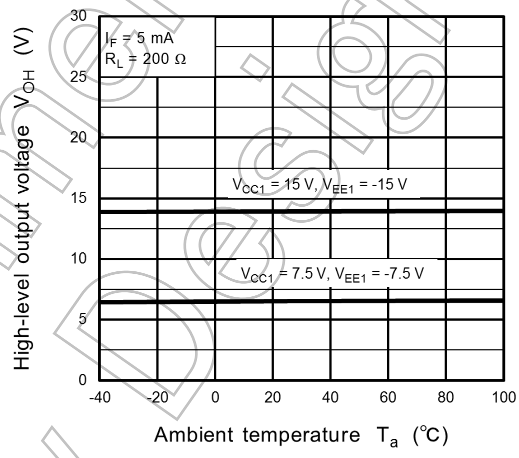


Fig. 13.2.10 V_{OH} - T_a

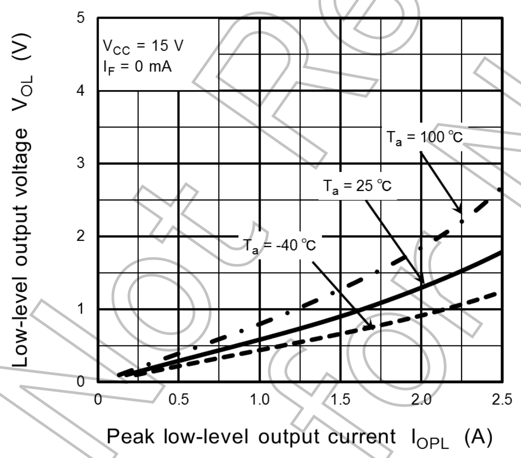


Fig. 13.2.11 V_{OL} - I_{OPL}

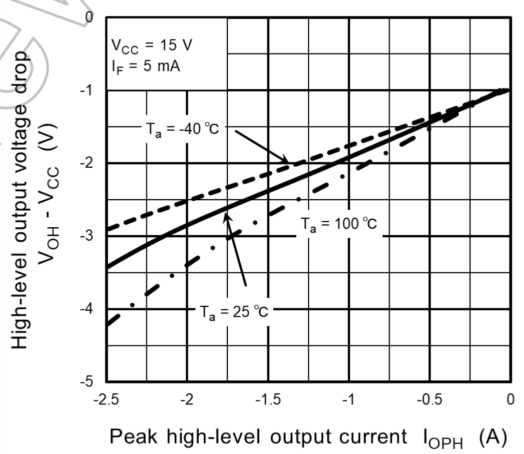


Fig. 13.2.12 $(V_{OH}$-$V_{CC})$ - I_{OPH}

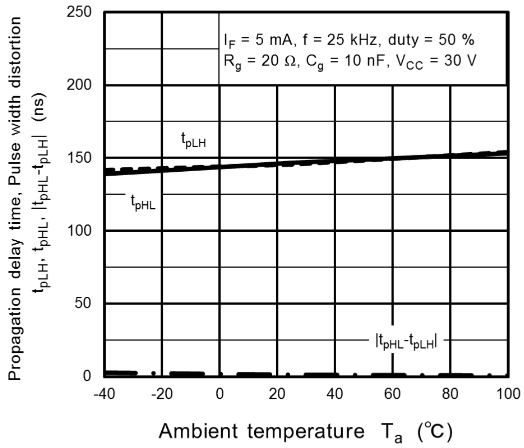


Fig. 13.2.13 t_{pLH},t_{pHL},|t_{pHL}-t_{pLH}| - T_a

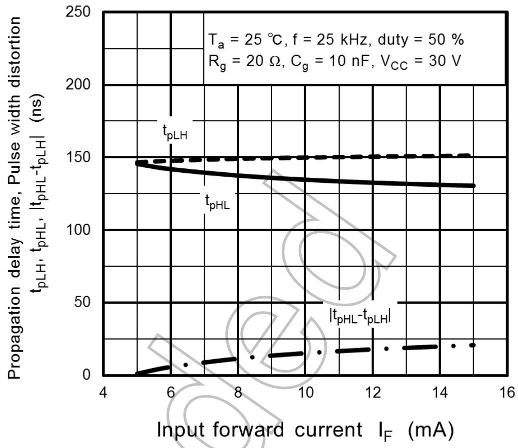


Fig. 13.2.14 t_{pLH},t_{pHL},|t_{pHL}-t_{pLH}| - I_F

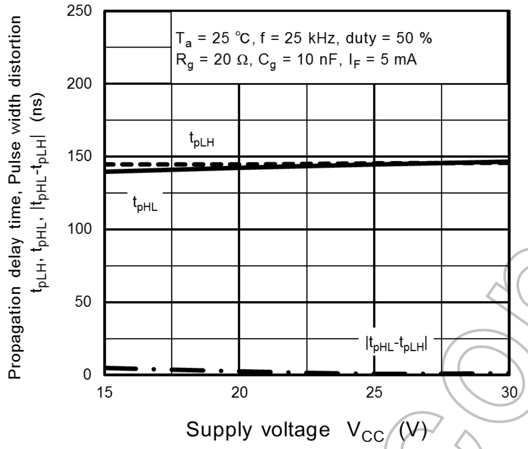


Fig. 13.2.15 t_{pLH},t_{pHL},|t_{pHL}-t_{pLH}| - V_{CC}

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

14. Soldering and Storage

14.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

- When using soldering reflow.
  The soldering temperature profile is based on the package surface temperature.
  (See the figure shown below, which is based on the package surface temperature.)
  Reflow soldering must be performed once or twice.
  The mounting should be completed with the interval from the first to the last mountings being 2 weeks.

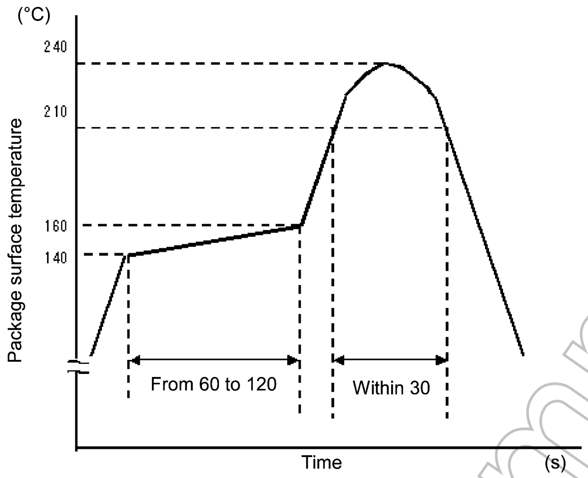


Fig. 14.1.1 An example of a temperature profile when Sn-Pb eutectic solder is used

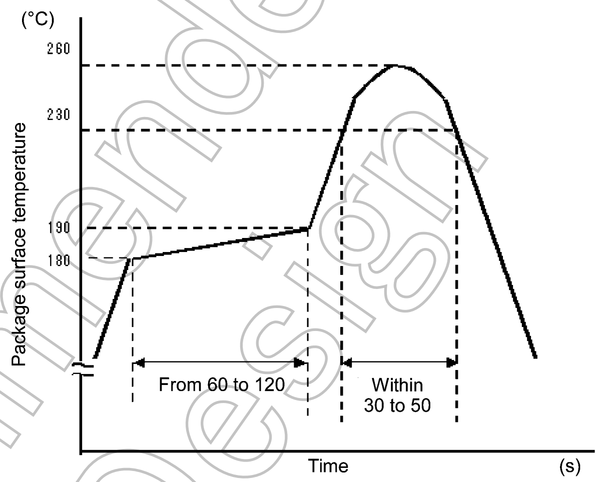


Fig. 14.1.2 An example of a temperature profile when lead(Pb)-free solder is used

- When using soldering flow (Applicable to both eutectic solder and Lead(Pb)-Free solder)
  Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.
  Mounting condition of 260 °C within 10 seconds is recommended.
  Flow soldering must be performed once.
- When using soldering Iron
  Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C
  Heating by soldering iron must be done only once per lead.

14.2. Precautions for General Storage

- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5 °C to 35 °C and 45 % to 75 %, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

15. Land Pattern Dimensions (for reference only)

Unit: mm

TLP350

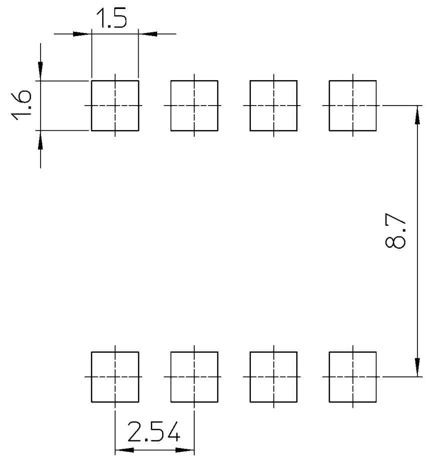


Fig. 15.1 **Lead forming and taping option** (LF1), (TP1), (LF5), (TP5)

TLP350F

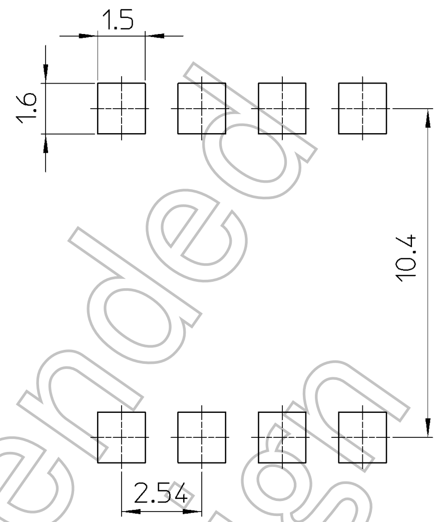
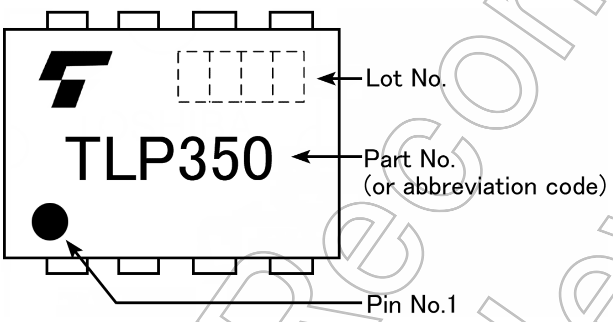


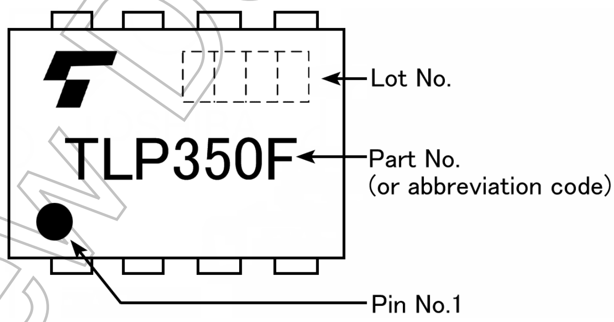
Fig. 15.2 **Lead forming and taping option** (LF4), (TP4)

16. Marking (Note)

TLP350



TLP350F



Note: A different marking is used for photocouplers that have been qualified according to option (D4) of EN60747. See Fig.17.4 and Fig.17.5.

17. EN60747-5-5 Option (D4) Specification

- Part number: TLP350, TLP350F **(Note 1)**
- The following part naming conventions are used for the devices that have been qualified according to option (D4) of EN60747.

Example: TLP350(D4-TP1,F)

D4: EN60747 option
TP1: Tape type
F: [[G]]/RoHS COMPATIBLE **(Note 2)**

Note 1: Use TOSHIBA standard type number for safety standard application.
e.g., TLP350(D4-TP1,F) → TLP350

Note 2: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.
RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Description		Symbol	Rating	Unit
Application classification for rated mains voltage ≤ 300 Vrms for rated mains voltage ≤ 600 Vrms			I-IV I-III	—
Climatic classification			40 / 125 / 21	—
Pollution degree			2	—
Maximum operating insulation voltage	TLPxxx type	V_{IORM}	890	Vpeak
	TLPxxxF type		1140	
Input to output test voltage, Method A V_{pr} = 1.6 × V_{IORM}, type and sample test t_p = 10 s, partial discharge < 5 pC	TLPxxx type	V_{pr}	1424	Vpeak
	TLPxxxF type		1824	
Input to output test voltage, Method B V_{pr} = 1.875 × V_{IORM}, 100 % production test t_p = 1 s, partial discharge < 5 pC	TLPxxx type	V_{pr}	1670	Vpeak
	TLPxxxF type		2140	
Highest permissible overvoltage (transient overvoltage, t_{pr} = 60 s)		V_{TR}	8000	Vpeak
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve) current (input current I_F, P_{so} = 0) power (output or total power dissipation) temperature		I_{si} P_{so} T_s	100 800 150	mA mW °C
Insulation resistance	V_{IO} = 500 V, T_a = 25 °C V_{IO} = 500 V, T_a = 100 °C V_{IO} = 500 V, T_a = T_s	R_{si}	$\geq 10^{12}$ $\geq 10^{11}$ $\geq 10^{9}$	Ω

Fig. 17.1 EN60747 Isolation Characteristics

		7.62 mm pitch TLPxxx type	10.16 mm pitch TLPxxxF type
Minimum creepage distance	Cr	7.0 mm	8.0 mm
Minimum clearance	Cl	7.0 mm	8.0 mm
Minimum insulation thickness	ti	0.4 mm	
Comparative tracking index	CTI	175	

Fig. 17.2 Insulation Related Specifications (Note)

Note: If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. (e. g., at a standard distance between soldering eye centers of 7.5 mm). If this is not permissible, the user shall take suitable measures.

Note: This photocoupler is suitable for **safe electrical isolation** only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

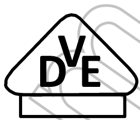


Fig. 17.3 Marking on Packing for EN60747

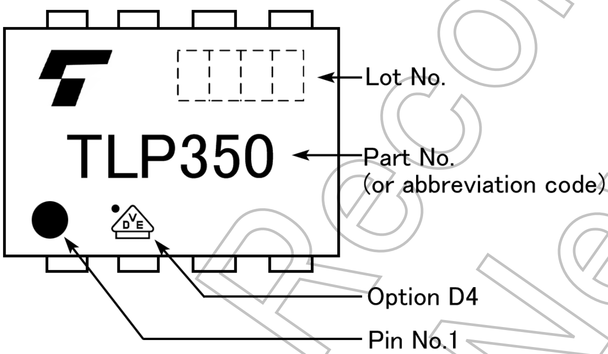


Fig. 17.4 Marking Example (Note)

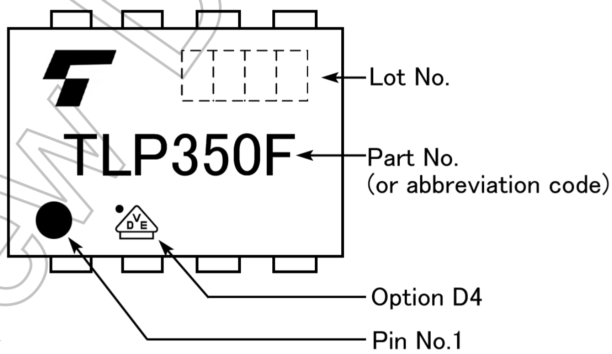


Fig. 17.5 Marking Example (Note)

Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN60747.

Figure 1 Partial discharge measurement procedure according to EN60747
Destructive test for qualification and sampling tests.

Method A

(for type and sampling tests, destructive tests)

t_1, t_2	= 1 to 10 s
t_3, t_4	= 1 s
t_p (Measuring time for partial discharge)	= 10 s
t_b	= 12 s
t_{ini}	= 60 s

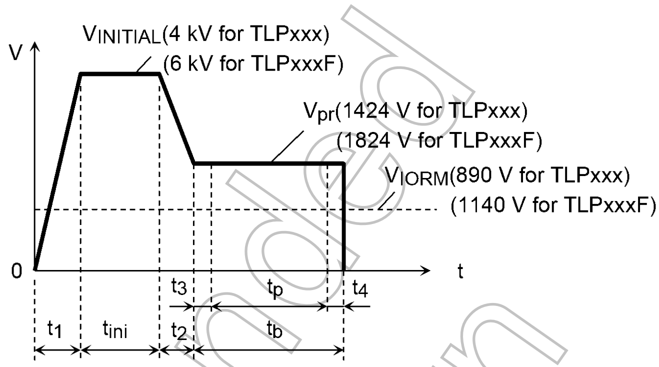


Figure 2 Partial discharge measurement procedure according to EN60747
Non-destructive test for 100 % inspection.

Method B

(for sample test, non-destructive test)

t_3, t_4	= 0.1 s
t_p (Measuring time for partial discharge)	= 1 s
t_b	= 1.2 s

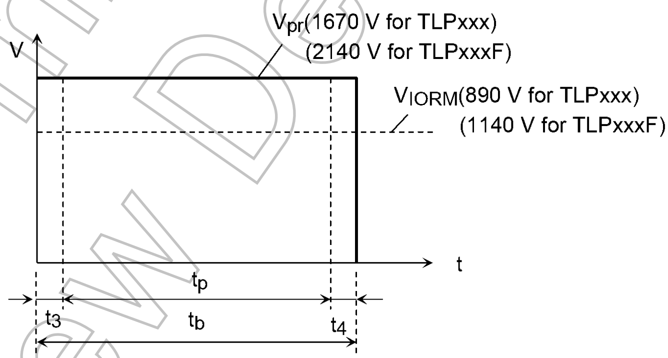


Figure 3 Dependency of maximum safety ratings on ambient temperature

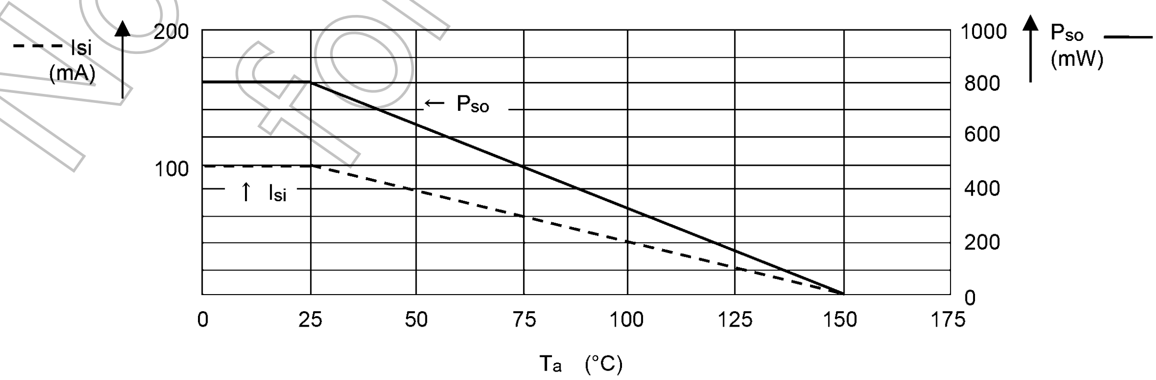
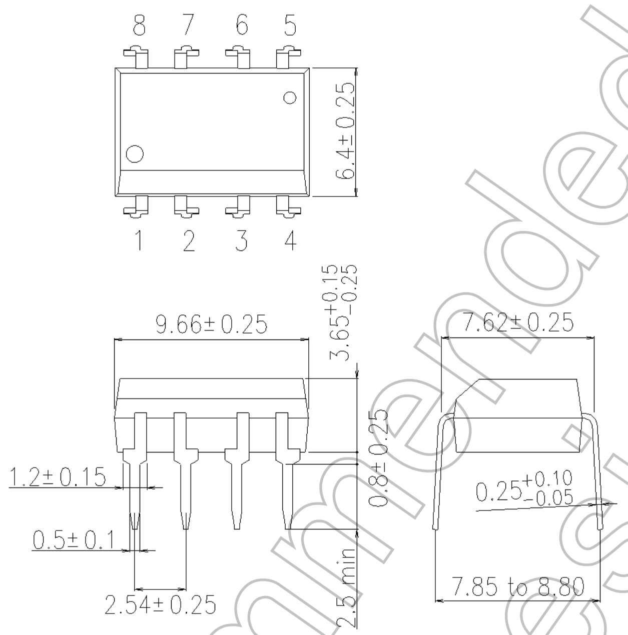


Fig. 17.6 Measurement Procedure

Package Dimensions

Unit: mm

TLP350



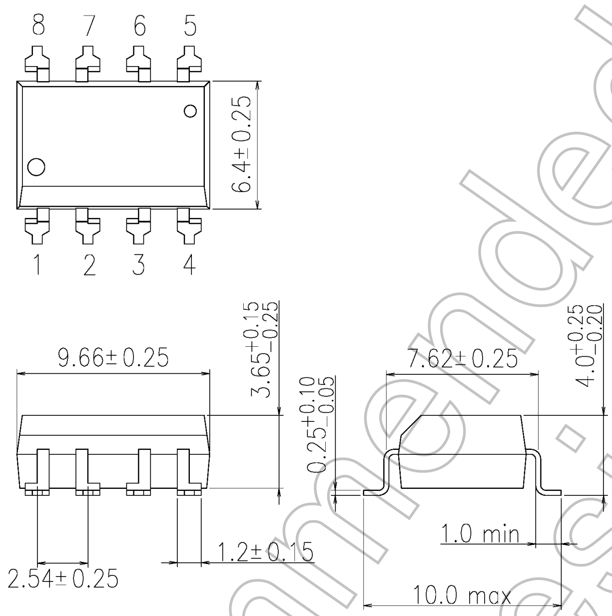
Weight: 0.54 g (typ.)

Package Name(s)
TOSHIBA: 11-10C4S

Package Dimensions

Unit: mm

TLP350(LF1,TP1)



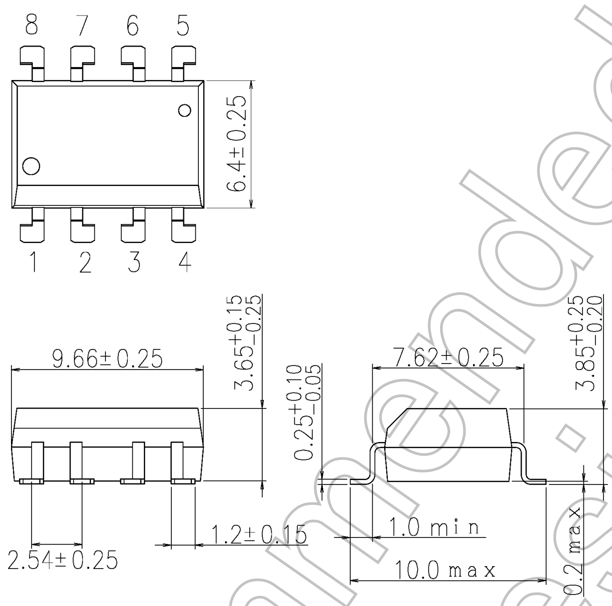
Weight: 0.53 g (typ.)

Package Name(s)
TOSHIBA: 11-10C401S

Package Dimensions

Unit: mm

TLP350(LF5,TP5)



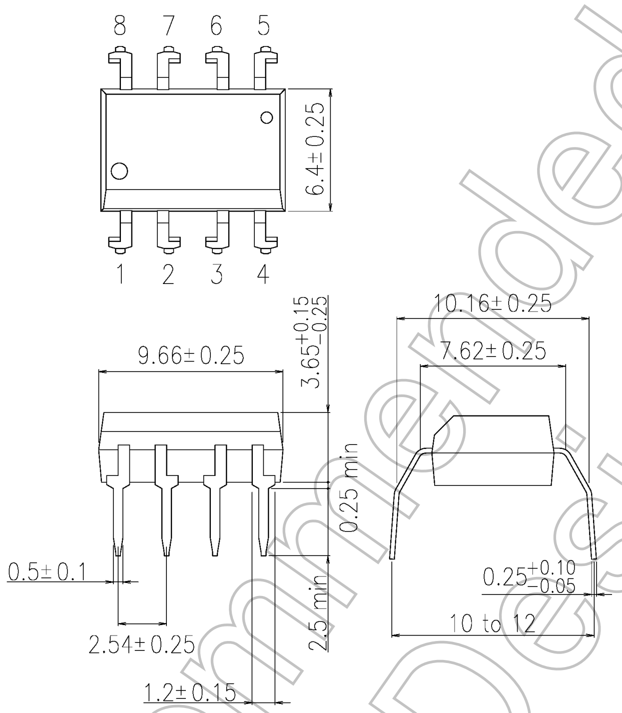
Weight: 0.53 g (typ.)

Package Name(s)
TOSHIBA: 11-10C405S

Package Dimensions

Unit: mm

TLP350F



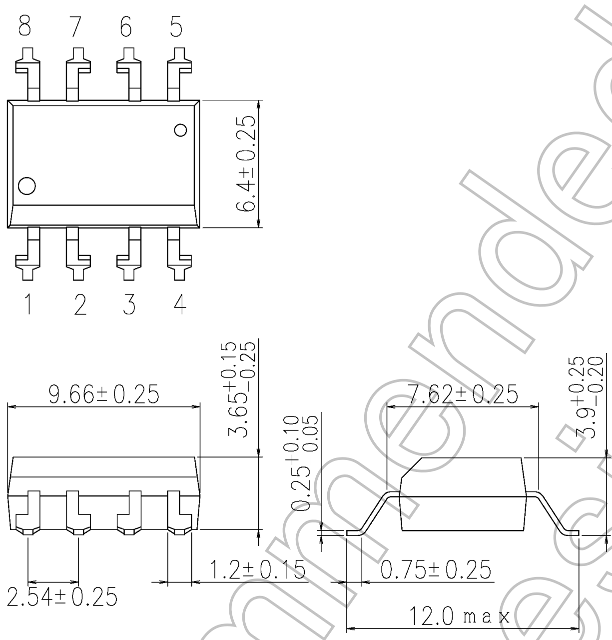
Weight: 0.54 g (typ.)

Package Name(s)
TOSHIBA: 11-10C402S

Package Dimensions

Unit: mm

TLP350F(LF4,TP4)



Weight: 0.53 g (typ.)

Package Name(s)
TOSHIBA: 11-10C404S

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