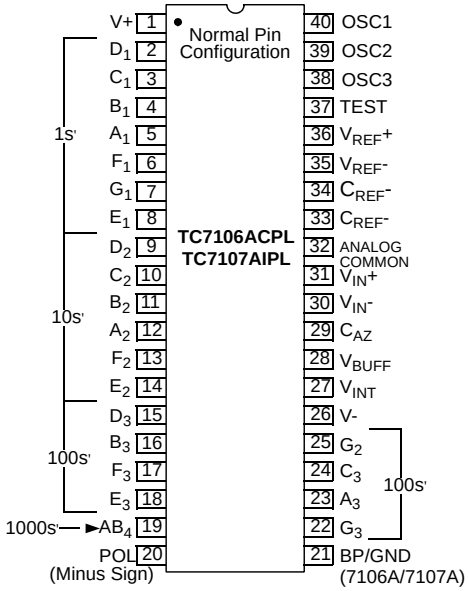
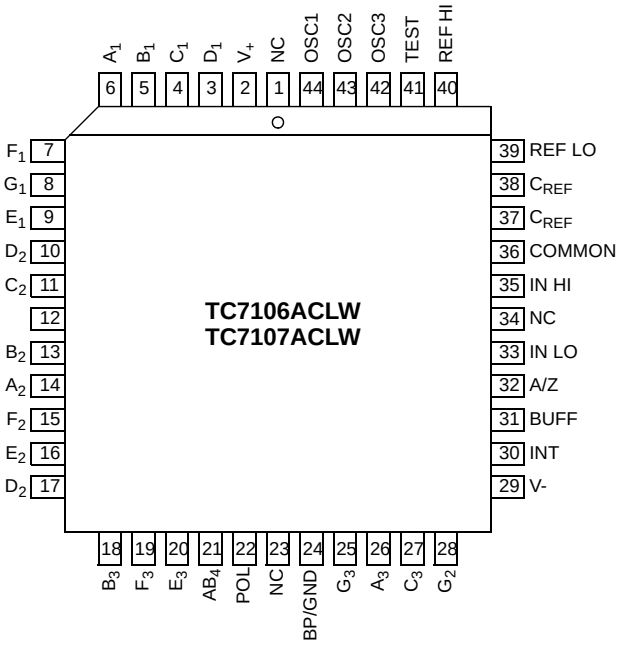
Package Type

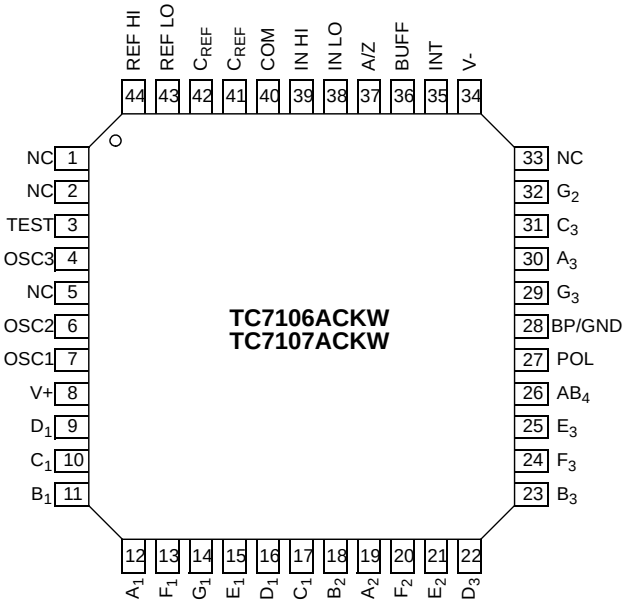
40-Pin PDIP



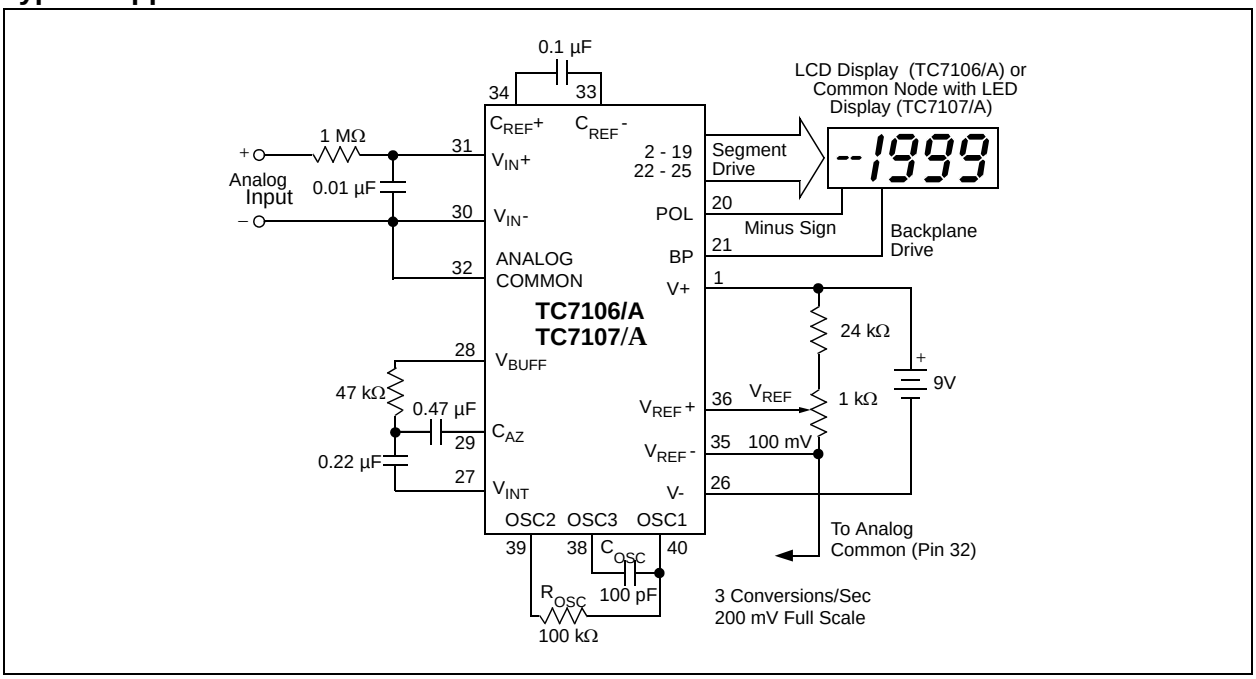
44-Pin PLCC



44-Pin MQFP



Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

TC7106A

Supply Voltage (V+ to V-) 15V
Analog Input Voltage (either Input) **(Note 1)** ..... V+ to V-

Reference Input Voltage (either Input) ..... V+ to V-
Clock Input ..... Test to V+
Package Power Dissipation ($T_A \leq 70°C$) **(Note 2)**:

40-Pin PDIP 1.23W
44-Pin PLCC 1.23W
44-Pin MQFP 1.00W

Operating Temperature Range:
C (Commercial) Devices ..... 0°C to +70°C
I (Industrial) Devices ..... -25°C to +85°C

Storage Temperature Range ..... -65°C to +150°C

TC7107A

Supply Voltage (V+) ..... +6V
Supply Voltage (V-) ..... -9V
Analog Input Voltage (either Input) **(Note 1)** ..... V+ to V-

Reference Input Voltage (either Input) ..... V+ to V-
Clock Input ..... GND to V+
Package Power Dissipation ($T_A \leq 70°C$) **(Note 2)**:

40-Pin PDIP 1.23W
44-Pin PLCC 1.23W
44-Pin MQFP 1.00W

Operating Temperature Range:
C (Commercial) Devices ..... 0°C to +70°C
I (Industrial) Devices ..... -25°C to +85°C

Storage Temperature Range ..... -65°C to +150°C

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC7106/A AND TC7107/A ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise noted, specifications apply to both the TC7106/TC7106A and TC7107/TC7107A at T_A = +25°C, f_{CLOCK} = 48 kHz. Parts are tested in the circuit of the Typical Operating Circuit.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Input Reading	Z_{IR}	-000.0	±000.0	+000.0	Digital Reading	V_{IN} = 0.0V Full Scale = 200.0 mV
Ratiometric Reading		999	999/1000	1000	Digital Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full Scale)	R/O	-1	±0.2	+1	Counts	$V_{IN}- = + V_{IN}+ \cong$ 200 mV
Linearity (Maximum Deviation from Best Straight Line Fit)		-1	±0.2	+1	Counts	Full Scale = 200 mV or Full Scale = 2.000V
Common Mode Rejection Ratio **(Note 3)**	CMRR	—	50	—	µV/V	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200.0 mV
Noise (Peak to Peak Value not Exceeded 95% of Time)	e_N	—	15	—	µV	V_{IN} = 0V Full Scale - 200.0 mV
Leakage Current at Input	I_L	—	1	10	pA	V_{IN} = 0V
Zero Reading Drift		—	0.2	1	µV/°C	V_{IN} = 0V "C" Device = 0°C to +70°C
		—	1.0	2	µV/°C	V_{IN} = 0V "I" Device = -25°C to +85°C
Scale Factor Temperature Coefficient	TC_{SF}	—	1	5	ppm/°C	V_{IN} = 199.0 mV, "C" Device = 0°C to +70°C (Ext. Ref = 0 ppm°C)
		—	—	20	ppm/°C	V_{IN} = 199.0 mV "I" Device = -25°C to +85°C
Supply Current (Does not include LED Current For TC7107/A)	I_{DD}	—	0.8	1.8	mA	V_{IN} = 0.8
Analog Common Voltage (with Respect to Positive Supply)	V_C	2.7	3.05	3.35	V	25 kΩ Between Common and Positive Supply

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100 µA.
2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3: Refer to "Differential Input" discussion.
4: Backplane drive is in phase with segment drive for "OFF" segment, 180° out of phase for "ON" segment. Frequency is 20 times the conversion rate. Average DC component is less than 50 mV.

TC7106/A AND TC7107/A ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise noted, specifications apply to both the TC7106/TC7106A and TC7107/TC7107A at T_A = +25°C, f_{CLOCK} = 48 kHz. Parts are tested in the circuit of the Typical Operating Circuit.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Temperature Coefficient of Analog Common (with Respect to Positive Supply)	V_{CTC}	—	—	—	—	25 kΩ Between Common and Positive Supply
		7106/7/A 7106/7	20 80	50 —	ppm/°C ppm/°C	0°C ≤ T_A ≤ +70°C ("C" Commercial Temperature Range Devices)
Temperature Coefficient of Analog Common (with Respect to Positive Supply)	V_{CTC}	—	—	75	ppm/°C	0°C ≤ T_A ≤ +70°C ("I" Industrial Temperature Range Devices)
TC7106A ONLY Peak to Peak Segment Drive Voltage	V_{SD}	4	5	6	V	V+ to V- = 9V **(Note 4)**
TC7106A ONLY Peak to Peak Backplane Drive Voltage	V_{BD}	4	5	6	V	V+ to V- = 9V **(Note 4)**
TC7107A ONLY Segment Sinking Current (Except Pin 19)		5	8.0	—	mA	V+ = 5.0V Segment Voltage = 3V
TC7107A ONLY Segment Sinking Current (Pin 19)		10	16	—	mA	V+ = 5.0V Segment Voltage = 3V

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100 µA.
2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3: Refer to "Differential Input" discussion.
4: Backplane drive is in phase with segment drive for "OFF" segment, 180° out of phase for "ON" segment. Frequency is 20 times the conversion rate. Average DC component is less than 50 mV.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number (40-Pin PDIP) Normal	Pin No. (40-Pin PDIP) (Reversed	Symbol	Description
1	(40)	V+	Positive supply voltage.
2	(39)	D_1	Activates the D section of the units display.
3	(38)	C_1	Activates the C section of the units display.
4	(37)	B_1	Activates the B section of the units display.
5	(36)	A_1	Activates the A section of the units display.
6	(35)	F_1	Activates the F section of the units display.
7	(34)	G_1	Activates the G section of the units display.
8	(33)	E_1	Activates the E section of the units display.
9	(32)	D_2	Activates the D section of the tens display.
10	(31)	C_2	Activates the C section of the tens display.
11	(30)	B_2	Activates the B section of the tens display.
12	(29)	A_2	Activates the A section of the tens display.
13	(28)	F_2	Activates the F section of the tens display.
14	(27)	E_2	Activates the E section of the tens display.
15	(26)	D_3	Activates the D section of the hundreds display.
16	(25)	B_3	Activates the B section of the hundreds display.
17	(24)	F_3	Activates the F section of the hundreds display.
18	(23)	E_3	Activates the E section of the hundreds display.
19	(22)	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	POL	Activates the negative polarity display.
21	(20)	BP/GND	LCD Backplane drive output (TC7106A). Digital Ground (TC7107A).
22	(19)	G_3	Activates the G section of the hundreds display.
23	(18)	A_3	Activates the A section of the hundreds display.
24	(17)	C_3	Activates the C section of the hundreds display.
25	(16)	G_2	Activates the G section of the tens display.
26	(15)	V-	Negative power supply voltage.
27	(14)	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for more details.
28	(13)	V_{BUFF}	Integration resistor connection. Use a 47 kΩ resistor for a 200 mV full scale range and a 47 kΩ resistor for 2V full scale range.
29	(12)	C_{AZ}	The size of the auto-zero capacitor influences system noise. Use a 0.47 µF capacitor for 200 mV full scale, and a 0.047 µF capacitor for 2V full scale. See **Section 7.1 "Auto-Zero Capacitor (CAZ)"** on Auto-Zero Capacitor for more details.
30	(11)	V_{IN}-	The analog LOW input is connected to this pin.
31	(10)	V_{IN}+	The analog HIGH input signal is connected to this pin.
32	(9)	ANALOG COMMON	This pin is primarily used to set the Analog Common mode voltage for battery operation or in systems where the input signal is referenced to the power supply. It also acts as a reference voltage source. See **Section 8.3 "Analog Common (Pin 32)"** on ANALOG COMMON for more details.
33	(8)	C_{REF}-	See Pin 34.
34	(7)	C_{REF}+	A 0.1 µF capacitor is used in most applications. If a large Common mode voltage exists (for example, the V_{IN}- pin is not at analog common), and a 200 mV scale is used, a 1 µF capacitor is recommended and will hold the rollover error to 0.5 count.
35	(6)	V_{REF}-	See Pin 36.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number (40-Pin PDIP) Normal	Pin No. (40-Pin PDIP) (Reversed	Symbol	Description
36	(5)	$V_{REF}+$	The analog input required to generate a full scale output (1999 counts). Place 100 mV between Pins 35 and 36 for 199.9 mV full scale. Place 1V between Pins 35 and 36 for 2V full scale. See paragraph on Reference Voltage.
37	(4)	TEST	Lamp test. When pulled HIGH (to V+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	OSC3	See Pin 40.
39	(2)	OSC2	See Pin 40.
40	(1)	OSC1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section), connect Pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to Pin 39 and the 100 pF capacitor is tied to Pin 38.

3.0 DETAILED DESCRIPTION

(*All Pin designations refer to 40-Pin PDIP.*)

3.1 Dual Slope Conversion Principles

The TC7106A and TC7107A are dual slope, integrating Analog-to-Digital Converters. An understanding of the dual slope conversion technique will aid in following the detailed operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (De-integration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}). See Figure 3-1.

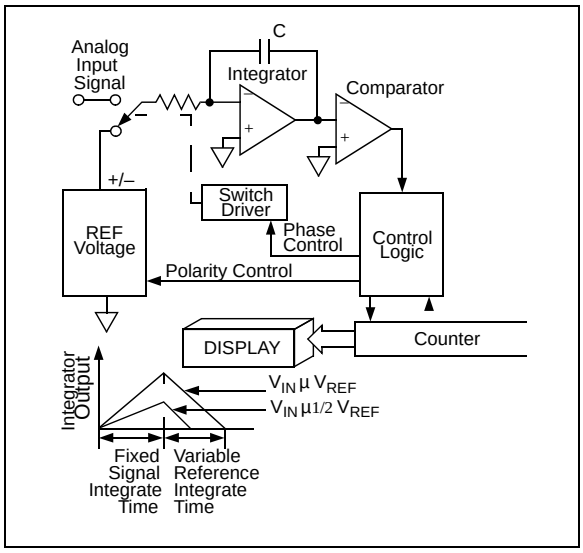


FIGURE 3-1: *Basic Dual Slope Converter.*

In a simple dual slope converter, a complete conversion requires the integrator output to “ramp-up” and “ramp-down.” A simple mathematical equation relates the input signal, reference voltage and integration time.

EQUATION 3-1:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

Where:

V_R	=	Reference voltage
T_{SI}	=	Signal integration time (fixed)
T_{RI}	=	Reference voltage integration time (variable).

For a constant V_{IN}:

EQUATION 3-2:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60Hz power line period (see Figure 3-2).

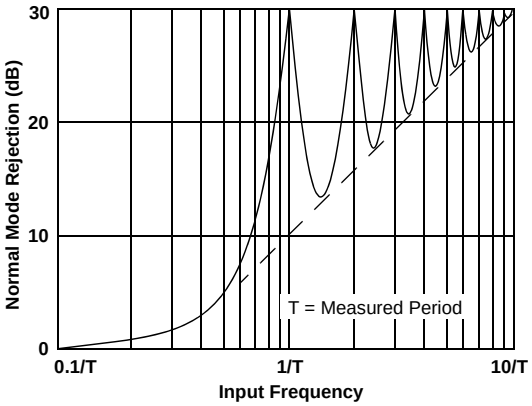


FIGURE 3-2: *Normal Mode Rejection of Dual Slope Converter.*

$$C_{INT} = \frac{(4000)\left(\frac{1}{F_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}}$$

Where:

F_{OSC}	=	Clock Frequency at Pin 38
V_{FS}	=	Full Scale Input Voltage
R_{INT}	=	Integrating Resistor
V_{INT}	=	Desired Full Scale Integrator Output Swing

4.0 ANALOG SECTION

In addition to the basic signal integrate and de-integrate cycles discussed, the circuit incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without adjusting external potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate, and reference integrate cycle.

4.1 Auto-Zero Cycle

During the auto-zero cycle, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The offset error referred to the input is less than 10 µV.

The auto-zero cycle length is 1000 to 3000 counts.

4.2 Signal Integrate Cycle

The auto-zero loop is entered and the internal differential inputs connect to $V_{IN}+$ and $V_{IN}-$. The differential input signal is integrated for a fixed time period. The TC7106/TC7106A signal integration period is 1000 clock periods or counts. The externally set clock frequency is divided by four before clocking the internal counters.

The integration time period is:

EQUATION 4-1:

$$T_{SI} = \frac{4}{F_{OSC}} \times 1000$$

Where:

F_{OSC} = Externally set clock frequency

The differential input voltage must be within the device Common mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, $V_{IN}-$ should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

4.3 Reference Integrate Phase

The third phase is reference integrate or de-integrate. $V_{IN}-$ is internally connected to analog common and $V_{IN}+$ is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero.

The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 counts.

The digital reading displayed is:

EQUATION 4-2:

$$1000 = \frac{V_{IN}}{V_{REF}}$$

5.0 DIGITAL SECTION (TC7106A)

The TC7106A (Figure 5-2) contains all the segment drivers necessary to directly drive a 3-1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions per second, the backplane frequency is 60Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal, the segment is “OFF.” An out of phase segment drive signal causes the segment to be “ON” or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is “ON” for negative analog inputs. If V_{IN}+ and V_{IN}- are reversed, this indicator will reverse.

When the TEST pin on the TC7106A is pulled to V+, all segments are turned “ON.” The display reads -1888. During this mode, the LCD segments have a constant DC voltage impressed. DO NOT LEAVE THE DISPLAY IN THIS MODE FOR MORE THAN SEVERAL MINUTES! LCD displays may be destroyed if operated with DC levels for extended periods.

The display font and the segment drive assignment are shown in Figure 5-1.

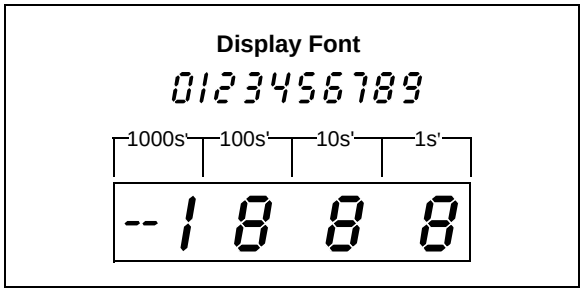


FIGURE 5-1: *Display Font and Segment Assignment*

In the TC7106A, an internal digital ground is generated from a 6-volt zener diode and a large P channel source follower. This supply is designed to absorb the large capacitive currents when the backplane voltage is switched.

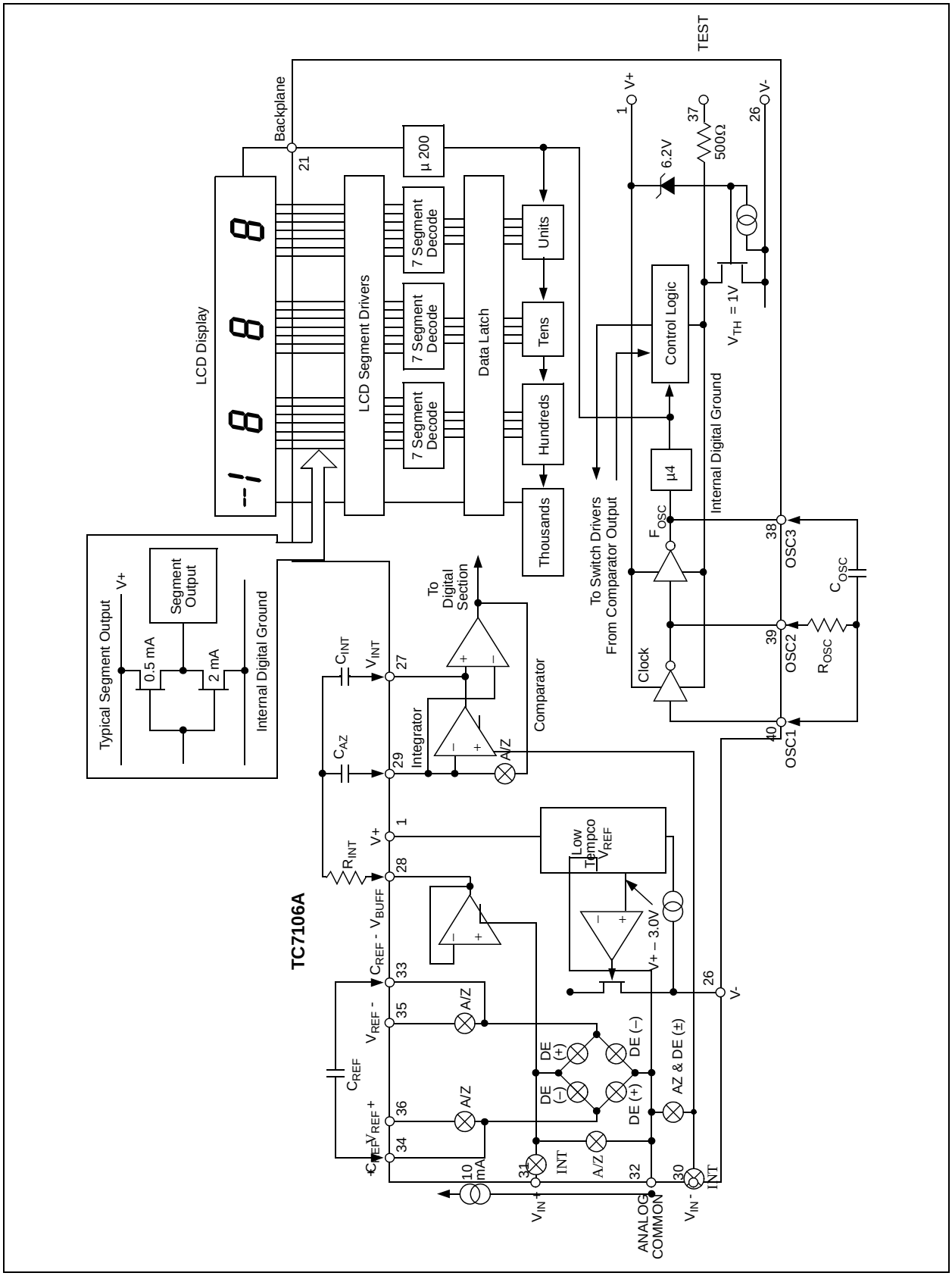


FIGURE 5-2: *TC7106A Block Diagram.*

6.0 DIGITAL SECTION (TC7107A)

Figure 6-2 shows a TC7106A block diagram. It is designed to drive common anode LEDs. It is identical to the TC7106A, except that the regulated supply and backplane drive have been eliminated and the segment drive is typically 8 mA. The 1000's output (Pin 19) sinks current from two LED segments, and has a 16 mA drive capability.

In both devices, the polarity indication is "ON" for negative analog inputs. If V_{IN}- and V_{IN}+ are reversed, this indication can be reversed also, if desired.

The display font is the same as the TC7106A.

6.1 System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 4000 counts, or 16,000 clock pulses. The 4000-count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

1. Auto-zero phase: 1000 to 3000 counts (4000 to 12000 clock pulses).

For signals less than full scale, the auto-zero phase is assigned the unused reference integrate time period:

2. Signal integrate: 1000 counts (4000 clock pulses).

This time period is fixed. The integration period is:

EQUATION 6-1:

$$T_{SI} = \frac{4}{F_{OSC}} \times 1000$$

Where:

F_{OSC} = Externally set clock frequency

3. Reference Integrate: 0 to 2000 counts (0 to 8000 clock pulses).

The TC7106A/TC7107A are drop-in replacements for the TC7106/TC7107 parts. External component value changes are not required to benefit from the low drift internal reference.

6.2 Clock Circuit

Three clocking methods may be used (see Figure 6-1):

1. An external oscillator connected to Pin 40.
2. A crystal between Pins 39 and 40.
3. An RC oscillator using all three pins.

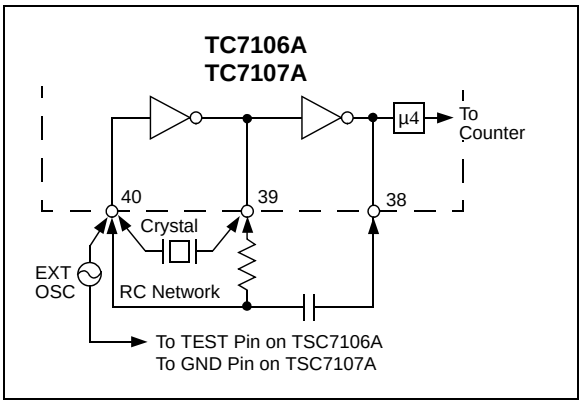


FIGURE 6-1: *Clock Circuits.*

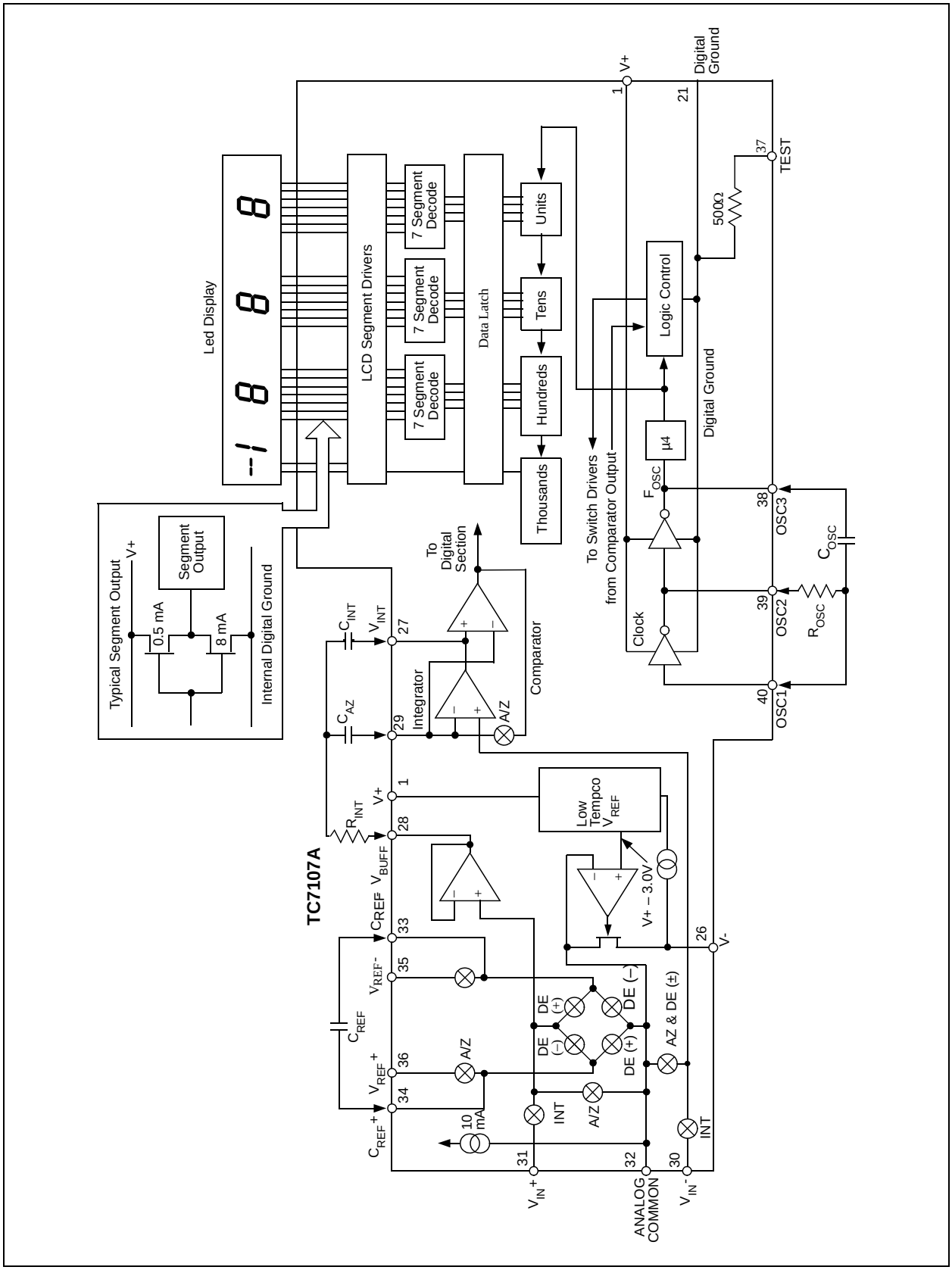


FIGURE 6-2: *TC7107A Block Diagram.*

7.0 COMPONENT VALUE SELECTION

7.1 Auto-Zero Capacitor (C_{AZ})

The C_{AZ} capacitor size has some influence on system noise. A 0.47 µF capacitor is recommended for 200 mV full scale applications where 1LSB is 100 µV. A 0.047 µF capacitor is adequate for 2.0V full scale applications. A mylar type dielectric capacitor is adequate.

7.2 Reference Voltage Capacitor (C_{REF})

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 µF capacitor is acceptable when V_{IN}- is tied to analog common. If a large Common mode voltage exists (V_{REF}- – analog common) and the application requires 200 mV full scale, increase C_{REF} to 1.0 µF. Rollover error will be held to less than 1/2 count. A mylar dielectric capacitor is adequate.

7.3 Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize the integrator output voltage swing without causing output saturation. Due to the TC7106A/TC7107A superior temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case, a ±2V full scale integrator output swing is satisfactory. For 3 readings/second (F_{OSC} = 48 kHz), a 0.22 µF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing.

An exact expression for C_{INT} is:

EQUATION 7-1:

$$C_{INT} = \frac{(4000)\left(\frac{1}{F_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}}$$

Where:

F_{OSC}	=	Clock Frequency at Pin 38
V_{FS}	=	Full Scale Input Voltage
R_{INT}	=	Integrating Resistor
V_{INT}	=	Desired Full Scale Integrator Output Swing

C_{INT} must have low dielectric absorption to minimize rollover error. A polypropylene capacitor is recommended.

7.4 Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 100 µA. The integrator and buffer can supply 20 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region, but not so large that printed circuit board leakage currents induce errors. For a 200 mV full scale, R_{INT} is 47 kΩ. 2.0V full scale requires 470 kΩ.

TABLE 7-1: COMPONENT VALUES AND NOMINAL FULL SCALE VOLTAGE

Component Value	Nominal Full Scale Voltage	
	200.0 mV	2.000V
C_{AZ}	0.47 µF	0.047 µF
R_{INT}	47 kΩ	470 kΩ
C_{INT}	0.22 µF	0.22 µF

Note: F_{OSC} = 48 kHz (3 readings per sec).

7.5 Oscillator Components

R_{OSC} (Pin 40 to Pin 39) should be 100 kΩ. C_{OSC} is selected using the equation:

EQUATION 7-2:

$$F_{OSC} = \frac{0.45}{RC}$$

Where:

F_{OSC}	=	48 kHz
C_{OSC}	=	100 pF

Note that F_{OSC} is divided by four to generate the TC7106A internal control clock. The backplane drive signal is derived by dividing F_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48 kHz, 40 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 Hz and 60 Hz.

7.6 Reference Voltage Selection

A full scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full Scale Voltage*	V_{REF}
200.0 mV	100.0 mV
2.000V	1.000V

* $V_{FS} = 2V_{REF}$

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400 mV for 2000 lb/in^2. Rather than dividing the input voltage by two, the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}-. The transducer output is connected between V_{IN}+ and analog common.

The internal voltage reference potential available at analog common will normally be used to supply the converter's reference. This potential is stable whenever the supply potential is greater than approximately 7V. In applications where an externally generated reference voltage is desired, refer to Figure 7-1.

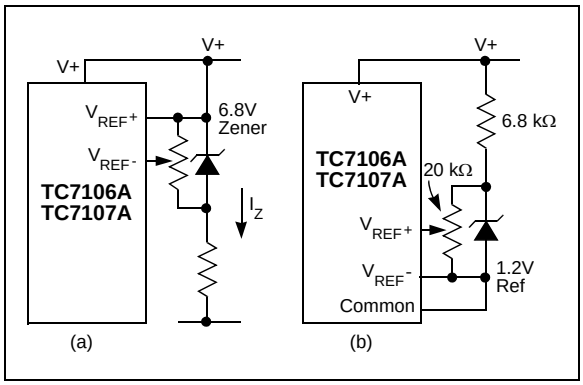


FIGURE 7-1: *External Reference.*

8.0 DEVICE PIN FUNCTIONAL DESCRIPTION

8.1 Differential Signal Inputs V_{IN}+ (Pin 31), V_{IN}- (Pin 30)

The TC7106A/TC7107A is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The typical range is V+ – 1.0 to V+ + 1V. Common mode voltages are removed from the system when the TC7106A/TC7107A operates from a battery or floating power source (isolated from measured system) and V_{IN}- is connected to analog common (V_{COM}) (see Figure 8-2).

In systems where Common mode voltages exist, the 86 dB Common mode rejection ratio minimizes error. Common mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worst-case condition exists if a large positive V_{CM} exists in conjunction with a full scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (see Figure 8-1). For such applications the integrator output swing can be reduced below the recommended 2.0V full scale swing. The integrator output will swing within 0.3V of V+ or V- without increasing linearity errors.

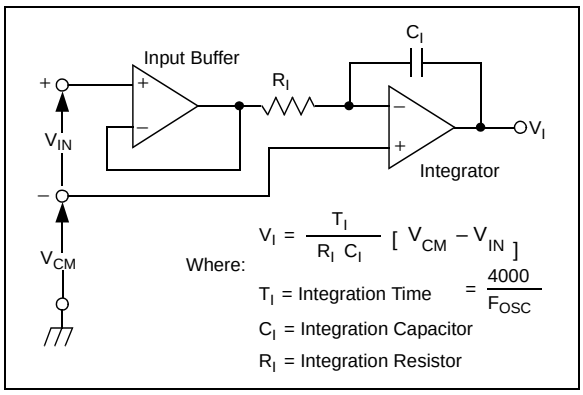


FIGURE 8-1: *Common Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$).*

8.2 Differential Reference V_{REF}+ (Pin 36), V_{REF}- (Pin 35)

The reference voltage can be generated anywhere within the V+ to V- power supply range.

To prevent rollover type errors being induced by large Common mode voltages, C_{REF} should be large compared to stray node capacitance.

The TC7106A/TC7107A circuits have a significantly lower analog common temperature coefficient. This gives a very stable voltage suitable for use as a reference. The temperature coefficient of analog common is 20 ppm/°C typically.

8.3 Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3.0V below V+. The potential is between 2.7V and 3.35V below V+. Analog common is tied internally to the N channel FET capable of sinking 20 mA. This FET will hold the common line at 3.0V should an external load attempt to pull the common line toward V+. Analog common source current is limited to 10 µA. Analog common is, therefore, easily pulled to a more negative voltage (i.e., below V+ – 3.0V).

The TC7106A connects the internal V_{IN}+ and V_{IN}- inputs to analog common during the auto-zero cycle. During the reference integrate phase, V_{IN}- is connected to analog common. If V_{IN}- is not externally connected to analog common, a Common mode voltage exists. This is rejected by the converter's 86 dB Common mode rejection ratio. In battery operation, analog common and V_{IN}- are usually connected, removing Common mode voltage concerns. In systems where V- is connected to the power supply ground, or to a given voltage, analog common should be connected to V_{IN}-.

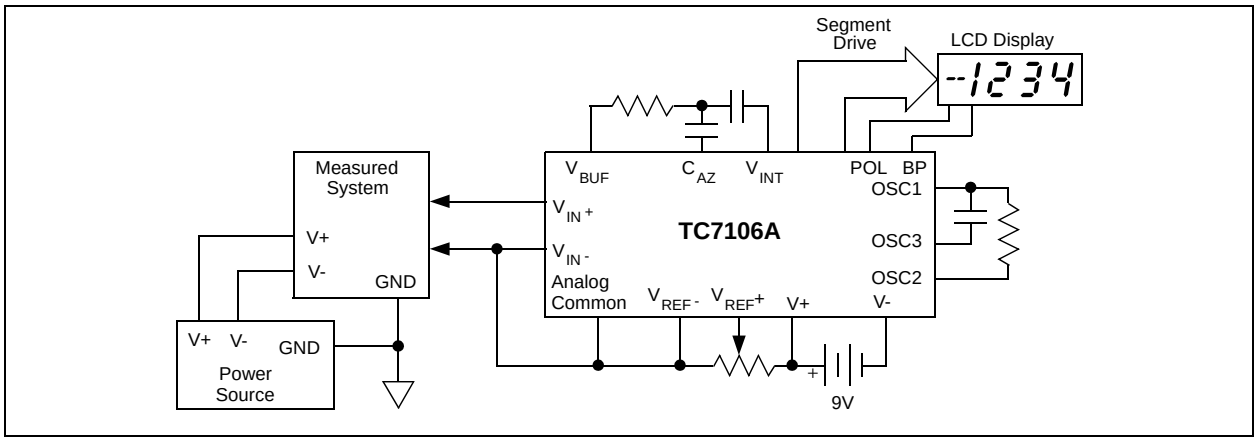


FIGURE 8-2: *Common Mode Voltage Removed in Battery Operation with V_{IN}- = Analog Common.*

The analog common pin serves to set the analog section reference or common point. The TC7106A is specifically designed to operate from a battery, or in any measurement system where input signals are not referenced (float), with respect to the TC7106A power source. The analog common potential of V+ – 3.0V gives a 6V end of battery life voltage. The common potential has a 0.001% voltage coefficient and a 15Ω output impedance.

With sufficiently high total supply voltage (V+ – V- > 7.0V), analog common is a very stable potential with excellent temperature stability, typically 20 ppm/°C. This potential can be used to generate the reference voltage. An external voltage reference will be unnecessary in most cases because of the 50 ppm/°C maximum temperature coefficient. See **Section 8.5 "Internal Voltage Reference"**.

8.4 TEST (Pin 37)

The TEST pin potential is 5V less than V+. TEST may be used as the negative power supply connection for external CMOS logic. The TEST pin is tied to the internally generated negative logic supply (Internal Logic Ground) through a 500Ω resistor in the TC7106A. The TEST pin load should be no more than 1 mA.

If TEST is pulled to V+ all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes with the TC7106A. With TEST = V+, the LCD segments are impressed with a DC voltage which will destroy the LCD.

The TEST pin will sink about 10 mA when pulled to V+.

8.5 Internal Voltage Reference

The analog common voltage temperature stability has been significantly improved (Figure 8-3). The "A" version of the industry standard circuits allow users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 8-4 shows analog common supplying the necessary voltage reference for the TC7106A/TC7107A.

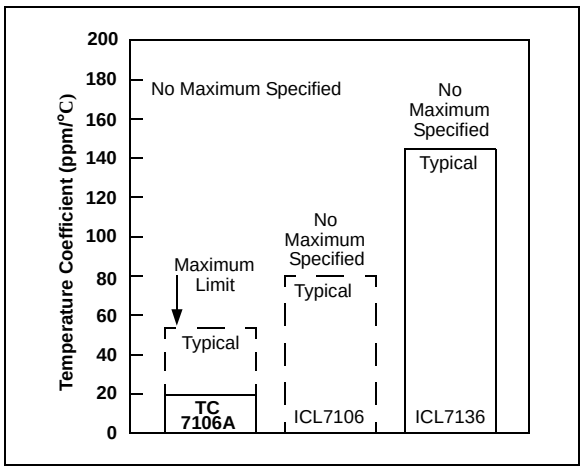


FIGURE 8-3: *Analog Common Temperature Coefficient.*

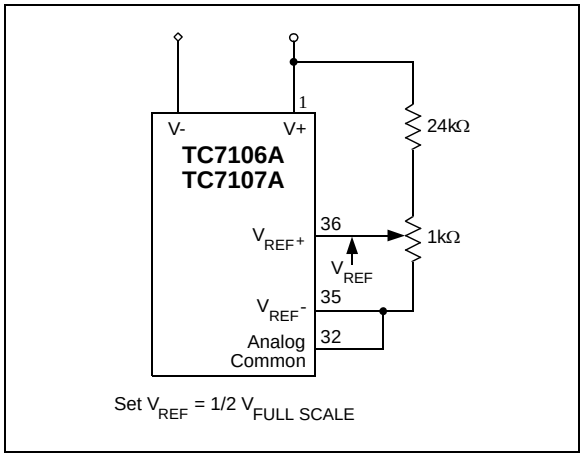


FIGURE 8-4: *Internal Voltage Reference Connection.*

9.0 POWER SUPPLIES

The TC7107A is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors, and an inexpensive IC (Figure 9-1).

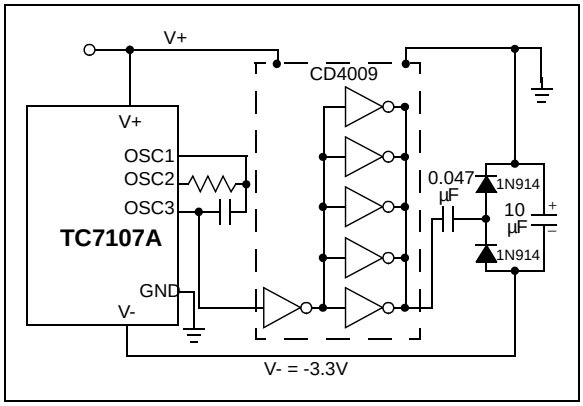


FIGURE 9-1: *Generating Negative Supply From +5V.*

In selected applications a negative supply is not required. The conditions to use a single +5V supply are:

- The input signal can be referenced to the center of the Common mode range of the converter.
- The signal is less than ±1.5V.
- An external reference is used.

The TSC7660 DC-to-DC converter may be used to generate -5V from +5V (Figure 9-2).

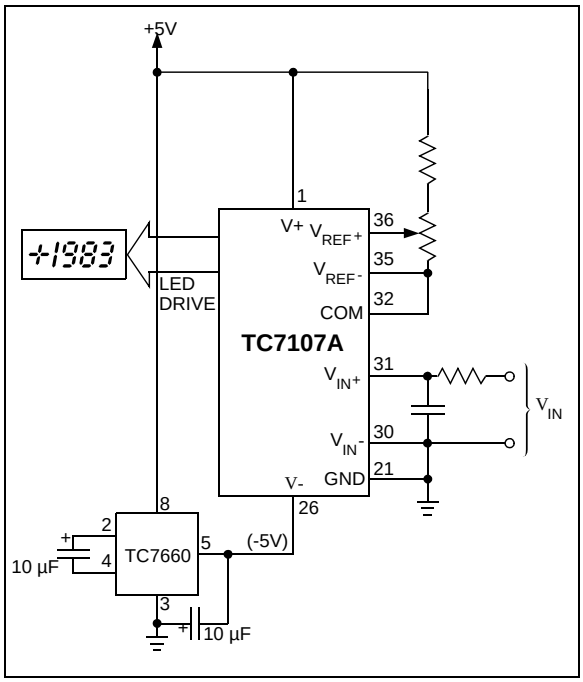


FIGURE 9-2: *Negative Power Supply Generation with TC7660.*

9.1 TC7107 Power Dissipation Reduction

The TC7107A sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing the LED common anode voltage, the TC7107A package power dissipation is reduced.

Figure 9-3 is a curve tracer display showing the relationship between output current and output voltage for a typical TC7107CPL. Since a typical LED has 1.8 volts across it at 7 mA, and its common anode is connected to +5V, the TC7107A output is at 3.2V (point A on Figure 9-3). Maximum power dissipation is 8.1 mA x 3.2V x 24 segments = 622 mW.

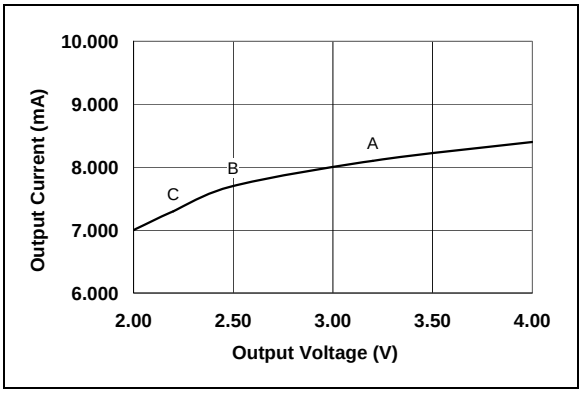


FIGURE 9-3: *TC7107 Output Current vs. Output Voltage.*

Notice, however, that once the TC7107A output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7V (point B in Figure 9-3) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is only 7.7 mA x 2.5V x 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38% (7.3 mA x 2.2V x 24 = 385 mW).

Reduced power dissipation is very easy to obtain. Figure 9-4 shows two ways: either a 5.1Ω, 1/4W resistor, or a 1A diode placed in series with the display (but not in series with the TC7107A). The resistor will reduce the TC7107A output voltage, when all 24 segments are “ON,” to point “C” of Figure 9-4. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point “B”.

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are “ON,” each “ON” output drops more voltage and current. For the best case of six segments (a “111” display) to worst-case (a “1888” display), the resistor will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, a diode may be used instead of the resistor.

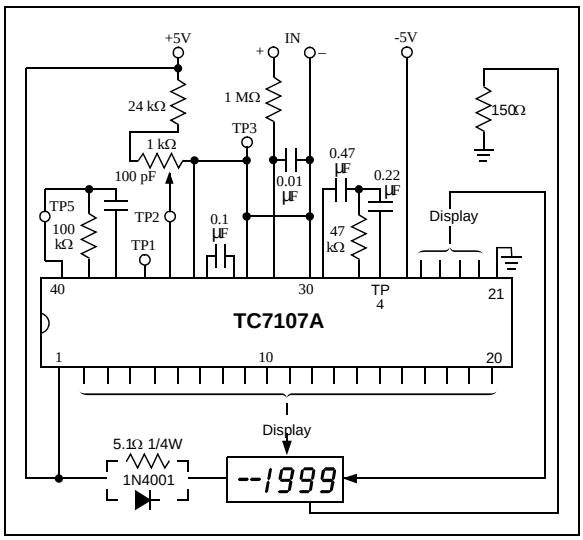


FIGURE 9-4: *Diode or Resistor Limits Package Power Dissipation.*

10.0 TYPICAL APPLICATIONS

10.1 Decimal Point and Annunciator Drive

The TEST pin is connected to the internally generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the TEST pin; its potential is approximately 5V below V+ (see Figure 10-1).

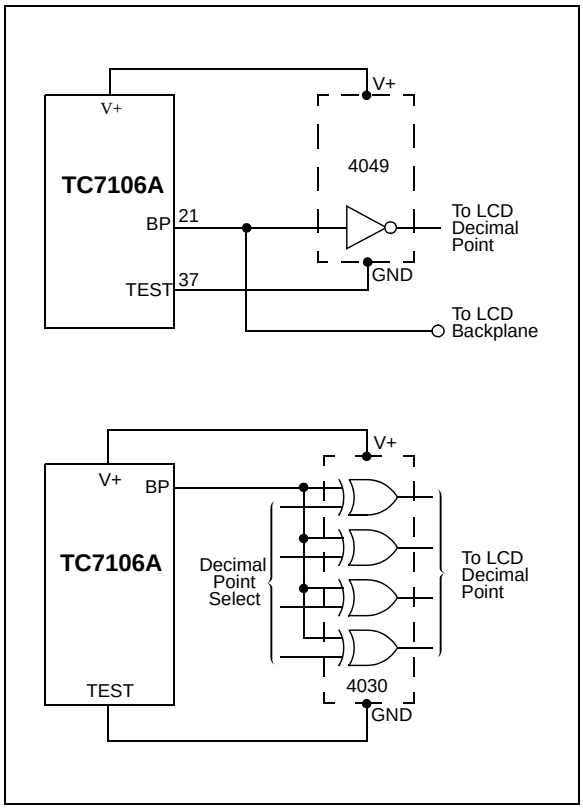


FIGURE 10-1: *Decimal Point Drive Using Test as Logic Ground.*

10.2 Ratiometric Resistance Measurements

The true differential input and differential reference make ratiometric reading possible. Typically in a ratiometric operation, an unknown resistance is measured, with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor is applied to the reference input. If the unknown equals the standard, the display will read 1000.

The displayed reading can be determined from the following expression:

EQUATION 10-1:

$$Displayed\ (Reading) = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000$$

The display will over range for:

$$R_{UNKNOWN} \geq 2 \times R_{STANDARD}$$

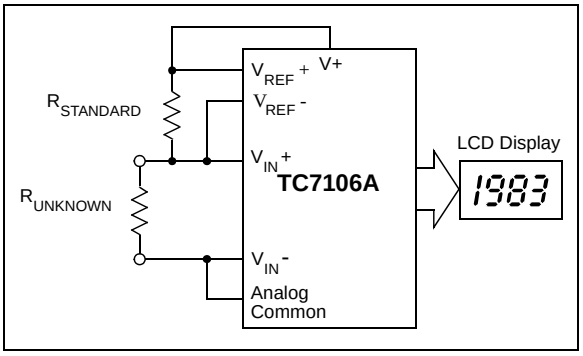


FIGURE 10-2: *Low Parts Count Ratiometric Resistance Measurement.*

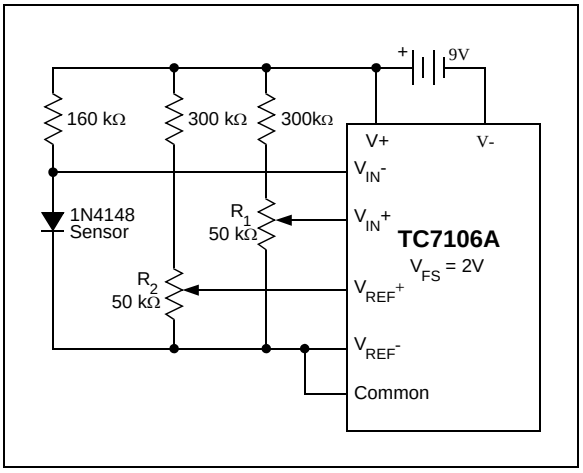


FIGURE 10-3: *Temperature Sensor.*

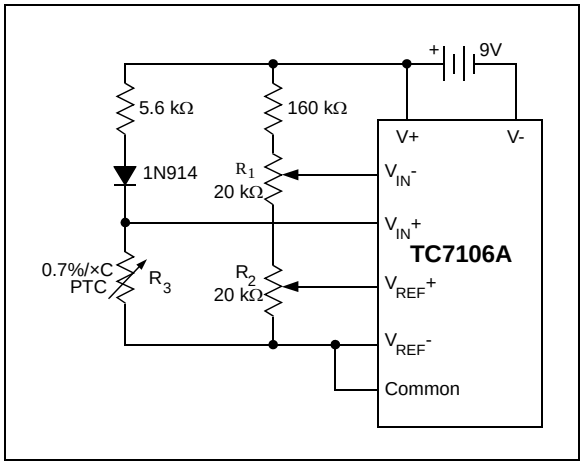


FIGURE 10-4: *Positive Temperature Coefficient Resistor Temperature Sensor.*

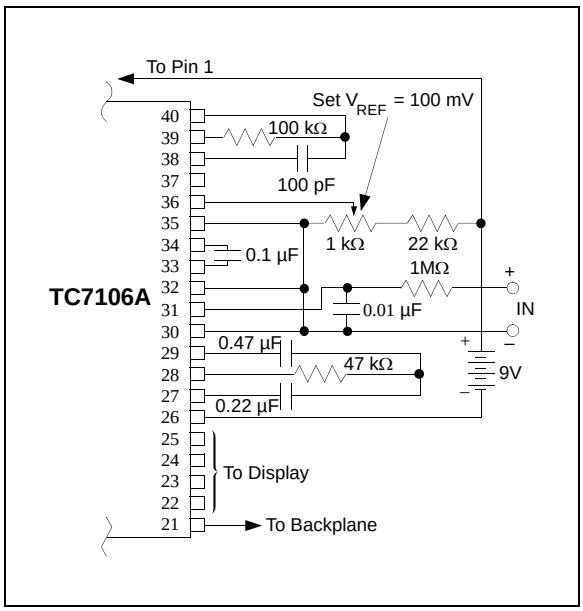


FIGURE 10-5: *TC7106A, Using the Internal Reference: 200 mV Full Scale, 3 Readings-Per-Second (RPS).*

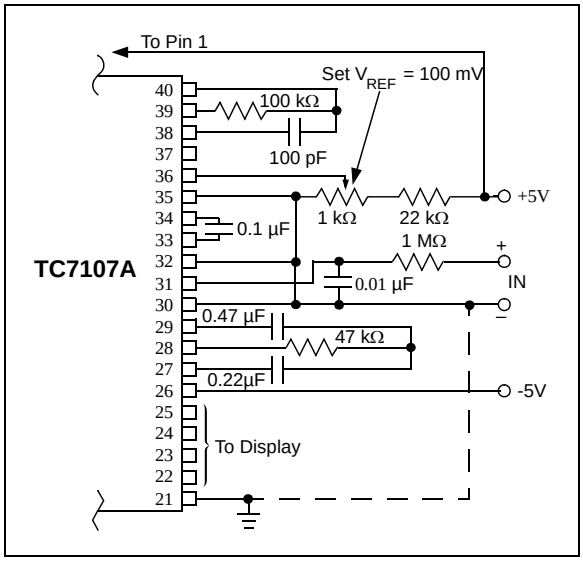


FIGURE 10-6: *TC7107 Internal Reference: 200 mV Full Scale, 3RPS, V_{IN}- Tied to GND for Single Ended Inputs.*

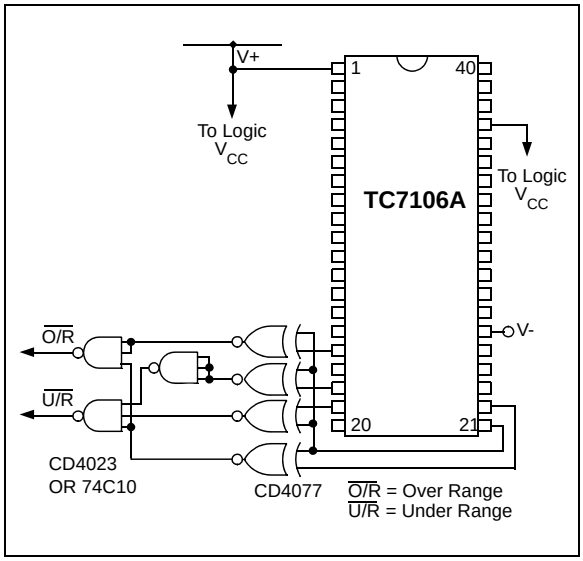


FIGURE 10-7: *Circuit for Developing Under Range and Over Range Signals from TC7106A Outputs.*

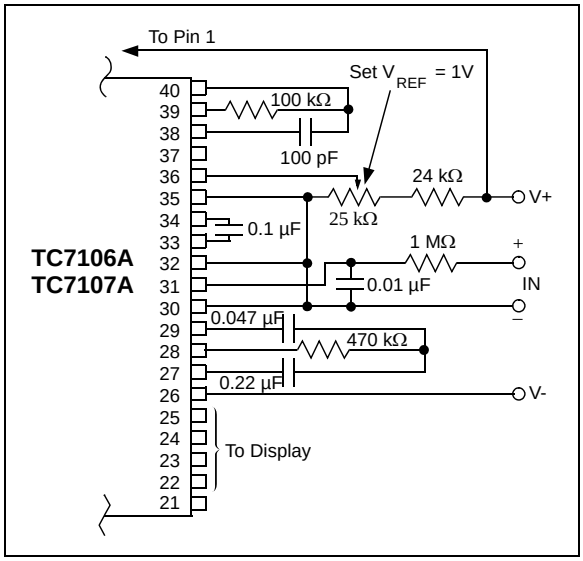


FIGURE 10-8: *TC7106/TC7107: Recommended Component Values for 2.00V Full Scale.*

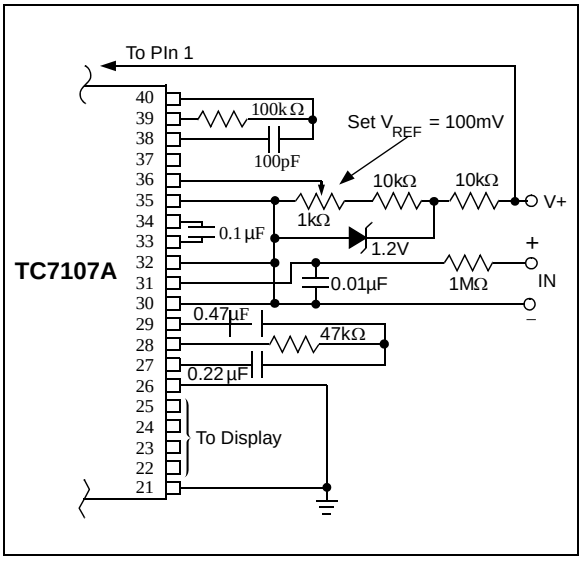


FIGURE 10-9: *TC7107 Operated from Single +5V Supply.*

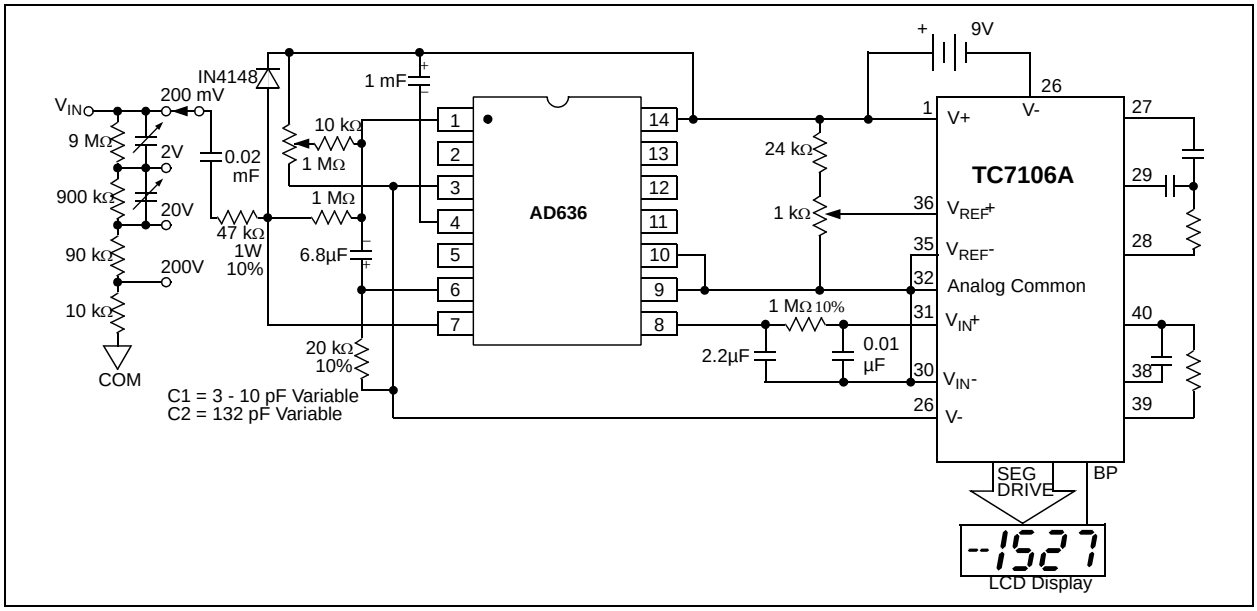


FIGURE 10-10: *3-1/2 Digit True RMS AC DMM.*

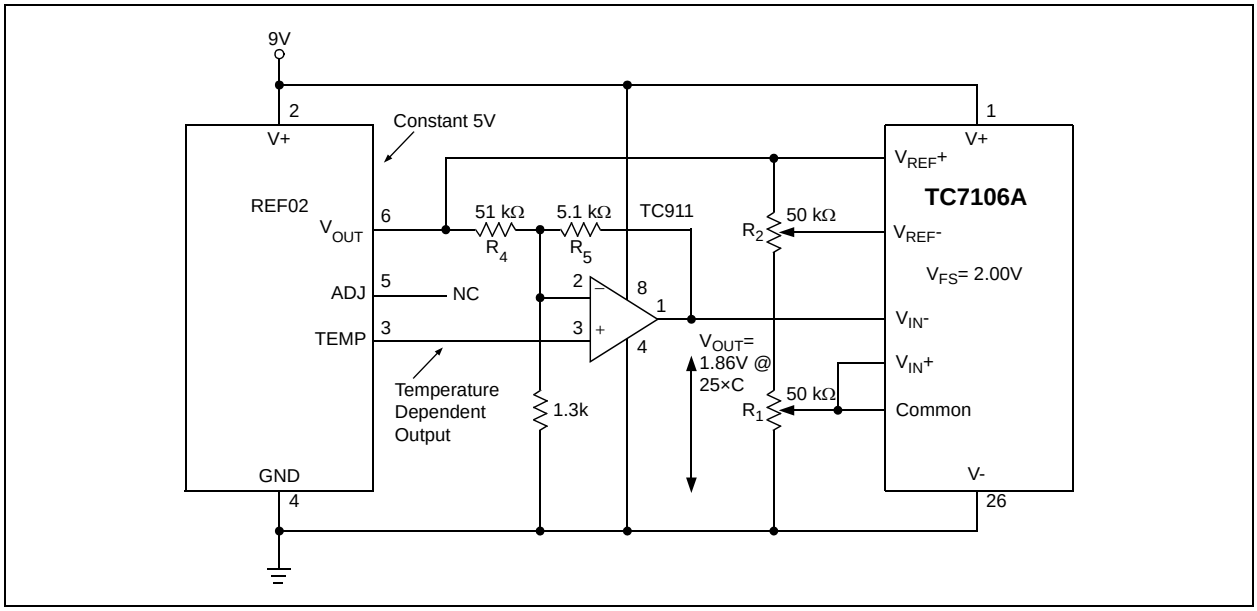
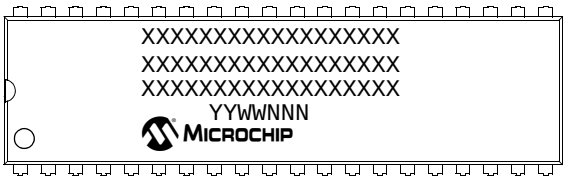


FIGURE 10-11: *Integrated Circuit Temperature Sensor.*

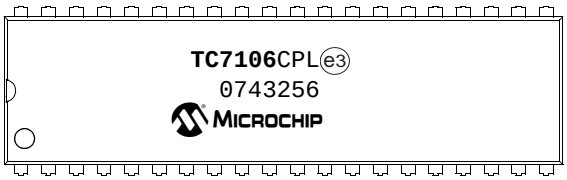
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

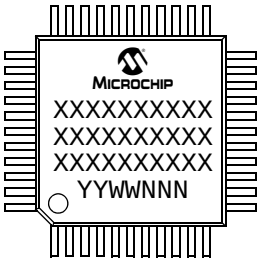
40-Pin PDIP



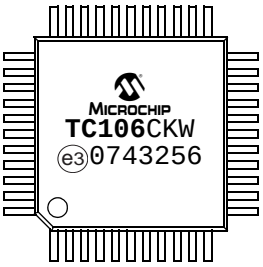
Example:



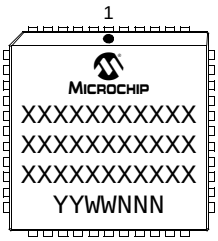
44-Pin MQFP



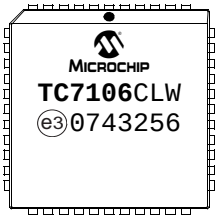
Example:



44-Pin PLCC



Example:

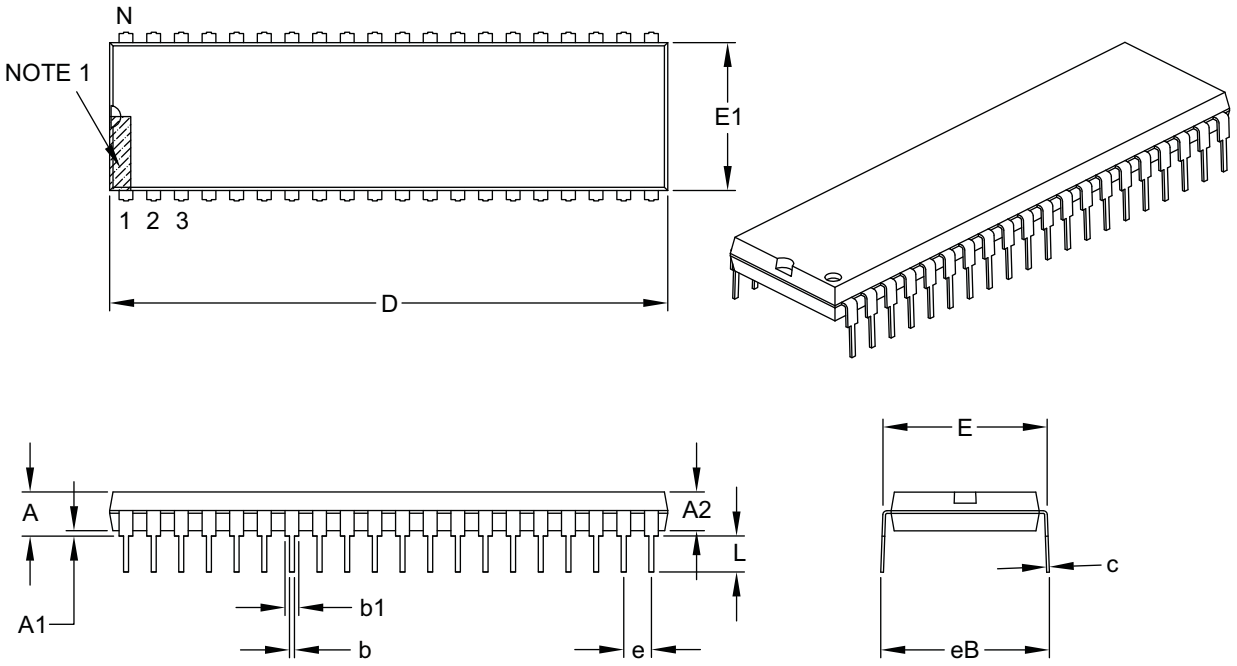


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

40-Lead Plastic Dual In-Line (PL) – 600 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.250
Molded Package Thickness	A2	.125	–	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.590	–	.625
Molded Package Width	E1	.485	–	.580
Overall Length	D	1.980	–	2.095
Tip to Seating Plane	L	.115	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.030	–	.070
Lower Lead Width	b	.014	–	.023
Overall Row Spacing §	eB	–	–	.700

Notes:

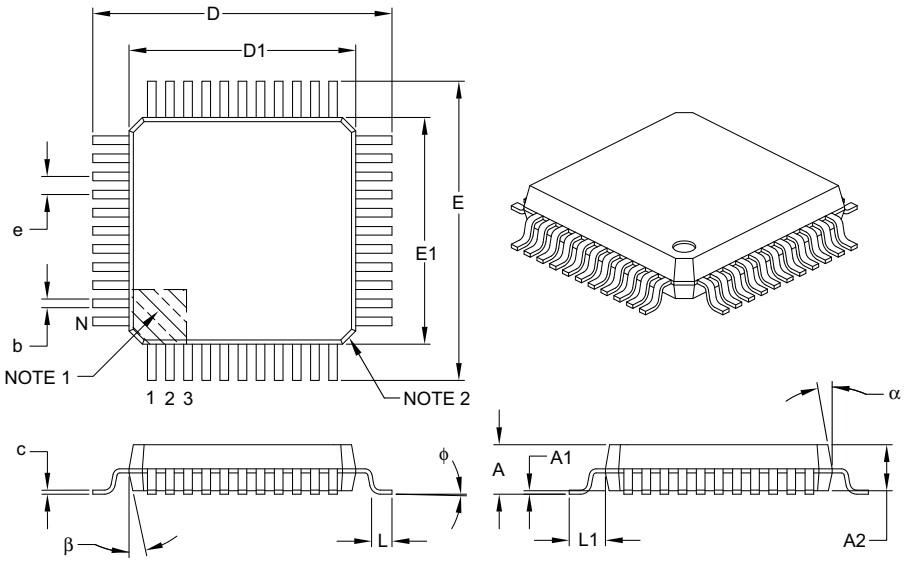
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-016B

44-Lead Plastic Metric Quad Flatpack (KW) – 10x10x2 mm Body, 3.20 mm [MQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	–	–	2.45
Molded Package Thickness	A2	1.80	2.00	2.20
Standoff §	A1	0.00	–	0.25
Foot Length	L	0.73	0.88	1.03
Footprint	L1		1.60 REF	
Foot Angle	φ	0°	–	7°
Overall Width	E		13.20 BSC	
Overall Length	D		13.20 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.11	–	0.23
Lead Width	b	0.29	–	0.45
Mold Draft Angle Top	α	5°	–	16°
Mold Draft Angle Bottom	β	5°	–	16°

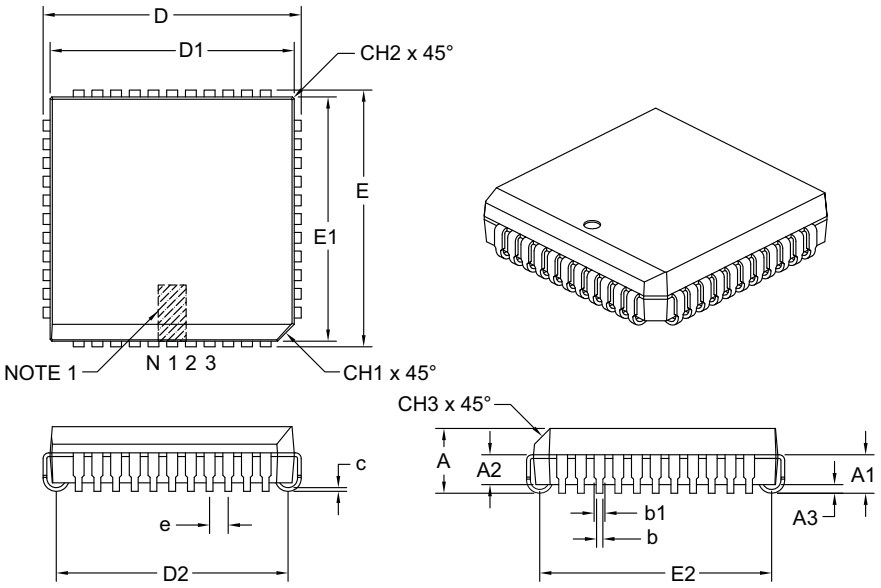
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. § Significant Characteristic.

Microchip Technology Drawing C04-071B

44-Lead Plastic Leaded Chip Carrier (LW) – Square [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		.050	
Overall Height	A	.165	.172	.180
Contact Height	A1	.090	.105	.120
Molded Package to Contact	A2	.062	–	.083
Standoff §	A3	.020	–	–
Corner Chamfer	CH1	.042	–	.048
Chamfers	CH2	–	–	.020
Side Chamfer	CH3	.042	–	.056
Overall Width	E	.685	.690	.695
Overall Length	D	.685	.690	.695
Molded Package Width	E1	.650	.653	.656
Molded Package Length	D1	.650	.653	.656
Footprint Width	E2	.582	.610	.638
Footprint Length	D2	.582	.610	.638
Lead Thickness	c	.0075	–	.0125
Upper Lead Width	b1	.026	–	.032
Lower Lead Width	b	.013	–	.021

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

Microchip Technology Drawing C04-048B

NOTES:

APPENDIX A: REVISION HISTORY

Revision D (February 2008)

The following is the list of modifications.

1. Updated **Section 11.0 "Packaging Information"**.
2.
3. Added Appendix A.
4. Updated the Product Identification System page.

Revision C (April 2006)

The following is the list of modifications:

- Undocumented Changes.

Revision B (May 2002)

The following is the list of modifications:

- Undocumented Changes.

Revision A (April 2002)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XXX
Device	Temperature Range	Package	Tape & Reel

Device:	TC7106: 3-3/4 Digit A/D, with Frequency Counter and Probe TC7106A: 3-3/4 Digit A/D, with Frequency Counter and Probe TC7106: 3-3/4 Digit A/D, with Frequency Counter and Probe TC7107A: 3-3/4 Digit A/D, with Frequency Counter and Probe	
Temperature Range:	C I	= 0°C to +70°C = -25°C to +85°C
Package:	LW PL KW	= Plastic Leaded Chip Carrier (PLCC), 44-lead = Plastic DIP, (600 mil Body), 40-lead = Plastic Metric Quad Flatpack, (MQFP), 44-lead
Tape & Reel:	713	= Tape and Reel

Examples:

a)	TC7106CLW:	3-3/4 A/D Converter, 44LD PLCC package.
b)	TC7106CPL:	3-3/4 A/D Converter, 40LD PDIP package.
c)	TC7106CKW713:	3-3/4 A/D Converter, 44LD MQFP package, Tape and Reel.
a)	TC7106ACLW:	3-3/4 A/D Converter, 44LD PLCC package.
b)	TC7106ACPL:	3-3/4 A/D Converter, 40LD PDIP package.
c)	TC7106ACKW713:	3-3/4 A/D Converter, 44LD MQFP package, Tape and Reel
a)	TC7107CLW:	3-3/4 A/D Converter, 44LD PLCC package.
b)	TC7107CLP:	3-3/4 A/D Converter, 40LD PDIP package.
c)	TC7107CKW713:	3-3/4 A/D Converter, 44LD MQFP package Tape and Reel.
a)	TC7107ACLW:	3-3/4 A/D Converter, 44LD PLCC package.
b)	TC7107ACLP:	3-3/4 A/D Converter, 40LD PDIP package.
c)	TC7107ACKW:	3-3/4 A/D Converter, 44LD MQFP package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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