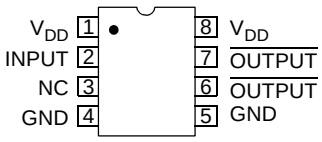
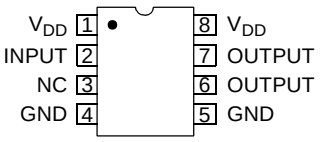
Package Types

8-Pin PDIP/SOIC[1, 2]

TC4451

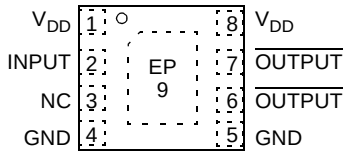


TC4452

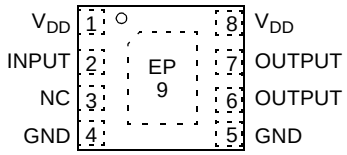


8-Pin DFN-S[1, 2]

TC4451

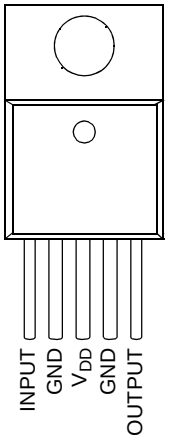


TC4452



5-Pin TO-220[1, 2]

TC4451
TC4452

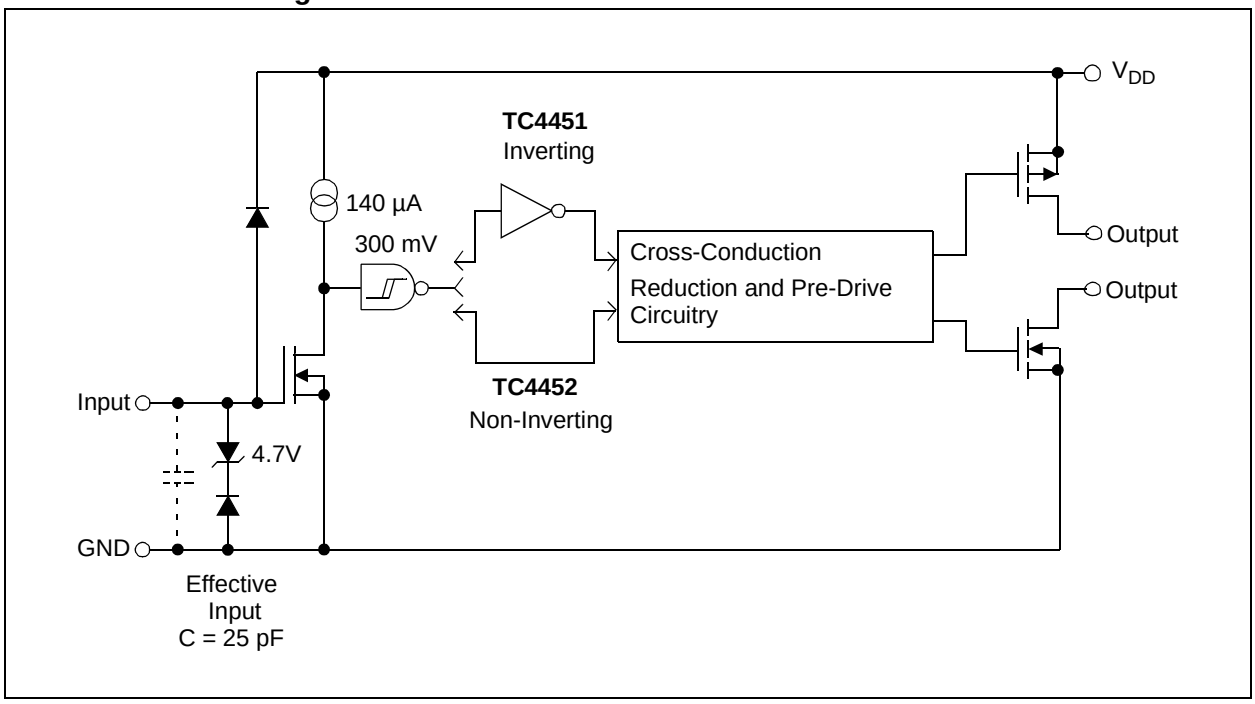


Tab is Common to V_{DD}

Note 1: Duplicate pins must both be connected for proper operation.

2: Exposed thermal pad (EP) of the DFN-S package is electrically isolated; see Table 3-1.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage .....+20V
Input Voltage .....(V_{DD} + 0.3V) to (GND – 5V)
Input Current (V_{IN} > V_{DD}).....50 mA

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Logic ‘1’, High Input Voltage	V_{IH}	2.4	1.5	—	V	
Logic ‘0’, Low Input Voltage	V_{IL}	—	1.3	0.8	V	
Input Current	I_{IN}	-10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Input Voltage	V_{IN}	-5	—	V_{DD} + 0.3	V	
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	1.0	1.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	0.9	1.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	13	—	A	V_{DD} = 18V
Continuous Output Current	I_{DC}	2.6	—	—	A	10V ≤ V_{DD} ≤ 18V **(Note 2, Note 3)**
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	>1.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µs
Switching Time (Note 1)						
Rise Time	t_R	—	30	40	ns	**Figure 4-1**, C_L = 15,000 pF
Fall Time	t_F	—	32	40	ns	**Figure 4-1**, C_L = 15,000 pF
Propagation Delay Time	t_{D1}	—	44	52	ns	**Figure 4-1**, C_L = 15,000 pF
Propagation Delay Time	t_{D2}	—	44	52	ns	**Figure 4-1**, C_L = 15,000 pF
Power Supply						
Power Supply Current	I_S	—	140	200	µA	V_{IN} = 3V
		—	40	100	µA	V_{IN} = 0V
Operating Input Voltage	V_{DD}	4.5	—	18.0	V	
V_{DD} Ramp Rate	SV_{DD}	0.2	—	—	V/ms	

Note 1: Switching times ensured by design.
2: Tested during characterization, not production tested.
3: Valid for AT and MF packages only. T_A = +25°C.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

Electrical Specifications: Unless otherwise noted, over the operating temperature range with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	—	2.2	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	—	2.0	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	—	35	60	ns	**Figure 4-1**, C_L = 15,000 pF
Fall Time	t_F	—	38	60	ns	**Figure 4-1**, C_L = 15,000 pF
Propagation Delay Time	t_{D1}	—	55	65	ns	**Figure 4-1**, C_L = 15,000 pF
Propagation Delay Time	t_{D2}	—	55	65	ns	**Figure 4-1**, C_L = 15,000 pF
Power Supply						
Power Supply Current	I_S	—	200	400	µA	V_{IN} = 3V
		—	50	150	µA	V_{IN} = 0V
Operating Input Voltage	V_{DD}	4.5	—	18.0	V	
V_{DD} Ramp Rate	SV_{DD}	0.2	—	—	V/ms	

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range (V)	T_A	-40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 5L-TO-220	θ_{JA}	—	39.5	—	°C/W	Without heat sink
Thermal Resistance, 8L-6x5 DFN-S	θ_{JA}	—	35.7	—	°C/W	Typical four-layer board with vias to ground plane
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

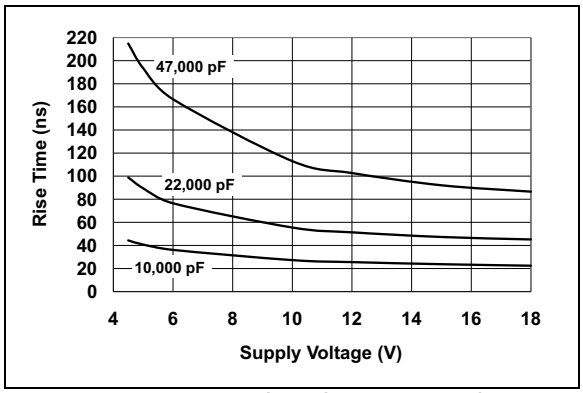


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

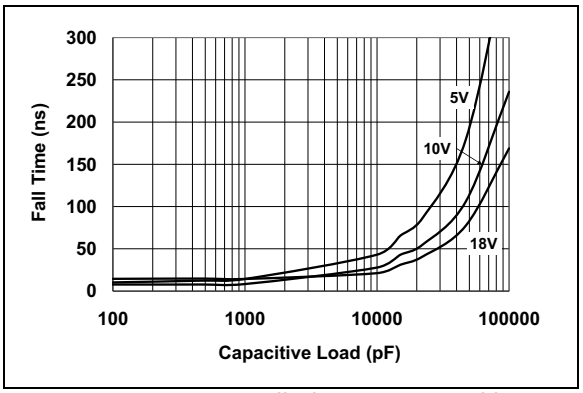


FIGURE 2-4: *Fall Time vs. Capacitive Load.*

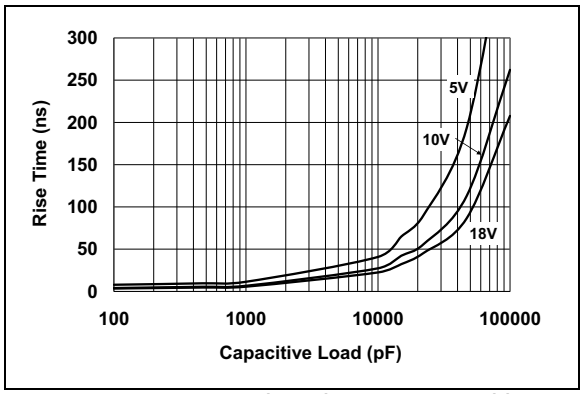


FIGURE 2-2: *Rise Time vs. Capacitive Load.*

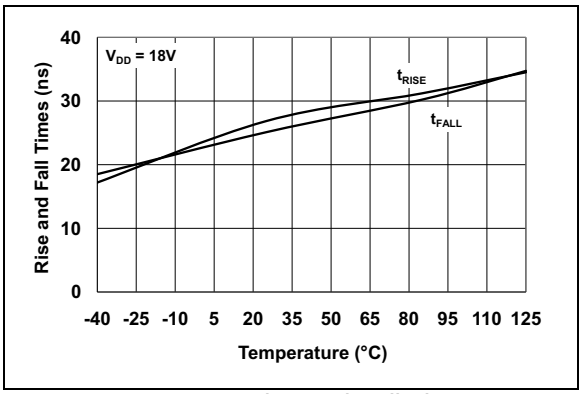


FIGURE 2-5: *Rise and Fall Times vs. Temperature.*

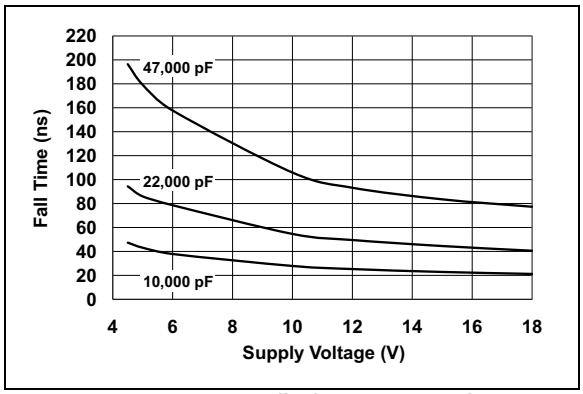


FIGURE 2-3: *Fall Time vs. Supply Voltage.*

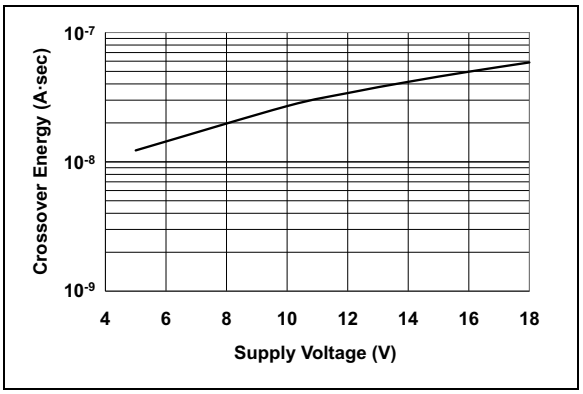


FIGURE 2-6: *Crossover Energy vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

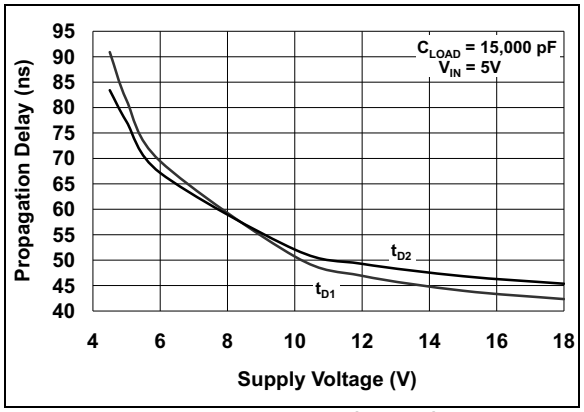


FIGURE 2-7: *Propagation Delay vs. Supply Voltage.*

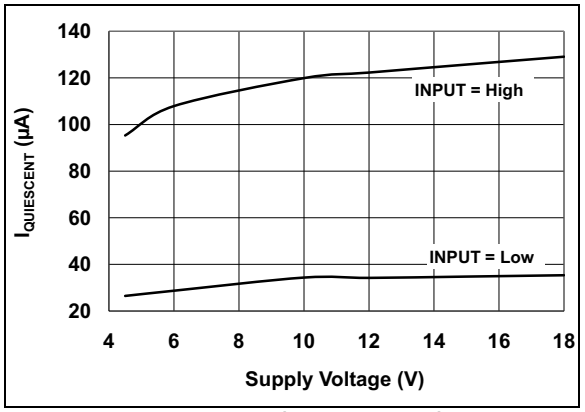


FIGURE 2-10: *Quiescent Supply Current vs. Supply Voltage.*

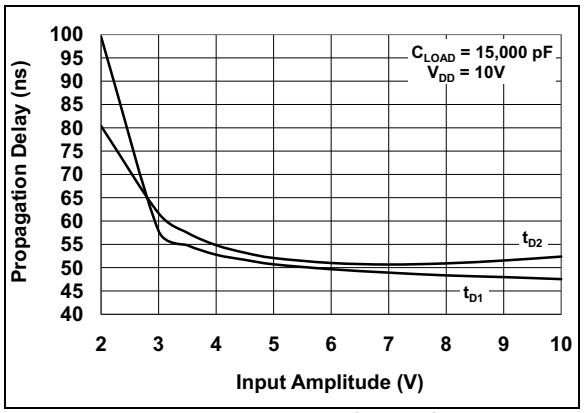


FIGURE 2-8: *Propagation Delay vs. Input Amplitude.*

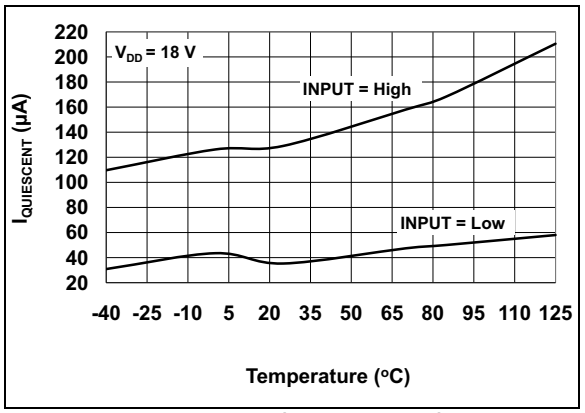


FIGURE 2-11: *Quiescent Supply Current vs. Temperature.*

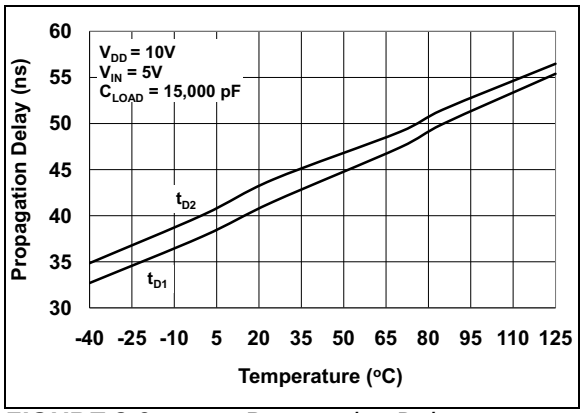


FIGURE 2-9: *Propagation Delay vs. Temperature.*

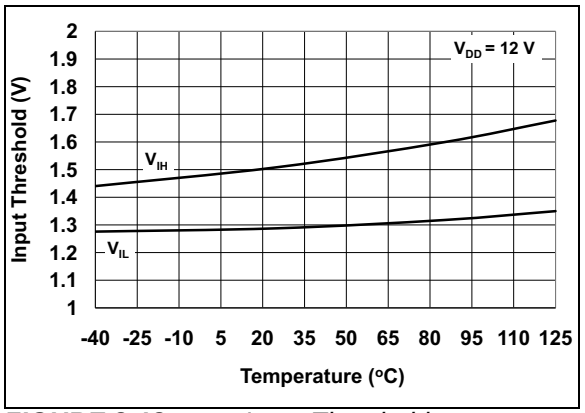


FIGURE 2-12: *Input Threshold vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

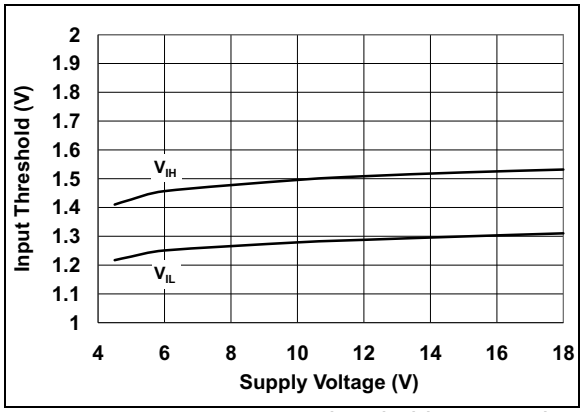


FIGURE 2-13: *Input Threshold vs. Supply Voltage.*

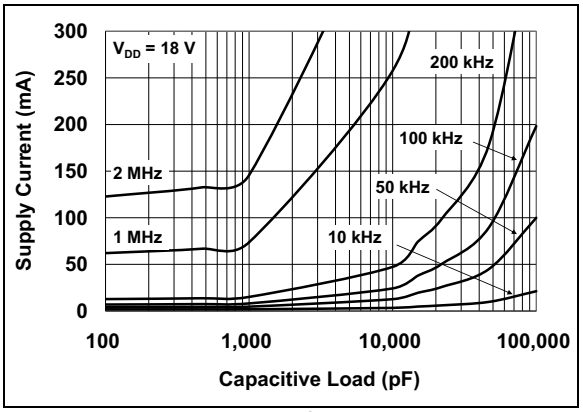


FIGURE 2-16: *Supply Current vs. Capacitive Load (V_{DD} = 18V).*

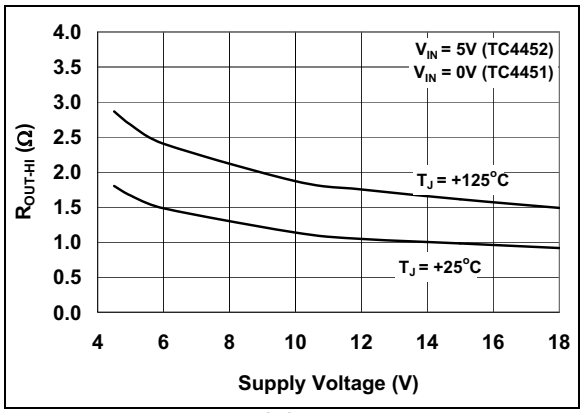


FIGURE 2-14: *High State Output Resistance vs. Supply Voltage.*

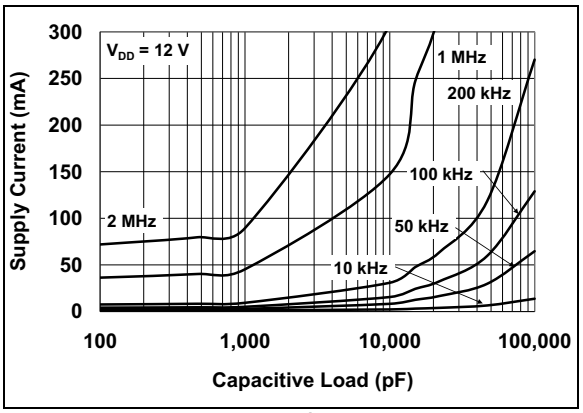


FIGURE 2-17: *Supply Current vs. Capacitive Load (V_{DD} = 12V).*

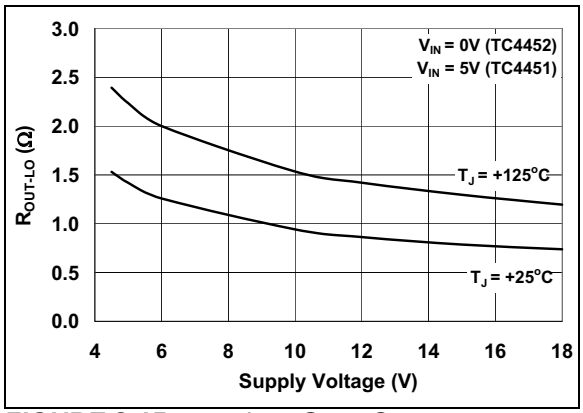


FIGURE 2-15: *Low State Output Resistance vs. Supply Voltage.*

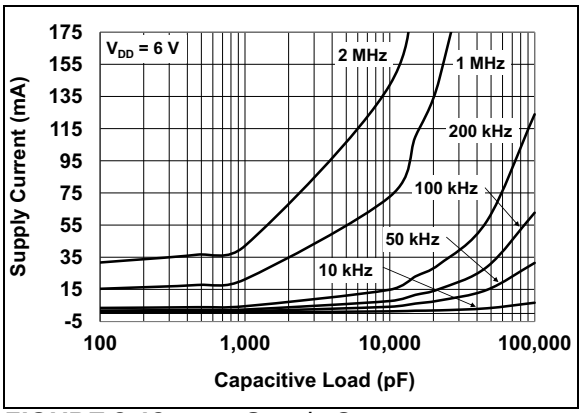


FIGURE 2-18: *Supply Current vs. Capacitive Load (V_{DD} = 6V).*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

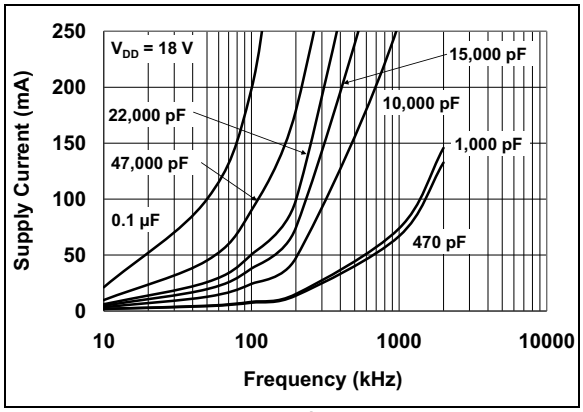


FIGURE 2-19: *Supply Current vs. Frequency (V_{DD} = 18V).*

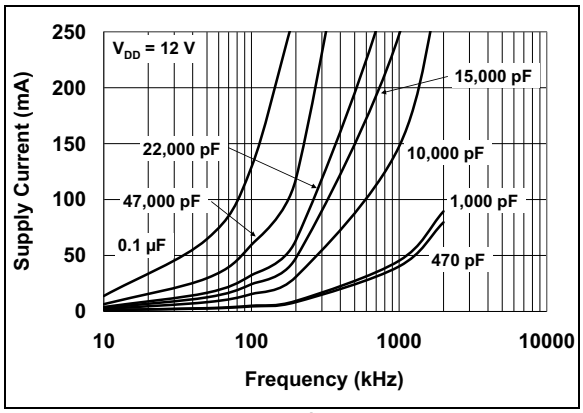


FIGURE 2-20: *Supply Current vs. Frequency (V_{DD} = 12V).*

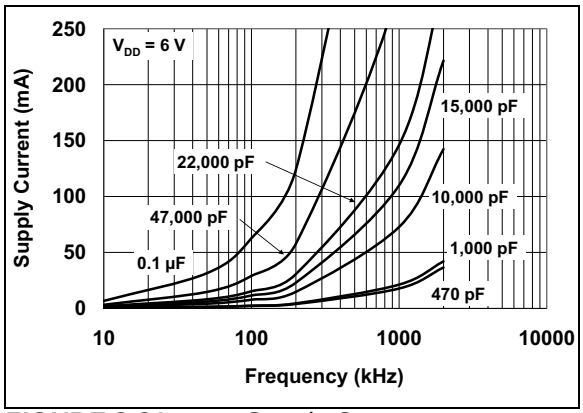


FIGURE 2-21: *Supply Current vs. Frequency (V_{DD} = 6V).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

8-Pin PDIP, SOIC	8-Pin DFN-S	5-Pin TO-220	Symbol	Description
1	1	—	V_{DD}	Supply input, 4.5V to 18V
2	2	1	INPUT	Control input, TTL/CMOS-compatible input
3	3	—	NC	No connection
4	4	2	GND	Ground
5	5	4	GND	Ground
6	6	5	OUTPUT/$\overline{\text{OUTPUT}}$	CMOS push-pull output
7	7	—	OUTPUT/$\overline{\text{OUTPUT}}$	CMOS push-pull output
8	8	3	V_{DD}	Supply input, 4.5V to 18V
—	9	—	EP	Exposed thermal pad
—	—	TAB	V_{DD}	Thermal tab is at the V_{DD} potential

3.1 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 18V with respect to the ground pin. The V_{DD} input should be bypassed to ground with a local ceramic capacitor. The value of the capacitor should be chosen based on the capacitive load that is being driven. A minimum value of 1.0 µF is suggested.

3.2 Control Input (INPUT)

The MOSFET driver input is a high-impedance, TTL/CMOS-compatible input. The input also has 300 mV of hysteresis between the high and low thresholds that prevents output glitching even when the rise and fall time of the input signal is very slow.

3.3 CMOS Push-Pull Output (OUTPUT, $\overline{\text{OUTPUT}}$)

The MOSFET driver output is a low-impedance, CMOS, push-pull style output capable of driving a capacitive load with 12A peak currents. The MOSFET driver output is capable of withstanding 1.5A peak reverse currents of either polarity.

3.4 Ground (GND)

The ground pins are the return path for the bias current and for the high peak currents that discharge the load capacitor. The ground pins should be tied into a ground plane or have very short traces to the bias supply source return.

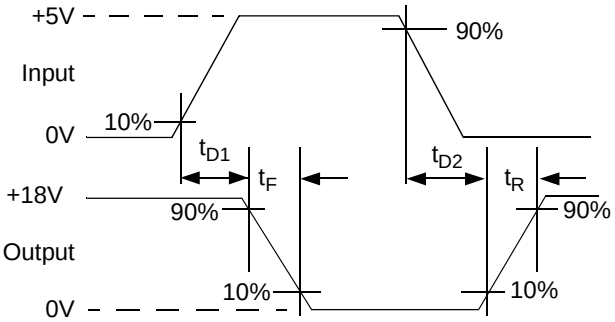
3.5 Exposed Thermal Pad (EP)

The exposed thermal pad of the 6x5 DFN-S package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board (PCB) to help remove heat from the package.

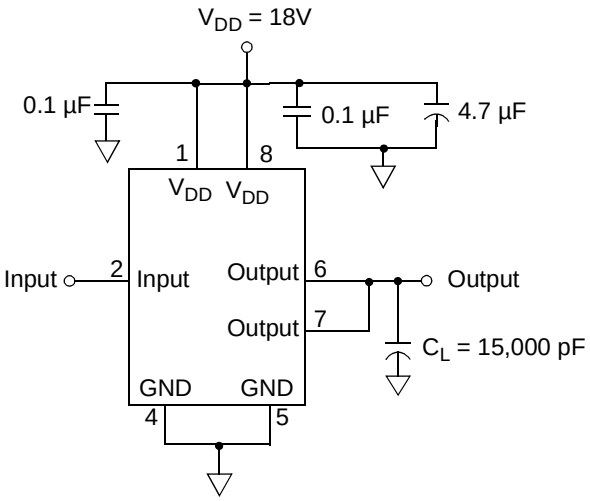
3.6 Thermal Tab

The thermal tab of the TO-220 package is connected to the V_{DD} potential of the device and this connection is used as a current-carrying path.

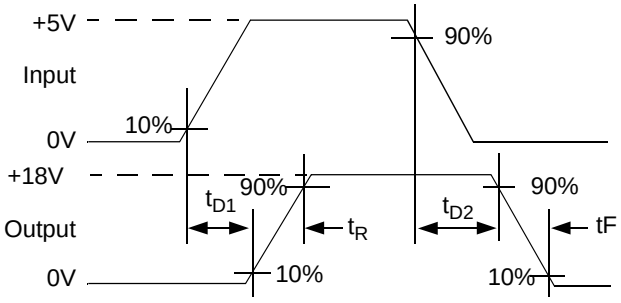
4.0 APPLICATIONS INFORMATION



Inverting Driver
TC4451



Input: 100 kHz, square wave
$t_{RISE} = t_{FALL} \leq 10$ ns



Non-Inverting Driver
TC4452

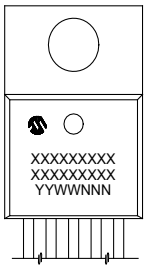
Note: Pinout shown is for the DFN-S, PDIP and SOIC packages.

FIGURE 4-1: *Switching Time Test Circuits.*

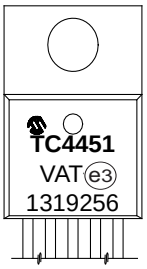
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

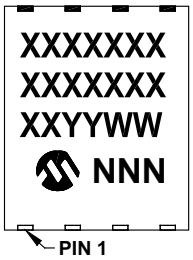
5-Lead TO-220



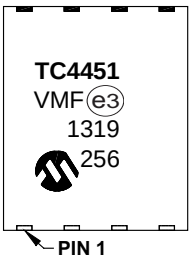
Example



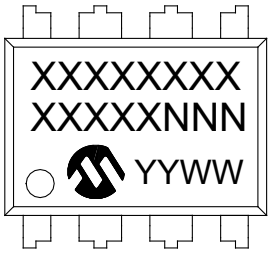
8-Lead DFN-S (6x5x0.9 mm)



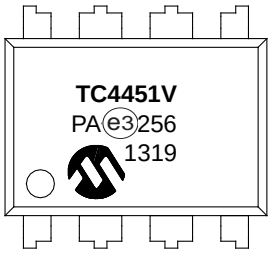
Example



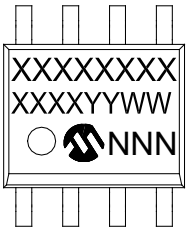
8-Lead PDIP (300 mil)



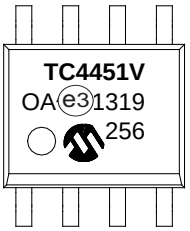
Example



8-Lead SOIC (3.90 mm)



Example

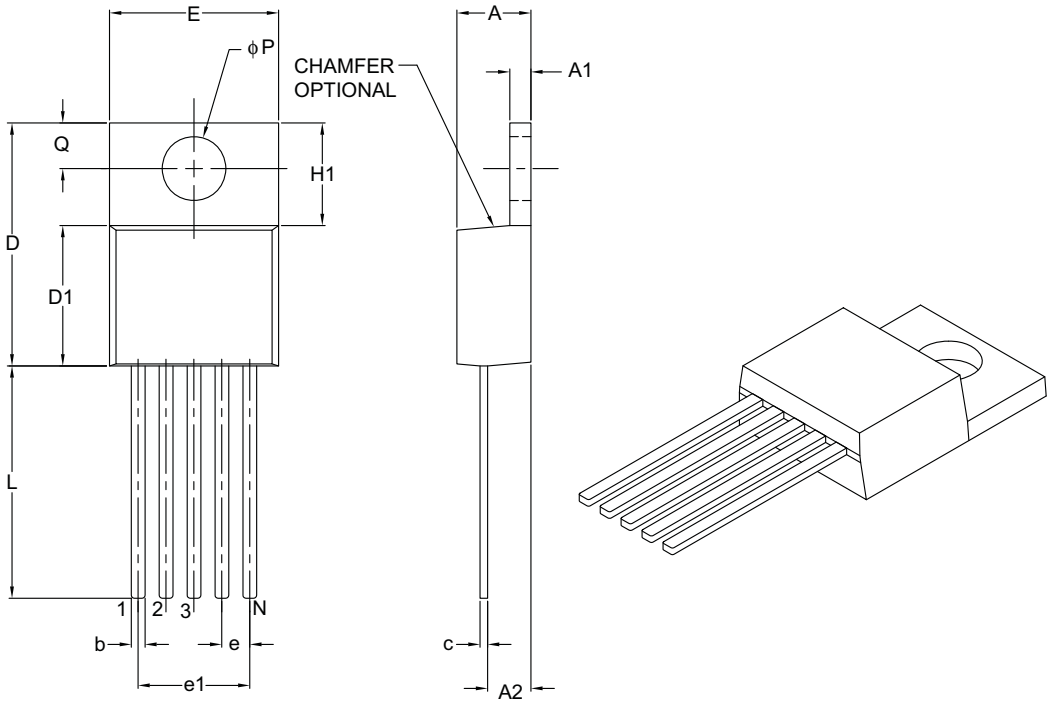


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Transistor Outline (AT) [TO-220]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		.067 BSC	
Overall Pin Pitch	e1		.268 BSC	
Overall Height	A	.140	–	.190
Overall Width	E	.380	–	.420
Overall Length	D	.560	–	.650
Molded Package Length	D1	.330	–	.355
Tab Length	H1	.204	–	.293
Tab Thickness	A1	.020	–	.055
Mounting Hole Center	Q	.100	–	.120
Mounting Hole Diameter	ϕP	.139	–	.156
Lead Length	L	.482	–	.590
Base to Bottom of Lead	A2	.080	–	.115
Lead Thickness	c	.012	–	.025
Lead Width	b	.015	.027	.040

Notes:

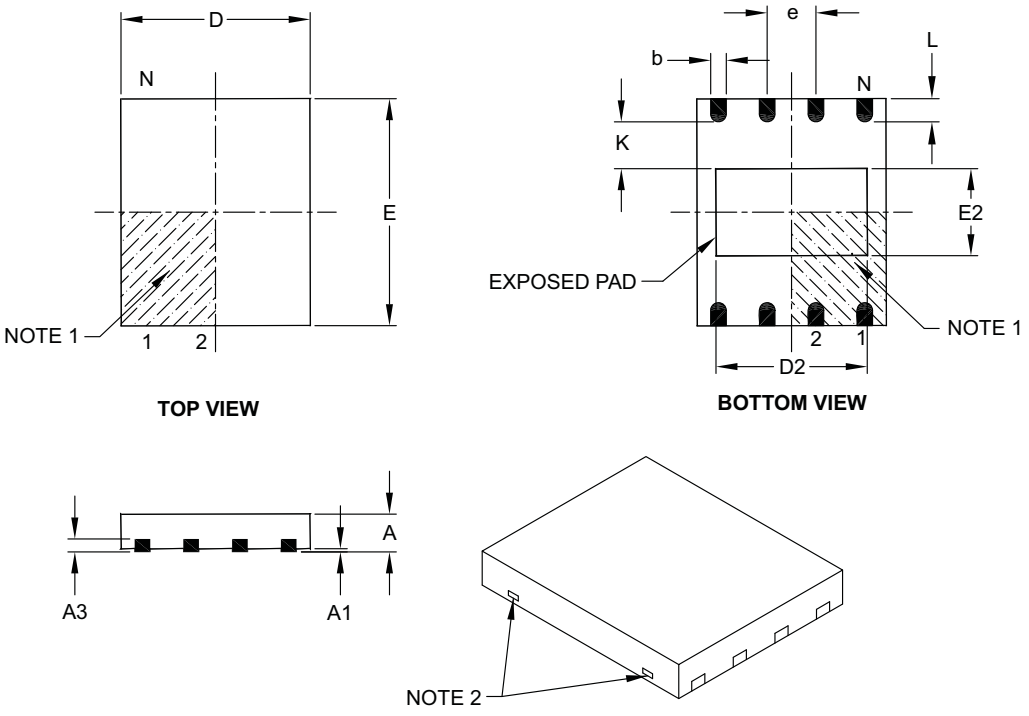
1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-036B

8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.01	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Overall Width	E		6.00 BSC	
Exposed Pad Length	D2	3.90	4.00	4.10
Exposed Pad Width	E2	2.20	2.30	2.40
Contact Width	b	0.35	0.40	0.48
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

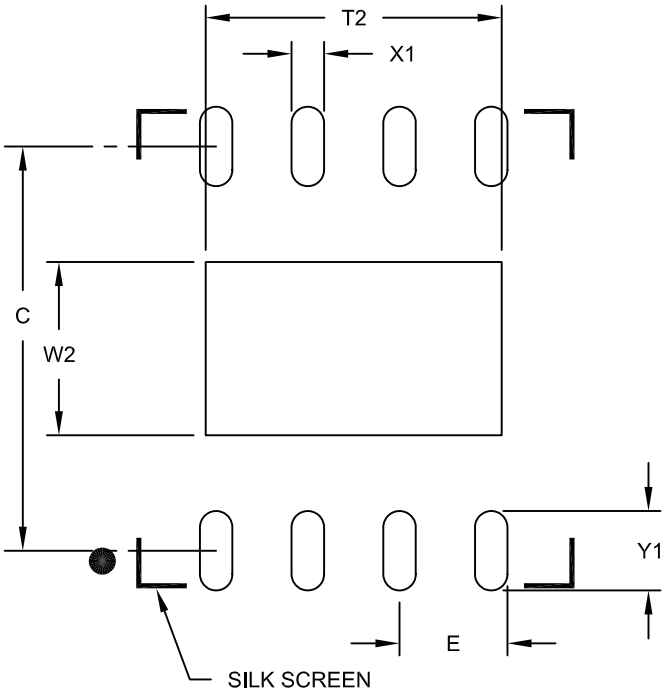
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

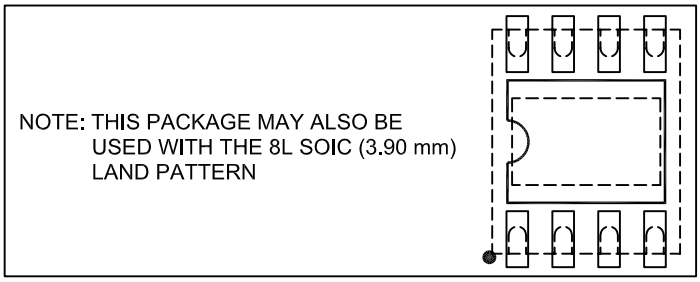
Microchip Technology Drawing C04-122B

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			4.10
Contact Pad Spacing	C		5.60	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.10

Notes:

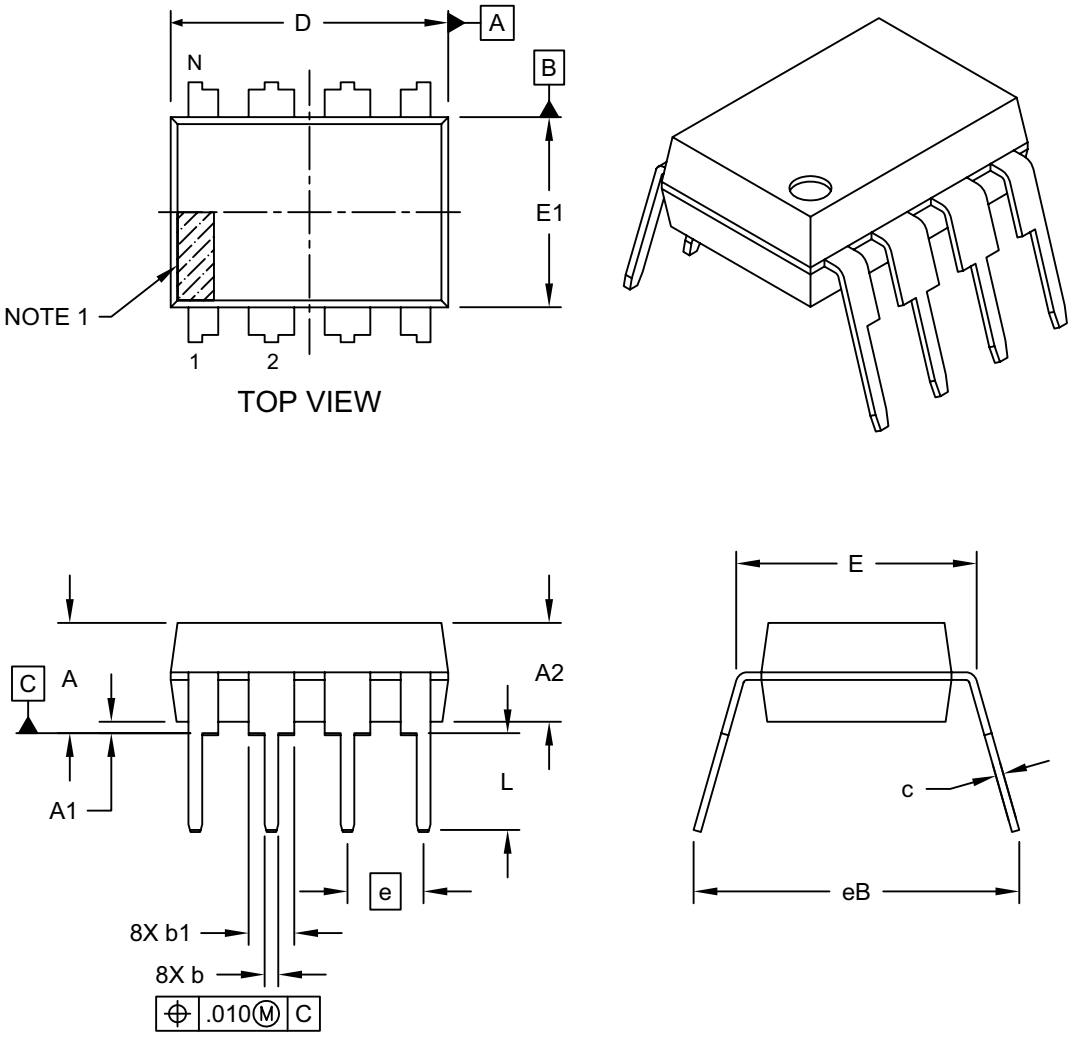
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2122A

8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

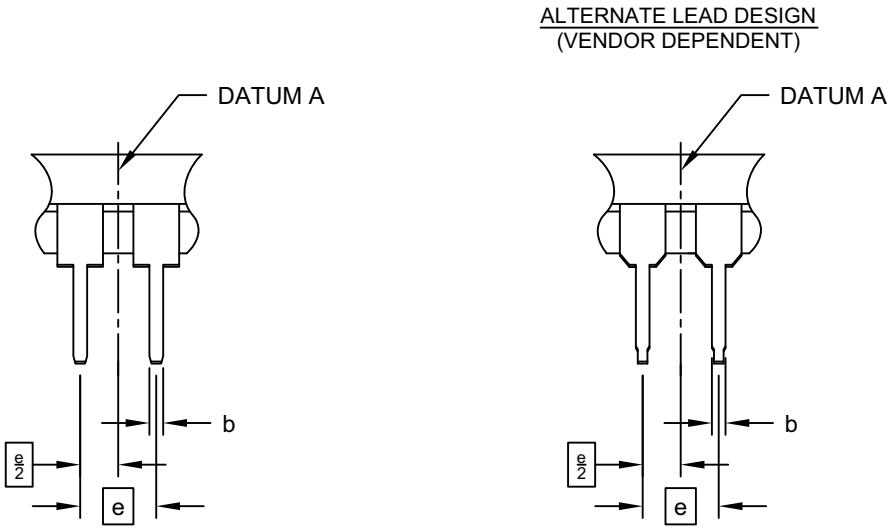
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-018D Sheet 1 of 2

8-Lead Plastic Dual In-Line (PA) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

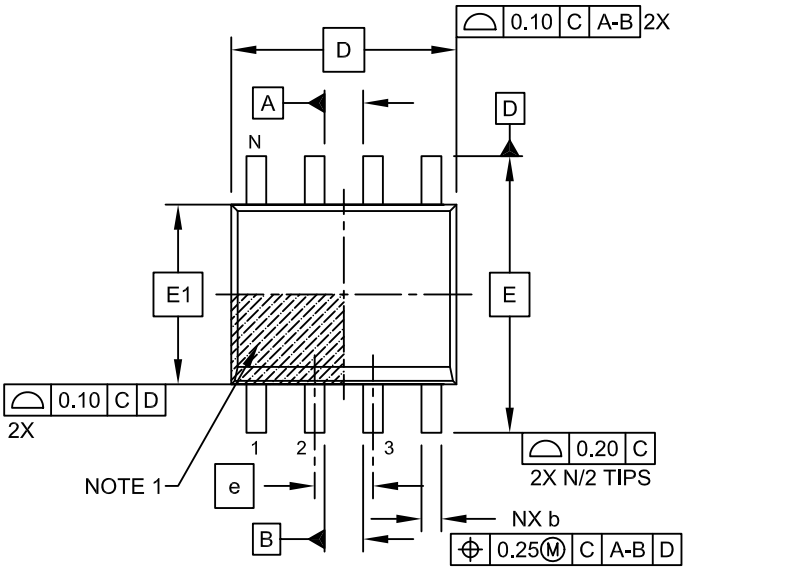
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

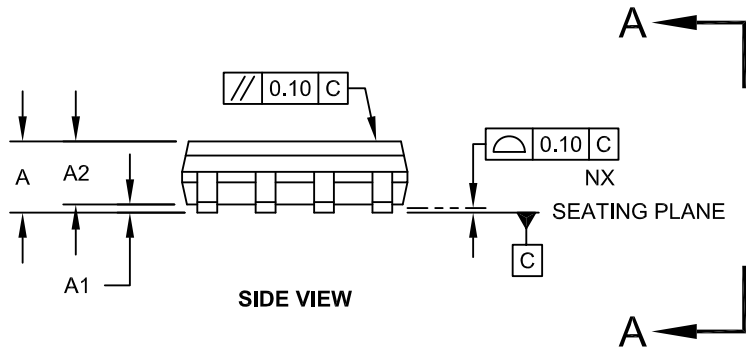
Microchip Technology Drawing No. C04-018D Sheet 2 of 2

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

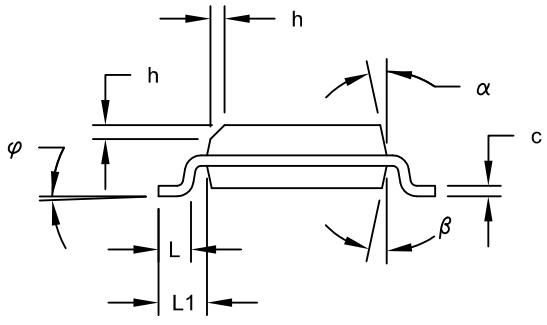
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

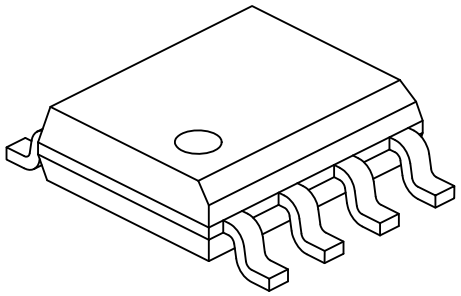


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (OA) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

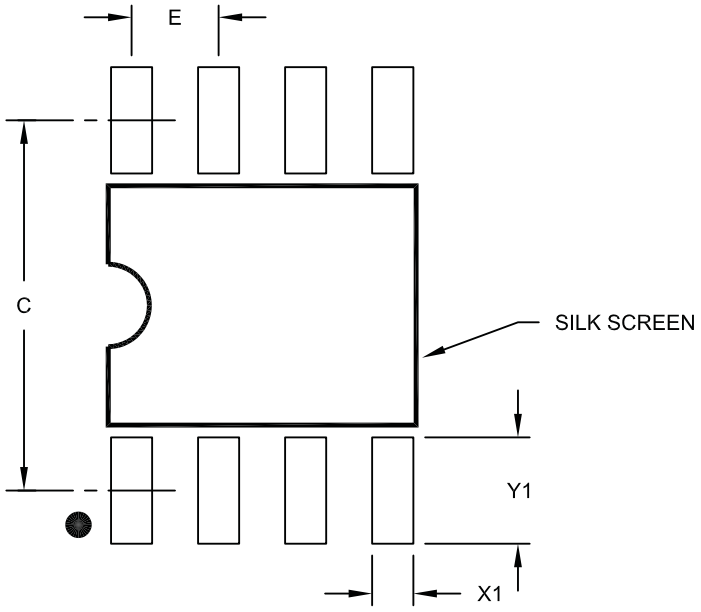
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (OA) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

APPENDIX A: REVISION HISTORY

Revision C (July 2014)

The following is the list of modifications:

1. Added value for Electrostatic Discharge (ESD) protection – Machine Model (MM) in General Description: column.
2. Updated package marking information and drawings in **Section 5.0, Packaging Information**.
3. Minor grammatical and spelling corrections.

Revision B (March 2012)

The following is the list of modifications:

1. Added V_{DD} Ramp Rate value in both DC Characteristics and DC Characteristics (Over Operating Temperature Range) tables.
2. Updated package thermal resistances values in Temperature Characteristics table.
3. Updated package specification drawings in **Section 5.0, Packaging Information** to show all available drawings.

Revision A (February 2006)

- Original release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XXX
Device	Temperature Range	Package	Tape & Reel

Device:	TC4451:	12A High-Speed MOSFET Driver, Inverting
	TC4452:	12A High-Speed MOSFET Driver, Non-Inverting
Temperature Range:	V =	-40°C to +125°C
Package: *	AT =	TO-220, 5-lead
	MF =	Dual, Flat, No-Lead (6x5 mm Body), 8-lead
	MF713 =	Dual, Flat, No-Lead (6x5 mm Body), 8-lead (Tape and Reel)
	PA =	Plastic DIP (300 mil Body), 8-lead
	OA =	Plastic SOIC (150 mil Body), 8-lead
	OA713 =	Plastic SOIC (150 mil Body), 8-lead (Tape and Reel)

*All package offerings are Pb Free (Lead Free).

Examples:

a) TC4451VAT: 12A High-Speed Inverting MOSFET Driver, TO-220 package

b) TC4451VOA: 12A High-Speed Inverting MOSFET Driver, SOIC package

c) TC4451VMF: 12A High-Speed Inverting MOSFET Driver, DFN-S package

a) TC4452VPA: 12A High-Speed Non-Inverting MOSFET Driver, PDIP package

b) TC4452VOA: 12A High-Speed Non-Inverting MOSFET Driver, SOIC package

c) TC4452VMF: 12A High-Speed Non-Inverting MOSFET Driver, DFN-S package

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