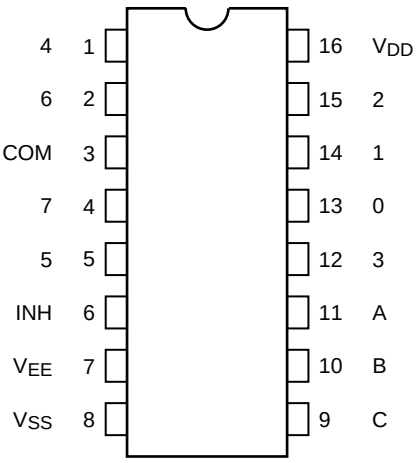
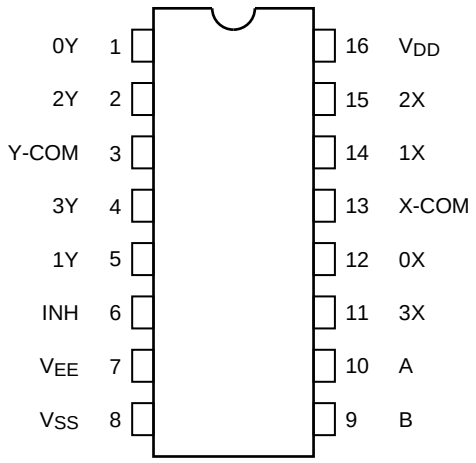
Pin Assignment (top view)

TC4051B



TC4052B



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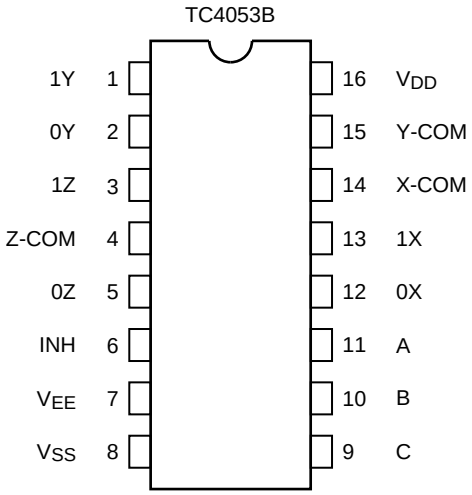


Truth Table

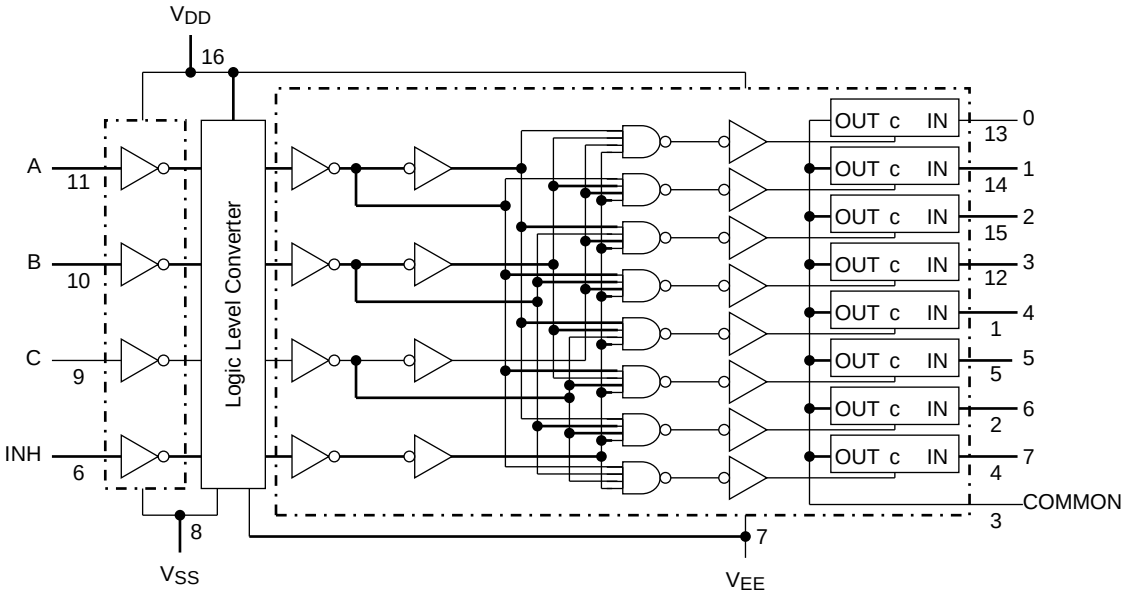
Control Inputs				"ON" Channel		
Inhibit	CΔ	B	A	TC4051B	TC4052B	TC4053B
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z
L	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	L	L	4	—	0X, 0Y, 1Z
L	H	L	H	5	—	1X, 0Y, 1Z
L	H	H	L	6	—	0X, 1Y, 1Z
L	H	H	H	7	—	1X, 1Y, 1Z
H	X	X	X	None	None	None

X: Don't care

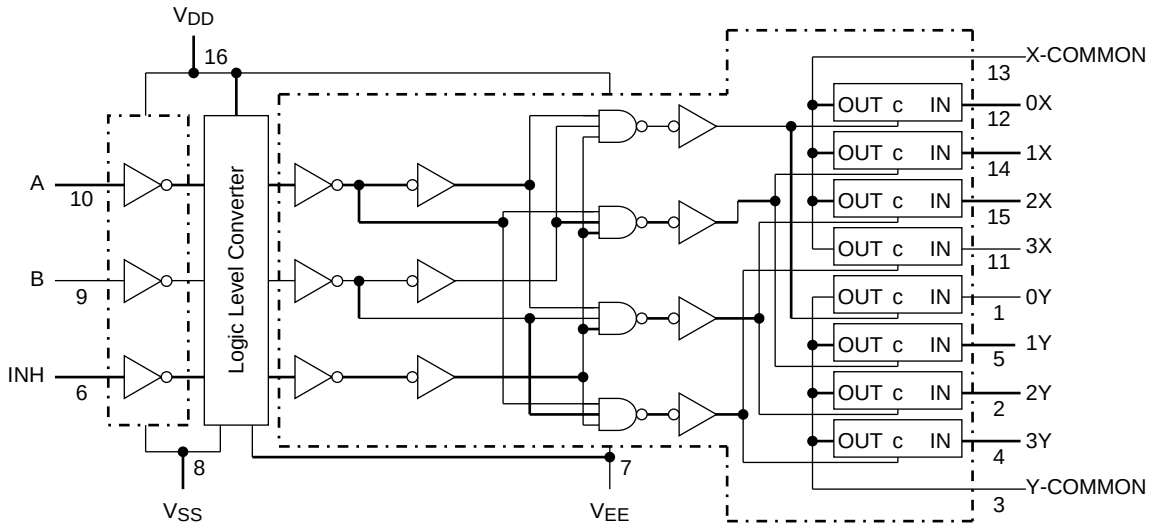
Δ: Except TC4052B

Logic Diagram

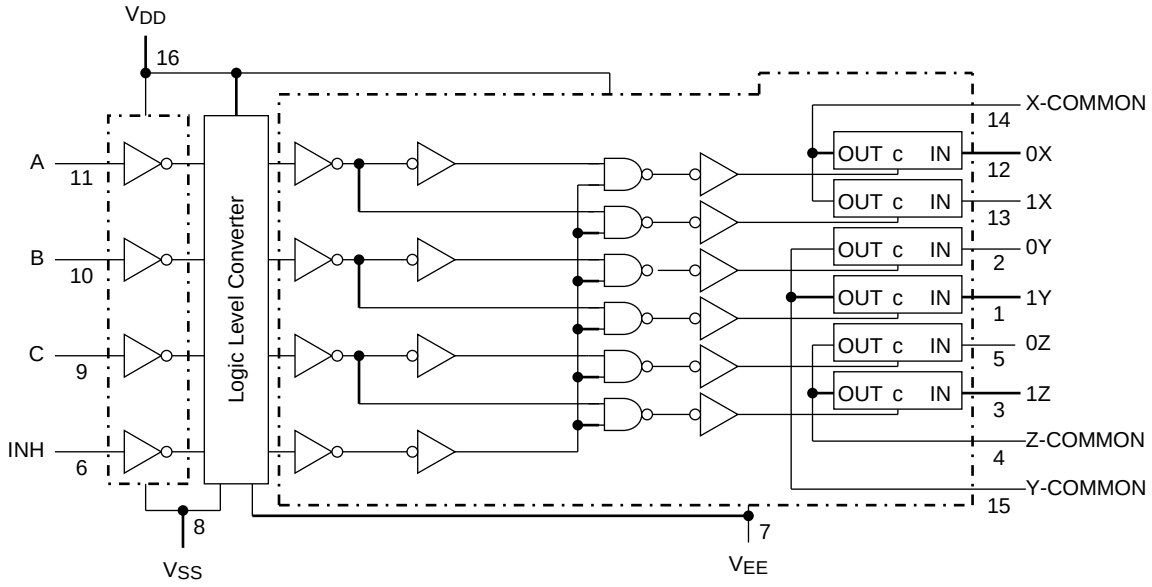
TC4051B



TC4052B



TC4053B



Truth Table

Control C	Impedance between IN-OUT (Note)
H	0.5 to 5 × 10^2 Ω
L	>10^9 Ω

Note: See electrical characteristics

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V_{DD}-V_{SS}	−0.5 to 20	V
DC supply voltage	V_{DD}-V_{EE}	−0.5 to 20	V
Control input voltage	V_{CIN}	V_{SS} − 0.5 to V_{DD} + 0.5	V
Switch I/O voltage	V_I/V_O	V_{EE} − 0.5 to V_{DD} + 0.5	V
Control input current	I_{CIN}	±10	mA
Potential difference across I/O during ON	V_I-V_O	−0.5 to 0.5	V
Power dissipation	P_D	300 (DIP)/180 (SOP/TSSOP)	mW
Operating temperature range	T_{opr}	−40 to 85	°C
Storage temperature range	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
DC supply voltage	V_{DD}-V_{SS}	—	3	—	18	V
	V_{DD}-V_{EE}	—	3	—	18	
Control input voltage	V_{IN}	—	V_{SS}	—	V_{DD}	V
Input/output voltage	V_{IN}/V_{OUT}	—	V_{EE}	—	V_{DD}	V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused Control inputs must be tied to either V_{DD} or V_{SS}.

Static Electrical Characteristics

Characteristics	Symbol	Test Condition	V_{SS} (V)	V_{EE} (V)	V_{DD} (V)	−40°C Min	−40°C Max	25°C Min	25°C Typ.	25°C Max	85°C Min	85°C Max	Unit
Control input high voltage	V_{IH}	V_{IS} = V_{DD} thru 1 kΩ; V_{EE} = V_{SS}; R_L = 1 kΩ to V_{SS}; I_{IS} < 2 μA on all OFF channels			5	3.5	—	3.5	2.75	—	3.5	—	V
					10	7.0	—	7.0	5.50	—	7.0	—	
					15	11.0	—	11.0	8.25	—	11.0	—	
Control input low voltage	V_{IL}				5	—	1.5	—	2.25	1.5	—	1.5	V
					10	—	3.0	—	4.5	3.0	—	3.0	
					15	—	4.0	—	6.75	4.0	—	4.0	
On-state resistance	R_{ON}	$0 \le V_{IS} \le V_{DD}$; R_L = 10 kΩ	0	0	5	—	850	—	240	950	—	1200	Ω
			0	0	10	—	210	—	110	250	—	300	
			0	0	15	—	140	—	80	160	—	200	
ΔOn-state resistance between any 2 switches	$R_{ON}\Delta$	—	0	0	5	—	—	—	10	—	—	—	Ω
			0	0	10	—	—	—	6	—	—	—	
			0	0	15	—	—	—	4	—	—	—	
Input/output leakage current	I_{OFF}	V_{IN} = 18 V, V_{OUT} = 0 V			18	—	±100	—	±0.01	±100	—	±1000	nA
		V_{IN} = 0 V, V_{OUT} = 18 V			18	—	±100	—	±0.01	±100	—	±1000	
Quiescent supply current	I_{DD}	V_{IN} = V_{SS}, V_{DD} (Note)			5	—	5.0	—	0.005	5.0	—	150	μA
					10	—	10	—	0.010	10	—	300	
					15	—	20	—	0.015	20	—	600	
Input current	I_{IN}	V_{IH} = 18 V			18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
		V_{IL} = 0 V			18	—	−0.1	—	-10^{-5}	−0.1	—	−1.0	
Input capacitance	C_{IN}	—			—	—	—	—	5	7.5	—	—	pF
Switch input capacitance	C_{IN}	—			—	—	—	—	10	—	—	—	pF
Output capacitance	C_{OUT}	TC4051B			10	—	—	—	58	—	—	—	pF
		TC4052B			10	—	—	—	30	—	—	—	
		TC4053B			10	—	—	—	17	—	—	—	
Feedthrough capacitance	C_{IN}-C_{OUT}	TC4051B			10	—	—	—	0.2	—	—	—	pF
		TC4052B			10	—	—	—	0.2	—	—	—	
		TC4053B			10	—	—	—	0.2	—	—	—	

Note: All valid input combinations.

Switching Characteristics (Ta = 25°C, C_L = 50 pF)

Characteristics	Symbol	Test Condition	V_{SS} (V)	V_{EE} (V)	V_{DD} (V)	Min	Typ.	Max	Unit
Phase difference between input to output	ϕ_{I-O}	—	0	0	5	—	15	45	ns
			0	0	10	—	8	20	
			0	0	15	—	6	15	
Propagation delay time (A, B, C, -OUT)	t_{pZL} t_{pZH} t_{pLZ} t_{pHZ}	R_L = 1 kΩ	0	0	5	—	170	550	ns
			0	0	10	—	90	240	
			0	0	15	—	70	160	
			0	−5	5	—	100	240	
			0	−7.5	7.5	—	80	160	
Propagation delay time (INH-OUT)	t_{pZL} t_{pZH}	R_L = 1 kΩ	0	0	5	—	120	380	ns
			0	0	10	—	60	200	
			0	0	15	—	50	160	
			0	−5	5	—	80	200	
			0	−7.5	7.5	—	60	160	
Propagation delay time (INH-OUT)	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	0	0	5	—	170	450	ns
			0	0	10	—	90	210	
			0	0	15	—	70	160	
			0	−5	5	—	100	210	
			0	−7.5	7.5	—	80	160	
−3dB cutoff frequency TC4051B	f_{max} (I-O)	R_L = 1 kΩ (Note 1)	−5	−5	5	—	20	—	MHz
TC4052B			−5	−5	5	—	30	—	
TC4053B			−5	−5	5	—	40	—	
Total harmonic distortion	—	R_L = 10 kΩ f = 1 kHz (Note 2)	−2.5	−2.5	2.5	—	0.15	—	%
			−5	−5	5	—	0.03	—	
			−7.5	−7.5	7.5	—	0.02	—	
−50dB feedthrough (switch off)	—	R_L = 1 kΩ (Note 3)	−5	−5	5	—	500	—	kHz
Crosstalk	—	R_L = 1 kΩ (Note 4)	−5	−5	5	—	1.5	—	MHz
Crosstalk (control-OUT)	—	R_{IN} = 1 kΩ R_{OUT} = 10 kΩ C_L = 15 pF	0	0	5	—	200	—	mV
			0	0	10	—	400	—	
			0	0	15	—	600	—	

Note 1: Sine wave of ±2.5 V_{p-p} shall be used for V_{is} and the frequency of 20 log 10 $\frac{V_{OS}}{V_{is}}$ = −3dB shall be f_{max}.

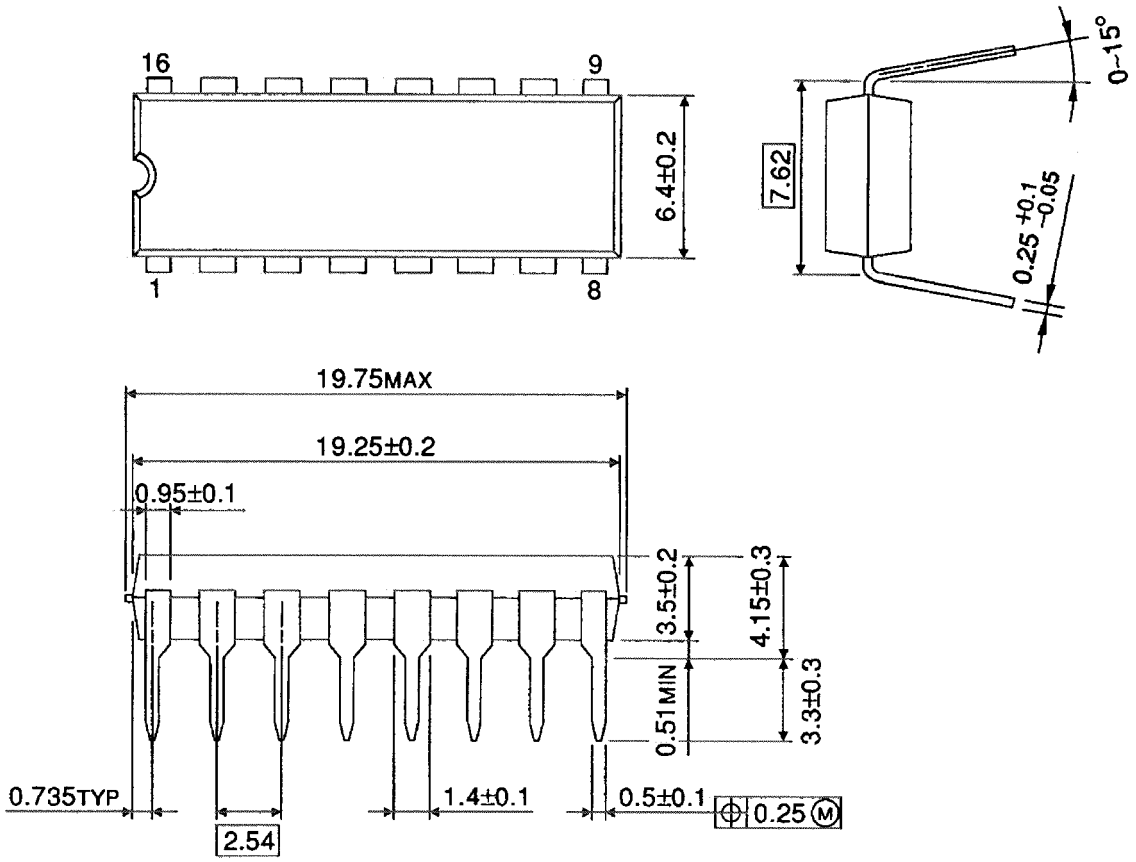
Note 2: V_{is} shall be sine wave of $\pm\left(\frac{V_{DD} - V_{EE}}{4}\right)$ p-p.

Note 3: Sine wave of ±2.5 V_{p-p} shall be used for V_{is} and the frequency of 20 log 10 $\frac{V_{OS}}{V_{is}}$ = −50dB shall be feed-through.

Note 4: Sine wave of ±2.5 V_{p-p} shall be used for V_{is} and the frequency of 20 log 10 $\frac{V_{OS}}{V_{is}}$ = −50dB shall be crosstalk.

Package Dimensions

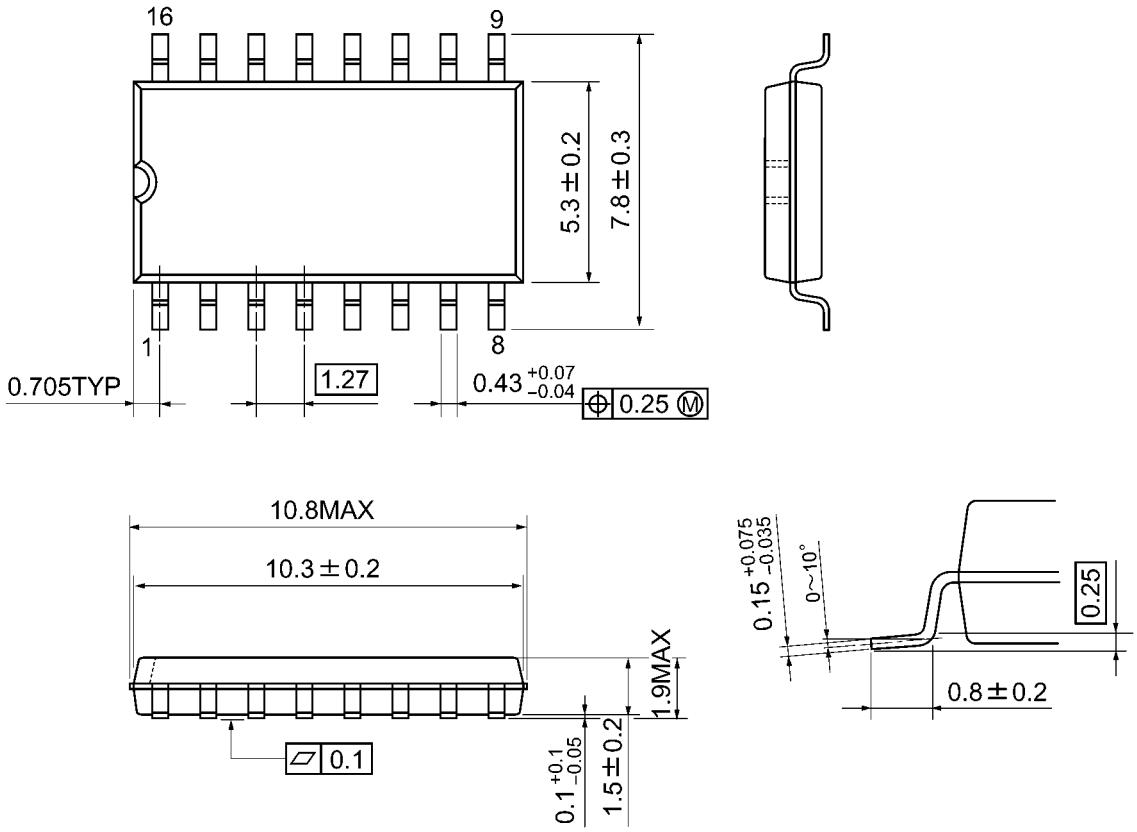
DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions

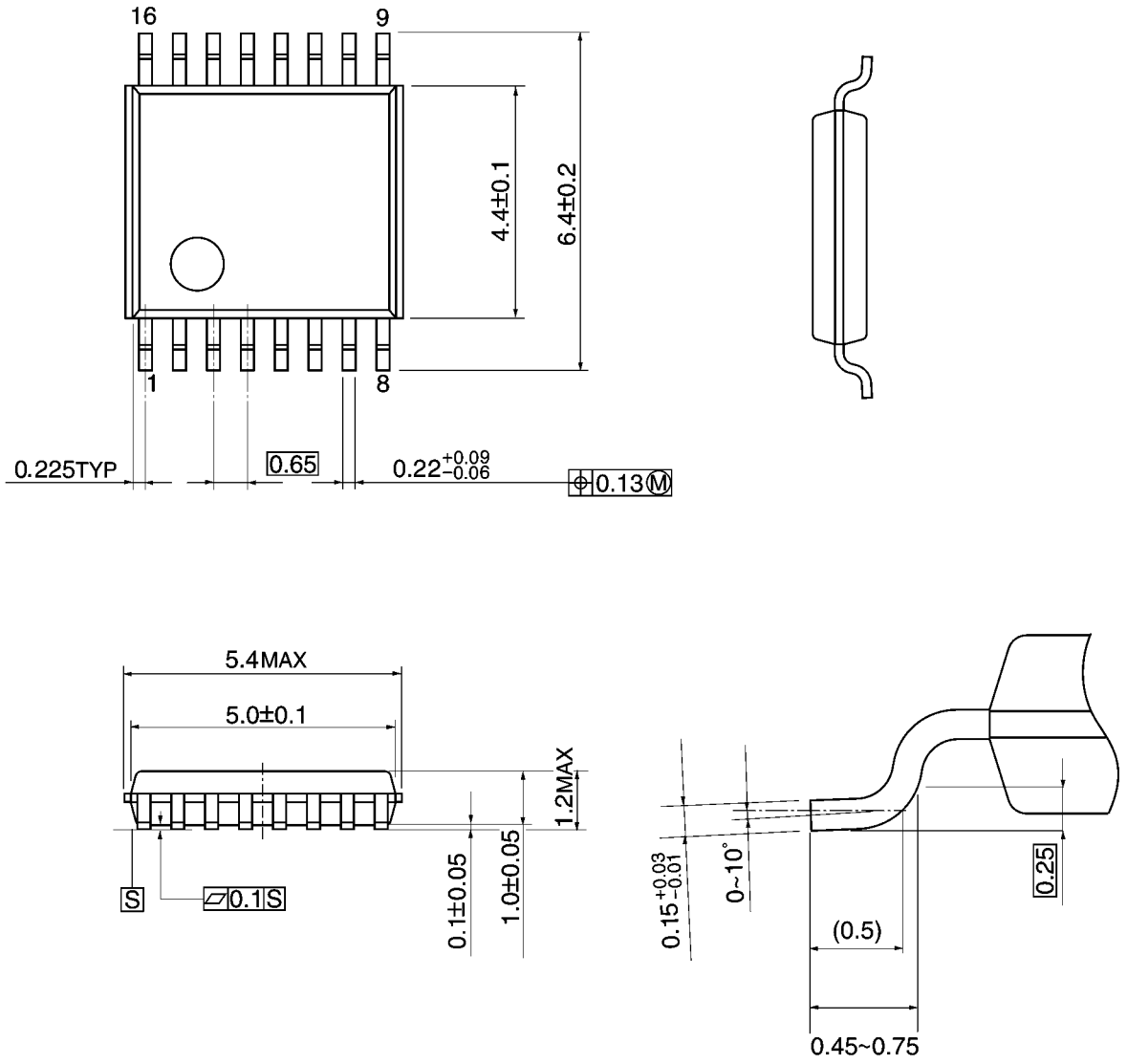
SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

Package Dimensions

TSSOP16-P-0044-0.65A Unit: mm



Weight: 0.06 g (typ.)

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