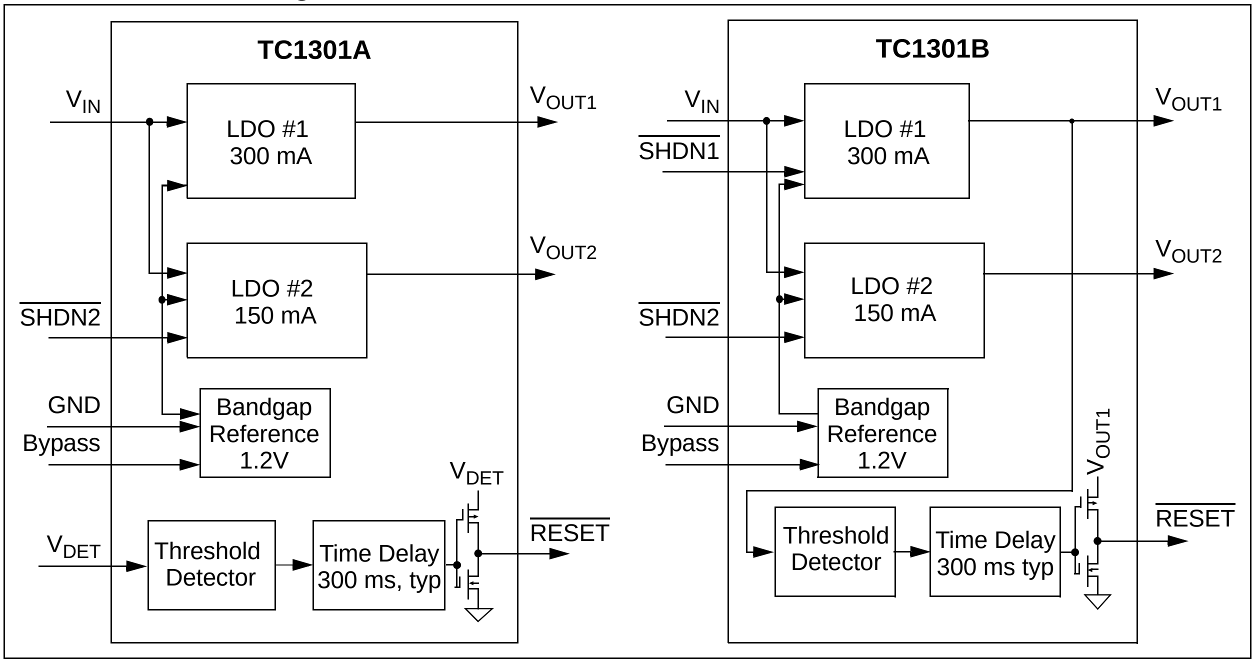
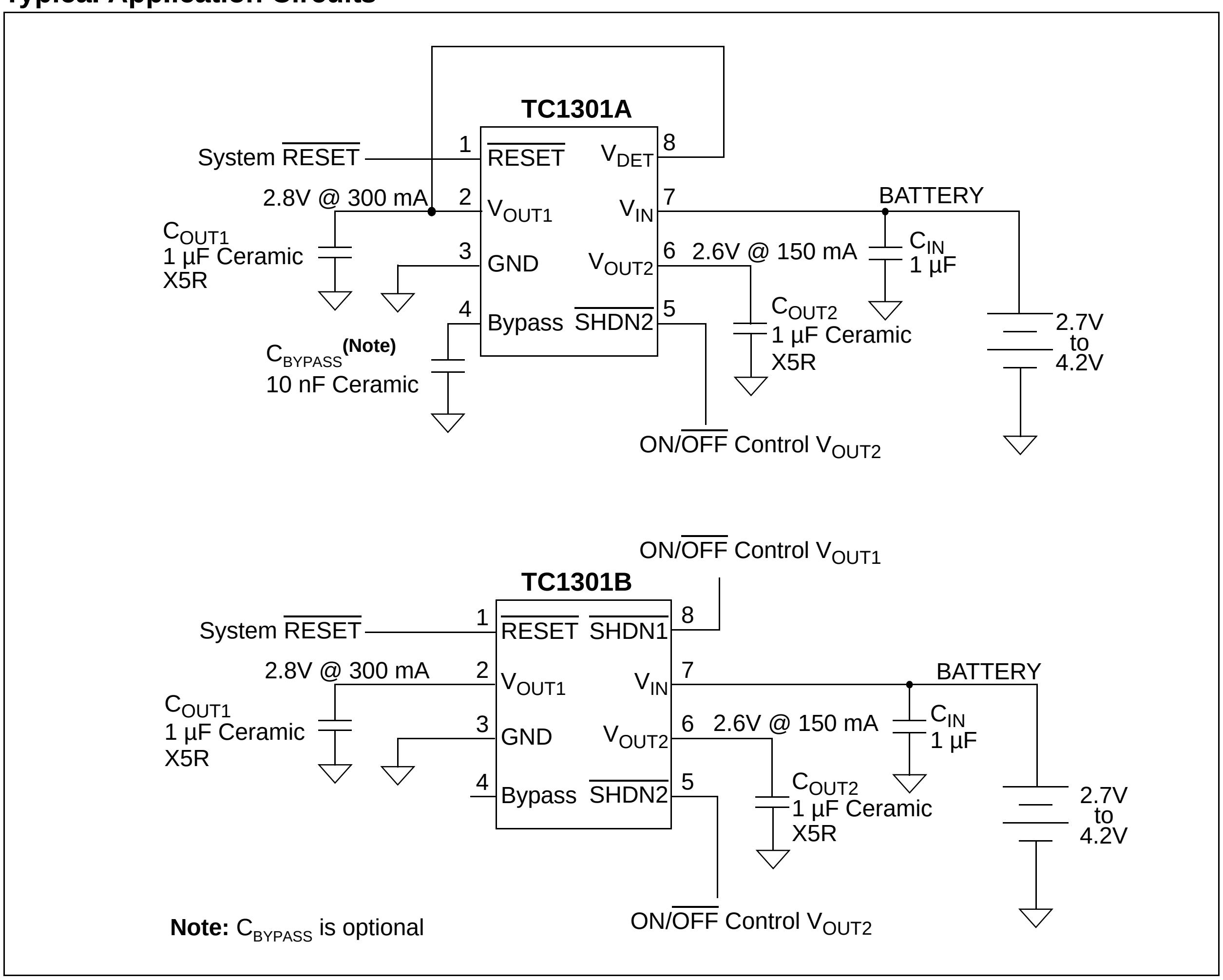
Functional Block Diagrams



Typical Application Circuits



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} 6.5V
Maximum Voltage on Any Pin ...... (V_{SS} – 0.3) to (V_{IN} + 0.3)V
Power Dissipation .... Internally Limited **(Note 7)**
Storage temperature .... -65°C to +150°C
Maximum Junction Temperature, T_J .... +150°C
Continuous Operating Temperature Range .. -40°C to +125°C
ESD protection on all pins, HBM, MM .... 4 kV, 400V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R$ +1V, $I_{OUT1} = I_{OUT2}$ = 100 µA, C_{IN} = 4.7 µF, $C_{OUT1} = C_{OUT2}$ = 1 µF, C_{BYPASS} = 10 nF, $\overline{SHDN} > V_{IH}$, T_A = +25°C.
Boldface type specifications apply for junction temperatures of -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Operating Voltage	V_{IN}	**2.7**	—	**6.0**	V	**Note 1**
Maximum Output Current	$I_{OUT1Max}$	**300**	—	—	mA	V_{IN} = 2.7V to 6.0V **(Note 1)**
Maximum Output Current	$I_{OUT2Max}$	**150**	—	—	mA	V_{IN} = 2.7V to 6.0V **(Note 1)**
Output Voltage Tolerance (V_{OUT1} and V_{OUT2})	V_{OUT}	**V_R – 2.5**	V_R±0.5	**V_R + 2.5**	%	**Note 2**
Temperature Coefficient (V_{OUT1} and V_{OUT2})	TCV_{OUT}	—	25	—	ppm/°C	**Note 3**
Line Regulation (V_{OUT1} and V_{OUT2})	$\Delta V_{OUT}/\Delta V_{IN}$	—	0.02	**0.2**	%/V	$(V_R+1V) \le V_{IN} \le 6V$
Load Regulation, $V_{OUT} \ge 2.5V$ (V_{OUT1} and V_{OUT2})	$\Delta V_{OUT}/V_{OUT}$	**-1**	0.1	**+1**	%	I_{OUTX} = 0.1 mA to I_{OUTMax} **(Note 4)**
Load Regulation, $V_{OUT} < 2.5V$ (V_{OUT1} and V_{OUT2})	$\Delta V_{OUT}/V_{OUT}$	**-1.5**	0.1	**+1.5**	%	I_{OUTX} = 0.1 mA to I_{OUTMax} **(Note 4)**
Thermal Regulation	$\Delta V_{OUT}/\Delta P_D$	—	0.04	—	%/W	**Note 5**
Dropout Voltage (Note 6)						
$V_{OUT1} \ge 2.7V$	$V_{IN} - V_{OUT}$	—	104	**180**	mV	I_{OUT1} = 300 mA
$V_{OUT2} \ge 2.6V$	$V_{IN} - V_{OUT}$	—	150	**250**	mV	I_{OUT2} = 150 mA
Supply Current						
TC1301A	$I_{IN(A)}$	—	103	**180**	µA	$\overline{SHDN2} = V_{IN}$, V_{DET} = OPEN, $I_{OUT1} = I_{OUT2}$ = 0 mA
TC1301B	$I_{IN(B)}$	—	114	**180**	µA	$\overline{SHDN1} = \overline{SHDN2} = V_{IN}$, $I_{OUT1} = I_{OUT2}$ = 0 mA

Note 1: The minimum V_{IN} has to meet two conditions: $V_{IN} \ge 2.7V$ and $V_{IN} \ge V_R + V_{DROPOUT}$.

2: V_R is defined as the higher of the two regulator nominal output voltages (V_{OUT1} or V_{OUT2}).

3: $TCV_{OUT} = ((V_{OUTmax} - V_{OUTmin}) * 10^6)/(V_{OUT} * \Delta T)$.

4: Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

5: Thermal regulation is defined as the change in output voltage at a time t after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at V_{IN} = 6V for t = 10 ms.

6: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its value measured at a 1V differential.

7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R$ +1V, $I_{OUT1} = I_{OUT2}$ = 100 µA, C_{IN} = 4.7 µF, $C_{OUT1} = C_{OUT2}$ = 1 µF, C_{BYPASS} = 10 nF, $\overline{SHDN} > V_{IH}$, T_A = +25°C.
Boldface type specifications apply for junction temperatures of -40°C to +125°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Shutdown Supply Current **TC1301A**	$I_{IN\_\overline{SHDNA}}$	—	58	**90**	µA	$\overline{SHDN2}$ = GND, V_{DET} = OPEN
Shutdown Supply Current **TC1301B**	$I_{IN\_\overline{SHDNB}}$	—	0.1	1	µA	$\overline{SHDN1} = \overline{SHDN2}$ = GND
Power Supply Rejection Ratio	PSRR	—	58	—	dB	f ≤ 100 Hz, $I_{OUT1} = I_{OUT2}$ = 50 mA, C_{IN} = 0 µF
Output Noise	eN	—	830	—	nV/(Hz)$^{1/2}$	f ≤ 1 kHz, $I_{OUT1} = I_{OUT2}$ = 50 mA, C_{IN} = 0 µF
Output Short-Circuit Current (Average)						
V_{OUT1}	I_{OUTsc}	—	200	—	mA	$R_{LOAD1} \leq 1\Omega$
V_{OUT2}	I_{OUTsc}	—	140	—	mA	$R_{LOAD2} \leq 1\Omega$
$\overline{SHDN}$ Input High Threshold	V_{IH}	**45**	—	—	$\%V_{IN}$	V_{IN} = 2.7V to 6.0V
$\overline{SHDN}$ Input Low Threshold	V_{IL}	—	—	**15**	$\%V_{IN}$	V_{IN} = 2.7V to 6.0V
Wake-Up Time (From $\overline{SHDN}$ mode), (V_{OUT2})	t_{WK}	—	5.3	20	µs	V_{IN} = 5V, $I_{OUT1} = I_{OUT2}$ = 30 mA, **See Figure 5-1**
Settling Time (From $\overline{SHDN}$ mode), (V_{OUT2})	t_S	—	50	—	µs	V_{IN} = 5V, $I_{OUT1} = I_{OUT2}$ = 50 mA, **See Figure 5-2**
Thermal Shutdown Die Temperature	T_{SD}	—	150	—	°C	V_{IN} = 5V, $I_{OUT1} = I_{OUT2}$ = 100 µA
Thermal Shutdown Hysteresis	T_{HYS}	—	10	—	°C	V_{IN} = 5V
Voltage Range	V_{DET}	1.0 **1.2**	—	6.0 **6.0**	V	T_A = 0°C to +70°C T_A = -40°C to +125°C
$\overline{RESET}$ Threshold	V_{TH}	-1.4 **-2.8**	— —	+1.4 **+2.8**	% %	 T_A = -40°C to +125°C
RESET Threshold Tempco	$\Delta V_{TH}/\Delta T$	—	**30**	—	ppm/°C	
V_{DET} $\overline{RESET}$ Delay	t_{RPD}	—	180	—	µs	$V_{DET} = V_{TH}$ to (V_{TH} – 100 mV), **See Figure 5-3**
$\overline{RESET}$ Active Time-out Period	t_{RPU}	**140**	300	**560**	ms	$V_{DET} = V_{TH}$ - 100 mV to V_{TH} + 100 mV, I_{SINK} = 1.2 mA, **See Figure 5-3**.
$\overline{RESET}$ Output Voltage Low	V_{OL}	—	—	**0.2**	V	$V_{DET} = V_{THmin}$, I_{SINK} = 1.2 mA, I_{SINK} = 100 µA for V_{DET} < 1.8V, **See Figure 5-3**
$\overline{RESET}$ Output Voltage High	V_{OH}	**0.9 V_{DET}**	—	—	V	$V_{DET} > V_{THmax}$, I_{SOURCE} = 500 µA, **See Figure 5-3**

Note 1: The minimum V_{IN} has to meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq V_R + V_{DROPOUT}$.
2: V_R is defined as the higher of the two regulator nominal output voltages (V_{OUT1} or V_{OUT2}).
3: $TCV_{OUT} = ((V_{OUTmax} - V_{OUTmin}) * 10^6)/(V_{OUT} * \Delta T)$.
4: Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.
5: Thermal regulation is defined as the change in output voltage at a time t after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at V_{IN} = 6V for t = 10 ms.
6: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its value measured at a 1V differential.
7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all limits are specified for: V_{IN} = +2.7V to +6.0V.						
Parameters	**Sym**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Junction Temperature Range	T_A	-40	—	+125	°C	Steady State
Storage Temperature Range	T_A	-65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	Transient
Thermal Package Resistances						
Thermal Resistance, 8LD MSOP	θ_{JA}	—	208	—	°C/W	Typical 4-Layer Board
Thermal Resistance, 8LD DFN	θ_{JA}	—	41	—	°C/W	Typical 4-Layer Board with Vias

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{IN} = V_R$ +1V, $I_{OUT1} = I_{OUT2}$ = 100 µA, C_{IN} = 4.7 µF, $C_{OUT1} = C_{OUT2}$ = 1 µF (X5R or X7R), C_{BYPASS} = 0 pF, $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$. For the TC1301A, $V_{DET} = V_{OUT1}$, $\overline{RESET}$ = OPEN, T_A = +25°C.

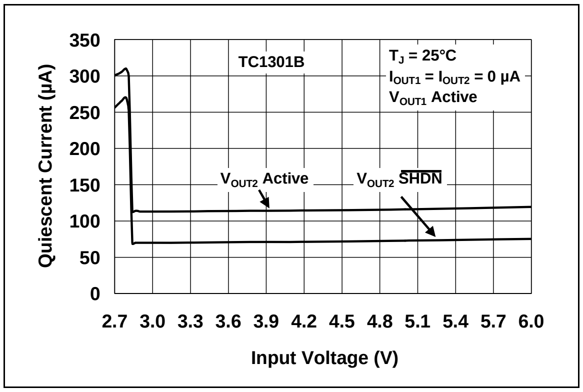


FIGURE 2-1: Quiescent Current vs. Input Voltage.

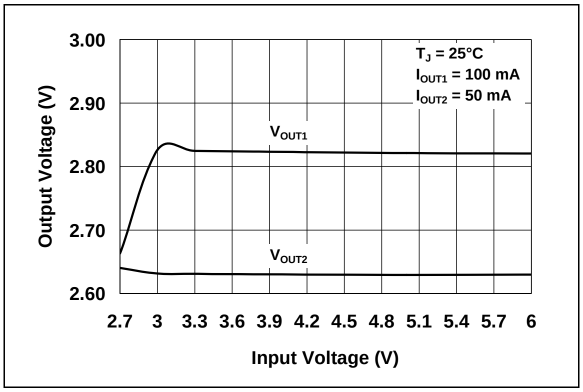


FIGURE 2-4: Output Voltage vs. Input Voltage.

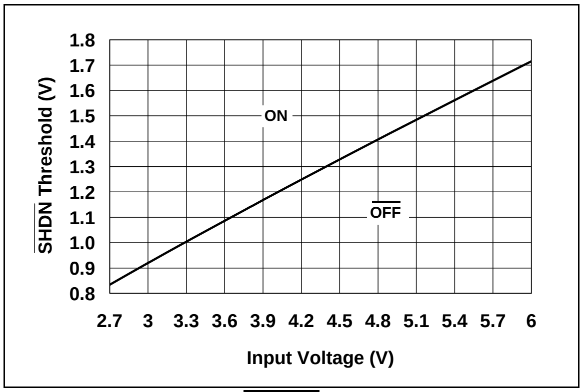


FIGURE 2-2: $\overline{SHDN}$ Voltage Threshold vs. Input Voltage.

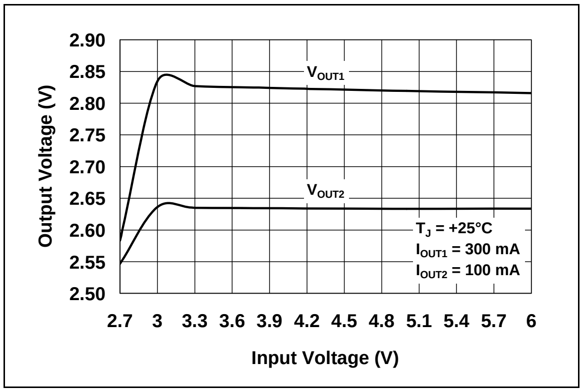


FIGURE 2-5: Output Voltage vs. Input Voltage.

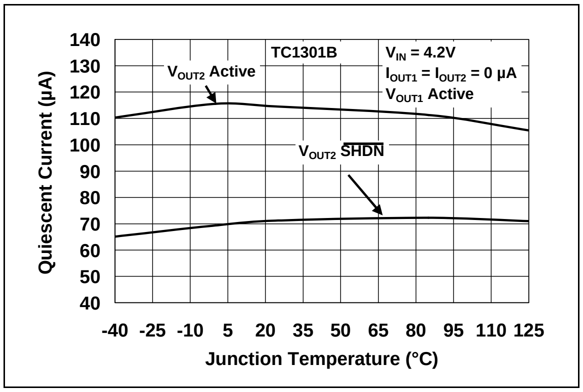


FIGURE 2-3: Quiescent Current vs. Junction Temperature.

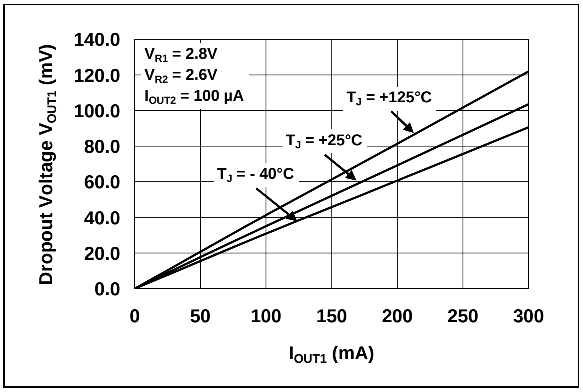


FIGURE 2-6: Dropout Voltage vs. Output Current (V_{OUT1}).

Note: Unless otherwise indicated, $V_{IN} = V_R + 1V$, $I_{OUT1} = I_{OUT2} = 100\ \mu A$, $C_{IN} = 4.7\ \mu F$, $C_{OUT1} = C_{OUT2} = 1\ \mu F$ (X5R or X7R), $C_{BYPASS} = 0$ pF, $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$. For the TC1301A, $V_{DET} = V_{OUT1}$, $\overline{RESET}$ = OPEN, $T_A = +25°C$.

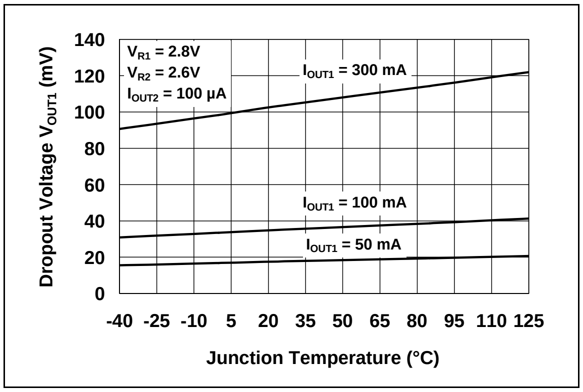


FIGURE 2-7: *Dropout Voltage vs. Junction Temperature (V_{OUT1}).*

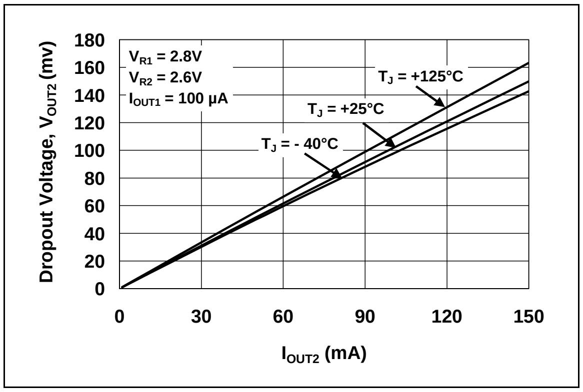


FIGURE 2-8: *Dropout Voltage vs. Output Current (V_{OUT2}).*

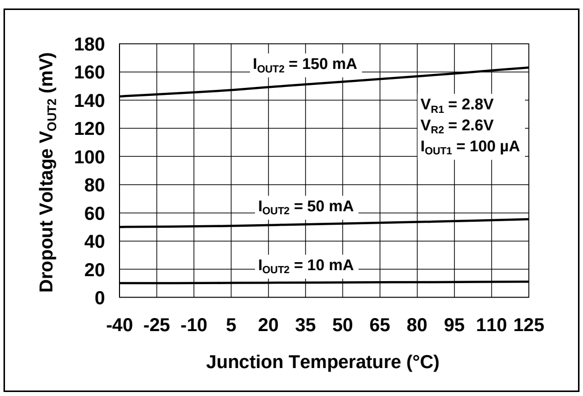


FIGURE 2-9: *Dropout Voltage vs. Junction Temperature (V_{OUT2}).*

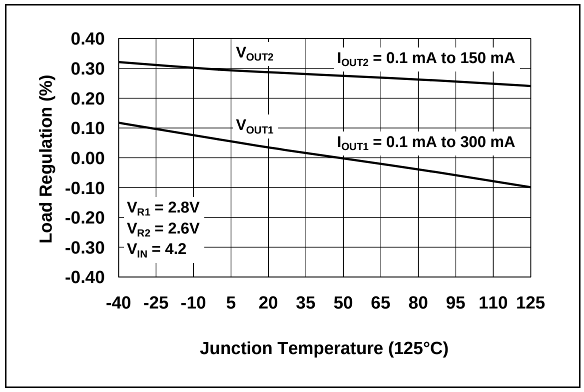


FIGURE 2-10: *V_{OUT1} and V_{OUT2} Load Regulation vs. Junction Temperature.*

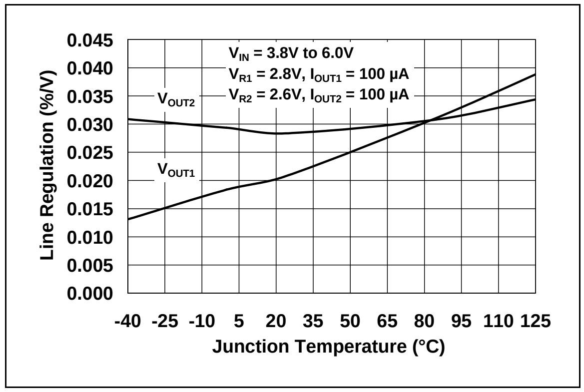


FIGURE 2-11: *V_{OUT1} and V_{OUT2} Line Regulation vs. Junction Temperature.*

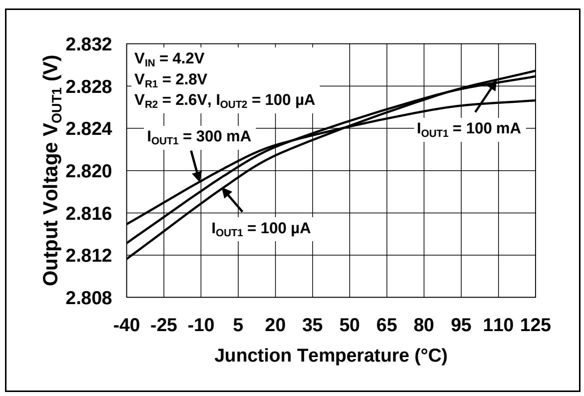


FIGURE 2-12: *V_{OUT1} vs. Junction Temperature.*

Note: Unless otherwise indicated, $V_{IN} = V_R + 1V$, $I_{OUT1} = I_{OUT2} = 100\ \mu A$, $C_{IN} = 4.7\ \mu F$, $C_{OUT1} = C_{OUT2} = 1\ \mu F$ (X5R or X7R), $C_{BYPASS} = 0$ pF, $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$. For the TC1301A, $V_{DET} = V_{OUT1}$, $\overline{RESET}$ = OPEN, $T_A = +25°C$.

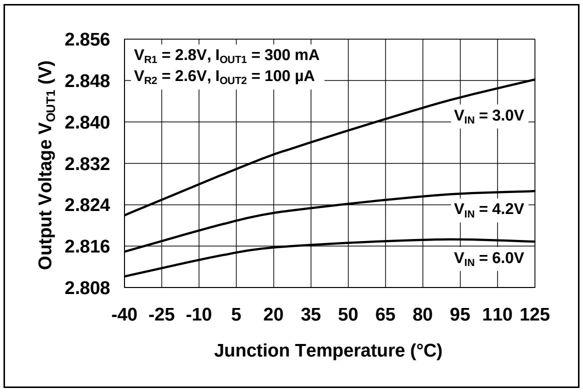


FIGURE 2-13: *V_{OUT1} vs. Junction Temperature.*

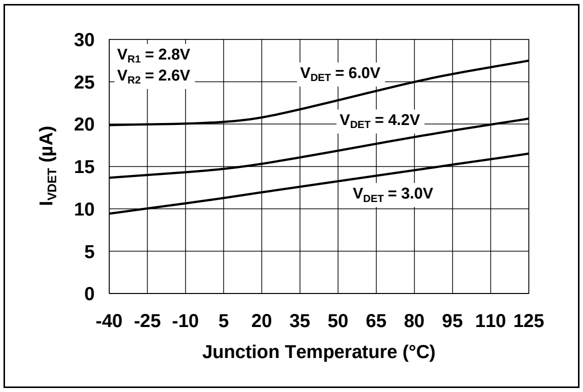


FIGURE 2-16: *I_{DET} current vs. Junction Temperature.*

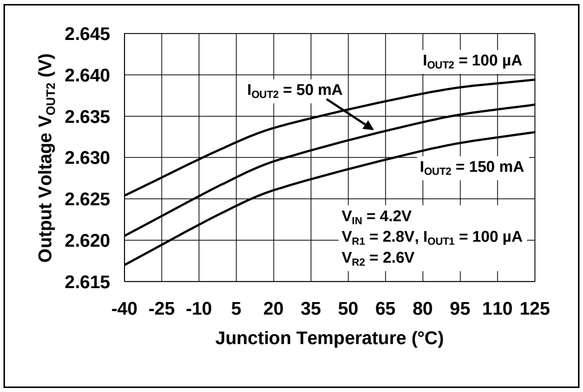


FIGURE 2-14: *V_{OUT2} vs. Junction Temperature.*

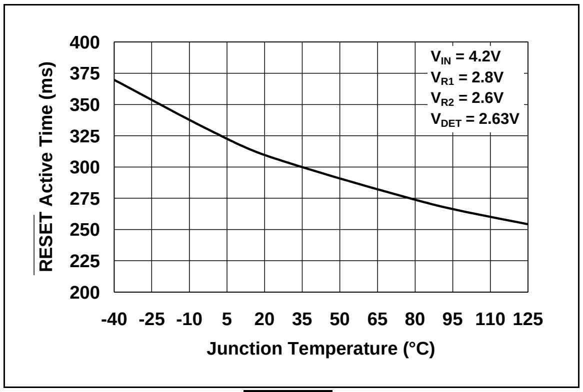


FIGURE 2-17: *$\overline{RESET}$ Active Time vs. Junction Temperature.*

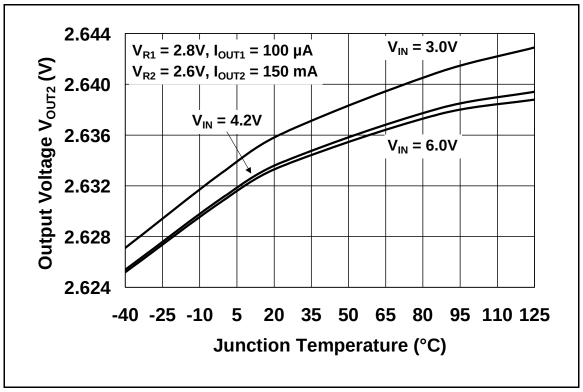


FIGURE 2-15: *V_{OUT2} vs. Junction Temperature.*

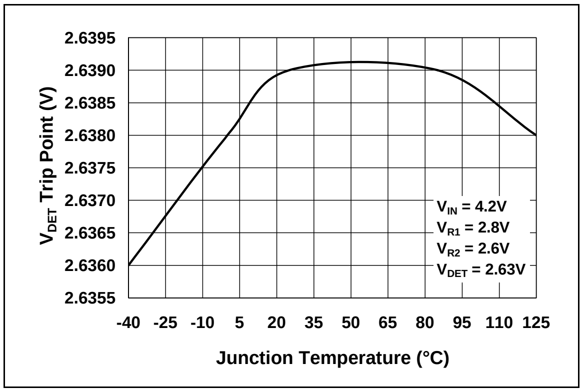


FIGURE 2-18: *V_{DET} Trip Point vs. Junction Temperature.*

Note: Unless otherwise indicated, $V_{IN} = V_R + 1V$, $I_{OUT1} = I_{OUT2} = 100\ \mu A$, $C_{IN} = 4.7\ \mu F$, $C_{OUT1} = C_{OUT2} = 1\ \mu F$ (X5R or X7R), $C_{BYPASS} = 0$ pF, $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$. For the TC1301A, $V_{DET} = V_{OUT1}$, $\overline{RESET}$ = OPEN, $T_A = +25°C$.

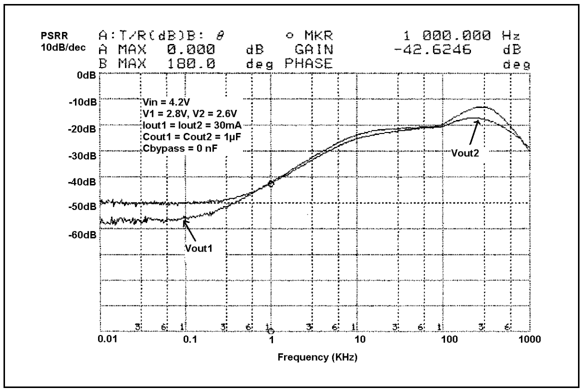


FIGURE 2-19: Power Supply Rejection Ratio vs. Frequency (without bypass capacitor).

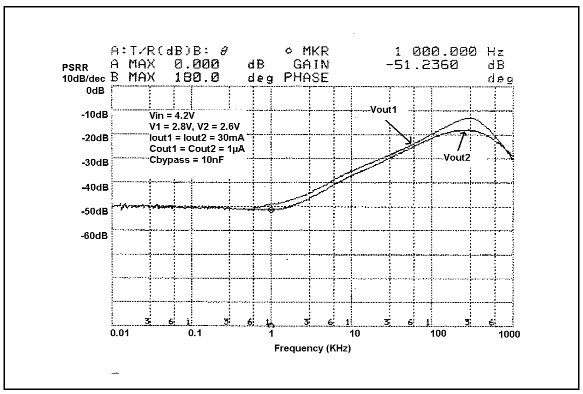


FIGURE 2-20: Power Supply Rejection Ratio vs. Frequency (with bypass capacitor).

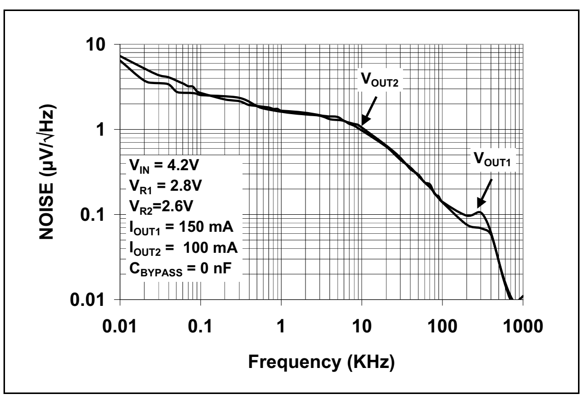


FIGURE 2-21: V_{OUT1} and V_{OUT2} Noise vs. Frequency (without bypass capacitor).

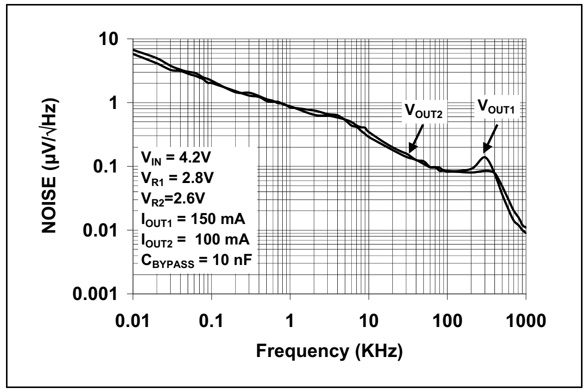


FIGURE 2-22: V_{OUT1} and V_{OUT2} Noise vs. Frequency (with bypass capacitor).

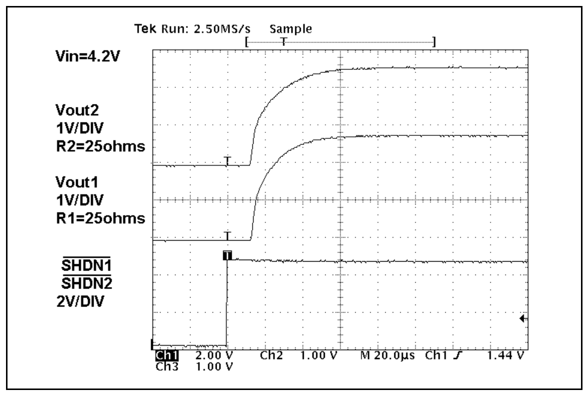


FIGURE 2-23: V_{OUT1} and V_{OUT2} Power-up from Shutdown TC1301B.

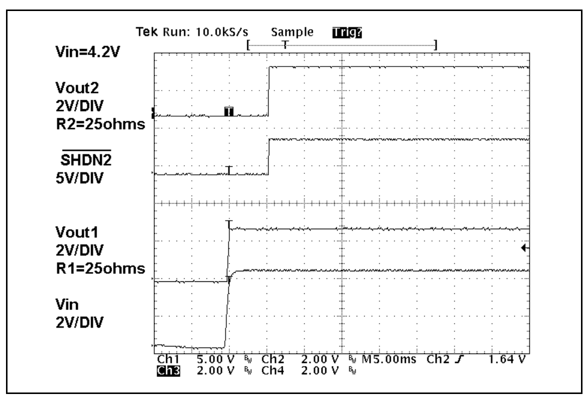


FIGURE 2-24: V_{OUT2} Power-up from Shutdown Input TC1301A.

Note: Unless otherwise indicated, $V_{IN} = V_R + 1V$, $I_{OUT1} = I_{OUT2} = 100\ \mu A$, $C_{IN} = 4.7\ \mu F$, $C_{OUT1} = C_{OUT2} = 1\ \mu F$ (X5R or X7R), $C_{BYPASS} = 0$ pF, $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$. For the TC1301A, $V_{DET} = V_{OUT1}$, $\overline{RESET}$ = OPEN, $T_A = +25°C$.

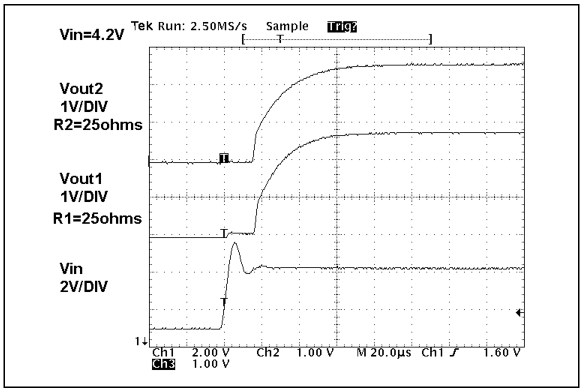


FIGURE 2-25: *V_{OUT1} and V_{OUT2} Power-up from Input Voltage TC1301B.*

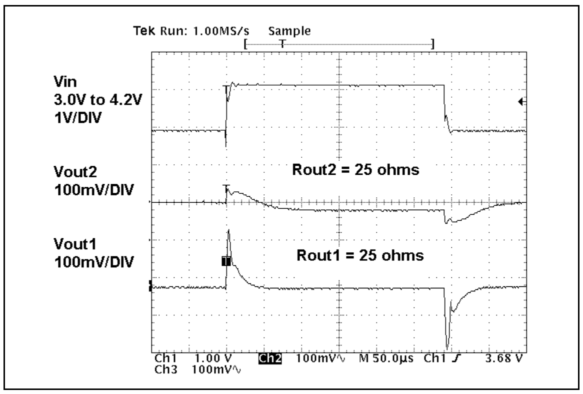


FIGURE 2-26: *Dynamic Line Response.*

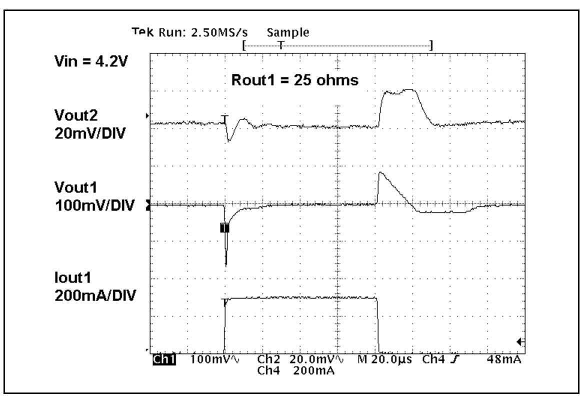


FIGURE 2-27: *300 mA Dynamic Load Step V_{OUT1}.*

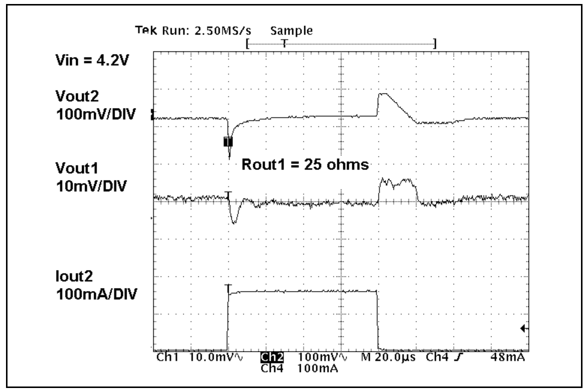


FIGURE 2-28: *150 mA Dynamic Load Step V_{OUT2}.*

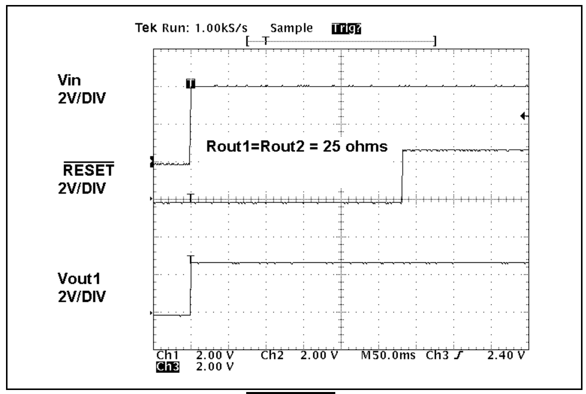


FIGURE 2-29: *$\overline{RESET}$ Power-Up From V_{IN} TC1301B.*

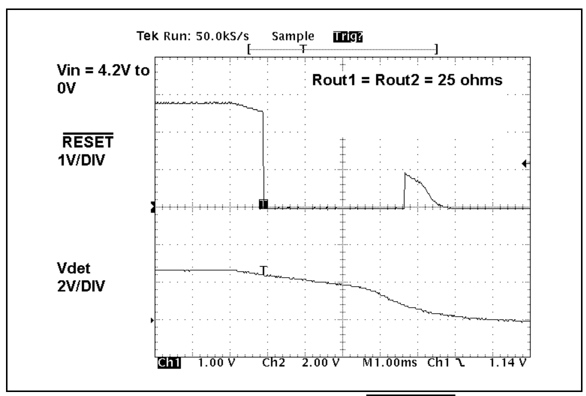


FIGURE 2-30: *TC1301A $\overline{RESET}$ Power-Down.*

Note: Unless otherwise indicated, $V_{IN} = V_R$ +1V, $I_{OUT1} = I_{OUT2}$ = 100 µA, C_{IN} = 4.7 µF, $C_{OUT1} = C_{OUT2}$ = 1 µF (X5R or X7R), C_{BYPASS} = 0 pF, $\overline{SHDN1} = \overline{SHDN2} > V_{IH}$. For the TC1301A, $V_{DET} = V_{OUT1}$, $\overline{RESET}$ = OPEN, T_A = +25°C.

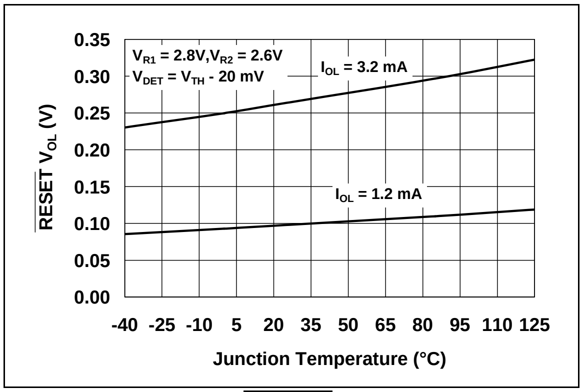


FIGURE 2-31: *$\overline{RESET}$ Output Voltage Low vs. Junction Temperature.*

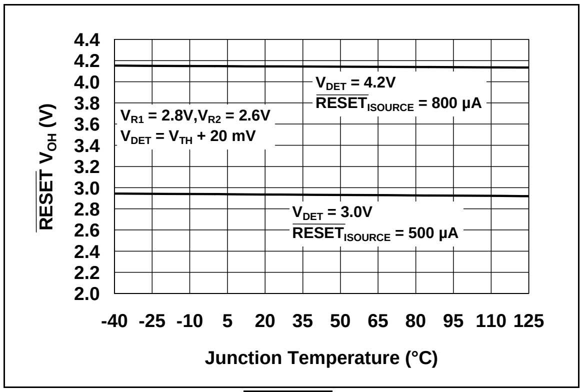


FIGURE 2-32: *$\overline{RESET}$ Output Voltage High vs. Junction Temperature.*

3.0 TC1301A PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: TC1301A PIN FUNCTION TABLE

Pin No.	Name	Function
1	$\overline{\text{RESET}}$	Push-pull output pin that will remain low while V_{DET} is below the reset threshold and for 300 ms after V_{DET} rises above the reset threshold.
2	V_{OUT1}	Regulated output voltage #1 capable of 300 mA.
3	GND	Circuit ground pin.
4	Bypass	Internal reference bypass pin. A 10 nF external capacitor can be used to further reduce output noise and improve PSRR performance.
5	$\overline{\text{SHDN2}}$	Output #2 shutdown control Input.
6	V_{OUT2}	Regulated output voltage #2 capable of 150 mA.
7	V_{IN}	Unregulated input voltage pin.
8	V_{DET}	Input pin for Voltage Detector (V_{DET}).

3.1 $\overline{\text{RESET}}$ Output Pin

The push-pull output pin is used to monitor the voltage on the V_{DET} pin. If the V_{DET} voltage is less than the threshold voltage, the $\overline{\text{RESET}}$ output will be held in the low state. As the V_{DET} pin rises above the threshold, the $\overline{\text{RESET}}$ output will remain in the low state for 300 ms and then change to the high state, indicating that the voltage on the V_{DET} pin is above the threshold.

3.2 Regulated Output Voltage #1 (V_{OUT1})

Connect V_{OUT1} to the positive side of the V_{OUT1} capacitor and load. It is capable of 300 mA maximum output current. V_{OUT1} output is available when V_{IN} is available; there is no pin to turn it $\overline{\text{OFF}}$. See TC1301B if ON/$\overline{\text{OFF}}$ control of V_{OUT1} is desired.

3.3 Circuit Ground Pin (GND)

Connect GND to the negative side of the input and output capacitor. Only the LDO internal circuitry bias current flows out of this pin (200 µA maximum).

3.4 Reference Bypass Input

By connecting an external 10 nF capacitor (typical) to the bypass input, both outputs (V_{OUT1} and V_{OUT2}) will have less noise and improved Power Supply Ripple Rejection (PSRR) performance. The LDO output voltage start-up time will increase with the addition of an external bypass capacitor. By leaving this pin unconnected, the start-up time will be minimized.

3.5 Output Voltage #2 Shutdown ($\overline{\text{SHDN2}}$)

ON/$\overline{\text{OFF}}$ control is performed by connecting $\overline{\text{SHDN2}}$ to its proper level. When the input of this pin is connected to a voltage less than 15% of V_{IN}, V_{OUT2} will be $\overline{\text{OFF}}$. If this pin is connected to a voltage that is greater than 45% of V_{IN}, V_{OUT2} will be turned ON.

3.6 Regulated Output Voltage #2 (V_{OUT2})

Connect V_{OUT2} to the positive side of the V_{OUT2} capacitor and load. This pin is capable of a maximum output current of 150 mA. V_{OUT2} can be turned ON and $\overline{\text{OFF}}$ using $\overline{\text{SHDN2}}$.

3.7 Unregulated Input Voltage Pin (V_{IN})

Connect the unregulated input voltage source to V_{IN}. If the input voltage source is located more than several inches away, or is a battery, a typical input capacitance of 1 µF to 4.7 µF is recommended.

3.8 Input Pin for Voltage Detector (V_{DET})

The voltage on the input of V_{DET} is compared with the preset V_{DET} threshold voltage. If the voltage is below the threshold, the $\overline{\text{RESET}}$ output will be low. If the voltage is above the V_{DET} threshold, the $\overline{\text{RESET}}$ output will be high after the $\overline{\text{RESET}}$ time period. The I_{DET} supply current is typically 9 µA at room temperature, with V_{DET} = 3.8V.

4.0 TC1301B PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

TABLE 4-1: TC1301B PIN FUNCTION TABLE

Pin No.	Name	Function
1	$\overline{\text{RESET}}$	Push-pull output pin that will remain low while V_{DET} is below the reset threshold and for 300 ms after V_{OUT1} rises above the reset threshold
2	V_{OUT1}	Regulated output voltage #1 capable of 300 mA
3	GND	Circuit ground pin
4	Bypass	Internal reference bypass pin. A 10 nF external capacitor can be used to further reduce output noise and improve PSRR performance
5	$\overline{\text{SHDN2}}$	Output #2 shutdown control Input
6	V_{OUT2}	Regulated output voltage #2 capable of 150 mA
7	V_{IN}	Unregulated input voltage pin
8	$\overline{\text{SHDN1}}$	Output #1 shutdown control input

4.1 $\overline{\text{RESET}}$ Output Pin

The push-pull output pin is used to monitor the output voltage (V_{OUT1}). If V_{OUT1} is less than the threshold voltage, the $\overline{\text{RESET}}$ output will be held in the low state. As V_{OUT1} rises above the threshold, the $\overline{\text{RESET}}$ output will remain in the low state for 300 ms and then change to the high state, indicating that the voltage on V_{OUT1} is above the threshold.

4.2 Regulated Output Voltage #1 (V_{OUT1})

Connect V_{OUT1} to the positive side of the V_{OUT1} capacitor and load. It is capable of 300 mA maximum output current. For the TC1301B, V_{OUT1} can be turned ON and $\overline{\text{OFF}}$ using the $\overline{\text{SHDN1}}$ input pin.

4.3 Circuit Ground Pin (GND)

Connect GND to the negative side of the input and output capacitor. Only the LDO internal circuitry bias current flows out of this pin (200 µA maximum).

4.4 Reference Bypass Input

By connecting an external 10 nF capacitor (typical) to bypass, both outputs (V_{OUT1} and V_{OUT2}) will have less noise and improved Power Supply Ripple Rejection (PSRR) performance. The LDO output voltage start-up time will increase with the addition of an external bypass capacitor. By leaving this pin unconnected, the start-up time will be minimized.

4.5 Output Voltage #2 Shutdown ($\overline{\text{SHDN2}}$)

ON/$\overline{\text{OFF}}$ control is performed by connecting $\overline{\text{SHDN2}}$ to its proper level. When this pin is connected to a voltage less than 15% of V_{IN}, V_{OUT2} will be $\overline{\text{OFF}}$. If this pin is connected to a voltage that is greater than 45% of V_{IN}, V_{OUT2} will be turned ON.

4.6 Regulated Output Voltage #2 (V_{OUT2})

Connect V_{OUT2} to the positive side of the V_{OUT2} capacitor and load. This pin is capable of a maximum output current of 150 mA. V_{OUT2} can be turned ON and $\overline{\text{OFF}}$ using $\overline{\text{SHDN2}}$.

4.7 Unregulated Input Voltage Pin (V_{IN})

Connect the unregulated input voltage source to V_{IN}. If the input voltage source is located more than several inches away or is a battery, a typical minimum input capacitance of 1 µF and 4.7 µF is recommended.

4.8 Output Voltage #1 Shutdown ($\overline{\text{SHDN1}}$)

ON/$\overline{\text{OFF}}$ control is performed by connecting $\overline{\text{SHDN1}}$ to its proper level. When this pin is connected to a voltage less than 15% of V_{IN}, V_{OUT1} will be $\overline{\text{OFF}}$. If this pin is connected to a voltage that is greater than 45% of V_{IN}, V_{OUT1} will be turned ON.

5.0 DETAILED DESCRIPTION

5.1 Device Overview

The TC1301A/B is a combination device consisting of one 300 mA LDO regulator with a fixed output voltage, V_{OUT1} (1.5V – 3.3V), one 150 mA LDO regulator with a fixed output voltage, V_{OUT2} (1.5V – 3.3V), and a microcontroller voltage monitor/$\overline{RESET}$ (2.2V to 3.2V).

For the TC1301A, the 300 mA output (V_{OUT1}) is always present, independent of the level of $\overline{SHDN2}$. The 150 mA output (V_{OUT2}) can be turned on/off by controlling the level of $\overline{SHDN2}$.

For the TC1301B, V_{OUT1} and V_{OUT2} each have independent shutdown input pins ($\overline{SHDN1}$ and $\overline{SHDN2}$) to control their respective outputs. In the case of the TC1301B, the voltage detect input of the microcontroller $\overline{RESET}$ function is internally connected to the V_{OUT1} output of the device.

5.2 LDO Output #1

LDO output #1 is rated for 300 mA of output current. The typical dropout voltage for V_{OUT1} = 104 mV @ 300 mA. A 1 µF (minimum) output capacitor is needed for stability and should be located as close to the V_{OUT1} pin and ground as possible.

5.3 LDO Output #2

LDO output #2 is rated for 150 mA of output current. The typical dropout voltage for V_{OUT2} = 150 mV. A 1 µF (minimum) capacitor is needed for stability and should be located as close to the V_{OUT2} pin and ground as possible.

5.4 $\overline{RESET}$ Output

The $\overline{RESET}$ output is used to detect whether the level on the input of V_{DET} (TC1301A) or V_{OUT1} (TC1301B) is above or below a preset threshold. If the voltage detected is below the preset threshold, the $\overline{RESET}$ output is capable of sinking 1.2 mA ($V_{\overline{RESET}}$ < 0.2V maximum). Once the voltage being monitored is above the preset threshold, the $\overline{RESET}$ output pin will transition from a logic-low to a logic-high after a 300 ms delay. The $\overline{RESET}$ output is a push-pull configuration and will actively pull the $\overline{RESET}$ output up to V_{DET} when not in $\overline{RESET}$.

5.5 Input Capacitor

Low input source impedance is necessary for the two LDO outputs to operate properly. When operating from batteries or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1.0 µF to 4.7 µF is recommended for most applications. When using large capacitors on the LDO outputs, larger capacitance is recommended on the LDO input. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will help reduce the input impedance and further reduce any high-frequency noise on the input and output of the LDO.

5.6 Output Capacitor

A minimum output capacitance of 1 µF for each of the TC1301A/B LDO outputs is necessary for stability. Ceramic capacitors are recommended because of their size, cost and environmental robustness qualities. Electrolytic (Tantalum or Aluminum) capacitors can be used on the LDO outputs as well. The Equivalent Series Resistance (ESR) requirements on the electrolytic output capacitors are between 0 and 2 ohms. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials, X7R and X5R, have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 uF X5R 0805 capacitor has an ESR of 50 milli-ohms. Larger LDO output capacitors can be used with the TC1301A/B to improve dynamic performance and power supply ripple rejection performance. A maximum of 10 µF is recommended. Aluminum electrolytic capacitors are not recommended for low temperature applications of < -25°C.

5.7 Bypass Input

The bypass pin is connected to the internal LDO reference. By adding capacitance to this pin, the LDO ripple rejection, input voltage transient response and output noise performance are all increased. A typical bypass capacitor between 470 pF to 10 nF is recommended. Larger bypass capacitors can be used, but results in a longer time-period for the LDO outputs to reach their rated output voltage when started from $\overline{SHDN}$ or V_{IN}.

5.8 GND

For the optimal noise and PSRR performance, the GND pin of the TC1301A/B should be tied to a quiet circuit ground. For applications that have switching or noisy inputs, tie the GND pin to the return of the output capacitor. Ground planes help lower inductance and voltage spikes caused by fast transient load currents and are recommended for applications that are subjected to fast load transients.

5.9 $\overline{SHDN1}$/$\overline{SHDN2}$ Operation

The TC1301A $\overline{SHDN2}$ pin is used to turn V_{OUT2} ON and OFF. A logic-high level on $\overline{SHDN2}$ will enable the V_{OUT2} output, while a logic-low on the $\overline{SHDN2}$ pin will disable the V_{OUT2} output. For the TC1301A, V_{OUT1} is not affected by $\overline{SHDN2}$ and will be enabled as long as the input voltage is present.

The TC1301B $\overline{SHDN1}$ and $\overline{SHDN2}$ pins are used to turn V_{OUT1} and V_{OUT2} ON and OFF. They operate independent of each other.

5.10 TC1301A $\overline{SHDN2}$ Timing

V_{OUT1} will rise independent of the level of $\overline{SHDN2}$ for the TC1301A. Figure 5-1 is used to define the wake-up time from shutdown (t_{WK}) and the settling time (t_S). The wake-up time is dependant upon the frequency of operation. The faster the $\overline{SHDN}$ pin is pulsed, the shorter the wake-up time will be.

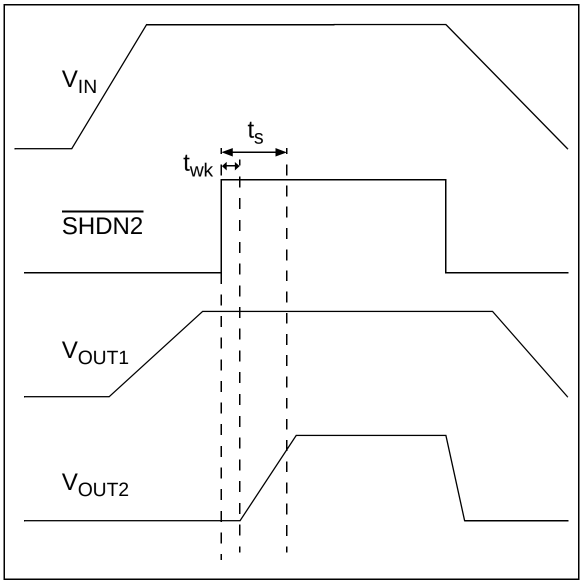


FIGURE 5-1: *TC1301A Timing.*

5.11 TC1301B $\overline{SHDN1}$ / $\overline{SHDN2}$ Timing

For the TC1301B, the $\overline{SHDN1}$ input pin is used to control V_{OUT1}. The $\overline{SHDN2}$ input pin is used to control V_{OUT2}, independent of the logic input on $\overline{SHDN1}$.

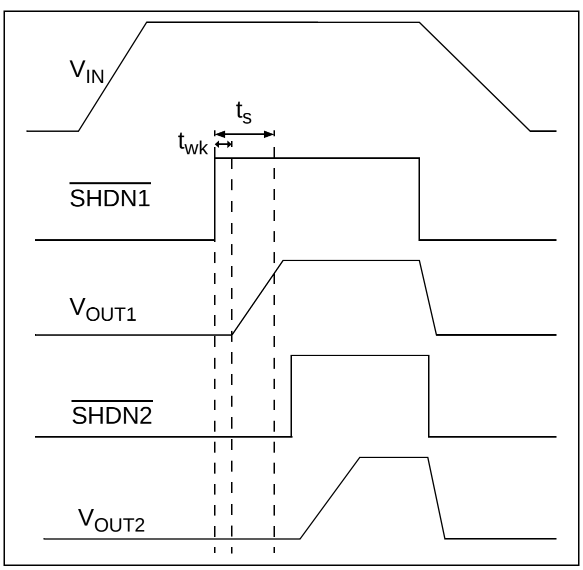


FIGURE 5-2: *TC1301B Timing.*

5.12 V_{DET} and $\overline{RESET}$ Operation

The TC1301A/B integrates an independent voltage reset monitor that can be used for low-battery input voltage detection or a microprocessor Power-On Reset (POR) function. The input voltage for the detector is different for the TC1301A than it is for the TC1301B. For the TC1301A, the input voltage to the detector is pin 8 (V_{DET}). For the TC1301B, the input voltage to the detector is internally connected to the output of LDO #1 (V_{OUT1}). The detected voltage is sensed and compared to an internal threshold. When the voltage on the V_{DET} pin is below the threshold voltage, the $\overline{RESET}$ output pin is low. When the voltage on the V_{DET} pin rises above the voltage threshold, the $\overline{RESET}$ output will remain low for typically 300 ms ($\overline{RESET}$ time-out period). After the $\overline{RESET}$ time-out period, the $\overline{RESET}$ output voltage will transition from the low output state to the high output state if the detected voltage pin remains above the threshold voltage.

The $\overline{RESET}$ output will be driven low within 180 µs of V_{DET} going below the $\overline{RESET}$ voltage threshold. The $\overline{RESET}$ output will remain valid for detected voltages greater than 1.2V overtemperature.

5.13 TC1301A $\overline{RESET}$ Timing

Figure 5-3 shows the $\overline{RESET}$ timing waveforms for the TC1301A. This diagram is also used to define the $\overline{RESET}$ active time-out period (t_{RPU}) and the V_{DET} $\overline{RESET}$ delay time (t_{RPD}).

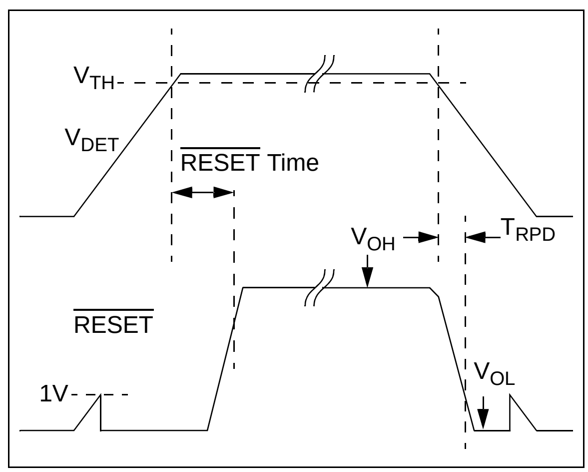


FIGURE 5-3: *TC1301A $\overline{RESET}$ Timing.*

5.14 TC1301B $\overline{RESET}$ Timing

The timing waveforms for the TC1301B $\overline{RESET}$ output are shown in Figure 5-4. Note that the $\overline{RESET}$ threshold input for the TC1301B is V_{OUT1}. The V_{OUT1} to $\overline{RESET}$ threshold detector connection is made internal in the case of the TC1301B.

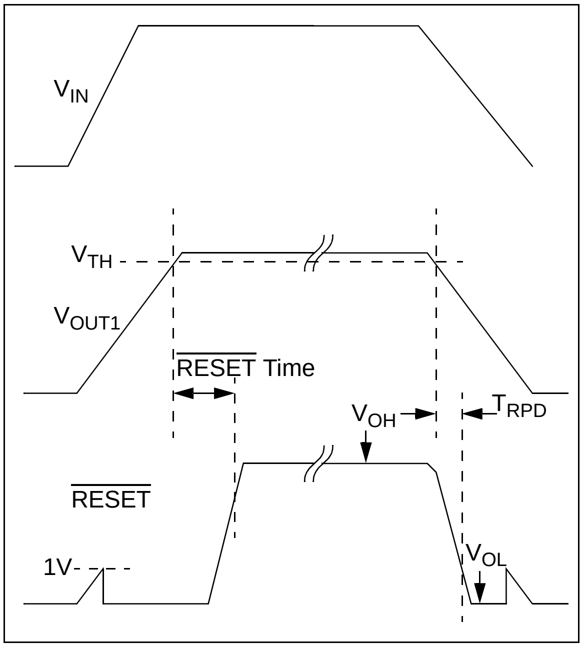


FIGURE 5-4: *TC1301B $\overline{RESET}$ Timing.*

5.15 Device Protection

5.15.1 OVERCURRENT LIMIT

In the event of a faulted output load, the maximum current the LDO output will permit to flow is limited internally for each of the TC1301A/B outputs. The peak current limit for V_{OUT1} is typically 1.1A, while the peak current limit for V_{OUT2} is typically 0.5A. During short-circuit operation, the average current is limited to 200 mA for V_{OUT1} and 140 mA for V_{OUT2}.The V_{DET} and $\overline{RESET}$ circuit will continue to operate in the event of an overcurrent on either output for the TC1301A. The voltage detect and $\overline{RESET}$ circuit will continue to operate in the event of an overcurrent on V_{OUT1} (or V_{OUT2}) for the TC1301B. In the event of an overcurrent on V_{OUT1}, the $\overline{RESET}$ will detect the absence of V_{OUT1}.

5.15.2 OVERTEMPERATURE PROTECTION

If the internal power dissipation within the TC1301A/B is excessive due to a faulted load or higher-than-specified line voltage, an internal temperature-sensing element will prevent the junction temperature from exceeding approximately 150°C. If the junction temperature does reach 150°C, both outputs will be disabled until the junction temperature cools to approximately 140°C. The device will resume normal operation. If the internal power dissipation continues to be excessive, the device will again shut off. The V_{DET} and $\overline{RESET}$ circuit will continue to operate normally during an overtemperature fault condition for both the TC1301A and TC1301B.

6.0 APPLICATION CIRCUITS/ ISSUES

6.1 Typical Application

The TC1301A/B is used for applications that require the integration of two LDO's and a microcontroller $\overline{\text{RESET}}$.

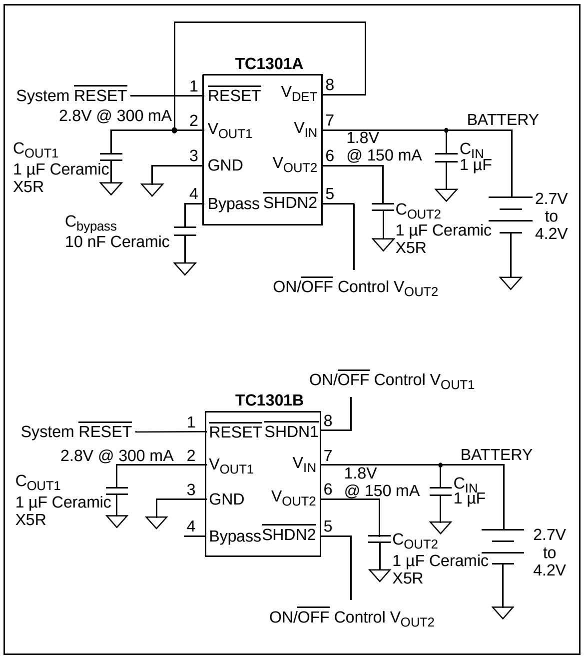


FIGURE 6-1: Typical Application Circuit TC1301A/B.

6.1.1 APPLICATION INPUT CONDITIONS

Package Type = 3x3 DFN8

Input Voltage Range = 2.7V to 4.2V

V_{IN} maximum = 4.2V

V_{IN} typical = 3.6V

V_{OUT1} = 300 mA maximum

V_{OUT2} = 150 mA maximum

System $\overline{\text{RESET}}$ Load = 10 kΩ

6.2 Power Calculations

6.2.1 POWER DISSIPATION

The internal power dissipation within the TC1301A/B is a function of input voltage, output voltage, output current and quiescent current. The following equation can be used to calculate the internal power dissipation for each LDO.

EQUATION 6-1:

$$P_{LDO} = (V_{IN(MAX)}) - V_{OUT(MIN)}) \times I_{OUT(MAX)})$$

Where:

P_{LDO} = LDO Pass device internal power dissipation

$V_{IN(MAX)}$ = Maximum input voltage

$V_{OUT(MIN)}$ = LDO minimum output voltage

In addition to the LDO pass element power dissipation, there is power dissipation within the TC1301A/B as a result of quiescent or ground current. The power dissipation as a result of the ground current can be calculated using the following equation. The V_{IN} pin quiescent current and the V_{DET} pin current are both considered. The V_{IN} current is a result of LDO quiescent current, while the V_{DET} current is a result of the voltage detector current.

EQUATION 6-2:

$$P_{I(GND)} = V_{IN(MAX)} \times (I_{VIN} + I_{VDET})$$

Where:

$P_{I(GND)}$ = Total current in ground pin

$V_{IN(MAX)}$ = Maximum input voltage

I_{VIN} = Current flowing in the V_{IN} pin with no output current on either LDO output

I_{VDET} = Current in the V_{DET} pin with $\overline{\text{RESET}}$ loaded

The total power dissipated within the TC1301A/B is the sum of the power dissipated in both of the LDO's and the $P(I_{GND})$ term. Because of the CMOS construction, the typical I_{GND} for the TC1301A/B is 116 µA. Operating at a maximum of 4.2V results in a power dissipation of 0.5 milliWatts. For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the TC1301A/B is 125°C. To estimate the internal junction temperature of the TC1301A/B, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ($R\theta_{JA}$) of the device. The thermal resistance from junction to ambient for the 3x3 DFN8 pin package is estimated at 41°C/W.

EQUATION 6-3:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{AMAX}$$

Where:

$T_{J(MAX)}$	=	Maximum continuous junction temperature
P_{TOTAL}	=	Total device power dissipation
$R\theta_{JA}$	=	Thermal resistance from junction-to-ambient
T_{AMAX}	=	Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction to ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

EQUATION 6-4:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

Where:

$P_{D(MAX)}$	=	Maximum device power dissipation
$T_{J(MAX)}$	=	Maximum continuous junction temperature
T_{AMAX}	=	Maximum ambient temperature
$R\theta_{JA}$	=	Thermal resistance from junction-to-ambient

EQUATION 6-5:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

Where:

$T_{J(RISE)}$	=	Rise in device junction temperature over the ambient temperature
$P_{D(MAX)}$	=	Maximum device power dissipation
$R\theta_{JA}$	=	Thermal resistance from junction-to-ambient

EQUATION 6-6:

$$T_J = T_{J(RISE)} + T_A$$

Where:

T_J	=	Junction Temperature
$T_{J(RISE)}$	=	Rise in device junction temperature over the ambient temperature
T_A	=	Ambient Temperature

6.3 Typical Application

Internal power dissipation, junction temperature rise, junction temperature, and maximum power dissipation are calculated in the following example. The power dissipation as a result of ground current is small enough to be neglected.

6.3.1 POWER DISSIPATION EXAMPLE

Package

Package Type = 3x3 DFN8

Input Voltage

V_{IN} = 2.7V to 4.2V

LDO Output Voltages and Currents

V_{OUT1} = 2.8V

I_{OUT1} = 300 mA

V_{OUT2} = 1.8V

I_{OUT2} = 150 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = 50°C

Internal Power Dissipation

Internal power dissipation is the sum of the power dissipation for each LDO pass device.

$P_{LDO1(MAX)} = (V_{IN(MAX)} - V_{OUT1(MIN)}) \times I_{OUT1(MAX)}$

P_{LDO1} = (4.2V - (0.975 x 2.8V)) x 300 mA

P_{LDO1} = 441.0 milliWatts

P_{LDO2} = (4.2V - (0.975 X 1.8V)) x 150 mA

P_{LDO2} = 366.8 milliWatts

$P_{TOTAL} = P_{LDO1} + P_{LDO2}$

P_{TOTAL} = 807.8 milliWatts

Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface-mount packages. The EIA/JEDEC specification is JESD51-7, "High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages". The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors such as copper area and thickness. Refer to AN792, "A Method To Determine How Much Power a SOT-23 Can Dissipate in Your Application" (DS00792), for more information regarding this subject.

$T_{J(RISE)} = P_{TOTAL} \times Rq_{JA}$

T_{JRISE} = 807.8 milliWatts x 41.0° C/W

T_{JRISE} = 33.1°C

Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below:

$$T_J = T_{JRISE} + T_{A(MAX)}$$

$$T_J = 83.1°C$$

Maximum Package Power Dissipation at 50°C Ambient Temperature

3X3DFN8 (41° C/W $R\theta_{JA}$)

$P_{D(MAX)}$ = (125°C - 50°C) / 41° C/W

$P_{D(MAX)}$ = 1.83 Watts

MSOP8 (208° C/W $R\theta_{JA}$)

$P_{D(MAX)}$ = (125°C - 50°C) / 208° C/W

$P_{D(MAX)}$ = 0.360 Watts

7.0 TYPICAL LAYOUT TC1301A

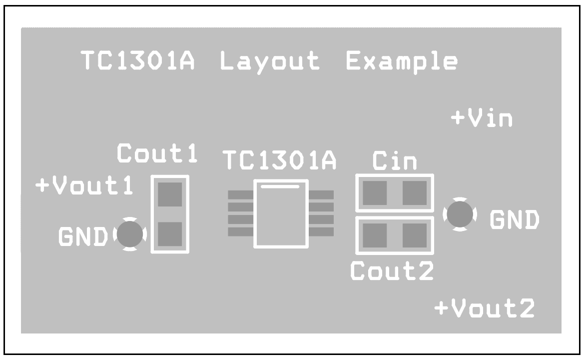


FIGURE 7-1: *MSOP8 Silk Screen Layer.*

When doing the physical layout for the TC1301A/B, the highest priority is placing the input and output capacitors as close to the device pins as is practical. Figure 7-1 above represents a typical placement of the components when using SMT0805 capacitors.

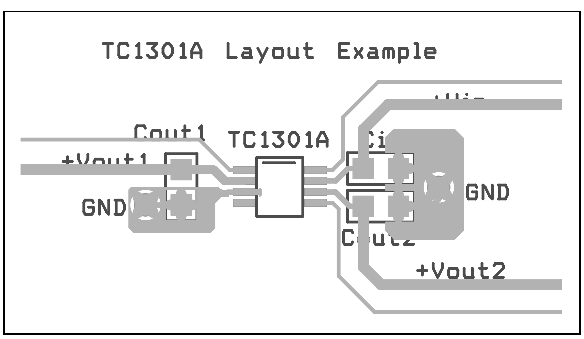


FIGURE 7-2: *MSOP8 Wiring Layer.*

A wiring example for the TC1301A is shown. The vias represent the connection to a ground plane that is below the wiring layer.

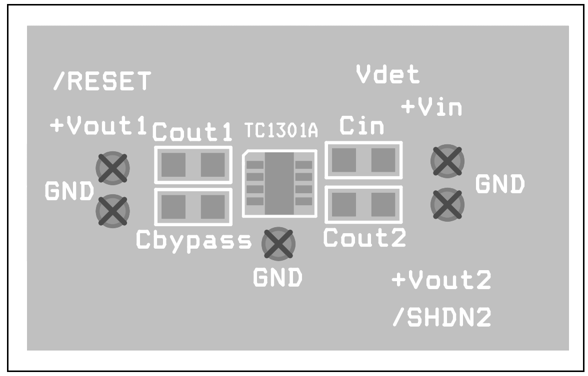


FIGURE 7-3: *3x3 DFN Silk-Screen Example.*

8-lead 3X3 DFN physical layout example with bypass capacitor.

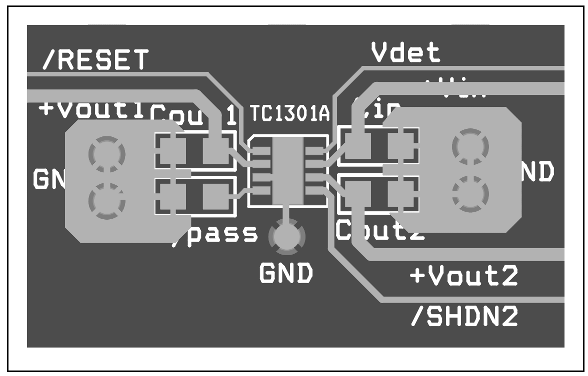


FIGURE 7-4: *3x3 DFN Top Metal Layer Example.*

Vias represent the connection to a ground plane that is below the wiring layer.

8.0 ADDITIONAL OUTPUT VOLTAGE AND THRESHOLD VOLTAGE OPTIONS

8.1 Output Voltage and Threshold Voltage Range

Table 8-1 describes the range of output voltage options available for the TC1301A/B. V_{OUT1} and V_{OUT2} can be factory preset from 1.5V to 3.3V in 100 mV increments. The V_{DET} (TC1301A) or threshold voltage (TC1301B) can be preset from 2.2V to 3.2V in 10 mV increments.

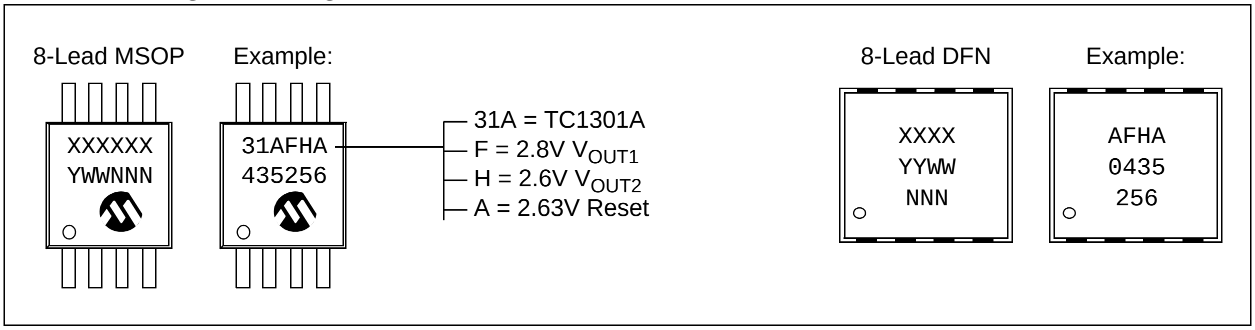
TABLE 8-1: CUSTOM OUTPUT VOLTAGE AND THRESHOLD VOLTAGE RANGES

V_{OUT1}	V_{OUT2}	V_{DET} Threshold
1.5V to 3.3V	1.5V to 3.3V	2.2V to 3.2V

For a listing of TC1301A/B standard parts, refer to the **Product Identification System** on **page 25**.

9.0 PACKAGING INFORMATION

9.1 Package Marking Information



X1 represents V_{OUT1} configuration:

Code	V_{OUT1}	Code	V_{OUT1}	Code	V_{OUT1}
A	3.3V	J	2.4V	S	1.5V
B	3.2V	K	2.3V	T	1.65V
C	3.1V	L	2.2V	U	2.85V
D	3.0V	M	2.1V	V	2.65V
E	2.9V	N	2.0V	W	1.85V
F	2.8V	O	1.9V	X	—
G	2.7V	P	1.8V	Y	—
H	2.6V	Q	1.7V	Z	—
I	2.5V	R	1.6V		

Xr represents the reset voltage range:

Code	Voltage	Code	Voltage
A	2.63V	J	—
B	2.2V	K	—
C	2.32V	L	—
D	2.5V	M	—
E	2.4V	N	—
F	2.6V	O	—
G	—	P	—
H	—	Q	—
I	—	R	—

X2 represents V_{OUT2} configuration:

Code	V_{OUT2}	Code	V_{OUT2}	Code	V_{OUT2}
A	3.3V	J	2.4V	S	1.5V
B	3.2V	K	2.3V	T	1.65V
C	3.1V	L	2.2V	U	2.85V
D	3.0V	M	2.1V	V	2.65V
E	2.9V	N	2.0V	W	1.85V
F	2.8V	O	1.9V	X	—
G	2.7V	P	1.8V	Y	—
H	2.6V	Q	1.7V	Z	—
I	2.5V	R	1.6V		

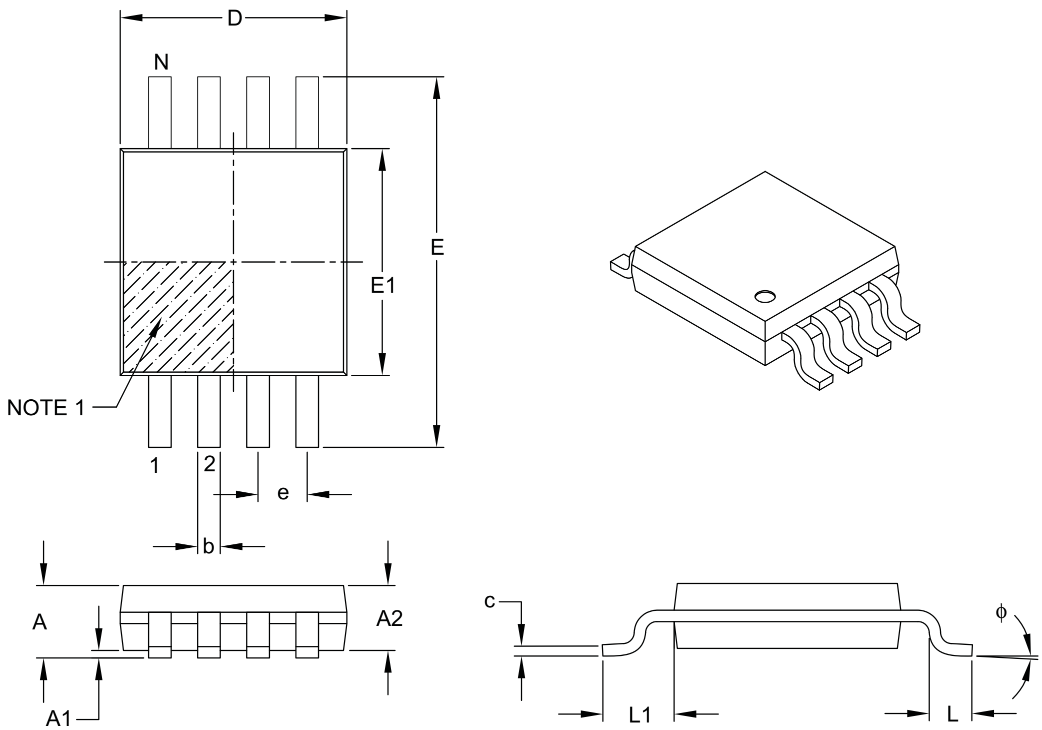
For a listing of TC1301A/B standard parts, refer to the **Product Identification System** section on **page 25**.

Legend:		
	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

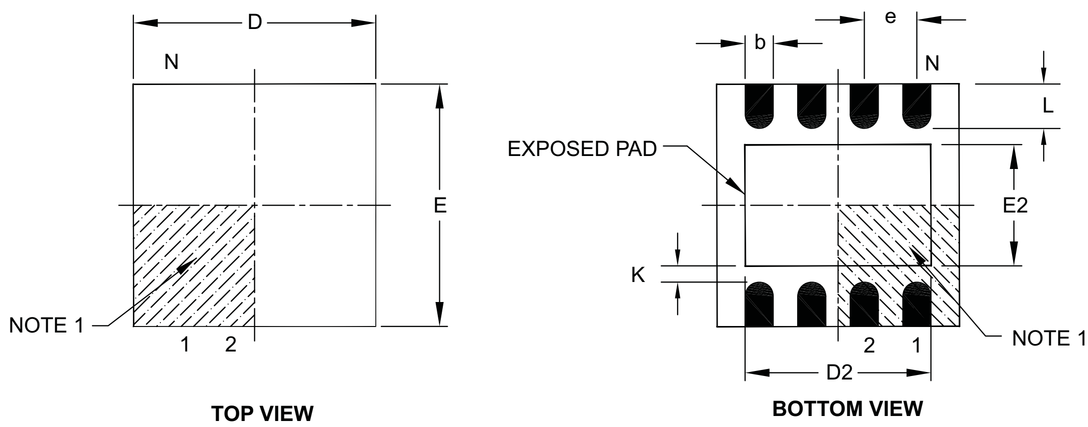
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

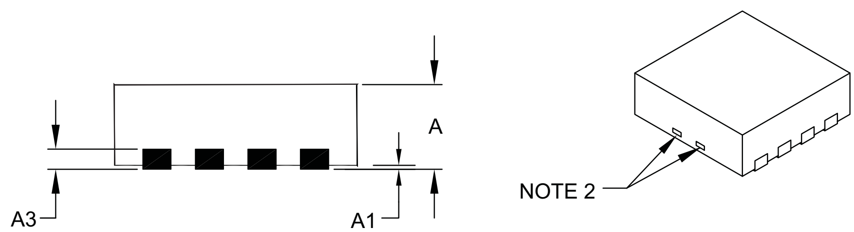
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

8-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





		Units	MILLIMETERS		
		Dimension Limits	MIN	NOM	MAX
Number of Pins	N			8	
Pitch	e			0.65 BSC	
Overall Height	A		0.80	0.90	1.00
Standoff	A1		0.00	0.02	0.05
Contact Thickness	A3			0.20 REF	
Overall Length	D			3.00 BSC	
Exposed Pad Width	E2		0.00	–	1.60
Overall Width	E			3.00 BSC	
Exposed Pad Length	D2		0.00	–	2.40
Contact Width	b		0.25	0.30	0.35
Contact Length	L		0.20	0.30	0.55
Contact-to-Exposed Pad	K		0.20	–	–

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-062B

APPENDIX A: REVISION HISTORY

Revision C (February 2008)

The following is the list of modifications.

1. Updated **Section 9.0 "Packaging Information"**.

Revision B (January 2005)

The following is the list of modifications.

1. Corrected the incorrect part number options shown on the Product Identification System page and changed the "standard" output voltage and reset voltage combinations.
2. Added Appendix A: Revision History.

Revision A (September 2003)

- Original data sheet release.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X-	X	X	X	X	XX	XX
TC1301	Type A/B	V_{OUT1}	V_{OUT2}	Reset Voltage	Temp Range	Package	Tube or Tape & Reel

Standard Configurations (V_{OUT1}, V_{OUT2}, Reset Voltage)

Device: TC1301A: Dual LDO with microcontroller RESET function and single shutdown input.
TC1301B: Dual LDO with microcontroller RESET function and dual shutdown inputs.

Standard Configurations: *

	V_{OUT1}/V_{OUT2}/Reset	Configuration Code
TC1301A	3.3 / 3.0 / 2.63	ADA
	3.3 / 1.8 / 2.63	APA
	3.0 / 2.8 / 2.63	DFA
	3.0 / 1.8 / 2.63	DPA
	2.8 / 3.0 / 2.63	FDA
	2.8 / 2.6 / 2.63	FHA
	1.8 / 2.8 / 2.32	PFC
	1.5 / 2.8 / 2.32	SFC
	2.85 / 1.85 / 2.63	UWA
TC1301B	3.3 / 3.0 / 2.63	ADA
	3.3 / 1.8 / 2.63	APA
	3.0 / 2.8 / 2.63	DFA
	3.0 / 1.8 / 2.63	DPA
	2.8 / 3.0 / 2.63	FDA
	2.8 / 2.6 / 2.63	FHA
	2.7 / 2.8 / 2.5	GFD
	2.7 / 3.0 / 2.50	GDD
	2.85 / 1.85 / 2.63	UWA

* Contact Factory for Alternate Output Voltage and Reset Voltage Configurations.

Temperature Range: V = -40°C to +125°C

Package:
MF = Dual Flat, No Lead (3x3 mm body), 8-lead
UA = Plastic Micro Small Outline (MSOP), 8-lead

Tube or Tape and Reel:
Blank = Tube
TR = Tape and Reel

Examples:

a) TC1301A-ADAVUA: 3.3, 3.0, 2.63, MSOP pkg.
b) TC1301A-APAVMFTR: 3.3 , 1.8, 2.63, 8LD DFN pkg. Tape and Reel
c) TC1301A-DFAVUATR: 3.0, 2.8 , 2.63, MSOP pkg. Tape and Reel
d) TC1301A-DPAVMF: 3.0, 1.8 , 2.63, 8LD DFN pkg.
e) TC1301A-FDAVMF: 2.8, 3.0, 2.63, 8LD DFN pkg.
f) TC1301A-FHAVMF: 2.8, 2.6, 2.63, DFN pkg.
g) TC1301A-PFCVUA: 1.8, 2.8, 2.32, MSOP pkg.
h) TC1301A-SFCVMFTR: 1.5, 2.8, 2.32, DFN pkg. Tape and Reel
i) TC1301A-UWAVUATR: 2.85, 1.85, 2.63, MSOP pkg. Tape and Reel

a) TC1301B-ADAVMF: 3.3, 3.0, 2.63, 8LD DFN pkg.
b) TC1301B-APAVMFTR: 3.3, 1.8, 2.63, 8LD DFN pkg. Tape and Reel
c) TC1301B-DFAVUA: 3.0, 2.8, 2.63, MSOP pkg.
d) TC1301B-DPAVUATR: 3.0, 1.8 ,2.63, MSOP pkg. Tape and Reel
e) TC1301B-FDAVMF: 2.8 ,3.0, 2.63, 8LD DFN pkg.
f) TC1301B-FHAVMFTR: 2.8, 2.6 ,2.63, 8LD DFN pkg. Tape and Reel
g) TC1301B-GDDVUA: 2.7, 3.0, 2.50, MSOP pkg.
h) TC1301B-GFDVMF: 2.7, 2.8, 2.5, 8LD DFN pkg.
i) TC1301B-UWAVUATR: 2.85, 1.85, 2.63, MSOP pkg. Tape and Reel

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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