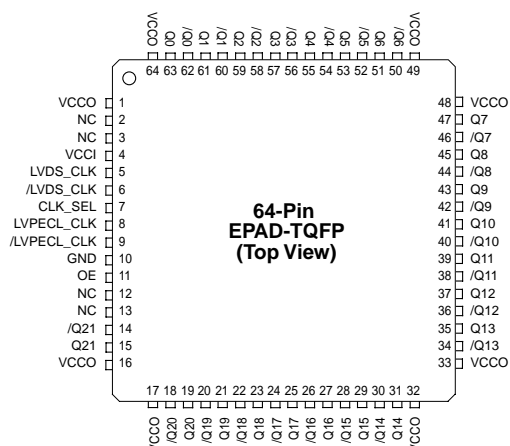


## PACKAGE/ORDERING INFORMATION

**64-Pin EPAD-TQFP (H64-1)**Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89825UHI	H64-1	Industrial	SY89825UHI	Sn-Pb
SY89825UHITR <sup>(2)</sup>	H64-1	Industrial	<b>SY89825UHI</b>	<b>SN-PB</b>
SY89825UHY <sup>(3)</sup>	H64-1	Industrial	SY89825UHY with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89825UHYTR <sup>(2,3)</sup>	H64-1	Industrial	SY89825UHY with Pb-Free bar-line indicator	Pb-Free Matte-Sn

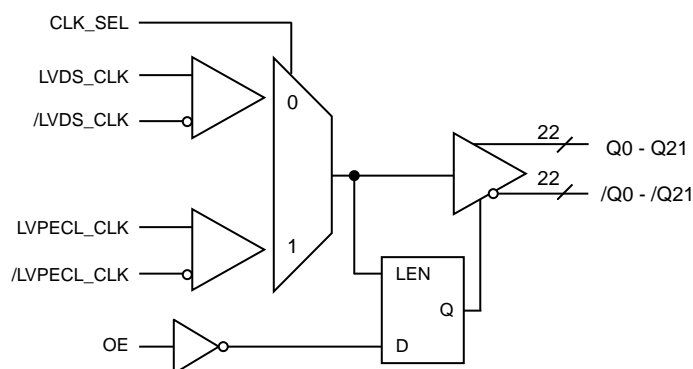
**Notes:**

- Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC electricals only.
- Tape and Reel.
- Pb-Free package recommended for new designs.

## PIN NAMES

Pin	Function
LVDS_CLK, /LVDS_CLK	Differential LVDS Inputs (Internal 100Ω termination included)
LVPECL_CLK, /LVPECL_CLK	Differential LVPECL Inputs.
CLK_SEL	Input CLK Select (LVTTTL)
OE	Output Enable (LVTTTL)
$Q_0 - Q_{21}$ , $/Q_0 - /Q_{21}$	Differential LVPECL Outputs. Terminate with 50Ω to $V_{CC}-2V$
GND	Ground
$V_{CCI}$	Power Supply. Connect to $V_{CC}$ on PCB. $V_{CCI}$ and $V_{CCO}$ are not internally connected
$V_{CCO}$	Power Supply for Output Buffer. Connect to $V_{CCI}$ on PCB. $V_{CCI}$ and $V_{CCO}$ are not internally connected

## LOGIC SYMBOL



## TRUTH TABLE

OE <sup>(1)</sup>	CLK_SEL	Q <sub>0</sub> – Q <sub>21</sub>	/Q <sub>0</sub> – /Q <sub>21</sub>
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	LVDS_CLK	/LVDS_CLK
1	1	LVPECL_CLK	/LVPECL_CLK

## SIGNAL GROUPS

Signal	I/O	Level
LVDS_CLK, /LVDS_CLK	Input	LVDS
Q <sub>0</sub> – Q <sub>21</sub> , /Q <sub>0</sub> – /Q <sub>21</sub>	Output	LVPECL
LVPECL_CLK, /LVPECL_CLK	Input	LVPECL
CLK_SEL, OE	Input	LVC MOS/LVTTL

## NOTE:

1. The OE (output enable) signal is synchronized with the low level of the LVDS\_CLK and LVPECL\_CLK signal.

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Value	Unit	
V <sub>CCI</sub> / V <sub>CCO</sub>	V <sub>CC</sub> Pin Potential to Ground Pin	–0.5 to +4.0	V	
V <sub>IN</sub>	Input Voltage	–0.5 to V <sub>CCI</sub>	V	
I <sub>OUT</sub>	DC Output Current	–50	mA	
T <sub>store</sub>	Storage Temperature	–65 to +150	°C	
θ <sub>JA</sub>	Package Thermal Resistance (Junction-to-Ambient) <u>With</u> exposed pad soldered to GND	– Still-Air (multi-layer PCB)	23	°C/W
		– 200lfpm (multi-layer PCB)	18	°C/W
		– 500lfpm (multi-layer PCB)	15	°C/W
	Exposed pad <u>not</u> soldered to GND	– Still-Air (multi-layer PCB)	44	°C/W
		– 200lfpm (multi-layer PCB)	36	°C/W
		– 500lfpm (multi-layer PCB)	30	°C/W
θ <sub>JC</sub>	Package Thermal Resistance (Junction-to-Case)	4.3	°C/W	

## NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**DC ELECTRICAL CHARACTERISTICS****Power Supply**

Symbol	Parameter	T <sub>A</sub> = -40°C			T <sub>A</sub> = +25°C			T <sub>A</sub> = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V <sub>CCI</sub> , V <sub>CCO</sub>	Power Supply <sup>(1)</sup>	2.37	—	3.6	2.37	—	3.8	2.37	—	3.6	V
I <sub>CC</sub>	Total Supply Current <sup>(2)</sup>	—	100	150	—	100	150	—	100	150	mA

**Notes:**

- V<sub>CCI</sub> and V<sub>CCO</sub> must be connected together on the PCB such that they remain at the same potential. V<sub>CCI</sub> and V<sub>CCO</sub> are not internally connected on the die.
- No load. Outputs floating.

**LVDS Input (V<sub>CC</sub> = 2.37V to 3.6V, GND = 0V)**

Symbol	Parameter	T <sub>A</sub> = -40°C			T <sub>A</sub> = +25°C			T <sub>A</sub> = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V <sub>IN</sub>	Input Voltage Range	0	—	2.4	0	—	2.4	0	—	2.4	V
V <sub>ID</sub>	Differential Input Swing	100	—	—	100	—	—	100	—	—	mV
I <sub>IL</sub>	Input Low Current <sup>(1)</sup>	-1.25	—	—	-1.25	—	—	-1.25	—	—	mA
R <sub>IN</sub>	LVDS Differential Input Resistance (LVDS_CLK to /LVDS_CLK)	80	100	120	80	100	120	80	100	120	Ω

**Note:**

- For I<sub>IL</sub>, both LVDS inputs are grounded.

**LVPECL Input/Output (V<sub>CC</sub> = 2.37V to 3.6V, GND = 0V)**

Symbol	Parameter	T <sub>A</sub> = -40°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>IH</sub>	Input HIGH Voltage (Single ended)	V <sub>CC</sub> - 1.165	V <sub>CC</sub> - 0.88	V <sub>CC</sub> - 1.165	V <sub>CC</sub> - 0.88	V <sub>CC</sub> - 1.165	V <sub>CC</sub> - 0.88	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> - 1.945	V <sub>CC</sub> - 1.625	V <sub>CC</sub> - 1.945	V <sub>CC</sub> - 1.625	V <sub>CC</sub> - 1.945	V <sub>CC</sub> - 1.625	V
V <sub>PP</sub>	Minimum Input Swing <sup>(1)</sup> LVPECL_CLK	600	—	600	—	600	—	mV
V <sub>CMR</sub>	Common Mode Range <sup>(2)</sup> LVPECL_CLK	-1.5	-0.4	-1.5	-0.4	-1.5	-0.4	V
V <sub>OH</sub>	Output HIGH Voltage <sup>(3)</sup>	V <sub>CCO</sub> - 1.085	V <sub>CCO</sub> - 0.880	V <sub>CCO</sub> - 1.025	V <sub>CCO</sub> - 0.880	V <sub>CCO</sub> - 1.025	V <sub>CCO</sub> - 0.880	V
V <sub>OL</sub>	Output LOW Voltage <sup>(3)</sup>	V <sub>CCO</sub> - 1.830	V <sub>CCO</sub> - 1.555	V <sub>CCO</sub> - 1.810	V <sub>CCO</sub> - 1.620	V <sub>CCO</sub> - 1.810	V <sub>CCO</sub> - 1.620	V
I <sub>IH</sub>	Input HIGH Current	—	150	—	150	—	150	μA
I <sub>IL</sub>	Input LOW Current	0.5	—	0.5	—	0.5	—	μA

**Notes:**

- The V<sub>PP</sub> (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay.
- V<sub>CMR</sub> is defined as the range within which the V<sub>IH</sub> level may vary, with the device still meeting the propagation delay specification. The numbers in the table are referenced to V<sub>CCI</sub>. The V<sub>IL</sub> level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V<sub>PP</sub> (min.). The lower end of the CMR range varies 1:1 with V<sub>CCI</sub>. The V<sub>CMR</sub> (min) will be fixed at 3.3V - |V<sub>CMR</sub> (min)|.
- Outputs loaded with 50Ω to V<sub>CC</sub> -2V.

**LVC MOS/LVTTL Control Inputs (OE, CLK\_SEL) (V<sub>CC</sub> = 2.37V to 3.6V, GND = 0V)**

Symbol	Parameter	T <sub>A</sub> = -40°C			T <sub>A</sub> = +25°C			T <sub>A</sub> = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V <sub>IH</sub>	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V
V <sub>IL</sub>	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V
I <sub>IH</sub>	Input HIGH Current	+20	—	-250	+20	—	-250	+20	—	-250	μA
I <sub>IL</sub>	Input LOW Current	—	—	-600	—	—	-600	—	—	-600	μA

**AC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>** $V_{CC} = 2.37V$  to  $3.6V$ ,  $GND = 0V$ 

Symbol	Parameter	$T_A = -40^{\circ}C$			$T_A = +25^{\circ}C$			$T_A = +85^{\circ}C$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
$f_{MAX}$	Max Toggle Frequency <sup>(2)</sup>	2	—	—	2	—	—	2	—	—	GHz
$t_{PHL}$ $t_{PLH}$	Propagation Delay (Differential) <sup>(3)</sup> LVPECL IN LVDS IN	0.600 0.800	— —	1.2 1.4	0.600 0.800	0.900 1.1	1.2 1.4	0.600 0.800	— —	1.2 1.4	ns
$t_{SKEW}$	Within-Device Skew <sup>(4)</sup>	—	—	35	—	20	35	—	—	35	ps
	Part-to-Part Skew <sup>(5)</sup>	—	100	200	—	100	200	—	100	200	ps
$t_{S(OE)}$	OE Set-Up Time <sup>(6)</sup>	1.0	—	—	1.0	—	—	1.0	—	—	ns
$t_{H(OE)}$	OE Hold Time <sup>(6)</sup>	0.5	—	—	0.5	—	—	0.5	—	—	ns
$t_{JITTER}$	Random Jitter <sup>(7)</sup>	—	—	1	—	—	1	—	—	1	ps <sub>(RMS)</sub>
	Cycle-to-Cycle Jitter <sup>(8)</sup>	—	—	1	—	—	1	—	—	1	ps <sub>(RMS)</sub>
	Total Jitter <sup>(9)</sup>	—	—	10	—	—	10	—	—	10	ps <sub>(PP)</sub>
$t_r$ $t_f$	Output Rise/Fall Time (20% – 80%)	300	—	600	300	450	600	300	—	600	ps
$t_{(switchover)}$	Input Switchover CLK_SEL-to-valid output	—	—	1.2	—	—	1.2	—	—	1.2	ns

**Notes:**

- Outputs loaded with  $50\Omega$  to  $V_{CC} - 2V$ . Airflow  $\geq 300$ lfpm.
- $f_{MAX}$  is defined as the maximum toggle frequency measured. Measured with a 750mV input signal, all loading with  $50\Omega$  to  $V_{CC} - 2V$ .
- Differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.
- The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature.
- The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature. Part-to-part skew is the total skew difference; pin-to-pin skew + part-to-part skew.
- Set-up and hold time applies to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold time does not apply. OE set-up time is defined with respect to the rising edge of the clock. OE HIGH to LOW transition ensures outputs remain disabled during the next clock cycle. OE LOW to HIGH transition enables normal operation of the next input clock.
- Random jitter is measured using K28.7 pattern, measured at  $\leq f_{MAX}$ .
- Cycle-to-cycle definition: the variation of periods between adjacent cycles,  $T_n - T_{n-1}$  where T is the time between rising edges of the output signal.
- Total jitter definition: with an ideal clock input of frequency  $\leq f_{MAX}$ , no more than one output edge in  $10^{20}$  output edges will deviate by more than the specified peak-to-peak jitter value.

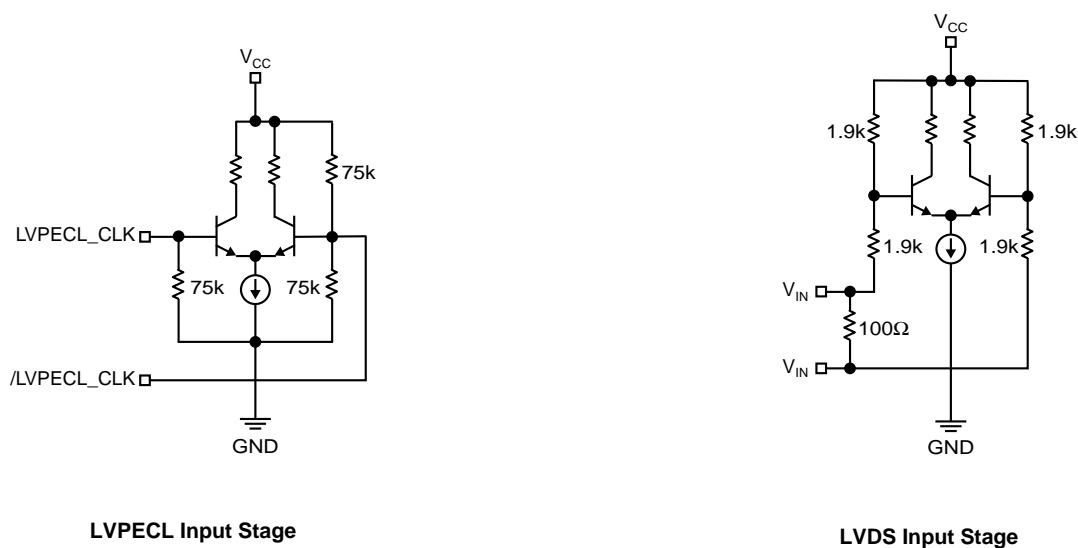
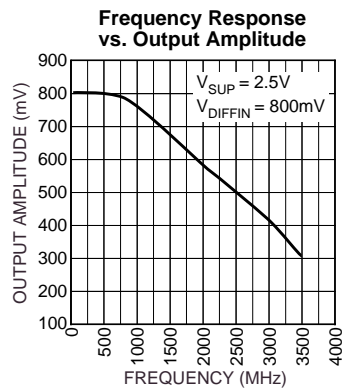
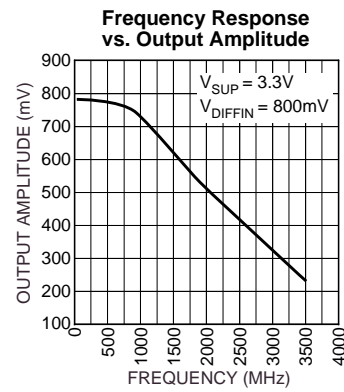
**LVDS/LVPECL INPUTS**

Figure 1. Simplified LVPECL &amp; LVDS Input Stage

TYPICAL CHARACTERISTICS



Frequency Response  
vs. Output Amplitude @2.5V



Frequency Response  
vs. Output Amplitude @3.3V

## LVPECL TERMINATION RECOMMENDATIONS

### Output Considerations

Be sure to properly terminate all outputs as shown below, or equivalent. For AC coupled applications, be sure to include a pull

down resistor at the output of each driver. The emitter follower outputs requires a DC current path to GND. Unused outputs can be left floating with minimal impact on skew and jitter.

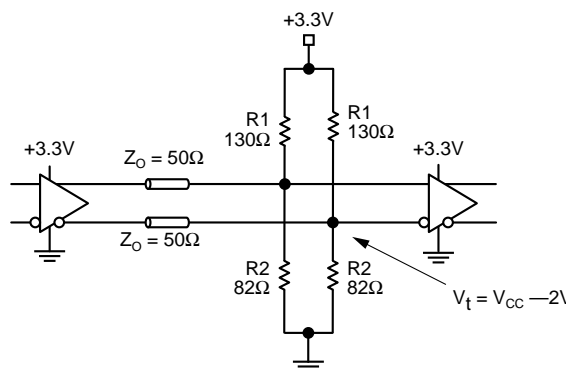


Figure 1. Parallel Termination-Thevenin Equivalent

#### Notes:

- For +2.5V systems:  
R1 = 250Ω  
R2 = 62.5Ω

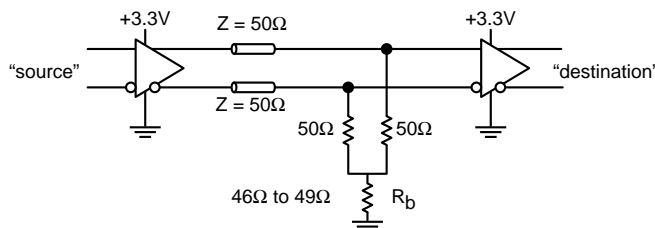
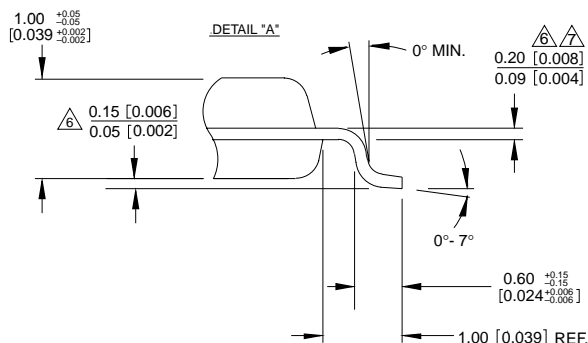
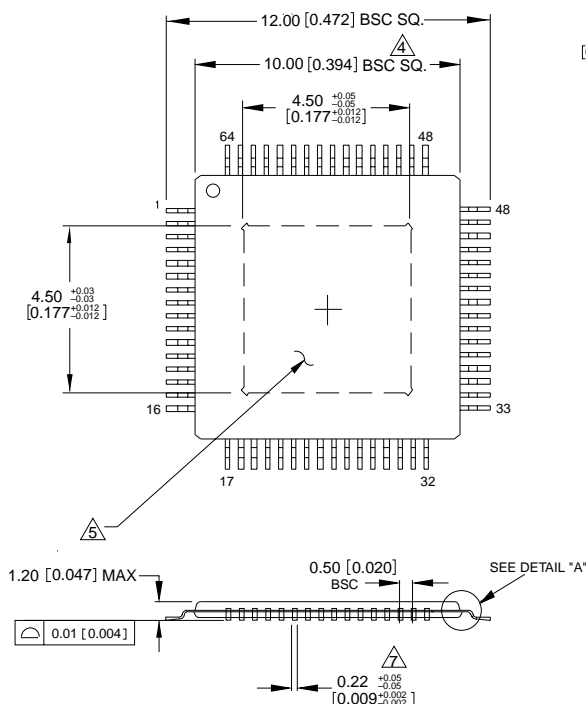


Figure 2. Three-Resistor "Y-Termination"

#### Notes:

- Power-saving alternative to Thevenin termination.
- Place termination resistors as close to destination inputs as possible.
- $R_b$  resistor sets the DC bias voltage equal to  $V_t$ . For +3.3V systems  $R_b = 46\Omega$  to  $49\Omega$ .
- Precision, low-cost 3-Resistor networks are available from resistor manufacturers such as Thin Film Technology ([www.thinfilm.com](http://www.thinfilm.com)).

**64-PIN EPAD-TQFP (DIE UP) (H64-1)****NOTES:**

1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. EXPOSED PAD: Cu WITH Sn/Pb PLATING.
4. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
5. DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.
6. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX  
MIN
7. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 03

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