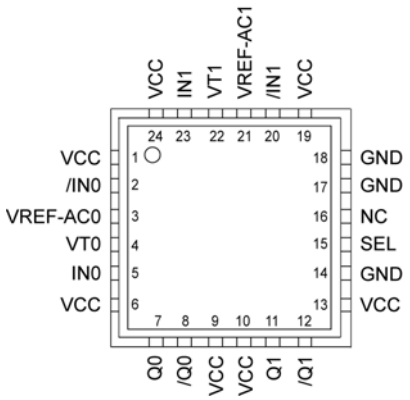
Ordering Information [1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89474UMG	QFN-24	Industrial	474U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89474UMGTR [2]	QFN-24	Industrial	474U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at TA = 25°C, DC Electricals Only.
2. Tape and Reel.

Pin Configuration



24-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
5, 2, 23, 20	IN0, /IN0 IN1, /IN1	Differential Inputs: These input pairs are the differential signal inputs to the device. They accept AC- or DC-coupled signals as small as 100mV (200mVpp). Note that these inputs will default to an undetermined state if left open. Each pin of a pair internally terminates to a VT pin through 50Ω. Please refer to the "Input Interface Applications" section for more details.
3, 21	VREF-AC0, VREF-AC1	Reference Voltage: These outputs bias to V_{CC} -1.2V. They are used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the corresponding VT pin. Bypass with 0.01µF low ESR capacitor to VCC. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. Please refer to the "Input Interface Applications" section for more details.
4, 22	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT0 and VT1 pins provide a center-tap to a termination network for maximum interface flexibility. Please refer to the "Input Interface Applications" section for more details.
1, 6, 9, 10, 13, 19, 24	VCC	Positive Power Supply: Connect to +2.5V ±5% power supply. Bypass with 0.1µF//0.01µF low ESR capacitors as close to VCC pins as possible.
7, 8 11, 12	Q0, /Q0 Q1, /Q1	Differential Outputs: These differential LVDS output pairs are a logic function of the IN0, IN1, and SEL inputs. Please refer to the truth table below for details. Unused output pairs should be terminated with 100Ω across the outputs.
15	SEL	This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. $V_{TH} = V_{CC}/2$. Please refer to the "Timing Diagram" section for more details.
14, 17, 18	GND, Exposed Pad	Ground: Ground pins and exposed pad must be connected to the same ground plane.

Truth Table

INPUTS					OUTPUTS	
IN0	**/IN0**	**IN1**	**/IN1**	**SEL**	**Q**	**/Q**
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... -0.5V to +4.0V
Input Voltage (V_{IN}) ..... -0.5V to V_{CC}
Termination Current
  IN, /IN ..... ±50mA
  V_T ..... ±100mA
V_{REF-AC} Current
  Source/sink Current on V_{REF-AC} ..... ±2mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... -65°C to 150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
QFN (θ_{JA})
  Still-Air ..... 50°C/W
QFN (Ψ_{JB})
  Junction-to-Board ..... 30°C/W

DC Electrical Characteristics[4]

T_A = –40°C to +85°C; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No load, max V_{CC}.		80	110	mA
R_{IN}	Input Resistance (IN-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input High Voltage (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH}-0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a. Note 5.	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN-/IN|	See Figure 1b.	0.2			V
V_{T_IN}	IN-to-V_T (IN, /IN)				1. 28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}-1.3	V_{CC}-1.2	V_{CC}-1.1	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and Ψ_{JB} values are determined for a 4-layer board in still air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IN} (max) is specified when V_T is floating.

LVDS Outputs DC Electrical Characteristics[6]

V_{CC} = 2.5V ±5%; T_A = -40°C to + 85°C; R_L = 100Ω across output pair; unless otherwise stated

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a	250	325		mV
V_{DIFF_OUT}	Differential Output Voltage Swing Q, /Q	See Figure 1b	500	650		mV
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in V_{OS} between complementary output states		-50		+50	mV

LVTTL/CMOS DC Electrical Characteristics[6]

V_{CC} = 2.5V ±5%; T_A = -40°C to + 85°C; unless otherwise stated

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		-125		30	µA
I_{IL}	Input LOW Current		-300			µA

Notes:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[7]

V_{CC} = 2.5V ±5%; T_A = -40°C to + 85°C; R_L = 100Ω across output pair; unless otherwise stated

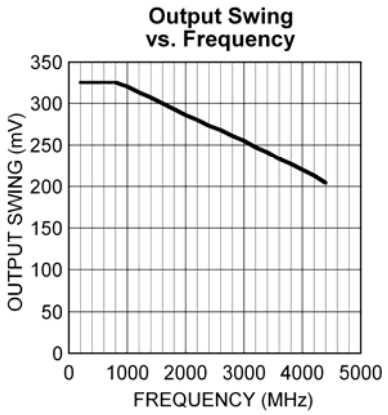
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	2.5	3.2		Gbps
		V_{OUT} ≥ 200mV Clock	2.5	4		GHz
t_{pd}	Differential Propagation Delay In-to-Q		220	320	470	ps
	SEL-to-Q	$V_{TH} = V_{CC}/2$	200	350	550	ps
t_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			158		fs/°C
t_{SKEW}	Output-to-Output Skew	Note 8		5	20	ps
	Part-to-Part Skew	Note 9			200	ps
t_{Jitter}	Data Random Jitter	Note 10			1	ps_{RMS}
	Deterministic Jitter	Note 11			10	ps_{PP}
	Clock Cycle-to-cycle Jitter	Note 12			1	ps_{RMS}
	Total Jitter	Note 13			10	ps_{PP}
	Crosstalk-Induced Jitter	Note 14			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing.	30		150	ps

Notes:

7. High-frequency AC-parameters are guaranteed by design and characterization.
8. Output-to-output skew is measured between two different outputs under identical transitions.
9. Part-to-part skew is defined for two parts with identical power supply voltages, at the same temperature, and with no skew of the edges at the respective inputs.
10. Random Jitter is measured with a K28.7 pattern, measured at ≤ f_{MAX}.
11. Deterministic Jitter is measured with both K28.5 and 2^{23}-1 PRBS pattern, measured at ≤ f_{MAX}.
12. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
13. Total Jitter definition: With an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
14. Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

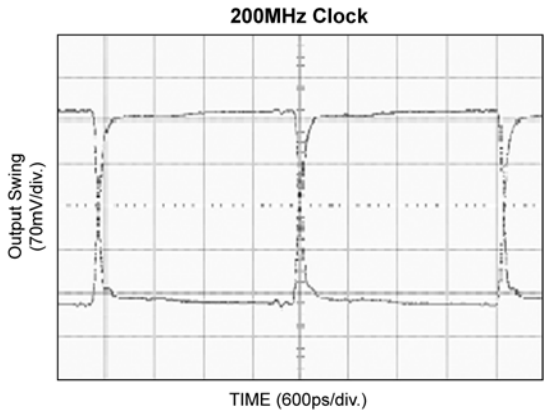
Typical Operating Characteristics

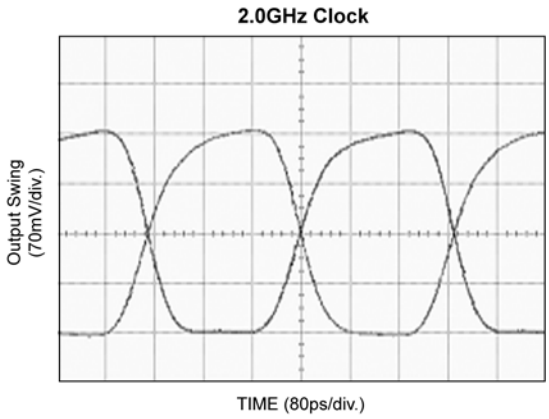
V_{CC} = 2.5V ±5%; V_{IN} > 400mV; T_A = 25°C, R_L = 100Ω across output pair; unless otherwise stated.

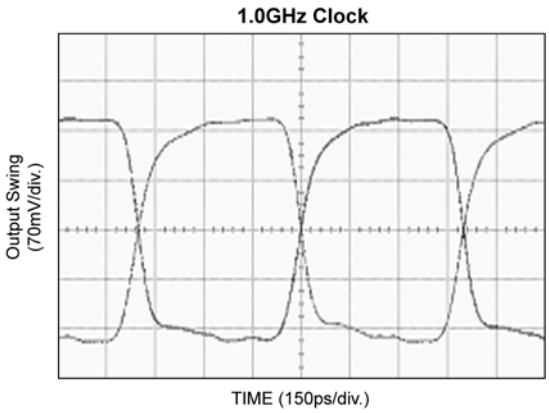


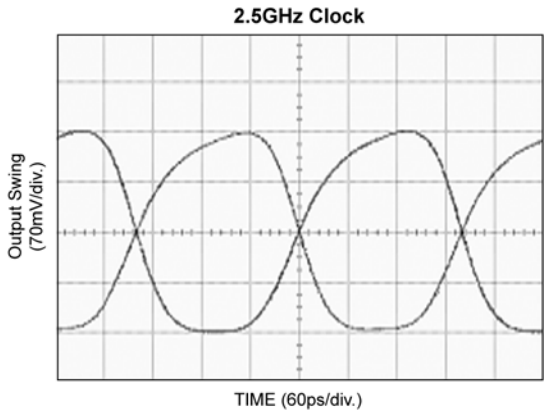
Functional Characteristics

V_{CC} = 2.5V ±5%; V_{IN} > 400mV; T_A = 25°C, R_L = 100Ω across output pair; unless otherwise stated.









Single-Ended and Differential Swings

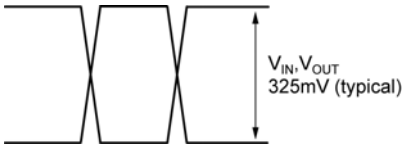


Figure 1a. Single-Ended Voltage Swing

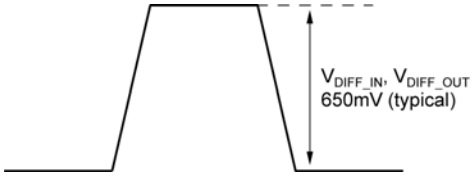
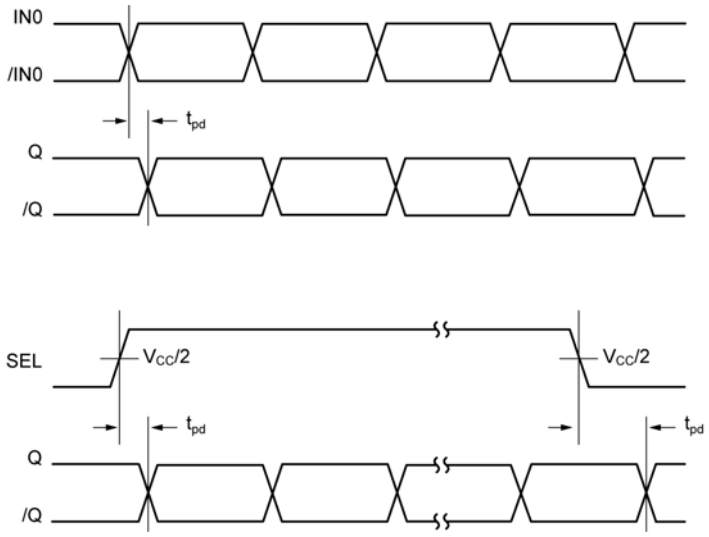


Figure 1b. Differential Voltage Swing

Timing Diagrams



Input and Output Stages

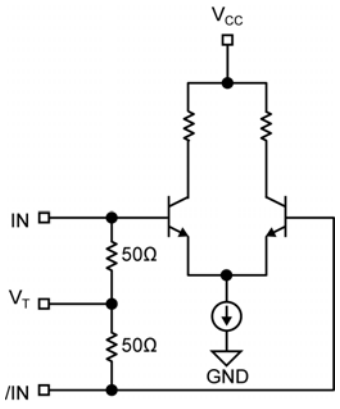


Figure 2. Simplified Differential Input Stage

Input Interface Applications

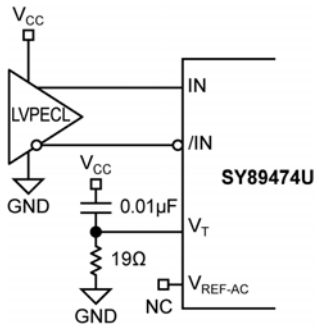


Figure 3a. LVPECL Interface (DC-Coupled)

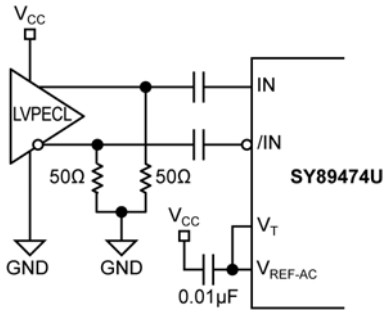
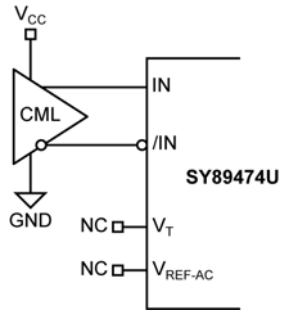


Figure 3b. LVPECL Interface (AC-Coupled)



Option: may connect V_T to V_{CC}.

Figure 3c. CML Interface (DC-Coupled)

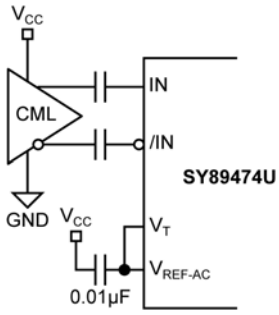


Figure 3d. CML Interface (AC-Coupled)

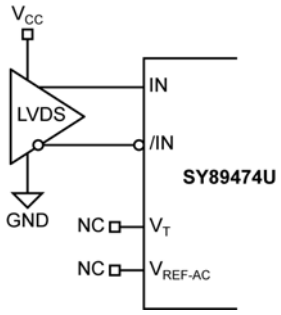


Figure 3e. LVDS Interface (DC-Coupled)

LVDS Output Interface Applications

LVDS specifies a small swing of 325mV typical, on a nominal 1.20V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

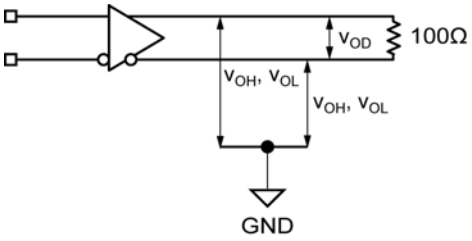


Figure 4a. LVDS Differential Measurement

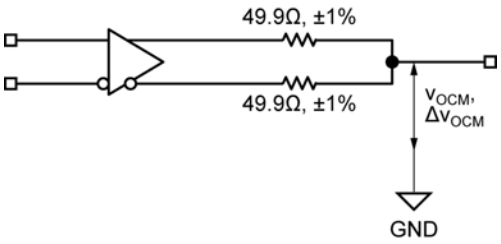
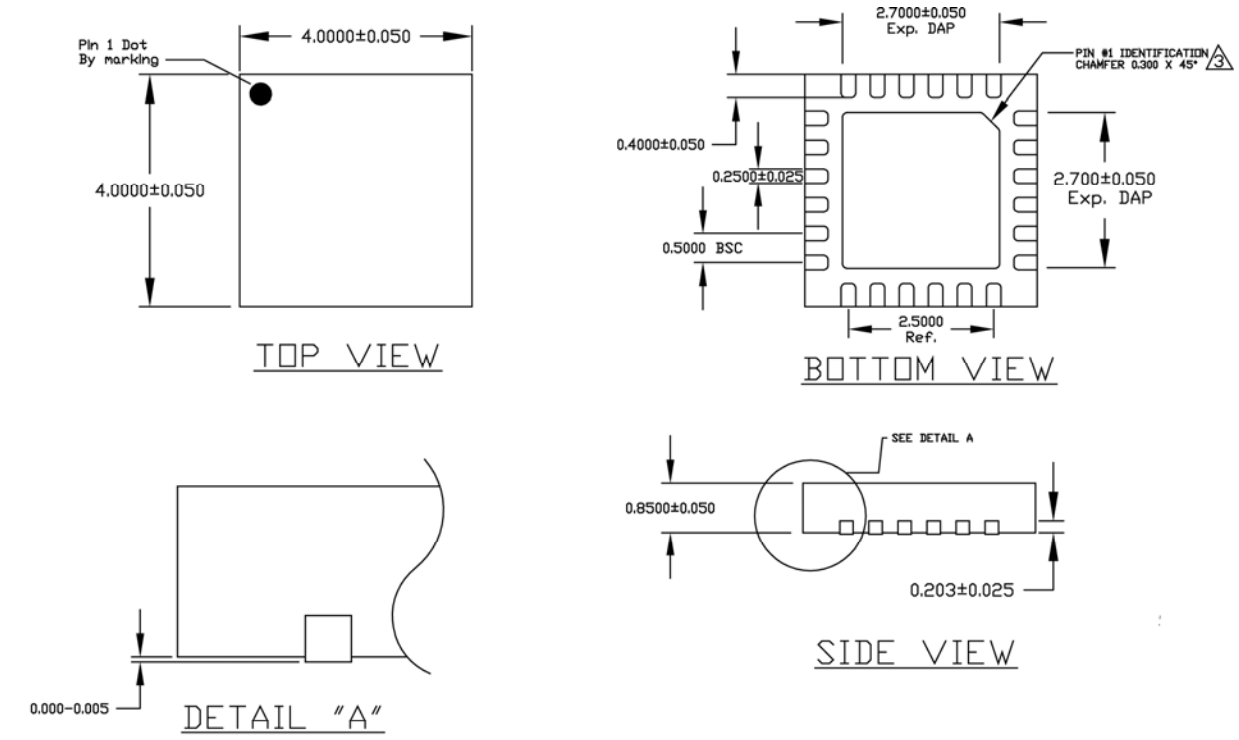


Figure 4b. LVDS Mode Measurement

Related Product and Support Information

Part Number	Function	Data Sheet Link
SY89473U	Precision LVPECL 2:1 Multiplexer with 1:2 Fanout and Internal Termination	www.micrel.com/product-info/products/sy89473u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Package Information



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS (mm).
2. THE PIN#1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
3. CHAMFER STYLE PIN 1 IDENTIFIER ON BOTTOM SIDE

24-Pin (4mm x 4mm) QFN

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