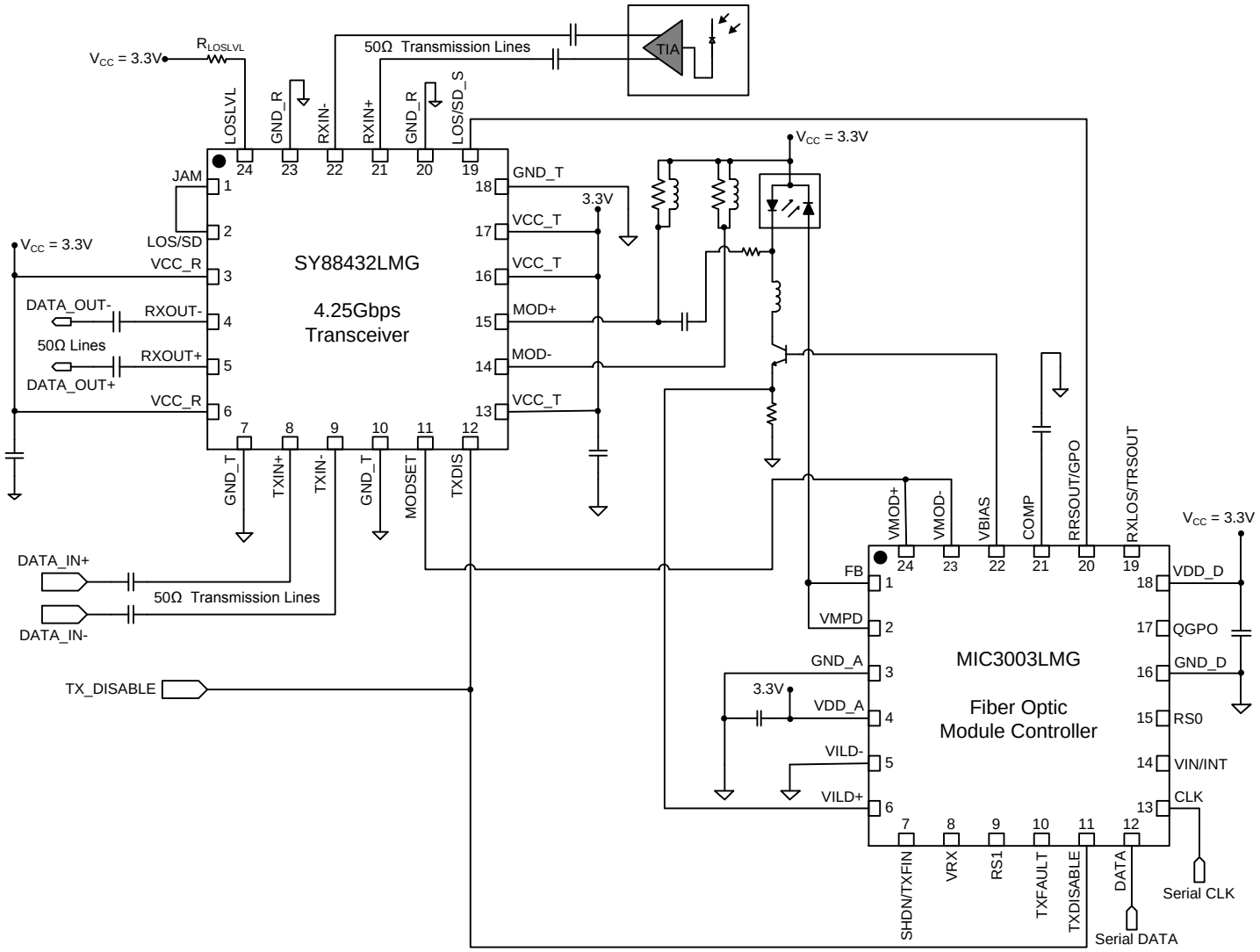
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88432LMG	4mm x 4mm QFN-24	Industrial	88432L with Pb-Free bar line indicator	NiPdAu Pb-Free
SY88432LMG TR[1]	4mm x 4mm QFN-24	Industrial	88432L with Pb-Free bar line indicator	NiPdAu Pb-Free

Note:

1. TR = Tape and Reel (1kpcs)

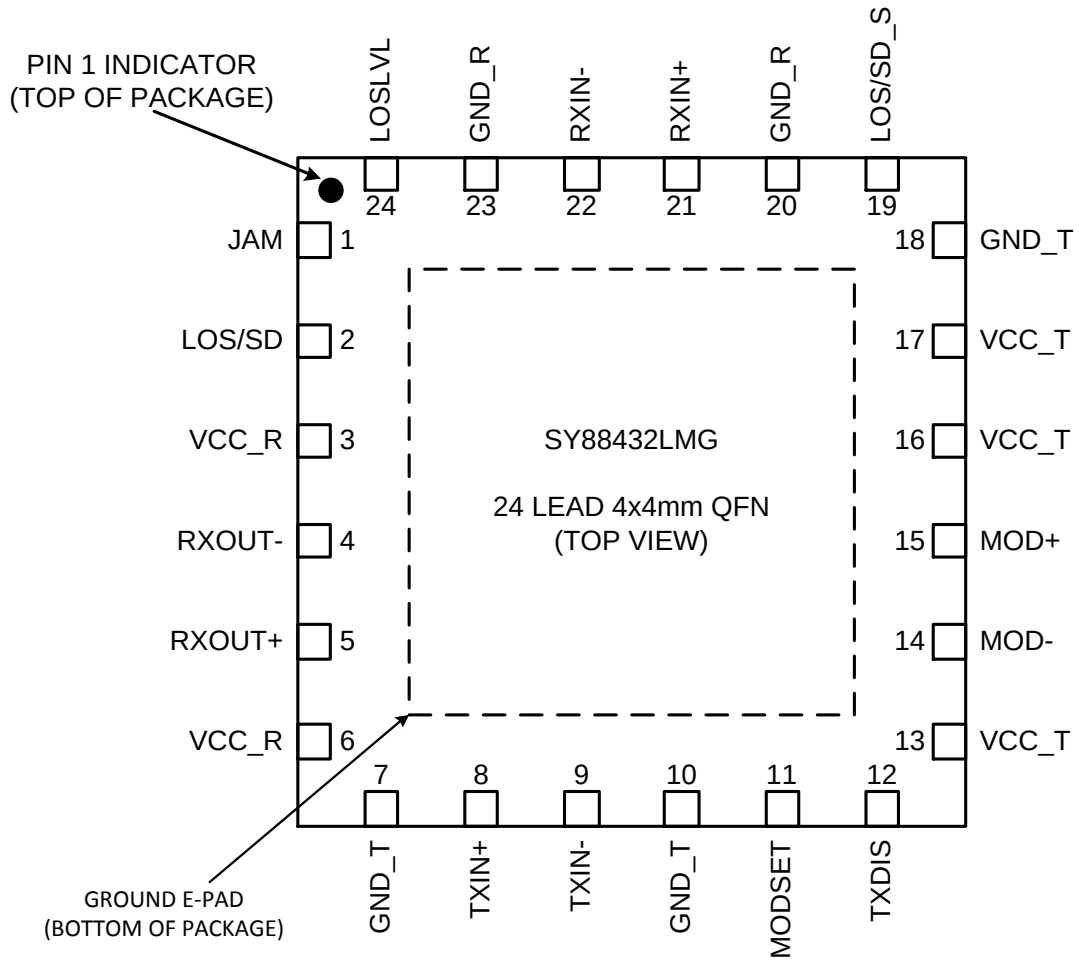
Typical Application: Single-ended AC-coupled Configuration[2]



Note:

2. For reference only. Please refer to the Evaluation or Reference board schematics for more complete information.

Pin Configuration



NOTE:
E-PAD MUST BE CONNECTED TO
THE PCB GROUND PLANE USING
THE CORRECT VIA ARRAY

24 Lead QFN (4x4mm)

Pin Description

Pin Number	Pin Name	Type	Pin Function
1	JAM	Logic Level Input	Active Low TTL Input. Determines whether the post amp output is enabled or disabled. **Operation when LOS/SD = LOS is selected:** HIGH = Post amp output is Disabled. LOW = Post amp output is Enabled. **Operation when LOS/SD = SD is selected:** HIGH = Post amp output is Enabled. LOW = Post amp output is Disabled. Default: Internally pulled-up with 25kΩ. Can be shorted to LOS/SD (pin 2) to create a SQUELCH function.
2	LOS/SD	Logic Level Output	Loss-of-Signal / Signal-Detect. Determined by LOS/SD_S pin setting. **Operation when LOS is selected by LOS/SD_S pin setting:** HIGH = when the data input amplitude falls below the threshold set by LOSLVL. LOW = when the data input amplitude rises above the threshold set by LOSLVL. **Operation when SD is selected by LOS/SD_S pin setting:** HIGH = when the data input amplitude rises above the threshold set by LOSLVL. LOW = when the data input amplitude falls below the threshold set by LOSLVL.
4, 5	RXOUT-, RXOUT+	CML Outputs	Receiver Differential CML Outputs. Unused output should be terminated 50Ω to V_{CC}.
8, 9	TXIN+, TXIN-	CML Inputs	Transmitter Differential Data CML Inputs. Data input signals for the laser diode driver section internally terminated with 50Ω to V_{CC}.
11	MODSET	Analog Input	Modulation Current Setting and Control. The modulation current is set by applying a voltage between 0V and 1.2V to this pin. 5kΩ input impedance.
12	TXDIS	Logic Level Input	Transmit Disable. Control signal that enables or disables the laser diode driver outputs. HIGH = Transmitter outputs are set as follows: MOD+ = HIGH; MOD- = LOW LOW = Transmitter outputs Enabled. Default: Internally pulled down with a 75kΩ resistor.
14, 15	MOD-, MOD+	Transmitter Output	Modulation current output. Must be AC coupled to the laser.
19	LOS/SD_S	Logic Level Input	LOS/SD Output Select. Determines whether LOS or SD is selected. HIGH = SD is selected on the LOS/SD output and JAM logic operation is: when JAM = High → Post amplifier output is Enabled. LOW = LOS is selected on the LOS/SD output and JAM logic operation is: when JAM = Low → Post amplifier output is Enabled. Default: Internally pulled up with a 25kΩ resistor.
21, 22	RXIN+, RXIN-	Receiver Inputs	Receiver Differential Data Inputs. Each input is internally terminated to V_{REF} (V_{CC} – 1.3V) with 50Ω resistors. Inputs are AC-coupled.
24	LOSLVL	Analog Input	Loss-of-Signal Level Set. A resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which LOS/SD will be asserted.
3, 6	VCC_R	Receiver Positive Supply Rail	Receiver Voltage Supply. Bypass with a 0.1uF || 0.01uF low ESR capacitor as close to VCC_R pin as possible.

Pin Description

Pin Number	Pin Name	Type	Pin Function
7, 10, 18	GND_T	Transmitter Ground	Transmitter Ground. Connect to the PCB ground plane.
13, 16, 17	VCC_T	Transmitter Positive Supply Rail	Transmitter Voltage Supply. Bypass with a 0.1uF || 0.01uF low ESR capacitor as close to VCC_T pin as possible.
20, 23, e-pad	GND_R	Receiver Ground	Receiver Ground. Connect to the PCB ground plane. The e-pad must be connected to the PCB ground plane using a via array to transfer the heat from the package to the PCB ground plane.

Transmitter - Laser Diode Driver Truth Table

TXIN+	TXIN-	TXDIS	MOD+ [3]	MOD-	Laser Output [4]
L	H	L	H	L	L
H	L	L	L	H	H
X	X	H	H	L	L

Notes:

3. $I_{MOD} \leq I_{MOD\_OFF}$ when MOD+ is HIGH.
4. Assuming that Laser is tied to MOD+

Absolute Maximum Ratings[5]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
TTL Control Input Voltage (V_{IN}) ..... 0V to V_{CC}
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[6]

Supply Voltage (V_{CC}) ..... +3.00V to +3.60V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[7]
Still-Air (θ_{JA}) ..... 50°C/W
Junction-to-Board (θ_{JB}) ..... 30.5°C/W

Notes:

5. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
6. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
7. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB using the recommended via pattern and size. Assumes a 4 layer PCB and still air.

Transceiver DC Electrical Characteristics[8]

V_{CC} = 3.3V ±10%, T_A = -40°C to +85°C. Typical values are V_{CC} = 3.3V, T_A = 25°C, I_{MOD} = 60mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	Without Modulation & Bias currents		90	130	mA
V_{IL}	TXDIS, LOS/SD_S, JAM, Input Low		-0.3		0.8	V
V_{IH}	TXDIS, LOS/SD_S, JAM, Input High		2		V_{CC} + 0.3	V
I_{IH}	TXDIS, LOS/SD_S, JAM, Input High	V_{IN} = V_{CC} ; Note 10			20	µA
I_{IL}	TXDIS, LOS/SD_S, JAM, Input Low	V_{IN} = 0.5V; Note 10	-0.3			mA
V_{OH}	LOS Output High Level	V_{CC} = 3.3V. IOH < 50uA	2			V
V_{OL}	LOS Output Low Level	I_{OL} = 2mA			0.5	V
I_{OH}	LOS Output Leakage	V_{OH} = V_{CC}			100	µA

Laser Diode Driver Electrical Characteristics[8]

V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C. Typical values are V_{CC} = 3.3V, T_A = 25°C, I_{MOD} = 60mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Data Rate	NRZ Data	0.155		4.25	Gbps
$R_{iIN(TXIN)}$	Input resistance (TXIN+,TXIN-)		45	50	55	Ω
$R_{iIN(IMOD\_SET)}$	Input resistance (MODSET)			5		kΩ
V_{ID}	Differential Input Voltage Swing	CML inputs	300		800	mV_{PP}
V_{MODSET}	Voltage Range on MODSET Pin		0		1.2	V
V_{MOD}	Voltage (MOD+, MOD-)	Note 9	V_{CC} – 1.5		V_{CC}	V
I_{MOD}	Modulation Current	AC-Coupled	10		60	mA
I_{MOD_OFF}	Modulation OFF current	MOD+ current when the device is disabled (TXDIS = HIGH)			200	µA
J_{TOTAL}	Total Jitter	@ 4.25Gbps data rate		20		ps
T_{PWDIS}	Pulse-Width Distortion	I_{MOD} range 10mA – 60mA		20		ps
t_r, t_f	Output Rise/Fall Times (20% to 80%)	15Ω Load		65	80	ps

Notes:

8. Specification for packaged product only.
9. MOD+ and MOD- are current outputs. This defines the voltage range the user must guarantee these pins remain within for proper operation.
10. TXDIS signal has an internal 75kΩ pull down resistor. For TXDIS: I_{IH} = 150µA Maximum. I_{IL} = 0.5µA Minimum.

Limiting Amplifier Electrical Characteristics

V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C. Typical values at V_{CC} = 3.3V, T_A = 25°C; R_{Load} = 50Ω to V_{CC};

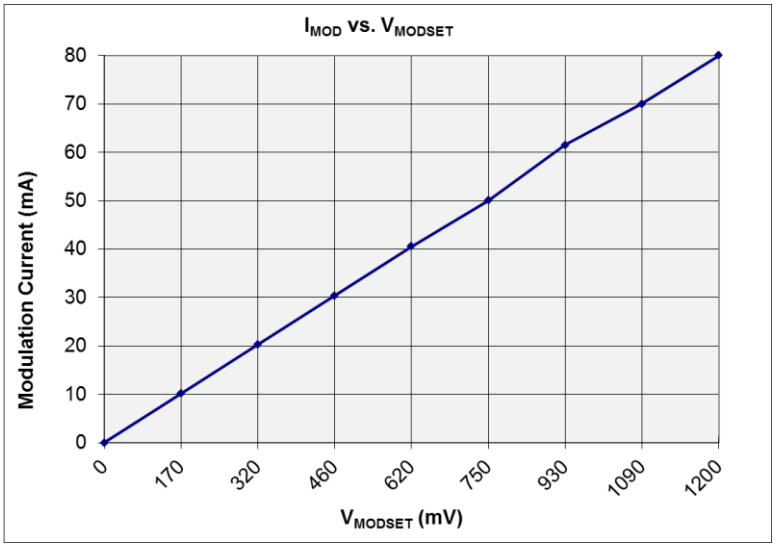
Symbol	Parameter	Condition	Min	Typ	Max	Units
LOSLVL	LOSLVL Voltage		Vcc-1.3		V_{CC}	V
V_{OH}	RXOUT+, RXOUT- High Voltage		V_{CC}-0.020	V_{CC}-0.005	V_{CC}	V
V_{OL}	RXOUT+, RXOUT- Low Voltage		V_{CC}-0.475	V_{CC}-0.400	V_{CC}-0.350	V
Z_0	Single-Ended Output Impedance		40	50	60	Ω
Z_I	Single-Ended Input Impedance		40	50	60	Ω
t_r, t_f	Output Rise/Fall Time (20% to 80%)	Note 1		60	120	ps
t_{JITTER}	Deterministic Random	Note 2 Note 3		10 1		ps ps
$V_{ID\_2.5G}$	Differential Input Voltage Swing	Note 7. See Fig #1.	10		1800	mV_{PP}
$V_{ID\_3.2G}$	Differential Input Voltage Swing	Note 7. See Fig #1.	10		1800	mV_{PP}
$V_{ID\_4.25G}$	Differential Input Voltage Swing	Note 7. See Fig #1.	15		1800	mV_{PP}
V_{OD}	Differential Output Voltage Swing	Note 1	600	800	950	mV_{PP}
T_{OFF}	LOS Release Time	Note 6		2	10	µs
T_{ON}	LOS Assert Time	Note 6		2	10	µs
LOS_{AL}	Low LOS Assert Level	R_{LOSLVL} = 15kΩ, Note 4		8		mV_{PP}
LOS_{DL}	Low LOS De-assert Level	R_{LOSLVL} = 15kΩ, Note 4		13		mV_{PP}
HYS_L	Low LOS Hysteresis	R_{LOSLVL} = 15kΩ, Note 5	2	3.5	6	dB
LOS_{AM}	Medium LOS Assert Level	R_{LOSLVL} = 5kΩ, Note 4	12	15		mV_{PP}
LOS_{DM}	Medium LOS De-assert Level	R_{LOSLVL} = 5kΩ, Note 4		24	33	mV_{PP}
HYS_M	Medium LOS Hysteresis	R_{LOSLVL} = 5kΩ, Note 5	2	3.7	6	dB
LOS_{AH}	High LOS Assert Level	R_{LOSLVL} = 100Ω, Note 4	34	40		mV_{PP}
LOS_{DH}	High LOS De-assert Level	R_{LOSLVL} = 100Ω, Note 4		65	83	mV_{PP}
HYS_H	High LOS Hysteresis	R_{LOSLVL} = 100Ω, Note 5	2	4	6	dB
$A_{V(Diff)}$	Differential Voltage Gain			38		dB
S_{21}	Single-Ended Small-Signal Gain		26	32		dB

Notes:

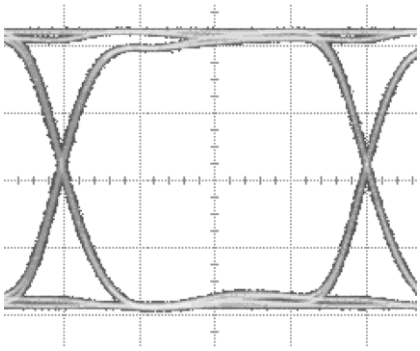
1. Amplifier in limiting mode. Input is a 200MHz square wave.
2. Deterministic jitter measured using 4.25Gbps K28.5 pattern, V_{ID} = 60mV_{PP}.
3. Random jitter measured using 4.25Gbps K28.7 pattern, V_{ID} = 60mV_{PP}.
4. See “Typical Operating Characteristics” for a graph showing how to choose a particular R_{LOSLVL} for a particular LOS assert and its associated de-assert amplitude.
5. This specification defines electrical hysteresis as 20log (LOS De-Assert/LOS Assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending upon the level of received optical power and ROSA characteristics. Based on that ratio, the optical hysteresis corresponding to the electrical hysteresis range 2dB-6 dB, shown in the AC characteristics table, will be 1dB-3dB Optical Hysteresis.
6. In real world applications, the LOS Release/Assert time can be strongly influenced by the RC time constant of the AC-coupling cap and the 50Ω input termination. To keep this time low, use a decoupling cap with the lowest value that is allowed by the data rate and the number of consecutive identical bits in the application (typical values are in the range of 0.001µF to 1.0µF).
7. Input swing required to achieve 30% mask margin with PRBS 2^7 pattern at specified data rate. See Fig #1 for differential and single-ended swing definitions.

Transmitter – Laser Diode Driver Typical Operating Characteristics

Driver Typical Functional Characteristics
V_{CC} = 3.3V ± 10%; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C; R_{Load} = 25Ω to V_{CC};

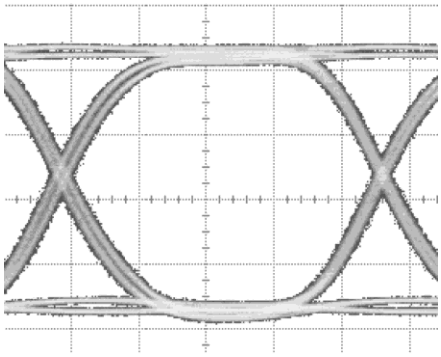


Electrical Eye Diagram @ 2.5Gbps PRBS 2^{23}, 25Ω load, 40 mA Modulation



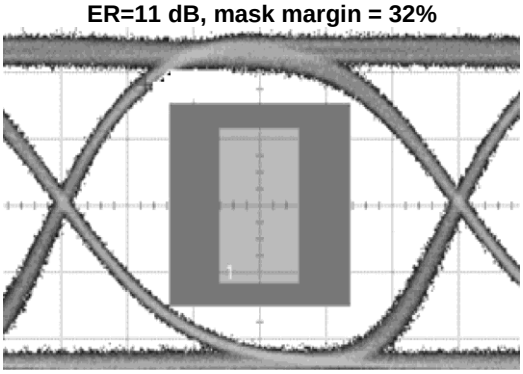
TIME (100 ps /div)

Electrical Eye Diagram @ 4.25Gbps PRBS 2^{23}, 25Ω load, 40 mA Modulation



TIME (50 ps /div)

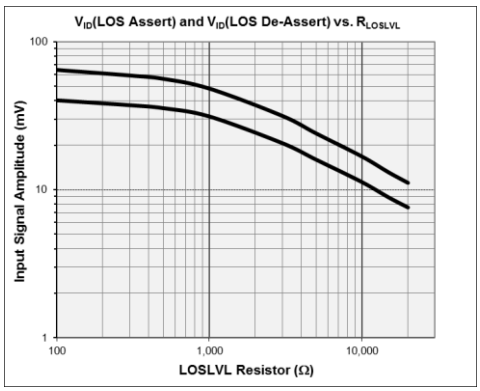
Optical Eye Diagram @ 2.5Gbps (STM16/OC48) ER=11 dB, mask margin = 32%

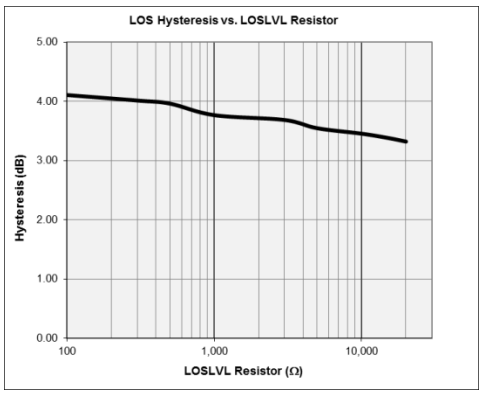


TIME (67 ps/div)

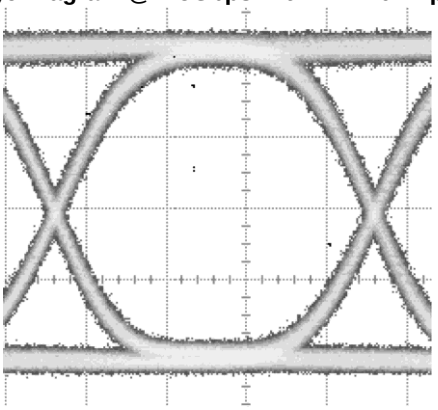
Receiver – Limiting Post Amplifier Typical Operating Characteristics

V_{CC} = 3.3 ± 10%; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C; R_{Load} = 50Ω to V_{CC};



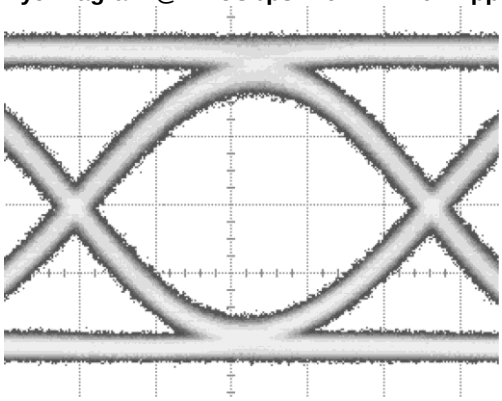


Eye Diagram @ 2.5Gbps with Vin=10mVpp



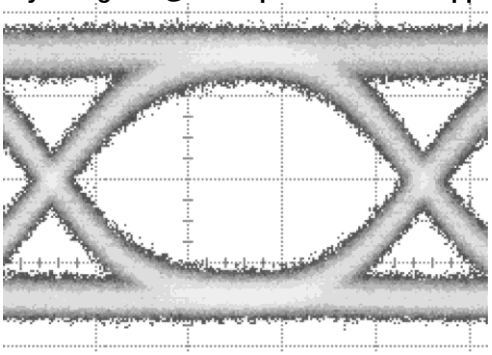
TIME (100 ps /div)

Eye Diagram @ 4.25Gbps with Vin=10mVpp



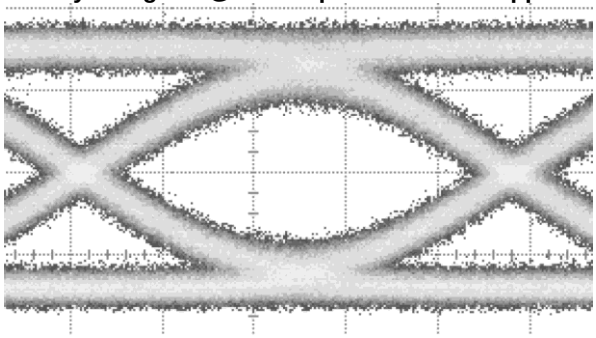
TIME (50 ps /div)

Eye Diagram @ 2.5Gbps with Vin=5mVpp



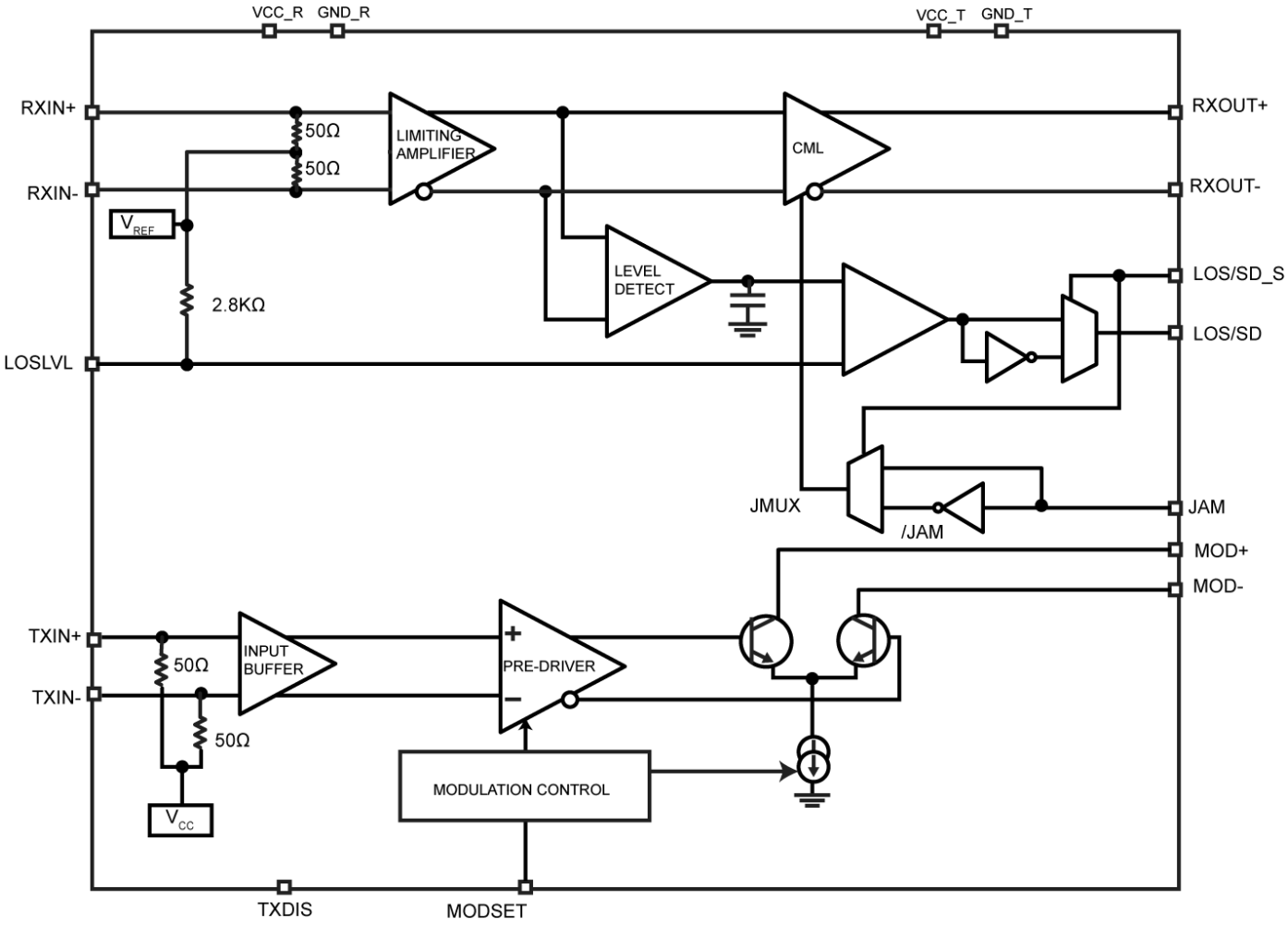
TIME (100 ps /div)

Eye Diagram @ 4.25Gbps with Vin=5mVpp



TIME (50 ps /div)

Transceiver Functional Block Diagram



Functional Description

Transmitter - Laser Diode Driver

The laser driver consists of three stages which include the input buffer stage, a pre-driver stage where the modulation current is set, and the output driver stage.

Input Buffer

The input stage is internally terminated to V_{CC} with 50Ω impedances. The input signals should be routed using 50Ω transmission lines and terminated with 50Ω impedances at the load.

Pre-Driver / Modulation Control

This stage is used to control the modulation current for the laser driver when an analog voltage between 0V to 1.2V is applied at the MODSET pin.

Output Driver

The output stage is an open-collector differential pair capable of driving modulation currents up to 60mA. It may be used single-ended or differentially. Specific care must be taken to ensure that outputs are terminated correctly for either mode of operation.

Figure 2 and 3 show input and output stages of the driver.

Receiver - Post Amplifier

The post amplifier detects and amplifies signals with data rates from 155Mbps and up to 4.25Gbps with amplitudes as low as $10mV_{PP}$.

To reduce the noise at the output of the post amplifier when the input signal is absent or lower than the minimum detectable level set by LOSLVL, a JAM pin is provided, which can be connected to LOS/SD output to turn off the output buffer when LOS is asserted or SD is de-asserted.

Input Amplifier/Buffer

Figure 4 shows a simplified schematic of the input stage. The high-sensitivity of the input amplifier allows signals as small as $10mV_{PP}$ to be detected and amplified. The input amplifier allows input signals as large as $1800mV_{PP}$.

Figure 1 shows the allowed input voltage swing. Small input signals below typically $12mV_{PP}$ are linearly amplified with a typical 38dB differential voltage gain. For input signals larger than $12mV_{PP}$, the output signal is limited to typically $800mV_{PP}$.

Output Buffer

The post amplifier CML output buffer is designed to drive 50Ω lines and is internally terminated with 50Ω to V_{CC}. Figure 5 shows a simplified schematic of the output stage which can be either AC-coupled (as shown) or DC-coupled.

Loss-of-Signal

The post amplifier generates a selectable chatter-free loss-of-signal (LOS) or signal detect (SD) open-collector TTL output as shown in Figure 6. LOS/SD is used to determine that the input amplitude is too small to be considered as a valid input.

When the LOS function is selected (LOS/SD_S=0), LOS/SD asserts high if the input amplitude falls below the threshold set by LOSLVL and de-asserts low otherwise.

If the SD function is selected (LOS/SD_S=1), LOS/SD asserts low if the input amplitude falls below the threshold set by LOSLVL and de-asserts high otherwise.

LOS/SD can be fed back to the JAM input to maintain output stability under a loss of signal condition. Jam de-asserts low the true output signal without removing the input signals.

Typically, 3dB LOS hysteresis is provided to prevent chattering.

Loss/Signal Detect Selection

A pin (LOS/SD_S) is provided to select between LOS (set to LOW) or SD (set to HIGH) function. It also controls the internal circuitry of JAM input to follow LOS/SD selection.

Loss-of-Signal-Level Set

A programmable LOS/SD level set pin (LOSLVL) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and LOSLVL sets the voltage at LOSLVL. This voltage ranges from V_{CC} to V_{CC} -1.3V. The external resistor creates a voltage divider between V_{CC} and V_{CC}-1.3V, as shown on Figure 7.

Hysteresis

The post amplifier provides typically 3.5dB LOS electrical hysteresis, which is defined as 20log ($VIN_{LOS\text{-}Assert}$ / $VIN_{LOS\text{-}De\text{-}Assert}$). Since the relationship between the voltage out of the ROSA to optical power at its input is linear, the optical hysteresis will be typically half of the electrical hysteresis reported in the datasheet, but in practice, the ratio between electrical and optical hysteresis is found to be within the range 1.5 to 1.8. Thus, 3.5dB electrical hysteresis will correspond to an optical hysteresis within the range 1.6dB to 2dB.

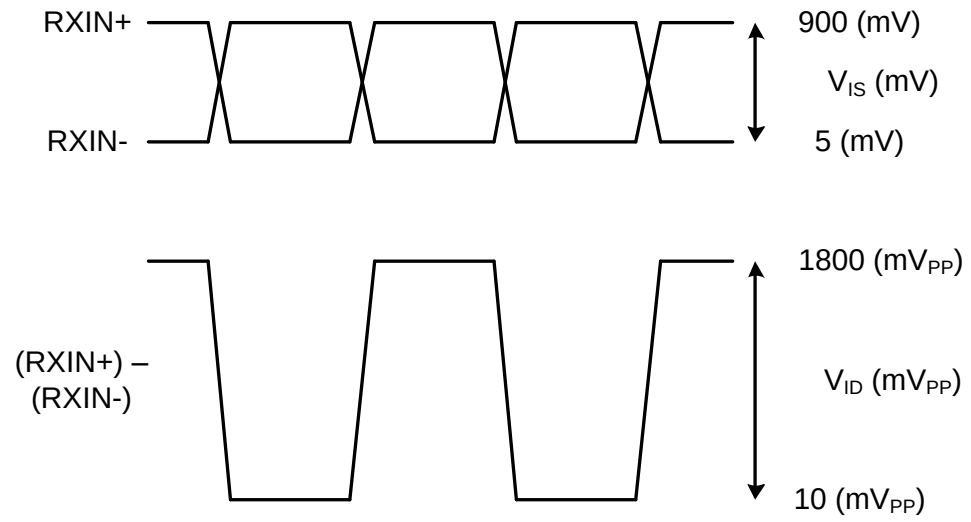


Figure 1. Transceiver V_{IS} and V_{ID} Definition

Input and Output Stages

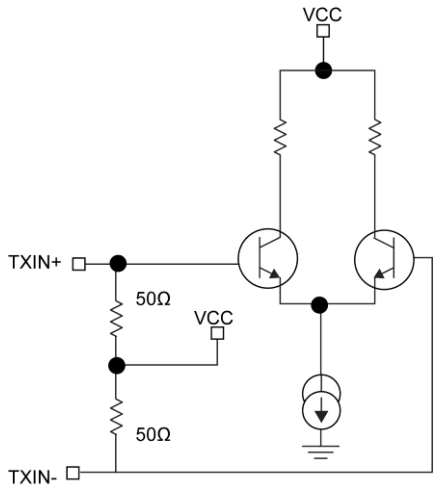


Figure 2. Laser Diode Driver Input Stage

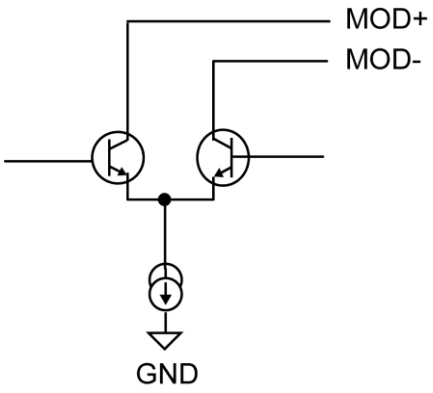


Figure 3. Simplified Laser Diode Driver Output Stage

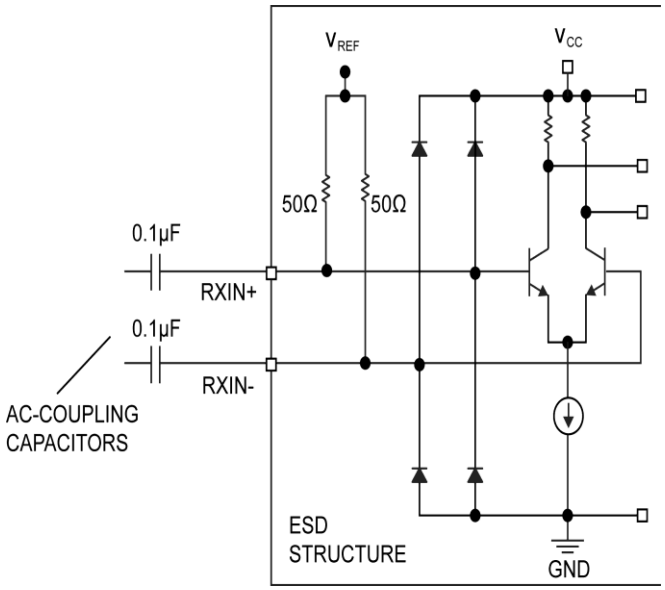


Figure 4. Receiver – Post Amplifier Input Structure

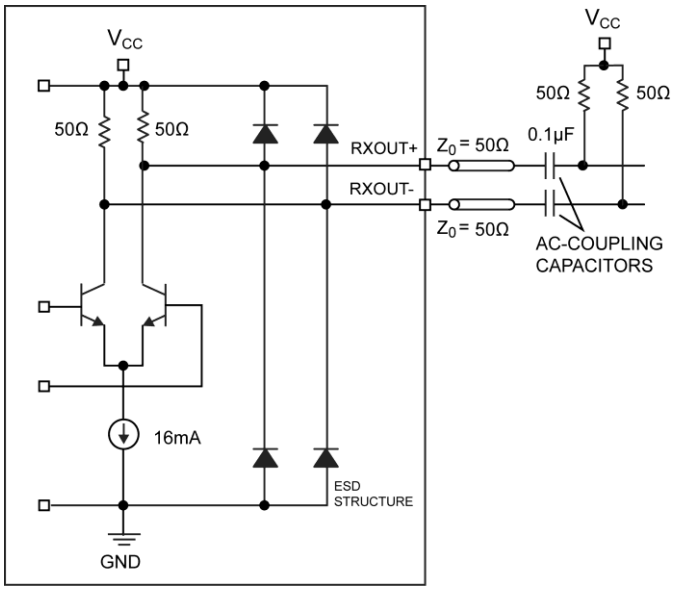


Figure 5. Receiver – Post Amplifier Output Structure

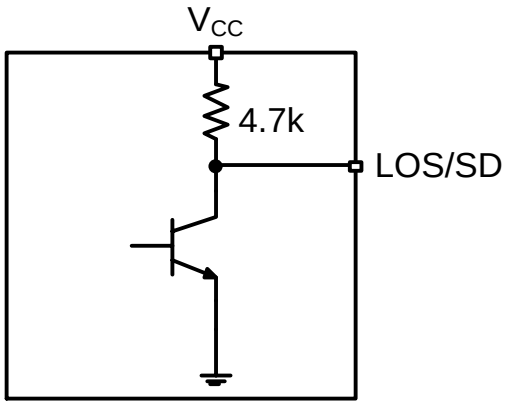


Figure 6. Receiver LOS/SD Output Structure

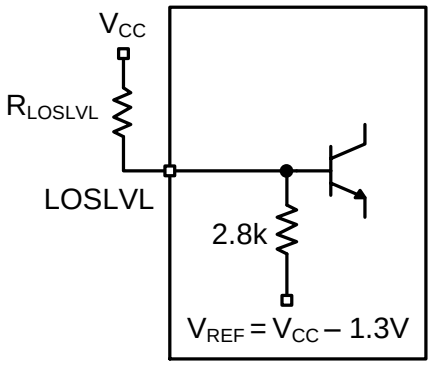


Figure 7. Receiver LOSLVL Setting Circuit

Note: Recommended value for R_{LOSLVL} is 15kΩ or less.

Application Hints

The typical applications drawing on the front page shows how to connect the driver to the laser in a single-ended configuration where the MOD- signal is disconnected from the laser anode and pulled up to V_{CC} with a resistor equal to the equivalent resistor of the load on MOD+, damping resistor plus the laser equivalent resistance.

Differential drive improves transition time and laser response. Driving the laser differentially will also minimize the cross talk with the rest of the circuitry on the board and especially the receiver.

Referring to Figure 8, the modulation current out of the driver is split between the pull-up network and the laser. If, for example, the total pull-up resistor is twice the sum of the damping resistor and laser equivalent series resistance, only two thirds (2/3) of the modulation current will be used by the laser.

To keep most of the modulation current going through the laser, it is necessary that the total pull-up resistors are high as possible. One solution consists of using a combination of resistor and inductor as shown in Figure 8 below. In this case, the headroom of the driver is VCC – R1 * αI_{mod}, where αI_{mod} is the portion of the modulation current that goes through the pull-up network.

The coupling capacitor creates a low-frequency cut-off in the circuit, and its value must be chosen to accommodate the lowest and the highest data rates. If the value of the cap is too high, it will degrade the performance at higher data rates. If its value is too small, it will not be able to hold a constant charge between the first bit and the last bit of a long string of identical bits in a low data rate application. Both cases lead to higher pattern-dependent jitter in the transmitter signal. 0.01-to-0.1μF is found to be good range for all applications from 155Mbps to 4.25Gbps

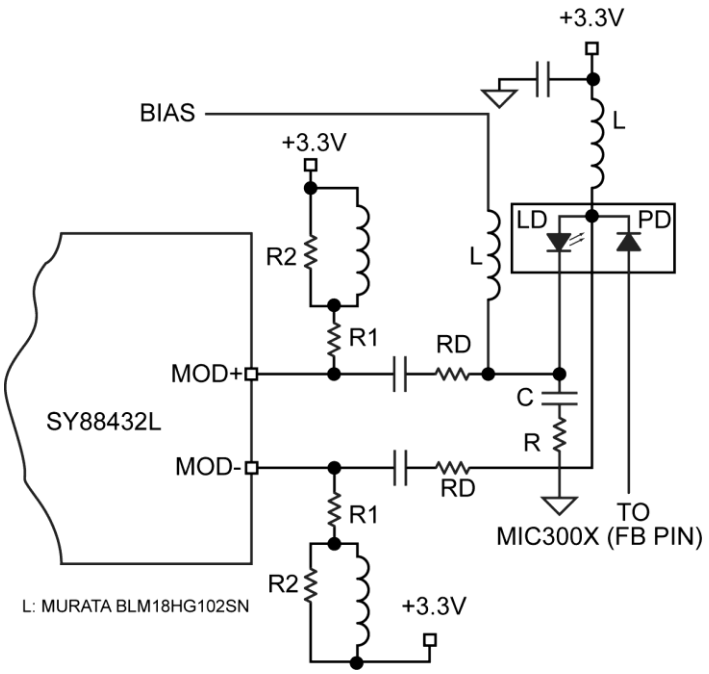
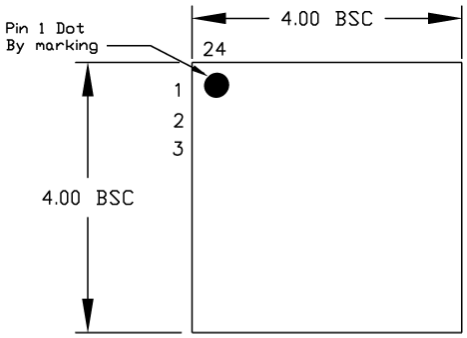
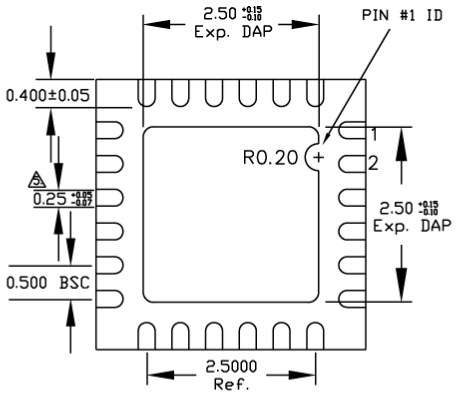


Figure 8. Transceiver Laser Driver Stage AC-coupled Differential Interface Network

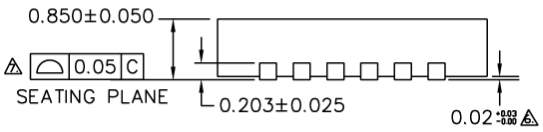
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

24 lead QFN (4 x 4 mm)

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