SPICE Device Model SUP/SUB75N06-08 Vishay Siliconix



Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static			•		
Gate Threshold Voltage	V _{GS(th)}	V_{DS} = V_{GS} , I_D = 250 μ A	3	3	V
On-State Drain Current ^a	I _{D(on)}	V_{DS} = 5 V, V_{GS} = 10 V	644		А
Drain-Source On-State Resistance ^a	r _{DS(on)}	V_{GS} = 10 V, I _D = 30 A	0.0072	0.007	Ω
		V_{GS} = 10 V, I _D = 30 A, T _J = 125°C	0.011		
		V_{GS} = 10 V, I _D = 30 A, T _J = 175°C	0.012		
Forward Transconductance ^a	g _{fs}	V_{DS} = 15 V, I _D = 30 A	75		S
Forward Voltage ^a	V _{SD}	$I_{\rm S}$ = 75 A, $V_{\rm GS}$ = 0 V	0.92	1	V
Dynamic [♭]			-		
Input Capacitance	C _{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	4659	4800	pF
Output Capacitance	Coss		939	910	
Reverse Transfer Capacitance	C _{rss}		291	270	
Total Gate Charge ^c	Qg	$V_{\rm DS}$ = 30 V, $V_{\rm GS}$ = 10 V, $I_{\rm D}$ = 75 A	83	85	nC
Gate-Source Charge ^c	Q _{gs}		28	28	
Gate-Drain Charge ^c	Q _{gd}		26	26	
Turn-On Delay Time ^c	t _{d(on)}	V_{DD} = 30 V, R_L = 0.47 Ω I_D \cong 75 A, V_{GEN} = 10 V, R_G = 2.5 Ω	30	20	ns
Rise Time ^c	tr		43	95	
Turn-Off Delay Time ^c	t _{d(off)}		54	65	
Fall Time ^c	t _f		67	20	
Reverse Recovery Time	t _{rr}	I _F = 75 A, di/dt = 100 A/μs	62	67	

Notes

a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing. c. Independent of operating temperature.



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T_C = 125°C

5°C

5

•

4

•

60

100

125

150

80

100

120

20

16

12

0

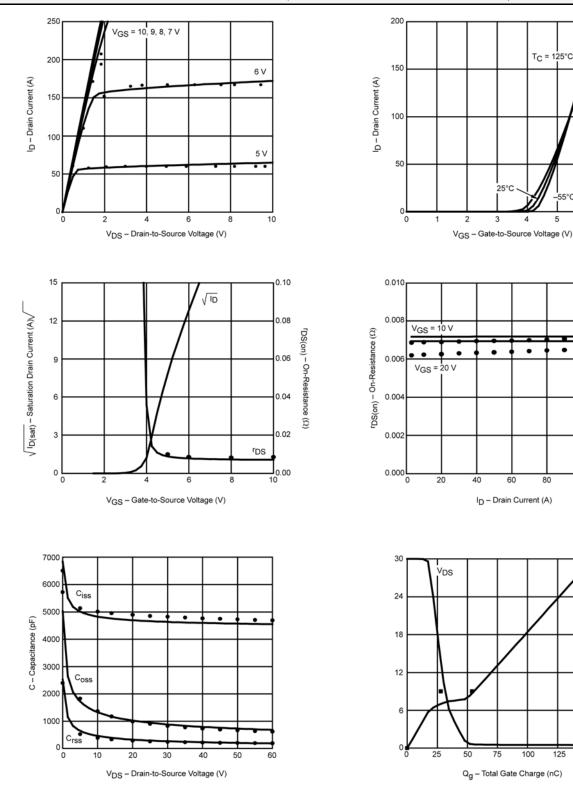
175

VGS

6

•

COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data

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Vishay

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