## SPICE Device Model SUP/SUB75N06-08 Vishay Siliconix



Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static			•		
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS}$ = $V_{GS}$ , $I_D$ = 250 $\mu$ A	3	3	V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS}$ = 5 V, $V_{GS}$ = 10 V	644		А
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS}$ = 10 V, I <sub>D</sub> = 30 A	0.0072	0.007	Ω
		$V_{GS}$ = 10 V, I <sub>D</sub> = 30 A, T <sub>J</sub> = 125°C	0.011		
		$V_{GS}$ = 10 V, I <sub>D</sub> = 30 A, T <sub>J</sub> = 175°C	0.012		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	$V_{DS}$ = 15 V, I <sub>D</sub> = 30 A	75		S
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	$I_{\rm S}$ = 75 A, $V_{\rm GS}$ = 0 V	0.92	1	V
Dynamic <sup>♭</sup>			-		
Input Capacitance	C <sub>iss</sub>	$V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1 MHz	4659	4800	pF
Output Capacitance	Coss		939	910	
Reverse Transfer Capacitance	C <sub>rss</sub>		291	270	
Total Gate Charge <sup>c</sup>	Qg	$V_{\rm DS}$ = 30 V, $V_{\rm GS}$ = 10 V, $I_{\rm D}$ = 75 A	83	85	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>		28	28	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>		26	26	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	$V_{DD}$ = 30 V, $R_L$ = 0.47 $\Omega$ I_D $\cong$ 75 A, $V_{GEN}$ = 10 V, $R_G$ = 2.5 $\Omega$	30	20	ns
Rise Time <sup>c</sup>	tr		43	95	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>		54	65	
Fall Time <sup>c</sup>	t <sub>f</sub>		67	20	
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 75 A, di/dt = 100 A/μs	62	67	

Notes

a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2%. b. Guaranteed by design, not subject to production testing. c. Independent of operating temperature.



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T<sub>C</sub> = 125°C

5°C

5

•

4

•

60

100

125

150

80

100

120

20

16

12

0

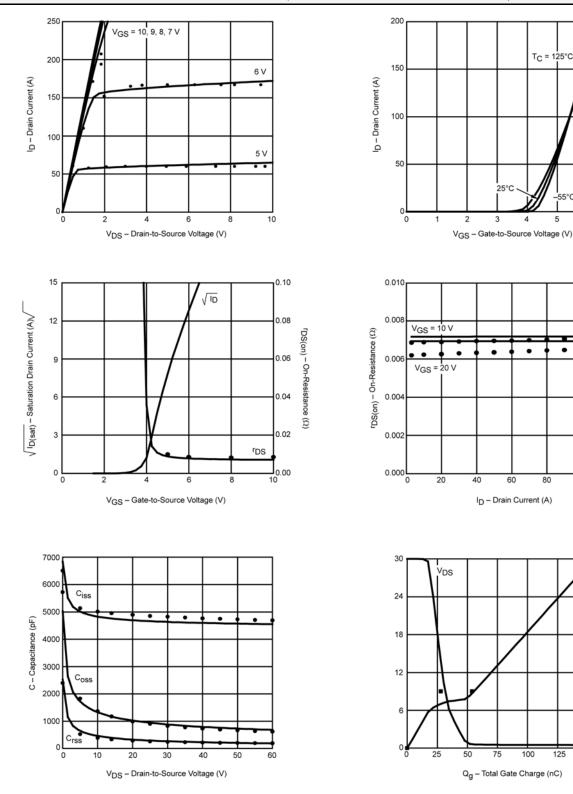
175

VGS

6

•

COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data

Document Number: 71866 S-71502-Rev. B, 06-Aug-07



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