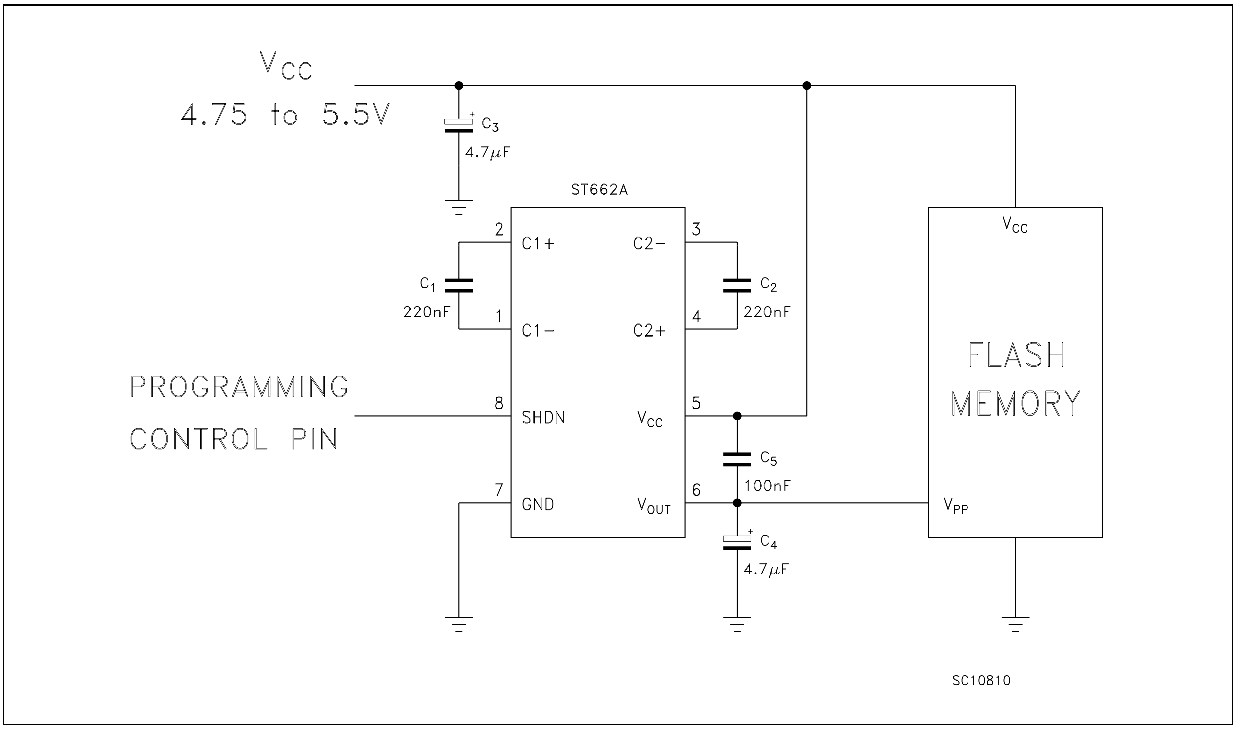
Contents

1 Application circuit

Figure 1. Typical application circuit



2 Pin configuration

Figure 2. Pin connections (top view)

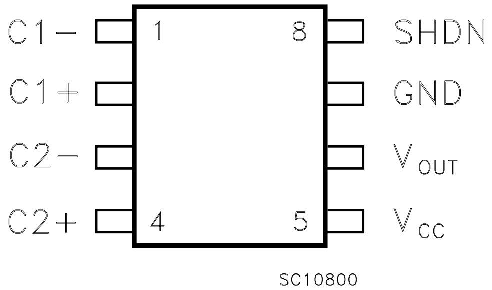


Table 2. Pin description

Pin n°	Symbol	Name and function
1	C1-	Negative terminal for the first charge pump capacitor
2	C1+	Positive terminal for the first charge pump capacitor
3	C2-	Negative terminal for the second charge pump capacitor
4	C2+	Positive terminal for the second charge pump capacitor
5	V_{CC}	Supply voltage
6	V_{OUT}	12 V output voltage $V_{OUT} = V_{CC}$ when in shutdown mode
7	GND	Ground
8	SHDN	Active high C-MOS logic level shutdown input. SHDN is internally pulled up to V_{CC}. Connect to GND for normal operation. In Shutdown mode the charge pumps are turned off and $V_{OUT} = V_{CC}$

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC input voltage to GND		-0.3 to 6	V
SHDN	Shutdown voltage		-0.3 to (V_{CC} + 0.3)	V
I_O	Output current continuous		50	A
P_D	Power dissipation		500	mW
T_{OP}	Operating ambient temperature range	AC series	0 to 70	°C
		AB series	-40 to 85	
T_{STG}	Storage temperature range		-40 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4. Thermal data

Symbol	Parameter	SO-8	Unit
R_{thJC}	Thermal resistance junction-case	20	°C/W

4 Electrical characteristics

Refer to the test circuits, V_{CC} = 4.5 V to 5.5 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise specified. Typical value are referred at T_A = 25 °C.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 0 to 20 mA	11.4	12	12.6	V
		I_O = 0 to 30 mA, V_{CC} = 4.75 to 5.5 V	11.4	12	12.6	
I_{Q1}	Quiescent current	NO LOAD, V_{SHDN} = 0		100	500	µA
I_{Q2}	Shutdown current	NO LOAD, $V_{SHDN} = V_{CC}$		1	10	µA
I_{SH}	Shutdown pin current	V_{SHDN} = 0, V_{CC} = 5V	-50	-12	-5	µA
		$V_{SHDN} = V_{CC}$ = 5V		0		µA
V_{IL}	Shutdown input low threshold				0.4	V
V_{IH}	Shutdown input high threshold		2.4			V
f_O	Oscillator frequency	V_{CC} = 5 V, I_O = 30 mA		400		kHz
n	Power efficiency	V_{CC} = 5 V, I_O = 30 mA		72		%
R_{SW}	V_{CC} - V_{OUT} switch impedance	$V_{SHDN} = V_{CC}$ = 5V, I_O = 100 µA		1	2	kΩ

Refer to the test circuits, V_{CC} = 4.5 V to 5.5 V, T_A = -40 to 125 °C, unless otherwise specified. Typical value are referred at T_A = 25 °C.

Table 6. Electrical characteristics for ST662AB-TRY (Automotive Grade)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	I_O = 0 to 20 mA	11.2	12	12.8	V
		I_O = 0 to 30 mA, V_{CC} = 4.75 to 5.5 V	11.2	12	12.8	
I_{Q1}	Quiescent current	NO LOAD, V_{SHDN} = 0		100	500	µA
I_{Q2}	Shutdown current	NO LOAD, $V_{SHDN} = V_{CC}$		1	15	µA
I_{SH}	Shutdown pin current	V_{SHDN} = 0, V_{CC} = 5V	-50	-12	-5	µA
		$V_{SHDN} = V_{CC}$ = 5V, T_A = 25°C		0		µA
V_{IL}	Shutdown input low threshold				0.4	V
V_{IH}	Shutdown input high threshold		2.4			V
f_O	Oscillator frequency	V_{CC} = 5 V, I_O = 30 mA, T_A = 25°C		400		kHz
n	Power efficiency	V_{CC} = 5 V, I_O = 30 mA, T_A = 25°C		72		%
R_{SW}	V_{CC} - V_{OUT} switch impedance	$V_{SHDN} = V_{CC}$ = 5V, I_O = 100 µA		1	2	kΩ

5 Typical performance characteristics

Figure 3. Output voltage vs. temperature (I_{OUT} = 50 mA)

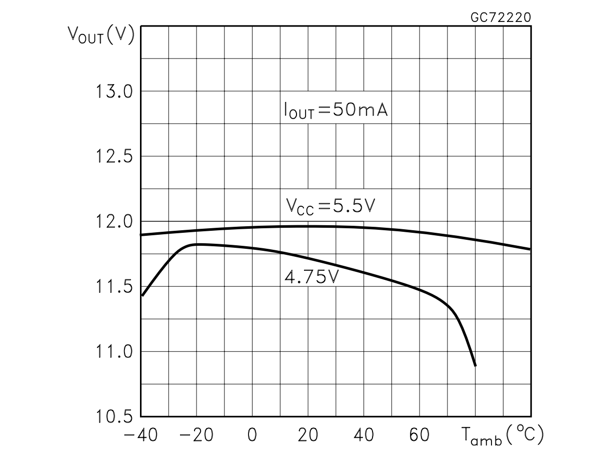


Figure 4. Output voltage vs. temperature (I_{OUT} = 30 mA)

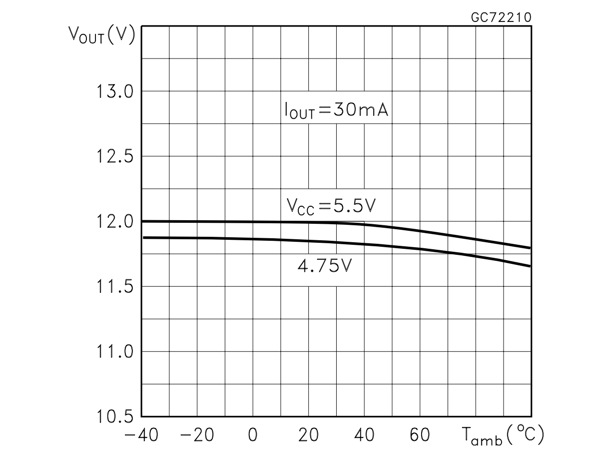


Figure 5. Supply current vs. temperature

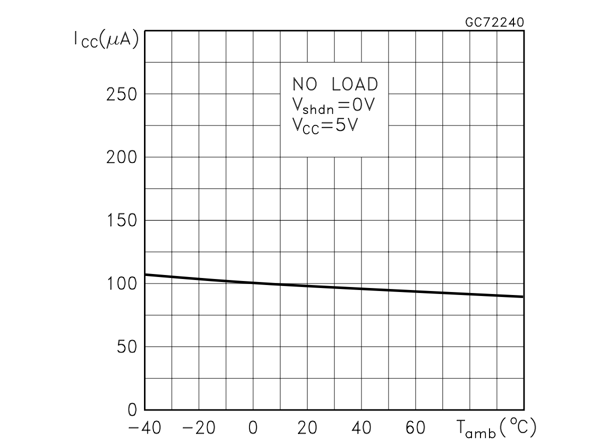


Figure 6. Supply current vs. supply voltage

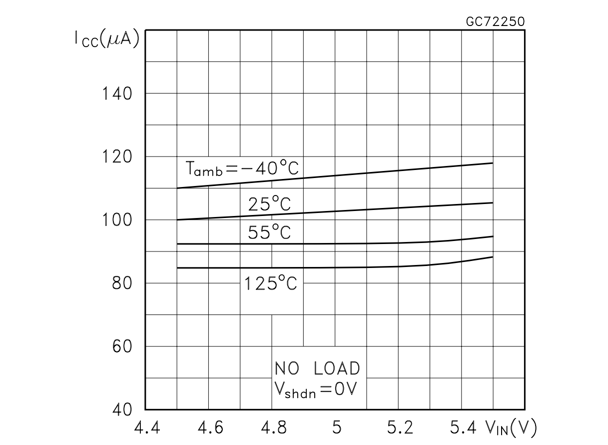


Figure 7. SHDN pin current vs. temperature

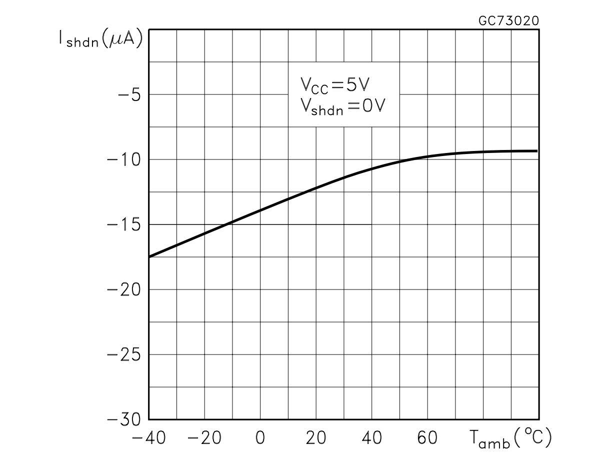


Figure 8. Output voltage vs. shutdown input

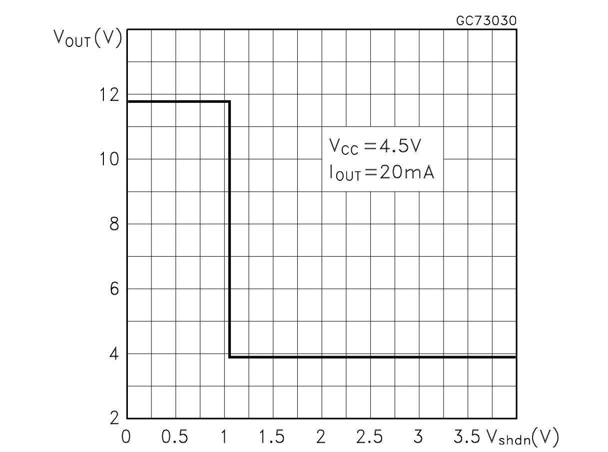


Figure 9. Output voltage vs. shutdown input voltage (No load)

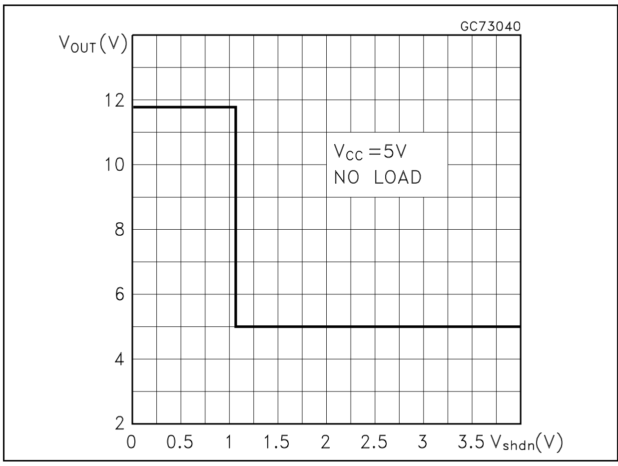


Figure 10. Output voltage vs. shutdown input voltage (I_{OUT} = 30 mA)

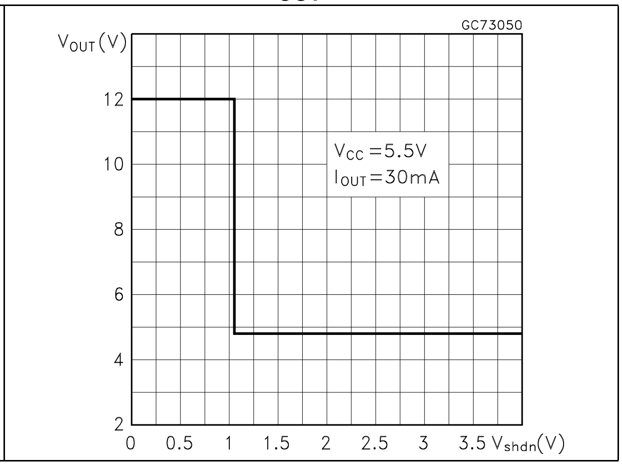
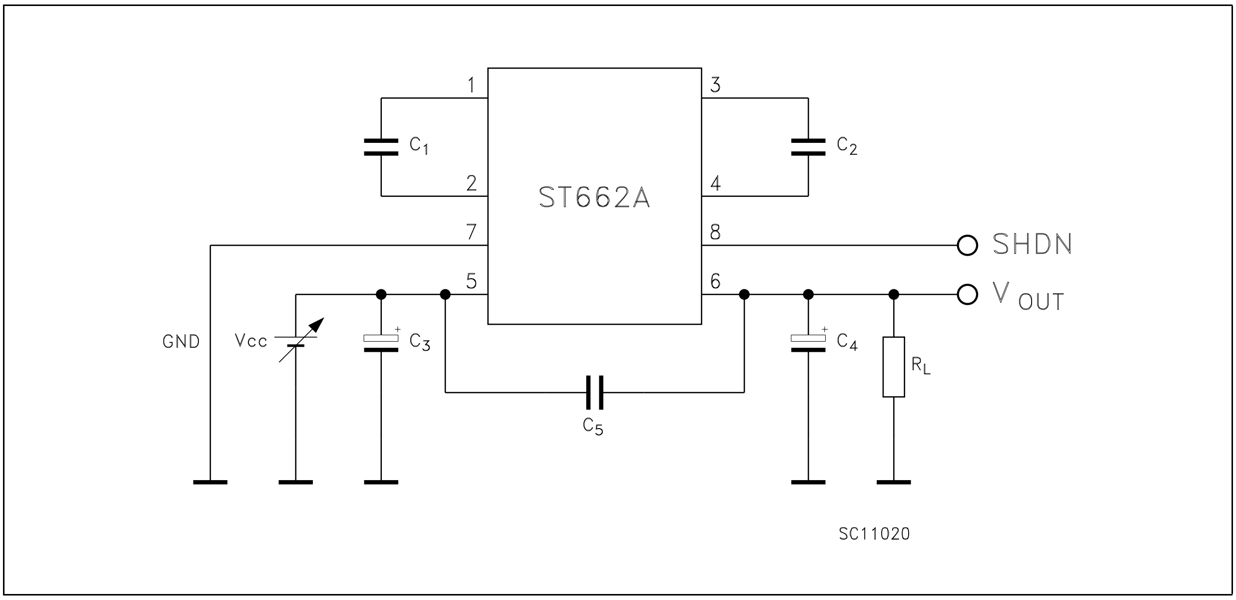


Figure 11. Test circuit



6 Description

The ST662 is an IC developed to provide a 12 V regulated output 30 mA from voltage input as low as 4.75 without any inductors. It is useful for a wide range of applications and its performances make it ideal for Flash memory programming supply.

An evaluation kit is provided to facilitate the application. This include a single-side demo board designed for surface-mount components.The operating principle of ST662 (see *Figure 12*) is to charge C1 and C2 capacitor by closing the S1 switch (while S2 is opened) at the V_{CC} voltage. After S1 is opened and S2 closed so that C1 and C2 capacitors are placed in series one to each other, and both are in series with V_{IN}. The sum of V_{C1} and V_{C2} and V_I is applied to the capacitor C4. This works as voltage triple. An amplifier error checks the output voltage and blocks the oscillator if the output voltage is greater than 12 V. The shutdown pin is internally pulled to V_{CC}. When it is held low the output voltage rises to +12 V. *Figure 13* shows the transition time of the shut down pin when the V_{SHDN} goes from 5 V to 0 V. Input logic levels of this input are CMOS compatible Applying a logic high at this input, the V_{OUT} oscillator is blocked and the V_{OUT} is reach the V_I value by D1. In this condition I_{CC} is low as 1 µA. The *Figure 14* shows the transition time of the shut down pin when the V_{SHDN} goes from 0 V to 5 V.

Figure 12. Operating principle circuit

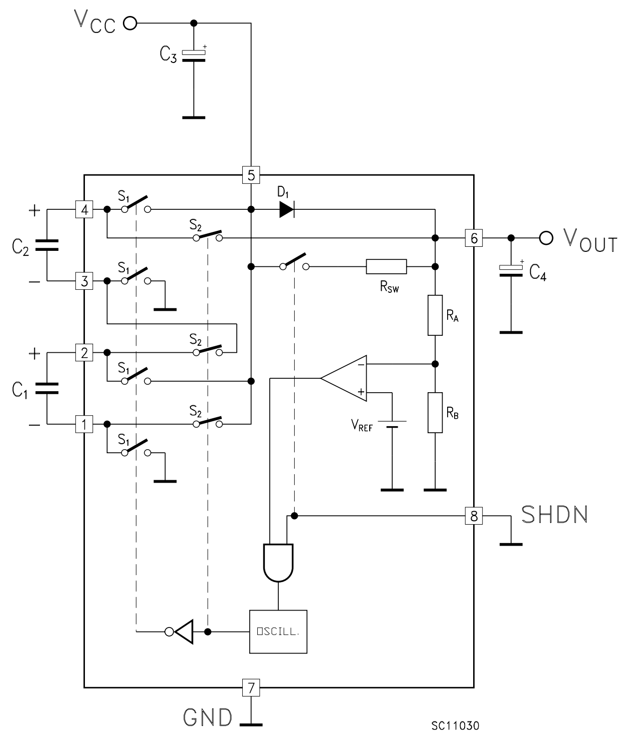
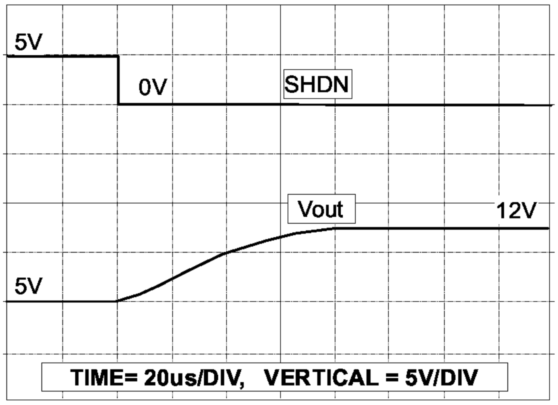
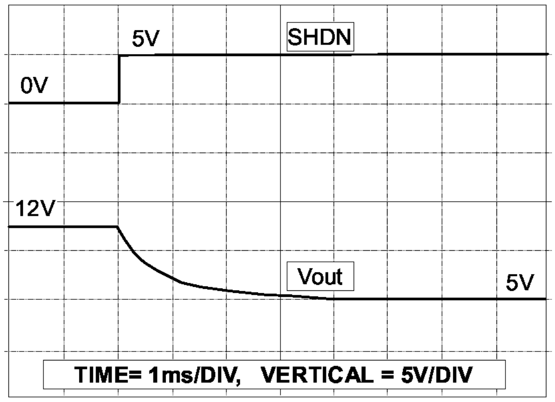


Figure 13. Exiting shutdown



V_{CC} = 5 V, I_{OUT} = 200 µA

Figure 14. Entering shutdown



V_{CC} = 5 V, I_{OUT} = 200 µA

7 Application circuit

Based on fast charge/discharge of capacitors, this circuit involves high di/dt values limited only by R_{ON} of switches. This implies a critical layout design due to the need to minimize inductive paths and place capacitors as close as possible to the device.

A good layout design is strongly recommended for noise reason. For best performance, use very short connections to the capacitors and the values shown in *Table 7*.

C3 and C4 must have low ESR in order to minimize the output ripple. Their values can be reduced to 2 μF and 1 μF, respectively, when using ceramic capacitors, but must be of 10 μF or larger if aluminium electrolytic are chosen.

C5 must be placed as close to the device as possible and could be omitted if very low output noise performance are not required.

Figure 15 and *Figure 16* show, respectively, our EVALUATION kit layout and the relatively.

Figure 15. KIT layout

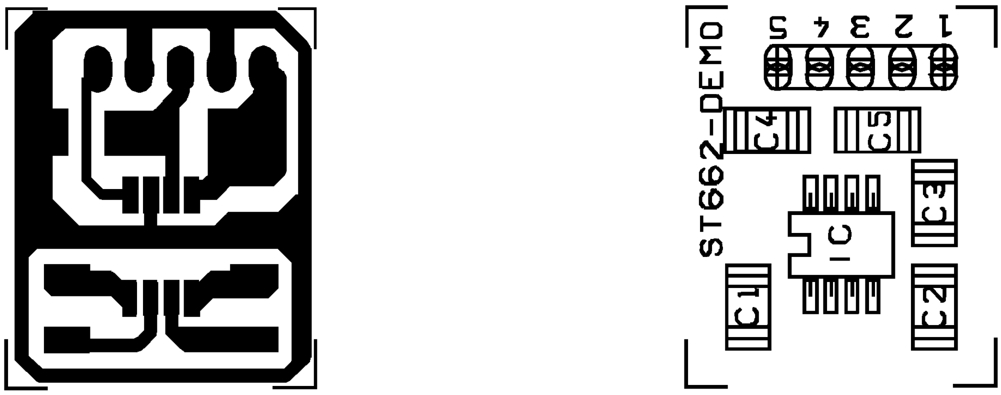


Figure 16. Electrical schematic

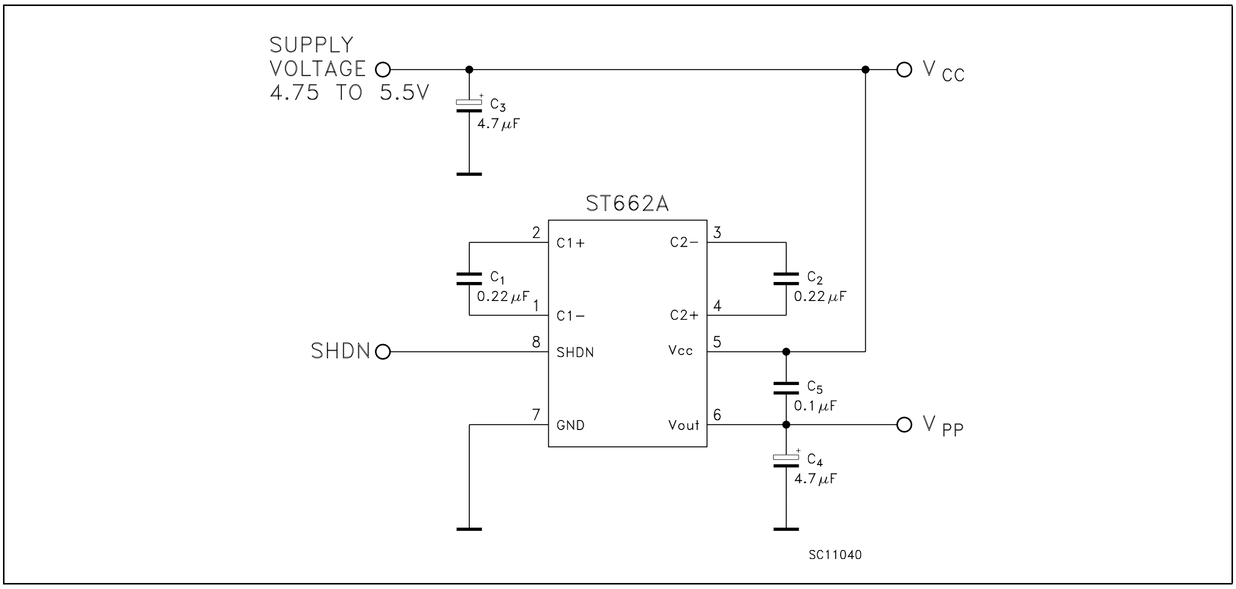


Table 7. List of component

Capacitor	Type	Value (μF)
Charge pump C1	Ceramic	0.22
Charge pump C1	Ceramic	0.22
Input C3	Electrolytic tantalum	4.7
Output C4	Electrolytic tantalum	4.7
Decoupling C5	Ceramic	0.1

7.1 ST662A output performance

Figure 17. Output voltage vs. output current

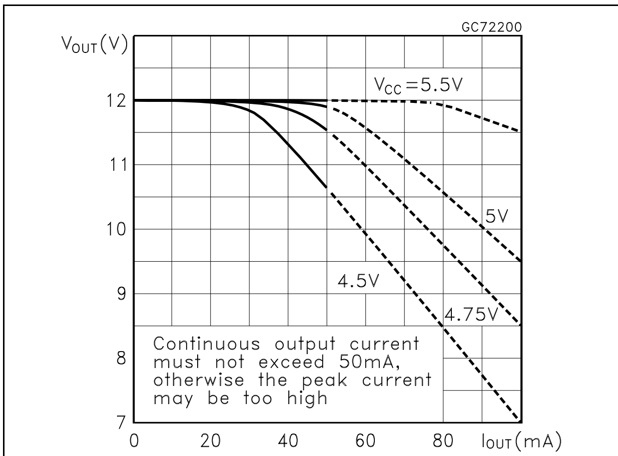


Figure 18. Efficiency vs. output current

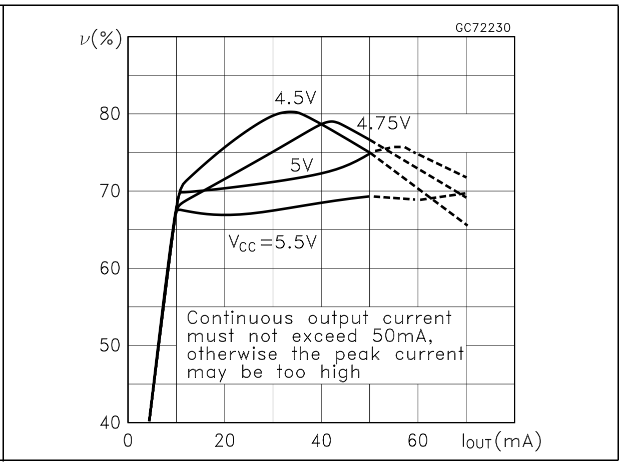
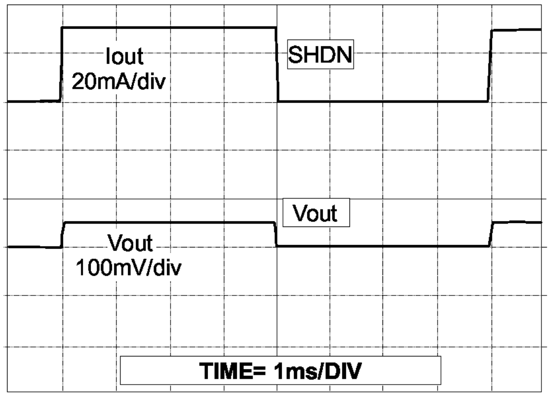
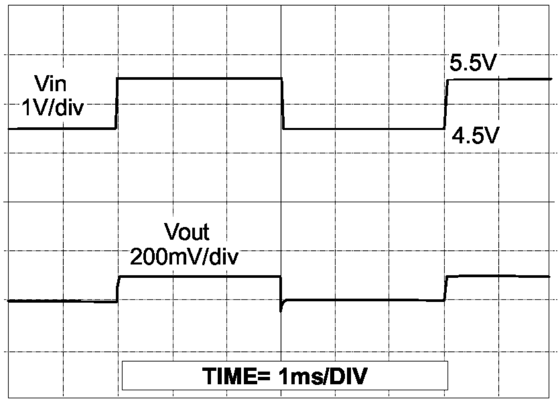


Figure 19. Load transient response (I_{OUT} = 0 to 30 mA)



V_{CC} = 5 V, I_{OUT} = 0 to 30mA

Figure 20. Load transient response (I_{OUT} = 30 mA)



V_{CC} = 4.5 to 5.5V, I_{OUT} = 30 mA

8 How to increase output current or output voltage capability

Current capability is limited by R_{ON} of internal switches. It is possible to increase it connecting in parallel two or more ST662A devices; each one of them can supply 30 mA. The *Figure 19* shows the electric schematic. The capacitors C3, C4 and C5 must be placed very close to the ICs on the board. If this is not possible, you can place two different capacitors, each of them of half value, very close to the respective integrated circuit.

Figure 23 show the output current capability of the proposed circuit.

If an output voltage greater than 12 V is required, it's possible to realize the circuit of the following diagram *Figure 22*. The relevant output current capability is shown in *Figure 24* in which is shown the output voltage vs. load current.

Figure 21. Application circuit for two ST662A in parallel

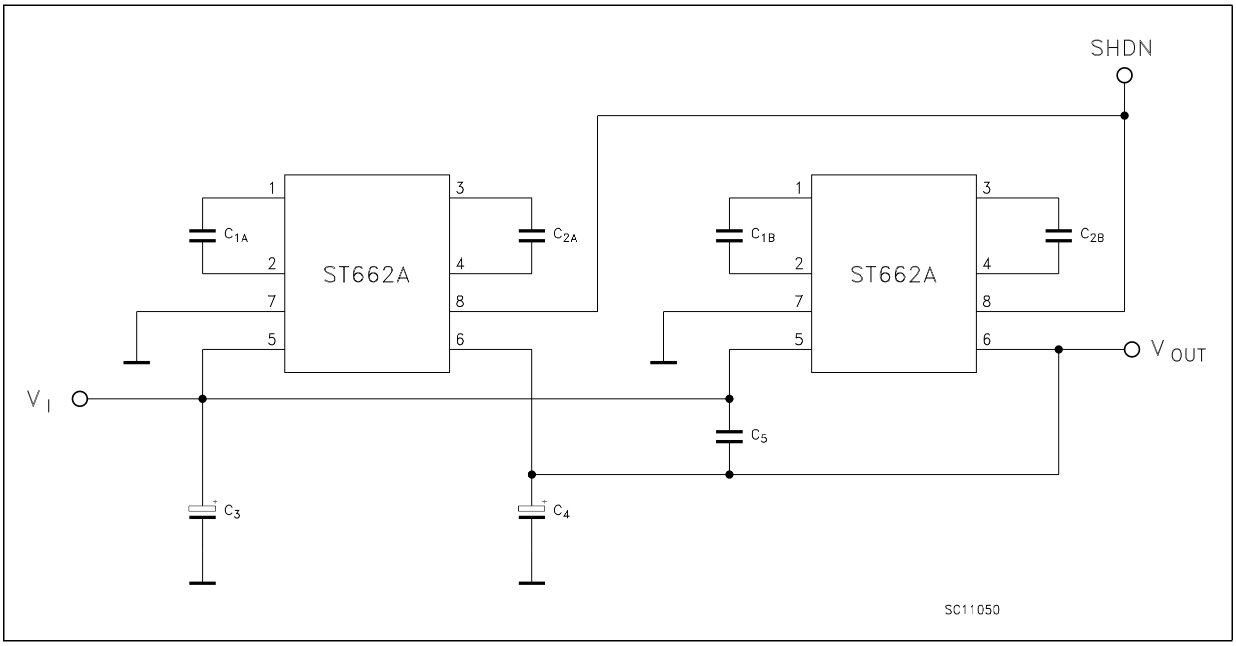


Table 8. List of component

Capacitor	Type	Value (µF)
C1A	Ceramic	0.22
C2A	Ceramic	0.22
C1B	Ceramic	0.22
C2B	Ceramic	0.22
C3	Electrolytic Tantalum	10
C4	Electrolytic Tantalum	10
C5	Ceramic	0.22

Figure 22. Application circuit for output voltage greater than 12 V

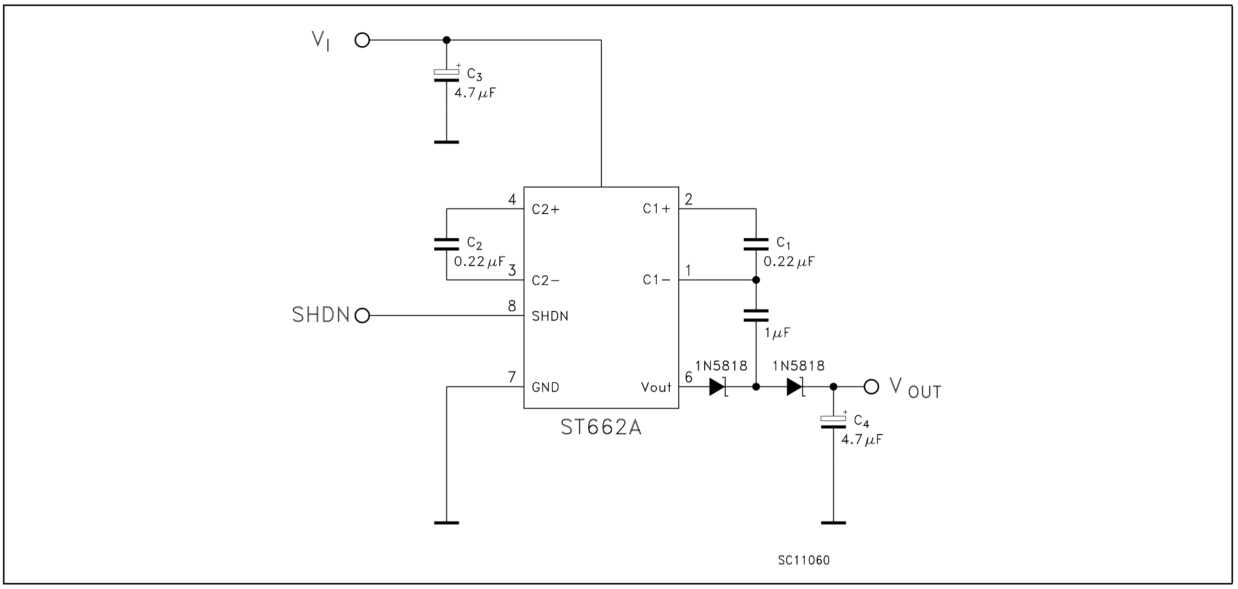


Figure 23. Output voltage for application with two device in parallel

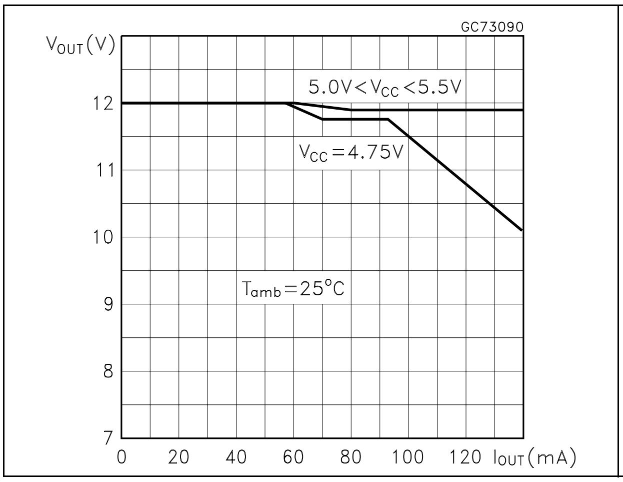
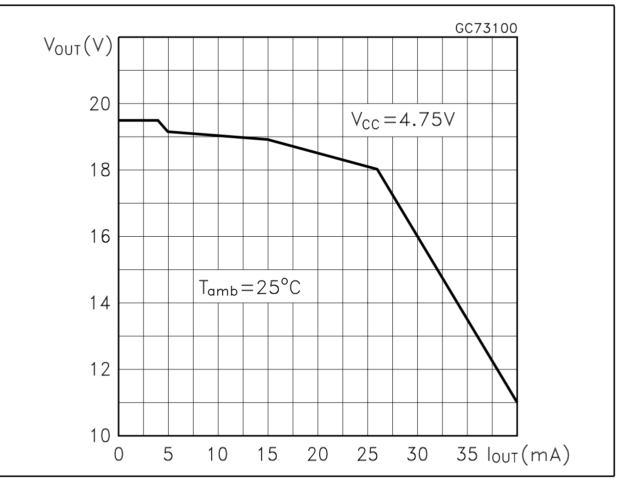


Figure 24. Output voltage for application with output voltage greater than 12 V

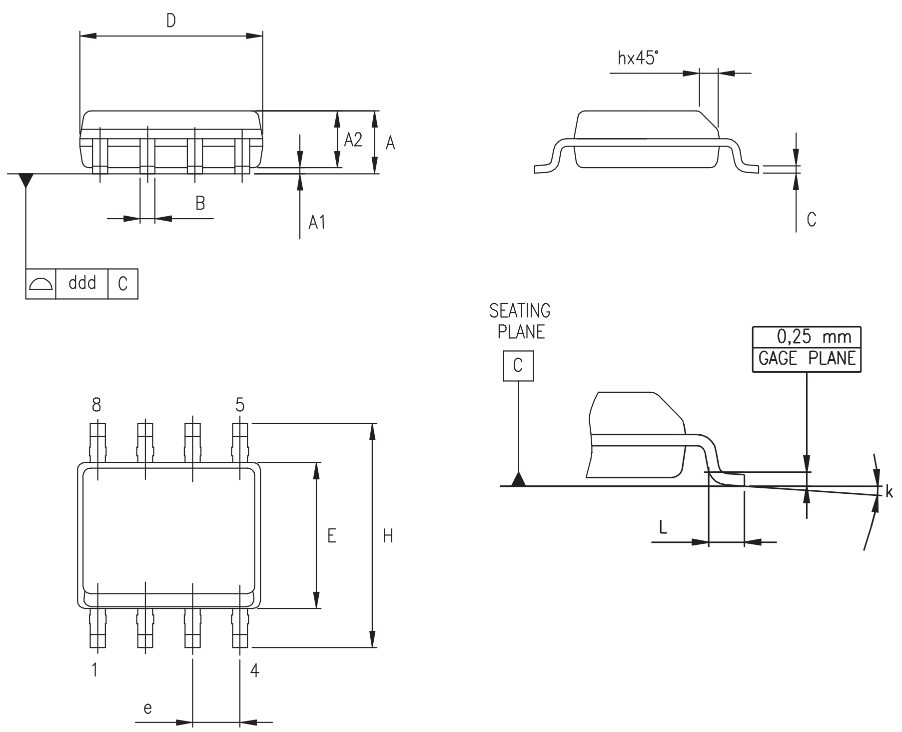


9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

SO-8 mechanical data

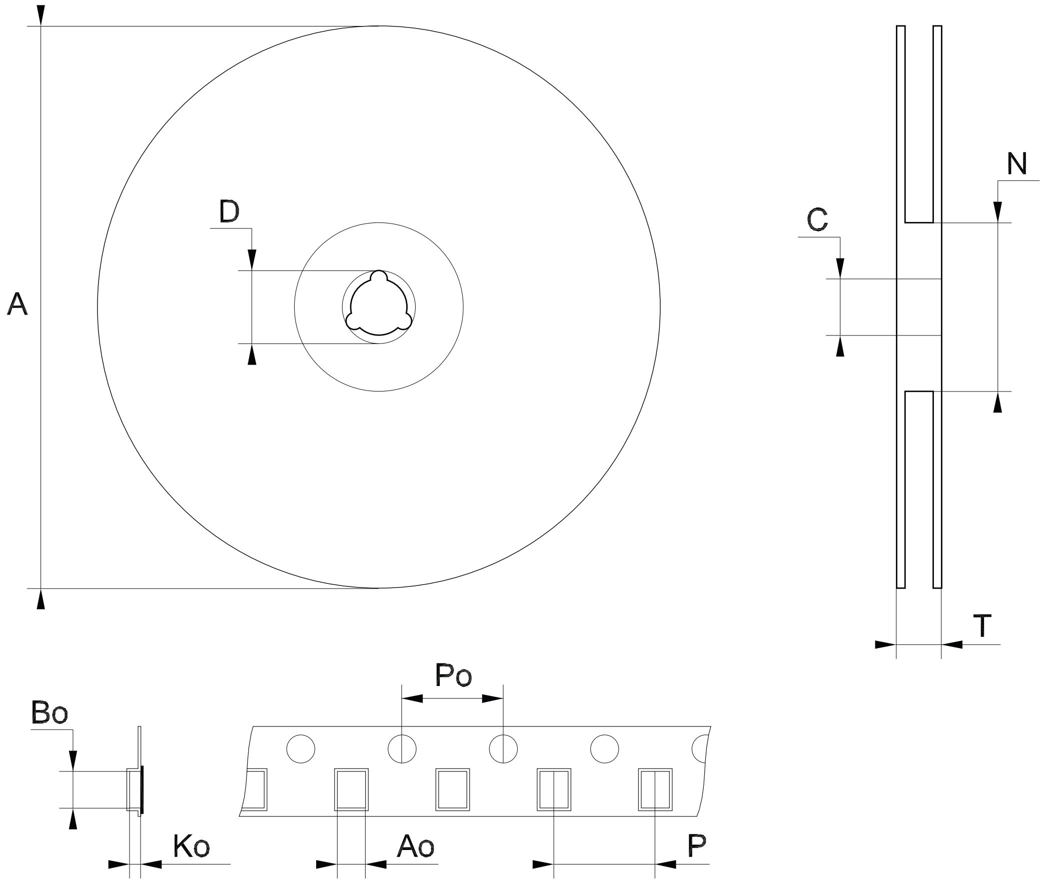
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



0016023/C

Tape & reel SO-8 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

10 Revision history

Table 9. Document revision history

Date	Revision	Changes
16-Jul-2007	5	Device summary updated.
07-Feb-2008	6	Modified: *Table 1 on page 1*.
19-Feb-2008	7	Add new order code for Automotive grade products see *Table 1 on page 1*.
03-Aug-2010	8	Modified *Features on page 1*.

Please Read Carefully: