## FUNCTIONAL BLOCKS

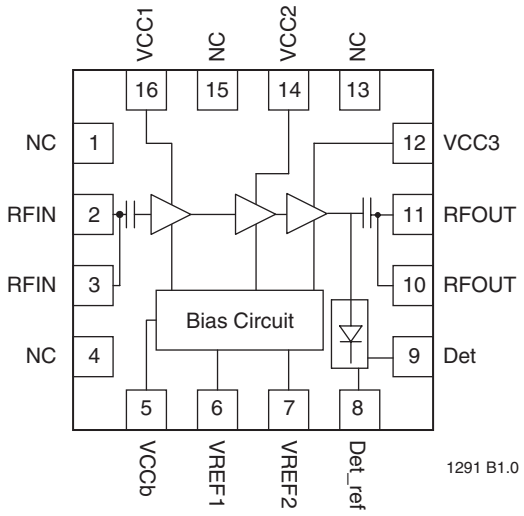


**FIGURE 1: Functional Block Diagram6**

## PIN ASSIGNMENTS

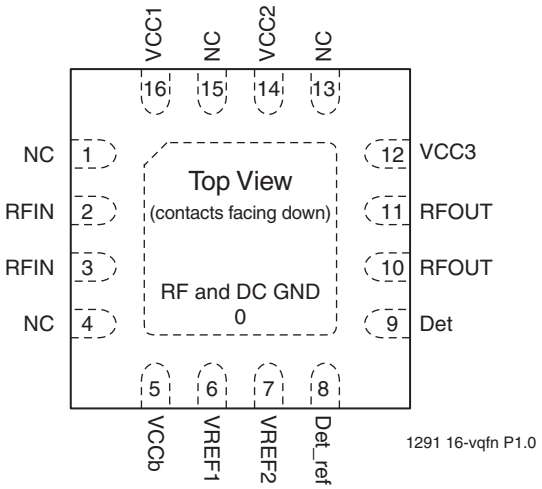


**FIGURE 2: Pin Assignments for 16-contact VQFN**

## PIN DESCRIPTIONS

**TABLE 1: Pin Description**

| Symbol | Pin No. | Pin Name | Type[1] | Function |
|---|---|---|---|---|
| GND | 0 | Ground | | The center pad should be connected to RF ground with several low inductance, low resistance vias. |
| NC | 1 | No Connection | | Unconnected pins. |
| RFIN | 2 | | I | RF input, DC decoupled |
| RFIN | 3 | | I | RF input, DC decoupled |
| NC | 4 | No Connection | | Unconnected pins. |
| VCCb | 5 | Power Supply | PWR | Supply voltage for bias circuit |
| VREF1 | 6 | | PWR | 1st and 2nd stage idle current control |
| VREF2 | 7 | | PWR | 3rd stage idle current control |
| Det_ref | 8 | | O | On-chip power detector reference |
| Det | 9 | | O | On-chip power detector |
| RFOUT | 10 | | O | RF output |
| RFOUT | 11 | | O | RF output |
| VCC3 | 12 | Power Supply | PWR | Power supply, 3rd stage |
| NC | 13 | No Connection | | Unconnected pins. |
| VCC2 | 14 | Power Supply | PWR | Power supply, 2nd stage |
| NC | 15 | No Connection | | Unconnected pins. |
| VCC1 | 16 | Power Supply | PWR | Power supply, 1st stage |

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1. I=Input, O=Output

## ELECTRICAL SPECIFICATIONS

The AC and DC specifications for the power amplifier interface signals. Refer to Table 2 for the DC voltage and current specifications. Refer to Figures 3 through 10 for the RF performance.

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Input power to pins 2 and 3 ($P_{IN}$) . . . . . +5 dBm
Average output power ($P_{OUT}$)[1] . . . . . +28 dBm
Supply Voltage at pins 5, 12, 14, 16 ($V_{CC}$) . . . . . -0.3V to +4.6V
Reference voltage to pins 6 ($V_{REF1}$) and pin 7 ($V_{REF2}$) . . . . . -0.3V to +3.6V
DC supply current ($I_{CC}$) . . . . . 500 mA
Operating Temperature ($T_A$) . . . . . -40ºC to +85ºC
Storage Temperature ($T_{STG}$) . . . . . -40ºC to +120ºC
Maximum Junction Temperature ($T_J$) . . . . . +150ºC
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds

1. Never measure with CW source. Pulsed single-tone source with <50% duty cycle is recommended. Exceeding the maximum rating of average output power could cause permanent damage to the device.

### Operating Range

| Range | Ambient Temp | $V_{CC}$ |
|---|---|---|
| Industrial | -40°C to +85°C | 3.3V |

**TABLE 2: DC Electrical Characteristics at 25ºC**

| Symbol | Parameter | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage at pins 5, 12, 14, 16 | 3.0 | 3.3 | 4.2 | V |
| $I_{CC}$ | Supply Current | | | | |
| | for 802.11g, 24 dBm | | 300 | | mA |
| | for 802.11b, 25 dBm | | 350 | | mA |
| $I_{CQ}$ | Idle current for 802.11g to meet EVM<4% @ 23dBm | | 80 | | mA |
| $I_{OFF}$ | Shut down current | | 1 | | µA |
| $V_{REG1}$ | Reference Voltage for 1st and 2nd Stage, with 270Ω resistor | 2.85 | 2.90 | 2.95 | V |
| $V_{REG2}$ | Reference Voltage for 3rd Stage, with 100Ω resistor | 2.85 | 2.90 | 2.95 | V |

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**TABLE 3: AC Electrical Characteristics for Configuration at 25°C**

| Symbol | Parameter | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|
| $F_{L-U}$ | Frequency range in 802.11b/g applications (see Figure 11) | 2400 | | 2485 | MHz |
| $P_{OUT}$ | Output power | | | | |
| | @ PIN = -10 dBm 11b signals | | 23 | | dBm |
| | @ PIN = -10 dBm 11g signals | | 23 | | dBm |
| G | Small signal gain | 31 | 32 | | dB |
| $G_{VAR1}$ | Gain variation over each band (2400-2485 MHz) | | | ±0.5 | dB |
| $G_{VAR2}$ | Gain ripple over channel (Gain variation over 20 MHz) | | 0.2 | | dB |
| ACPR | Meet 11b spectrum mask | 24 | 25 | | dBm |
| | Meet 11g OFDM 54 MBPS spectrum mask | 24 | 25 | | dBm |
| Added EVM | @ 23 dBm output with 11g OFDM 54 MBPS signal | | 3.5 | | % |
| 2f, 3f, 4f, 5f | Harmonics at 22 dBm, without trapping capacitors | | | -40 | dBc |

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## TYPICAL PERFORMANCE CHARACTERISTICS
## Test Conditions: $V_{CC}$ = 3.3V, $T_A$ = 25°C Unless otherwise specified.

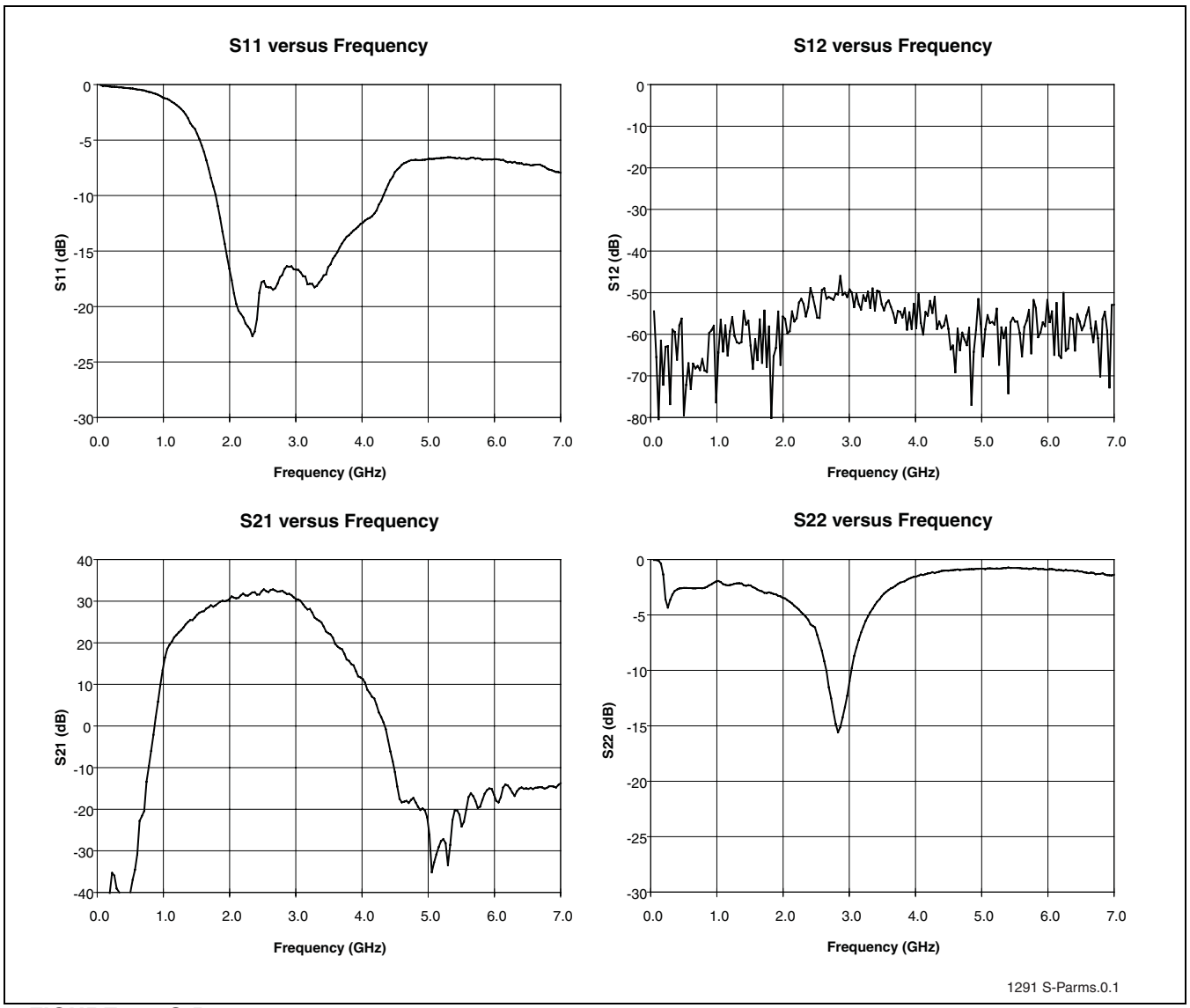



**FIGURE 3: S-Parameters**

## TYPICAL PERFORMANCE CHARACTERISTICS
**Test Conditions: $V_{CC}$ = 3.3V, $T_A$ = 25°C, 54 Mbps 802.11g OFDM Signal**

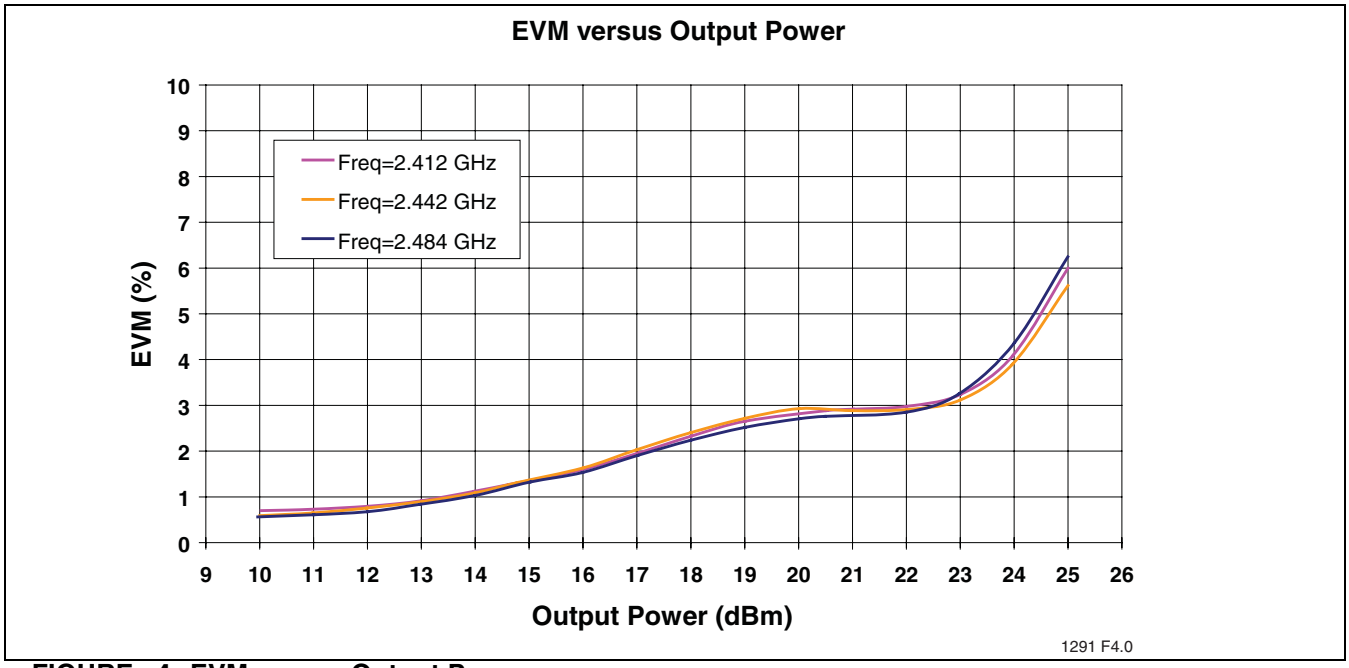



**FIGURE 4: EVM versus Output Power**

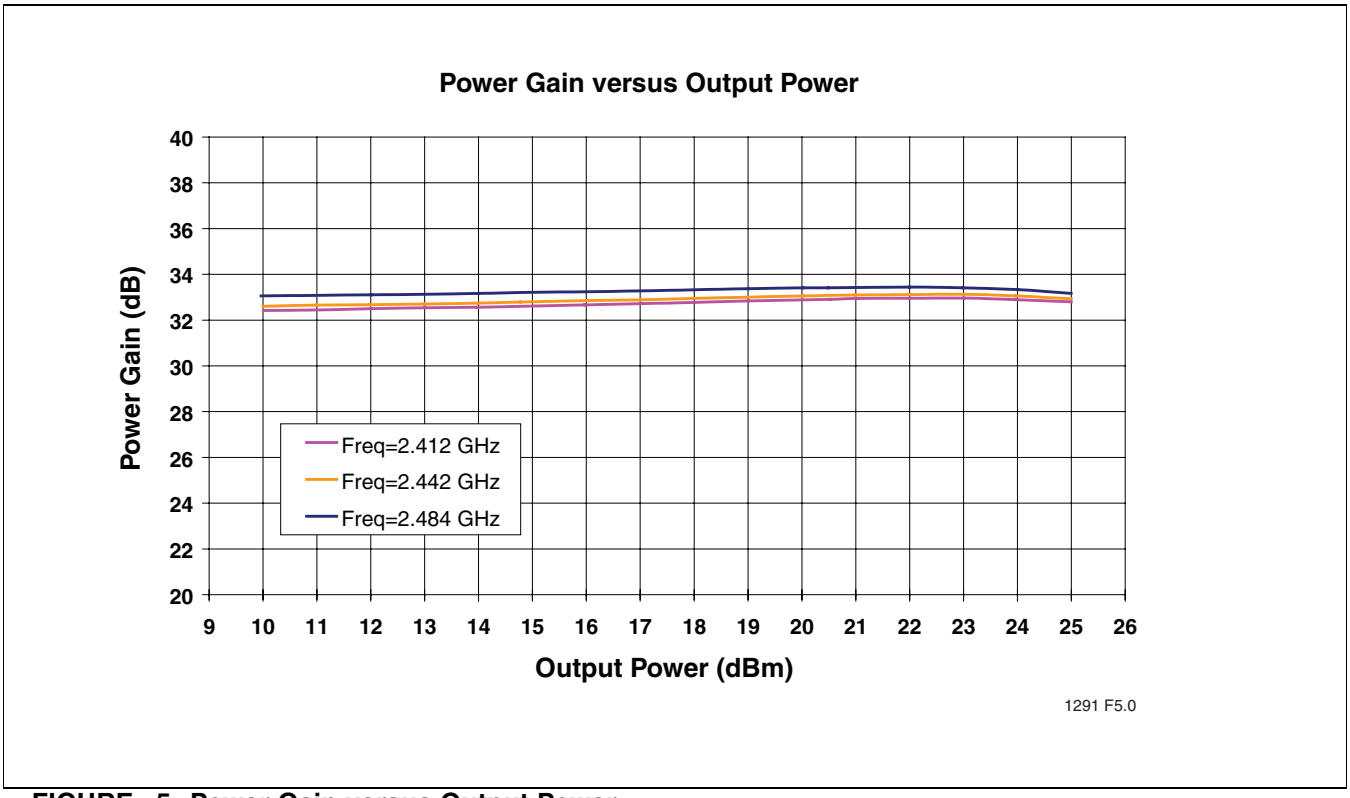



**FIGURE 5: Power Gain versus Output Power**

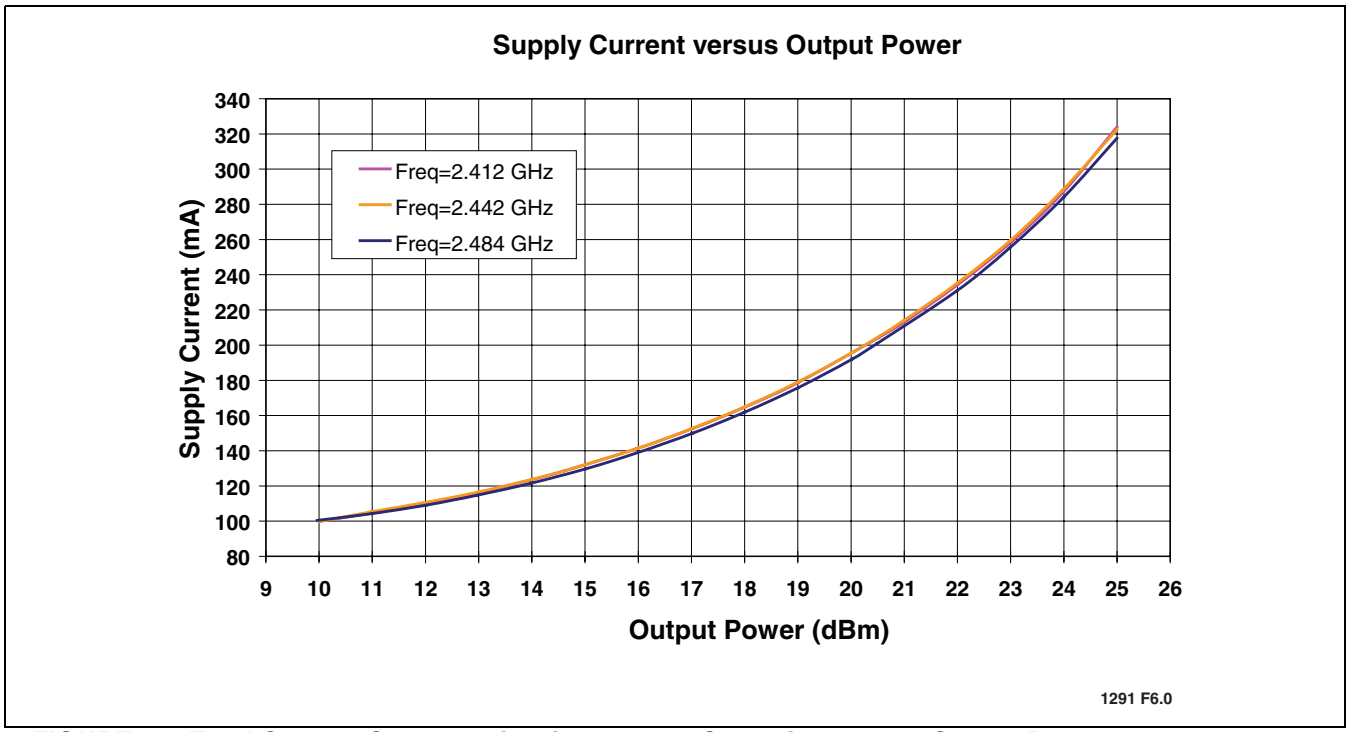



**FIGURE 6: Total Current Consumption for 802.11g Operation versus Output Power**

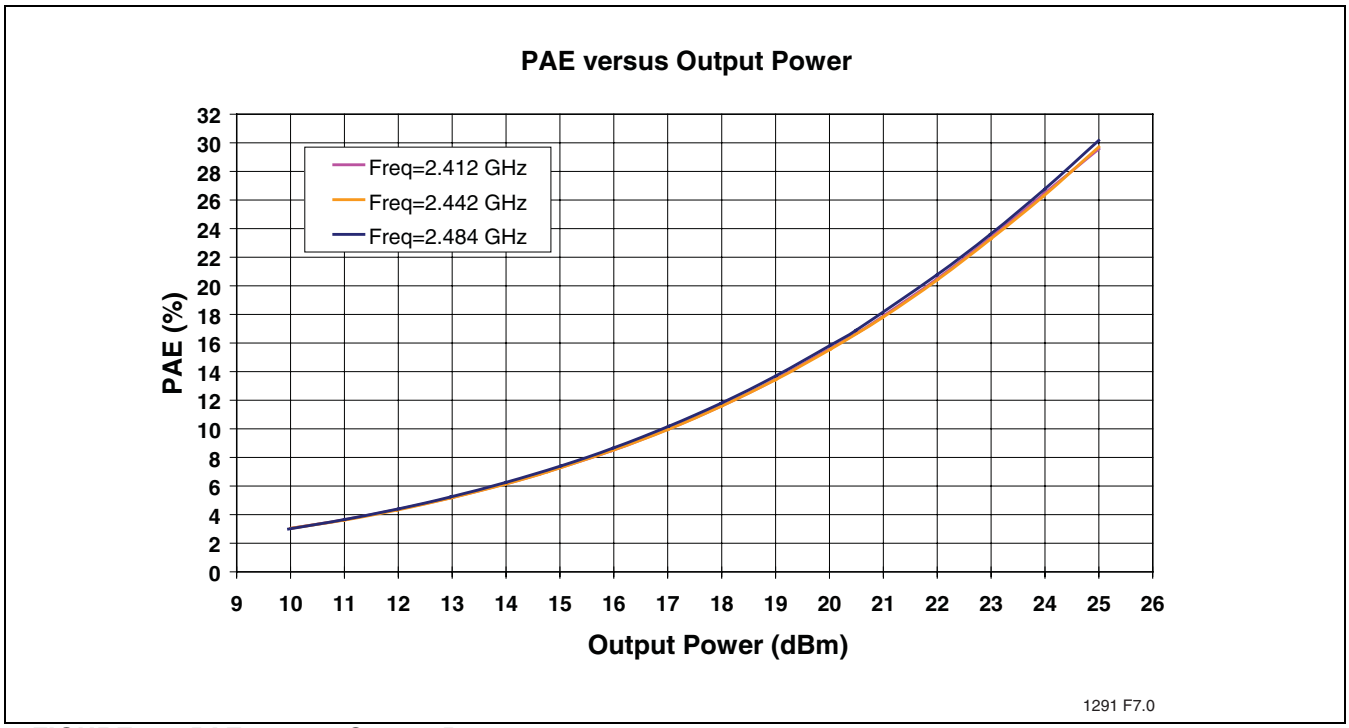



**FIGURE 7: PAE versus Output Power**

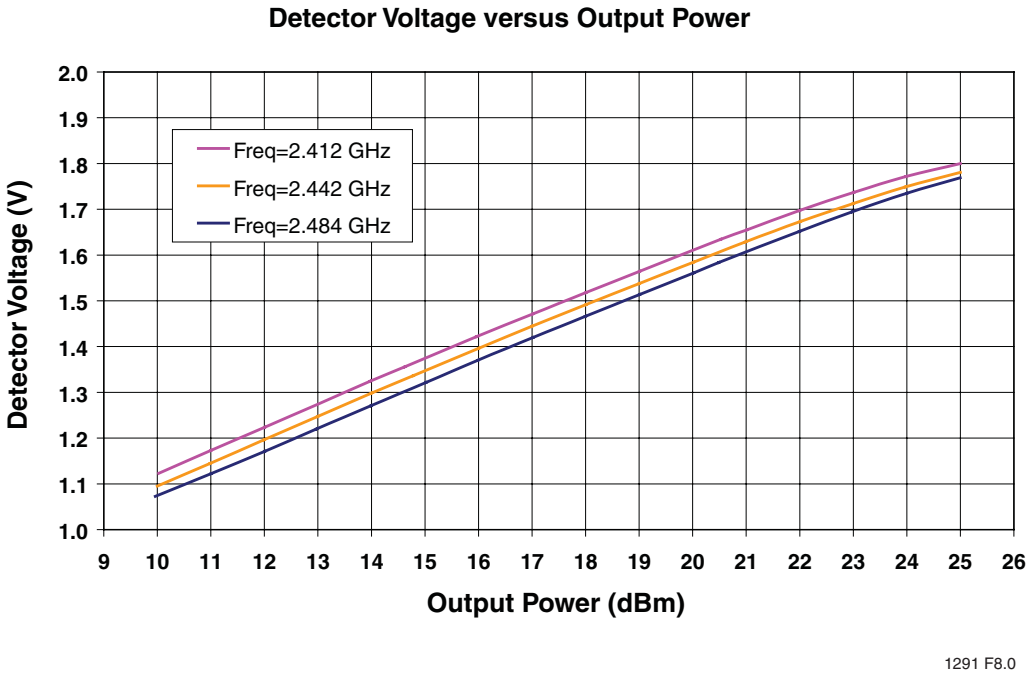



**FIGURE 8: Detector Characteristic versus Output Power**

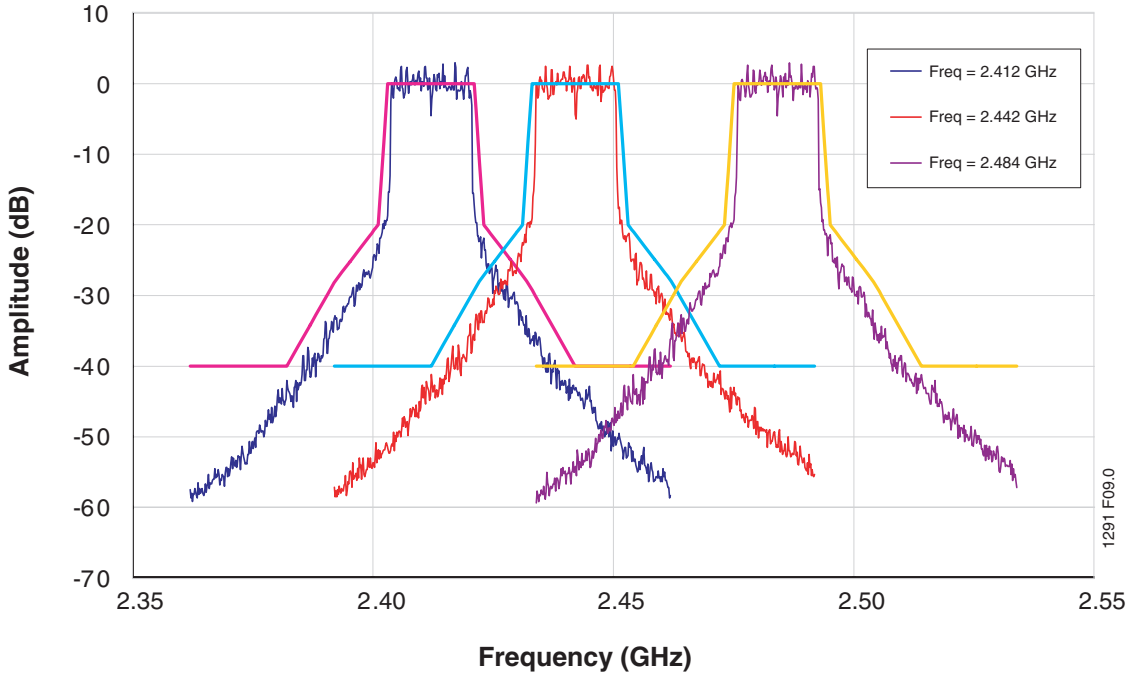



**FIGURE 9: 802.11g Spectrum Mask at 24 dBm, Total current 300 mA**

## TYPICAL PERFORMANCE CHARACTERISTICS
## Test Conditions: $V_{CC}$ = 3.3V, $T_A$=25°C, 1 Mbps 802.11b CCK signal

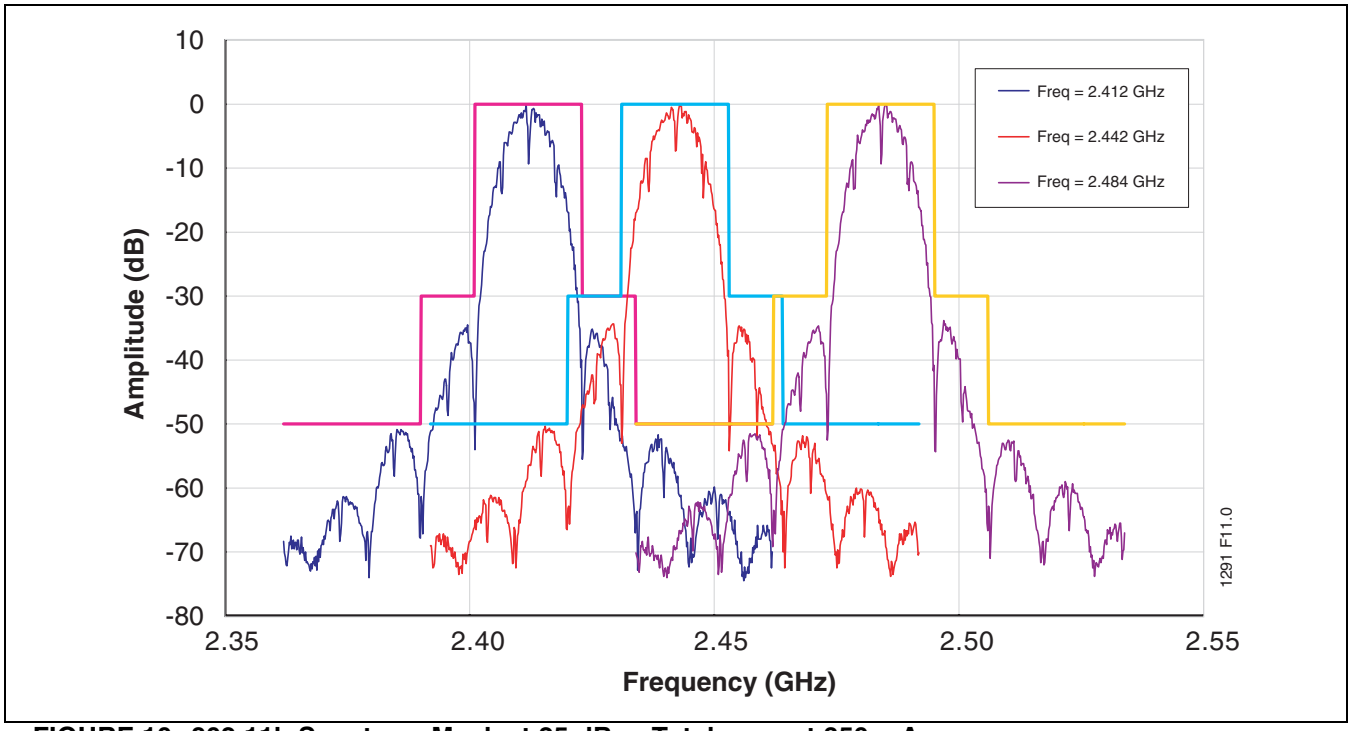



**FIGURE 10: 802.11b Spectrum Mask at 25 dBm, Total current 350 mA**

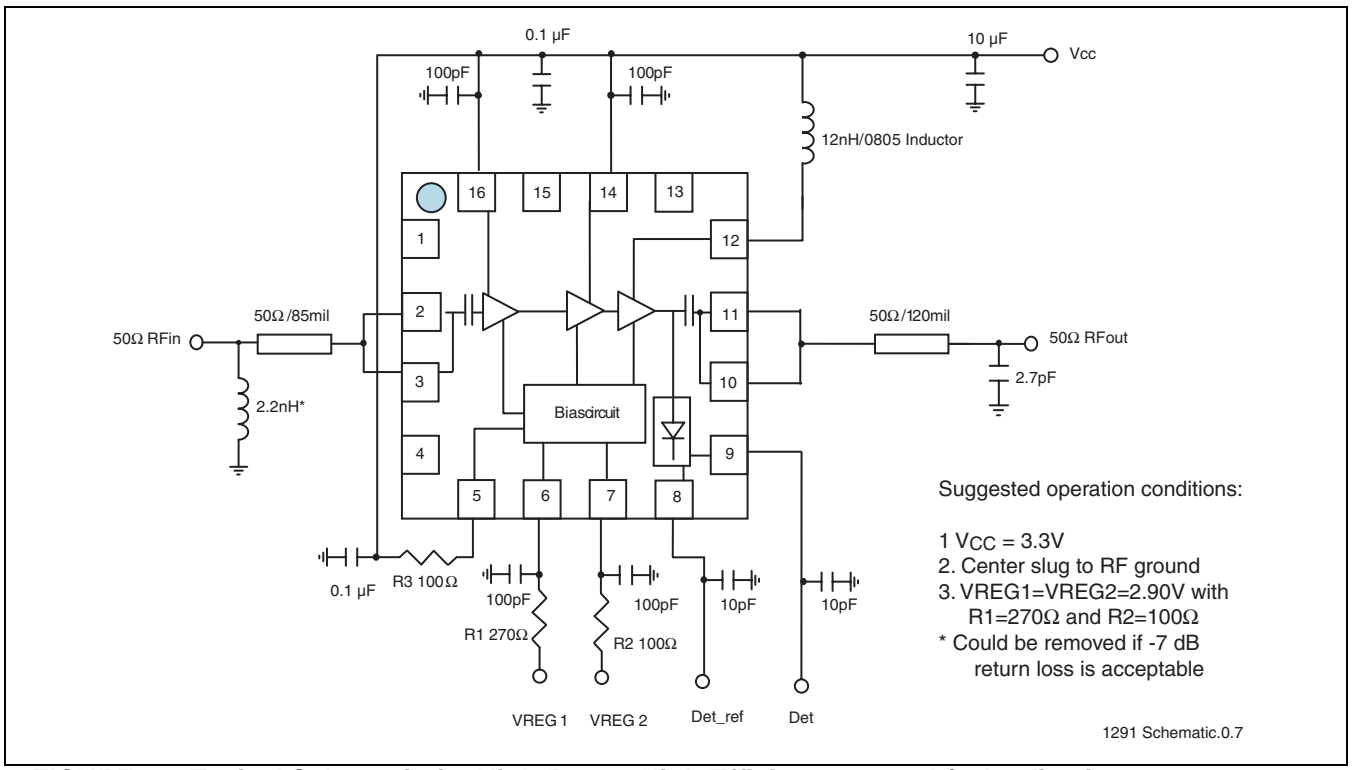
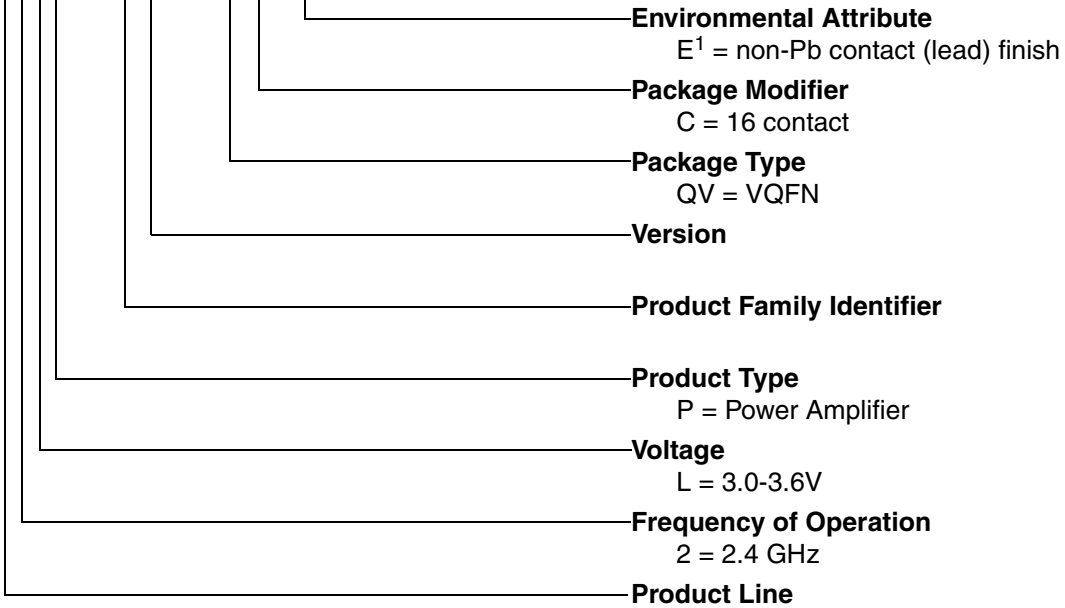



**FIGURE 11: Typical Schematic for High-Power, High-Efficiency 802.11b/g Applications**

## PRODUCT ORDERING INFORMATION

**SST12LP 15A - QVC E**
SSTXXLP XXX - XXX X




1. Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

### Valid combinations for SST12LP15A

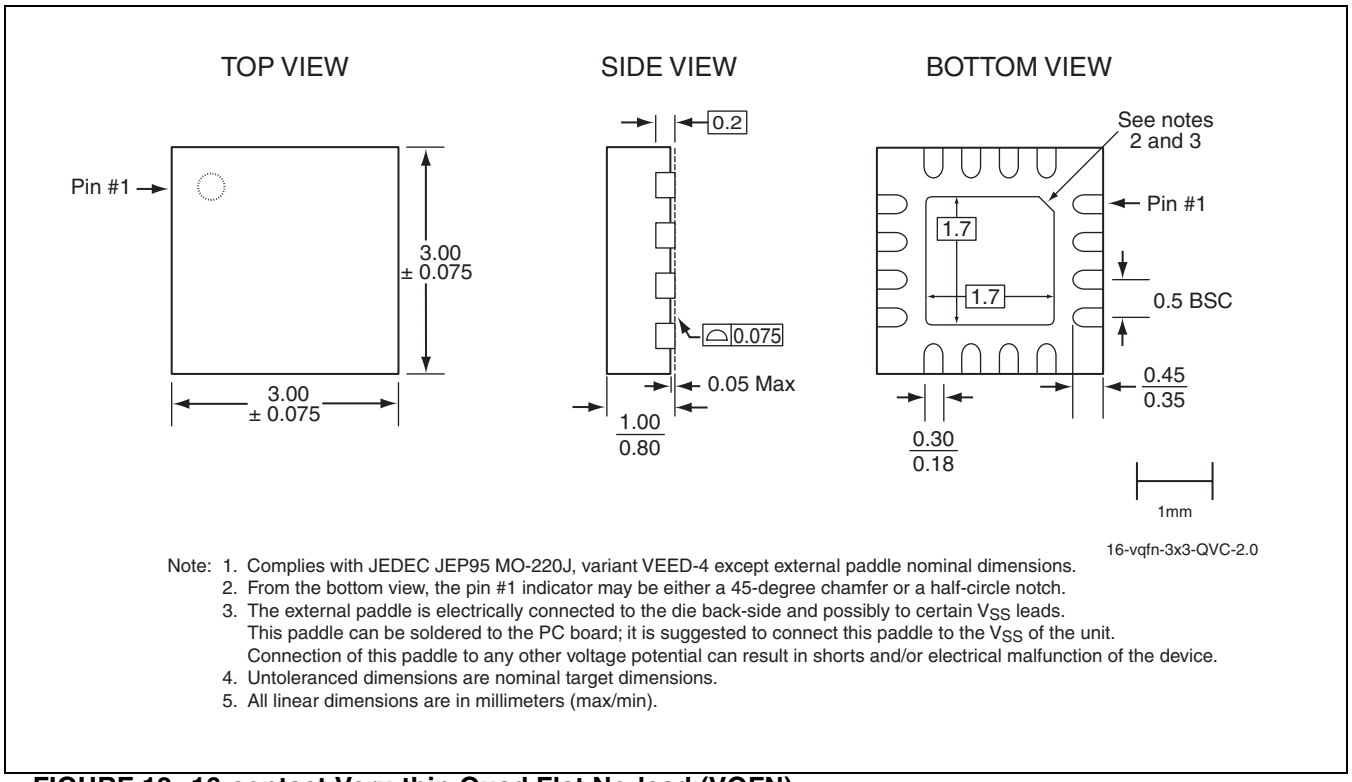
SST12LP15A-QVCE

### SST12LP15A Evaluation Kits

SST12LP15A-QVCE-K

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

## PACKAGING DIAGRAMS




Note: 1. Complies with JEDEC JEP95 MO-220J, variant VEED-4 except external paddle nominal dimensions.
2. From the bottom view, the pin #1 indicator may be either a 45-degree chamfer or a half-circle notch.
3. The external paddle is electrically connected to the die back-side and possibly to certain $V_{SS}$ leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the $V_{SS}$ of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.
4. Untoleranced dimensions are nominal target dimensions.
5. All linear dimensions are in millimeters (max/min).

**FIGURE 12: 16-contact Very-thin Quad Flat No-lead (VQFN)**
**SST Package Code: QVC**

**TABLE 4: Revision History**

| Revision | Description | Date |
|---|---|---|
| 00 | • Initial release of data sheet | Mar 2005 |
| 01 | • Updated values for gain and efficiency on page 1<br>• Updated values for VREG1 and VREG2 in Table 2 on page 4<br>• Removed stability parameter from Table 3 on page 5<br>• Updated the typical application schematic on page 10<br>• Updated QVC package drawing.<br>• Updated “Absolute Maximum Stress Ratings” on page 4 | Mar 2006 |
| 02 | • Added information for 2.3-2.4 and 2.5-2.6 applications<br>• Removed leaded part numbers | Jul 2006 |
| 03 | • Updated “Features:” and “Product Description” on page 1<br>• Revised Table 2 on page 4 and Table 3 on page 5<br>• Updated values in Figure 11 on page 10.<br>• Removed two schematics<br>• Updated Figures 3 - 8 | Sep 2008 |
| 04 | • Updated “Contact Information” on page 13. | Feb 2009 |

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