ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}.....+7V
Storage Temperature.....-65˚C to +150˚C

Power Dissipation
8-pin NSOIC.....1000mW
($Ø_{JA}$ = 62ºC/W)
8-pin PDIP.....1000mW
($Ø_{JA}$ = 62ºC/W)

ELECTRICAL CHARACTERISTICS

Typically 25ºC @ V_{CC} = +5V unless otherwise noted.

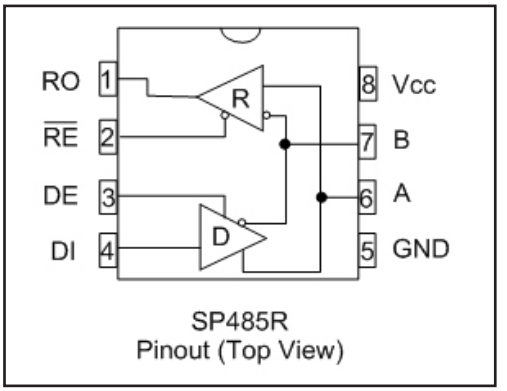
PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	I_{OUT} = -3.2mA
V_{OH}	2.4			Volts	I_{OUT} = 1.0mA
RS-485 DRIVER DC Characteristics					
Open Circuit Voltage			6.0	Volts	
Differential Output Voltage	1.5		5.0	Volts	R_L = 54Ω, C_L = 50pF
Balance			+/-0.2	Volts	$\|V_T\| - \|\overline{V_T}\|$
Common-Mode Output			3.0	Volts	
Output Current	28.0			mA	R_L = 54Ω
Short Circuit Current			+/-250	mA	Terminated in -7V to +12V
RS-485 DRIVER AC Characteristics					
Maximum Data Rate	5			Mbps	R_L = 54Ω,
Output Transition Time		30		ns	Rise/fall time, 10% to 90%
Propagation Delay, t_{PLH}		60	100	ns	See Figures 4 & 6, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF
Propagation Delay, t_{PHL}		60	100	ns	See Figures 4 & 6, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF
Driver Output Skew		5	15	ns	see Figures 4 and 6, $t_{SKEW} = \|t_{DPHL} - t_{DPLH}\|$
RS-485 RECEIVER DC Characteristics					
Output Voltage Low, V_{OL}			0.4	Volts	
Output Voltage High, V_{OH}	2.4			Volts	
Tri-State Output Current			+/-1	µA	0.4V ≤ V_{OUT} ≤ 2.4V; $\overline{RE}$ = Vcc

ELECTRICAL CHARACTERISTICS

Typically 25ºC @ V_{CC} = +5V unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-485 RECEIVER DC Characteristics (continued)					
Common Mode Range	-7.0		+12.0	Volts	
Receiver Sensitivity			+/-0.2	Volts	-7V ≤ V_{CM} ≤ +12V
Input Impedance	120	150		kΩ	-7V ≤ V_{CM} ≤ +12V
RS-485 RECEIVER AC Characteristics					
Maximum Data Rate	1			Mbps	
Propagation Delay; t_{PHL}			1200	ns	See Figures 4 & 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF
Propagation Delay; t_{PLH}			1200	ns	See Figures 4 & 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF
Differential Receiver Skew		60		ns	See Figures 4 & 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, t_{SKEW} = $\lvert t_{PHL} - t_{PLH} \rvert$
RS-485 DRIVER Enable / Disable Time					
Driver Enable to Output Low		40	500	ns	C_L = 15pF, see Figures 5 and 7, S_1 closed
Driver Enable to Output High		40	500	ns	C_L = 15pF, see Figures 5 and 7, S_2 closed
Driver Disable Time from Low		40	500	ns	C_L = 15pF, see Figures 5 and 7, S_1 closed
Driver Disable Time from High		40	500	ns	C_L = 15pF, see Figures 5 and 7, S_2 closed
RS-485 RECEIVER Enable / Disable Time					
Receiver Enable to Output Low		40	500	ns	C_L = 15pF, see Figures 3 and 9, S_1 closed
Receiver Enable to Output High		40	500	ns	C_L = 15pF, see Figures 3 and 9, S_2 closed
Receiver Disable from Low		40	500	ns	C_L = 15pF, see Figures 3 and 9, S_1 closed
Receiver Disable from High		40	500	ns	C_L = 15pF, see Figures 3 and 9, S_1 closed
POWER REQUIREMENTS					
Supply Voltage V_{CC}	+4.75		+5.25	Volts	
Supply Current I_{CC}, No Load		300	500	µA	$\overline{RE}$ = Vcc or 0V, DE = 0V
Supply Current I_{CC}, No Load		500	900	µA	$\overline{RE}$ = Vcc or 0V, DE = Vcc
ENVIRONMENTAL					
Operating Temperature					
Commercial (..C..)	0		+70	ºC	
Industrial (..E..)	-40		+85	ºC	
Storage Temperature	-65		+150	ºC	

PIN FUNCTION



Pin 1 - RO - Receiver Output

Pin 2 - $\overline{RE}$ - Receiver Output Enable Active LOW

Pin 3 - DE - Driver Output Enable Active HIGH

Pin 4 DI - Driver Input

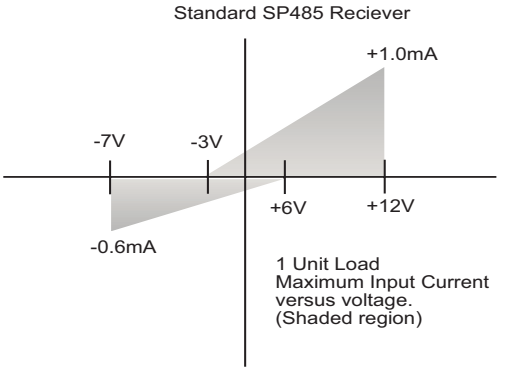
Pin 5 - GND - Ground Connection

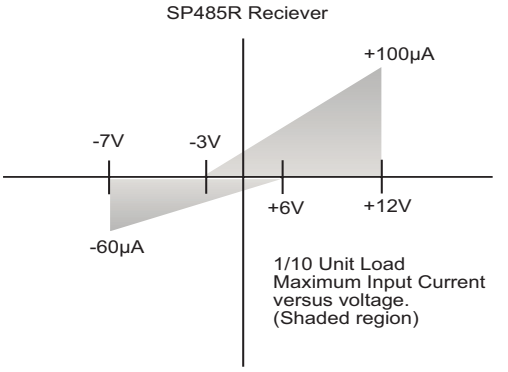
Pin 6 - A - Driver Output / Receiver input
Non-Inverting

Pin 7 - B - Driver Output / Receiver Input Inverting

Pin 8 - Vcc - Positive Supply 4.75V ≤ Vcc ≤ 5.25V

RECEIVER INPUT GRAPH





TEST CIRCUITS

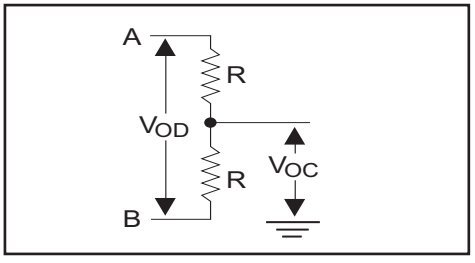


Figure 2. Driver DC Test Load Circuit

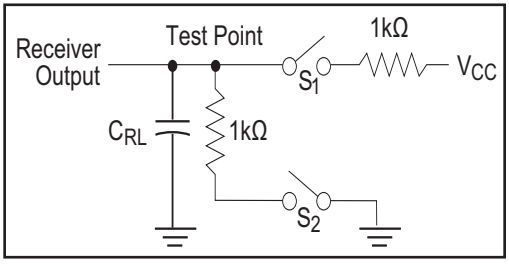


Figure 3. Receiver Timing Test Load Circuit

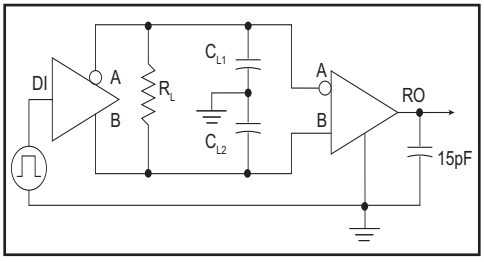


Figure 4. RS-485 Driver/Receiver Timing Test

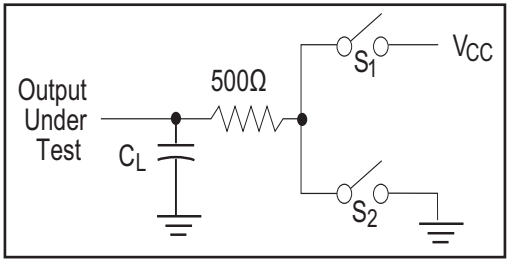


Figure 5. Driver Timing Test Load #2 Circuit

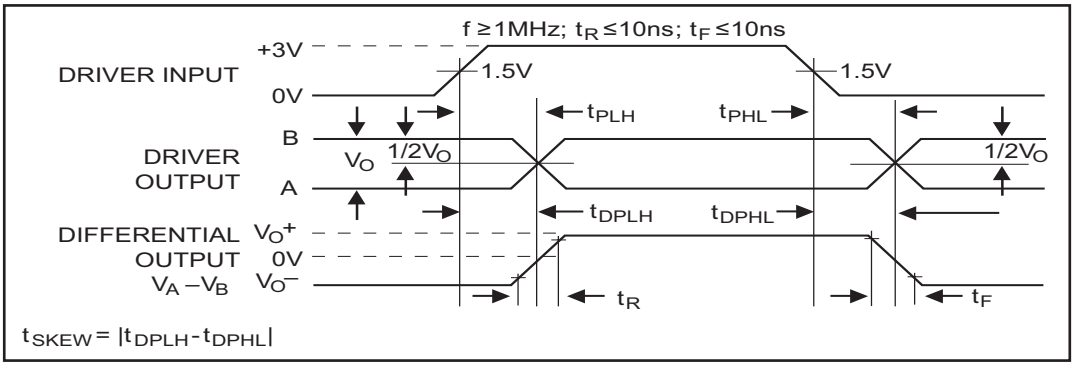


Figure 6. Driver Propagation Delays

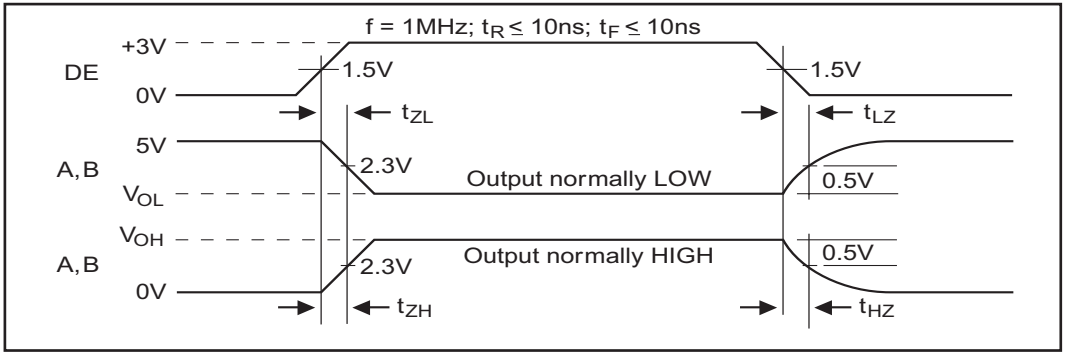


Figure 7. Driver Enable and Disable Times

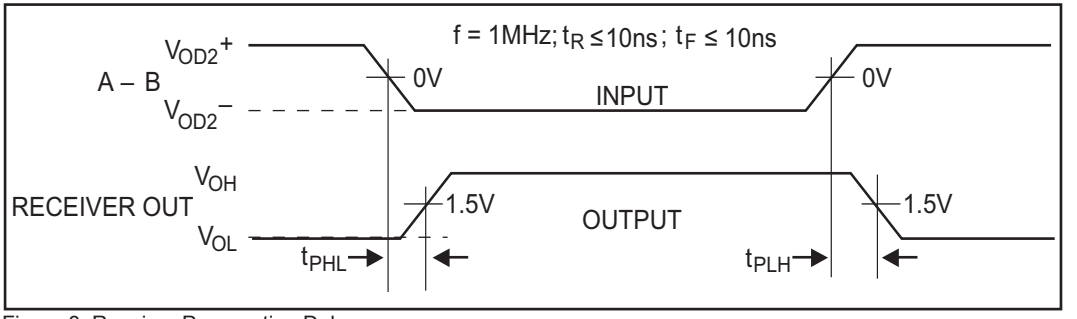


Figure 8. Receiver Propagation Delays

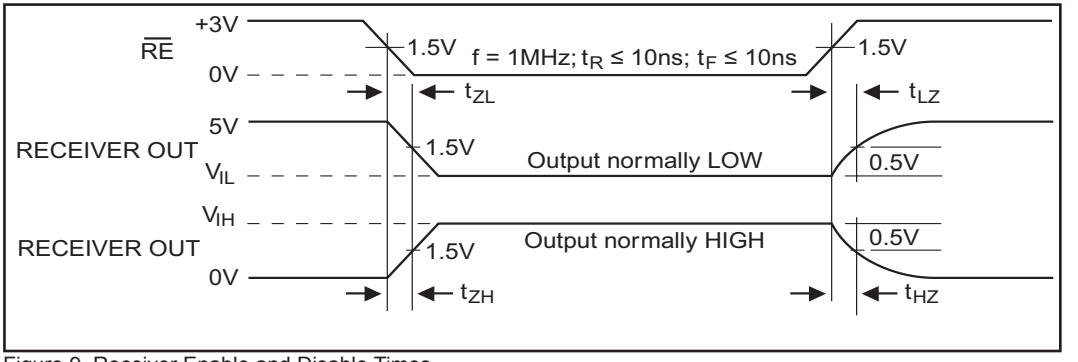


Figure 9. Receiver Enable and Disable Times

The **SP485R** is a low power RS-485 differential transceiver. Similar to the SP485, the **SP485R** contains a half-duplex driver and receiver with tri-state control. However, the **SP485R** is intended for increased connections on a single bus compared to the original RS-485 specifcation.

The RS-485 standard is ideal for multi-drop applications where one bus can contain many drivers and/or receivers.The RS-485 standard implementation allows up to 32 transceivers to be connected on to the data bus. RS-485 is also specified for driving higher speeds over long cable lengths of up to 4000 feet. The **SP485R** exceeds the standard by allowing up to 400 receivers to share the bus

DRIVERS

The driver output complies with the RS-485 electrical characteristics as specified by the standard. The output swings from 0V to Vcc and maintains greater than +1.5V with a 54Ω load attached between the two outputs. In adhering to the RS-485 specification, the driver outputs inherently comply with the RS-422 standard. With a load of 100Ω between the two outputs, the driver can sustain at least +2.0V.

The driver contains an enable pin (DE) which tri-states the output when DE is logic LOW. The outputs during the tri-state condition are at high impedance (>100kΩ). A logic HIGH enables the driver for normal operation. The driver can operate to at least 5Mbps.

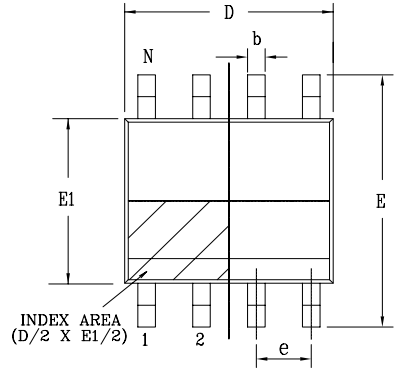
RECEIVERS

The **SP485R** receiver has differential inputs with an input sensitivity of lower than ±200mV. As mentioned above, the RS-485 specification allows up to 32 transceivers on the same bus. The **SP485R** allows over 400 transceivers on the same bus due to its high impedance of at least 120kΩ. This higher capacity allows more components to be attached to the same bus without degrading the signal quality. The drivers are still able to drive an equivalent 54Ω from the 320 transceivers with an input impedance of at least 120kΩ in parallel along with the two 125Ω cable termination resistors on each end.

The receiver contains an enable pin ($\overline{RE}$) which enables the receiver when a logic LOW is asserted. A logic HIGH will tri-state the receiver output and the inputs will maintain at least 120kΩ impedance. The reciever can operate to at least 1Mbps

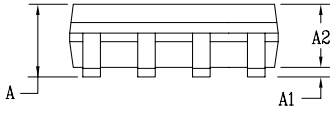
The receiver also contains a fail-safe feature which outputs a logic HIGH when the inputs are open as in a disconnected cable.

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/16/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	CHANGE DRAWING LOGO ADN COMPANY NAME	11/16/07	JL

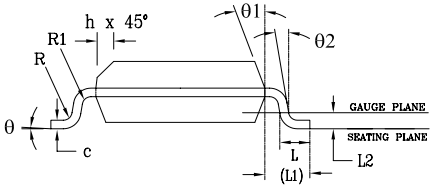


Top View

8 Pin SOICN JEDEC MS-012 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		



Side View

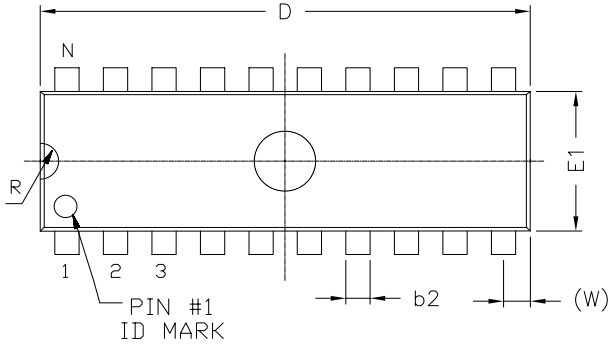


Front View

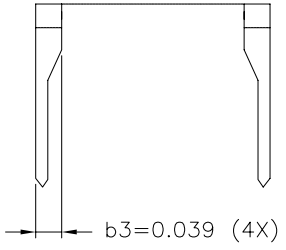
EXAR Powering Connectivity	EXAR CORPORATION		
	8 PIN SOICN PACKAGE OUTLINE		
Packaging Approval:		Drawing No:	8-PIN SOICN
By: JL	Date: 11/16/07	Revision: C	Sheet: 1 OF 1

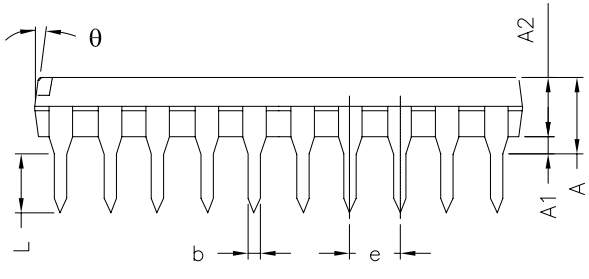
REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	04/26/06	JL
B	CHNAGE DRAWING LOGO AND COMPANY NAME	11/28/07	JL

REMARKS:
FOR 8LD AND 16LD
ALL END LEADS (4X)
ARE HALF LEAD TYPES

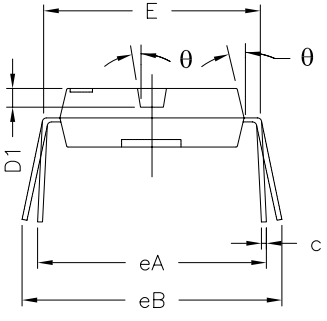


Top View





Side View



Front View

8 Pin PDIP JEDEC MS-001 Variation BA						
SYMBOLS	DIMENSIONS IN INCH (Control Unit)			DIMENSIONS IN MM (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	0.210	—	—	5.33
A1	0.015	—	—	0.38	—	—
A2	0.115	0.130	0.195	2.92	3.30	4.95
b	0.014	0.018	0.022	0.36	0.46	0.56
b2	0.045	0.060	0.070	1.14	1.52	1.78
c	0.008	0.010	0.014	0.20	0.25	0.36
D1	0.030	—	0.060	0.76	—	1.52
E	0.300	0.310	0.325	7.62	7.87	8.26
E1	0.240	0.250	0.280	6.10	6.35	7.11
e	0.100 BSC			2.54 BSC		
eA	0.300 BSC			7.62 BSC		
eB	—	—	0.430	—	—	10.92
L	0.115	0.130	0.150	2.92	3.30	3.81
W	0.075 REF			1.91 REF		
R	0.030 BSC			0.76 BSC		
θ	4°	7°	10°	4°	7°	10°
D	0.355	0.365	0.400	9.02	9.27	10.16
N	8			8		

EXAR Powering Connectivity	EXAR CORPORATION		
	8 PIN PDIP PACKAGE OUTLINE		
Packaging Approval:	Drawing No: 8-PIN PDIP		
By: JL / Date: 11/28/07	Revision: B	Sheet: 1 OF 1	

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP485RCN-L	0°C to +70°C	8-pin NSOIC
SP485RCN-L/TR	0°C to +70°C	8-pin NSOIC
SP485RCP-L	0°C to +70°C	8-pin PDIP
SP485REN-L	-40°C to +85°C	8-pin NSOIC
SP485REN-L/TR	-40°C to +85°C	8-pin NSOIC
SP485REP-L	-40°C to +85°C	8-pin PDIP

Note: /TR = Tape and Reel

REVISION HISTORY

DATE	REVISION	DESCRIPTION
06/21/04	--	Legacy Sipex Datasheet
07/23/09	1.0.0	Convert to Exar Format. Update ordering information as a result of discontinued Lead type package options per PDN 081126-01. Remove all reference to the discontinued SP481R.

Datasheet July 2009

Send your Interface technical inquiry with technical details to: uarttechsupport@exar.com