ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}.....-0.3V to +6.0V
V+ (NOTE 1).....-0.3V to +7.0V
V- (NOTE 1).....+0.3V to -7.0V
V+ + |V-| (NOTE 1).....+13V
I_{CC} (DC V_{CC} or GND current).....±100mA

Input Voltages
TxIN, $\overline{\text{ONLINE}}$, $\overline{\text{SHUTDOWN}}$, ...-0.3V to Vcc + 0.3V
RxIN.....±25V
Output Voltages
TxOUT.....±13.2V
RxOUT, $\overline{\text{STATUS}}$.....-0.3V to (V_{CC} +0.3V)
Short-Circuit Duration
TxOUT.....Continuous
Storage Temperature.....-65°C to +150°C

Power Dissipation per package
28-pin SSOP (derate 11.2mW/°C above +70°C).....900mW
28-pin TSSOP (derate 13.2mW/°C above +70°C).....1100mW

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V to +5.5V, C1 - C4 = 0.1µF (tested at 3.3V +/-5%), C1 - C4 = 0.22µF (tested at 3.3V +/-10%), C1 = 0.047µF and C2 - C4 = 0.33µF (tested at 5.0V +/-10%), T_{AMB} = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = 25°C

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current, AUTO ON-LINE®		1.0	10	µA	All RxIN open, $\overline{\text{ONLINE}}$ = GND, $\overline{\text{SHUTDOWN}}$ = V_{CC}, TxIN = GND or V_{CC}
Supply Current, Shutdown		1.0	10	µA	$\overline{\text{SHUTDOWN}}$ = GND, TxIN = Vcc or GND
Supply Current AUTO ON-LINE® Disabled		0.3	1.0	mA	$\overline{\text{ONLINE}}$ = $\overline{\text{SHUTDOWN}}$ = Vcc, no load, TxIN = GND or V_{CC}
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW HIGH	 2.4		0.8	 V V	V_{CC} = +3.3V or +5.0V, TxIN $\overline{\text{ONLINE}}$, $\overline{\text{SHUTDOWN}}$
Input Leakage Current		±0.01	±1.0	µA	TxIN, $\overline{\text{ONLINE}}$, $\overline{\text{SHUTDOWN}}$, T_{AMB} = +25°C
Output Leakage Current		±0.05	±10	µA	Receivers disabled
Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
Output Voltage HIGH	V_{CC} -0.6	V_{CC} -0.1		V	I_{OUT} = -1.0mA
DRIVER OUTPUTS					
Output Voltage Swing	±5.0	±5.4		V	All driver outputs loaded with 3KΩ to GND

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ELECTRICAL CHARACTERISTICS

V_{CC} = +3.0V to +5.5V, C1 - C4 = 0.1µF (tested at 3.3V +/-5%), C1 - C4 = 0.22µF (tested at 3.3V +/-10%), C1 = 0.047µF and C2 - C4 = 0.33µF (tested at 5.0V +/-10%), $T_{AMB} = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = 25°C

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER OUTPUTS (continued)					
Output Resistance	300			Ω	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V
Output Short-Circuit Current		±35	±60	mA	V_{OUT} = 0V
RECEIVER INPUTS					
Input Voltage Range	-25		25	V	
Input Threshold LOW	0.6	1.2		V	Vcc = 3.3V
Input Threshold LOW	0.8	1.5		V	Vcc = 5.0V
Input Threshold HIGH		1.5	2.4	V	Vcc = 3.3V
Input Threshold HIGH		1.8	2.4	V	Vcc = 5.0V
Input Hysteresis		0.5		V	
Input Resistance	3	5	7	kΩ	
AUTO ON-LINE® CIRCUITRY CHARACTERISTICS ($\overline{ONLINE}$ = GND, $\overline{SHUTDOWN}$ = VCC)					
$\overline{STATUS}$ Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
$\overline{STATUS}$ Output Voltage HIGH	V_{CC} -0.6			V	I_{OUT} = -1.0mA
Receiver Threshold to Drivers Enabled (t_{ONLINE})		200		µs	Figure 10
Receiver Positive or Negative Threshold to $\overline{STATUS}$ HIGH (t_{STSH})		0.5		µs	Figure 10
Receiver Positive or Negative Threshold to $\overline{STATUS}$ LOW (t_{STSL})		20		µs	Figure 10
TIMING CHARACTERISTICS					
Maximum Data Rate	250			kbps	R_L = 3KΩ, C_L = 1000pF, one driver switching
Receiver Propagation Delay t_{PHL} t_{PLH}		 0.15 0.15		µs	 Receiver input to Receiver output, C_L = 150pF
Receiver Output Enable Time		200		ns	Normal operation
Receiver Output Disable Time		200		ns	Normal operation
Driver Skew		100		ns	$\lvert t_{PHL} - t_{PLH} \rvert$, T_{AMB} = 25°C
Receiver Skew		50		ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Transition-Region Slew Rate			30	V/µs	Vcc = 3.3V, R_L = 3kΩ, T_{AMB} = 25°C, measurements taken from -3.0V to +3.0V or +3.0V to -3.0V

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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 250kbps data rate, all drivers loaded with 3kΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

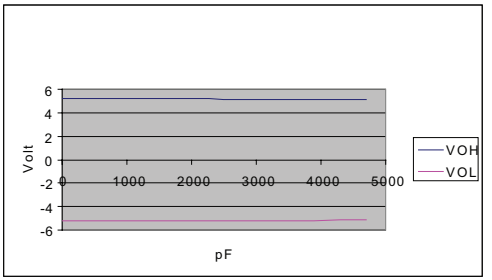

Figure 1. Transmitter Output Voltage VS. Load Capacitance

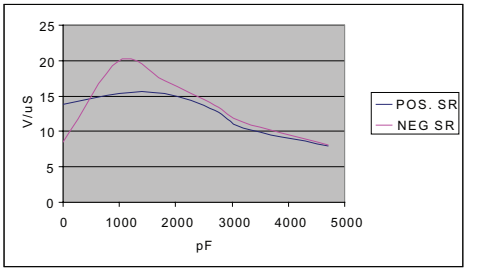

Figure 2. Slew Rate VS. Load Capacitance

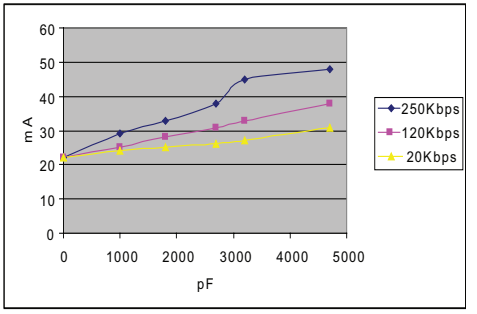

Figure 3. Supply Current VS. Load Capacitance when Transmitting Data

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NAME	FUNCTION	PIN NUMBER
C2+	Positive terminal of the symmetrical charge-pump capacitor C2.	1
GND	Ground.	2
C2-	Negative terminal of the symmetrical charge-pump capacitor C2.	3
V-	Regulated -5.5V output generated by the charge pump.	4
T_1OUT	RS-232 Driver Output.	5
T_2OUT	RS-232 Driver Output.	6
T_3OUT	RS-232 Driver Output.	7
R_1IN	RS-232 receiver input.	8
R_2IN	RS-232 receiver input.	9
T_4OUT	RS-232 Driver Output.	10
R_3IN	RS-232 receiver input.	11
T_5OUT	RS-232 Driver Output.	12
$\overline{\text{ONLINE}}$	Apply logic HIGH to override **AUTO ON-LINE®** circuitry keeping drivers active ($\overline{\text{SHUTDOWN}}$ must also be logic HIGH, refer to Table 2).	13
$\overline{\text{SHUTDOWN}}$	Apply logic LOW to shut down drivers and charge pump. This overrides all **AUTO ON-LINE®** circuitry and $\overline{\text{ONLINE}}$ (Refer to table 2).	14
$\overline{\text{STATUS}}$	TTL/CMOS Output indicating if a RS-232 signal is present on any receiver input.	15
$\overline{R_1\text{OUT}}$	Non-Inverting receiver - 1 output, active in shutdown.	16
T_5IN	TTL/CMOS driver input.	17
R_3OUT	TTL/CMOS receiver output.	18
T_4IN	TTL/CMOS driver input.	19
R_2OUT	TTL/CMOS receiver output.	20
R_1OUT	TTL/CMOS receiver output.	21
T_3IN	TTL/CMOS driver input.	22
T_2IN	TTL/CMOS driver input.	23
T_1IN	TTL/CMOS driver input.	24
C1-	Negative terminal of the symmetrical charge-pump capacitor C1.	25
Vcc	+3.0V to +5.5V supply voltage.	26
V+	Regulated +5.5V output generated by the charge pump.	27
C1+	Positive terminal of the symmetrical charge-pump capacitor C1.	28

Table 1. Device Pin Description

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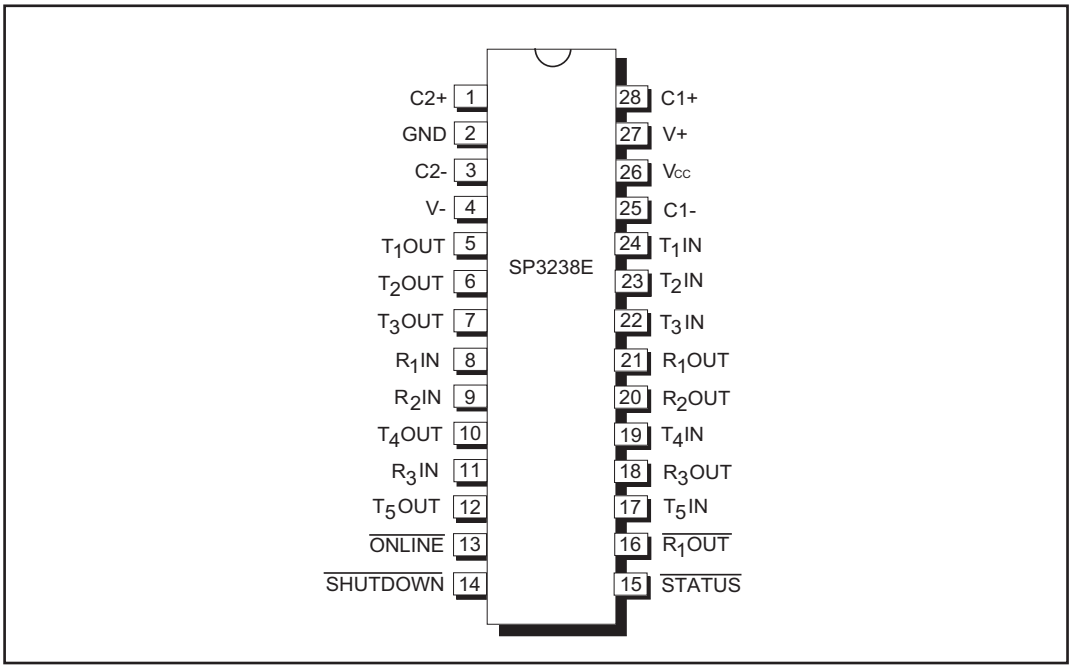

Figure 4. SP3238E Pinout Configuration

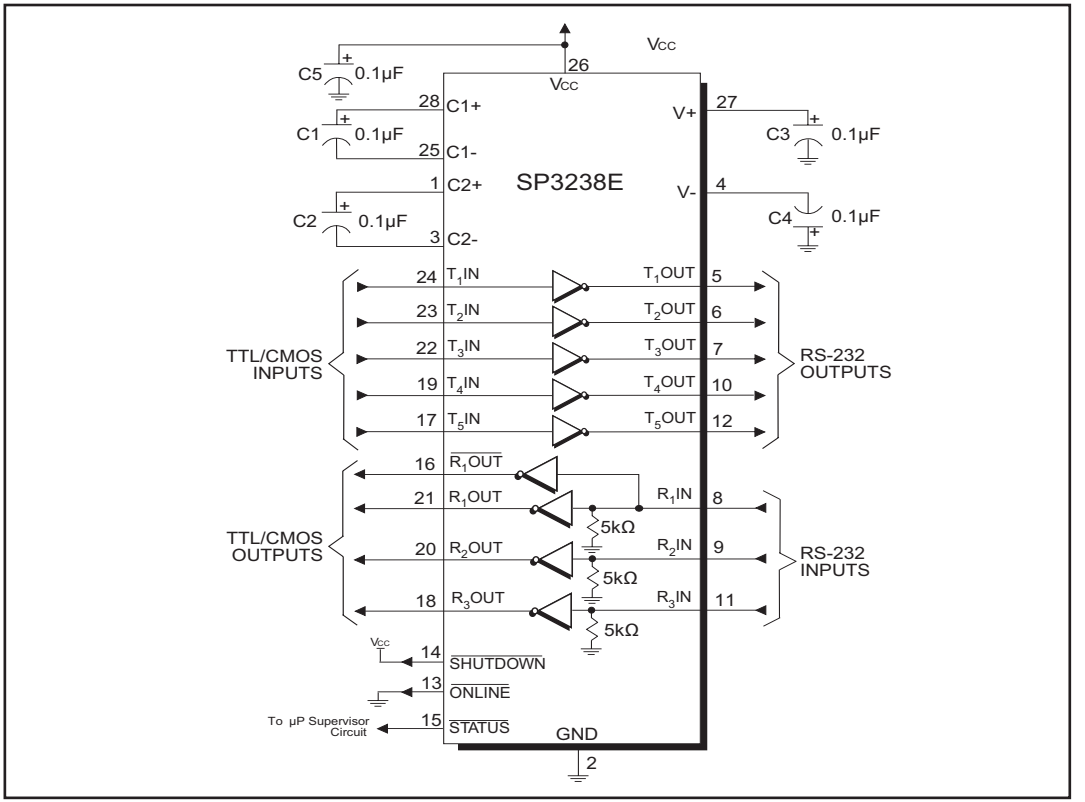

Figure 5. SP3238E Typical Operating Circuit

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DESCRIPTION

The SP3238E device meets the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The SP3238E devices feature Exar's proprietary and patented (U.S.-- 5,306,954) on-board charge pump circuitry that generates ±5.5V RS-232 voltage levels from a single +3.0V to +5.5V power supply. The SP3238E devices can guarantee a data rate of 250kbps fully loaded.

The SP3238E is a 5-driver/3-receiver device, ideal for portable or hand-held applications. The SP3238E includes one complementary always-active receiver that can monitor an external device (such as a modem) in shutdown. This aids in protecting the UART or serial controller IC by preventing forward biasing of the protection diodes where V_{CC} may be disconnected.

The SP3238E device is an ideal choice for power sensitive designs. The SP3238E device features **AUTO ON-LINE®** circuitry which reduces the power supply drain to a 1µA supply current.

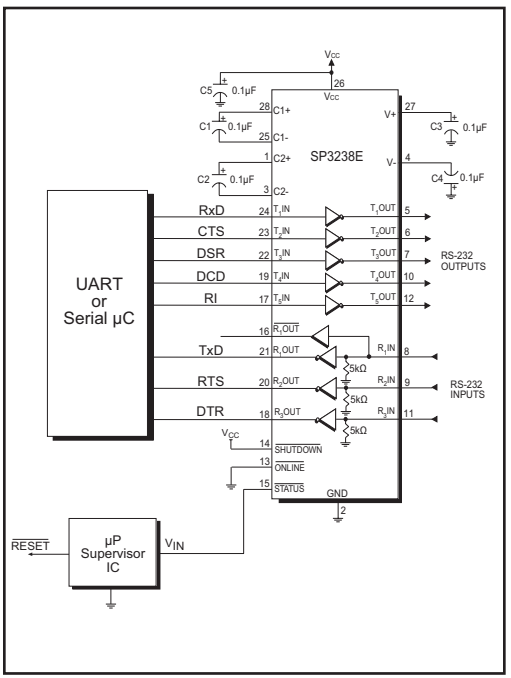

Figure 6. Interface Circuitry Controlled by Microprocessor Supervisory Circuit

In many portable or hand-held applications, an RS-232 cable can be disconnected or a connected peripheral can be turned off. Under these conditions, the internal charge pump and the drivers will be shut down. Otherwise, the system automatically comes online. This feature allows design engineers to address power saving concerns without major design changes.

THEORY OF OPERATION

The SP3238E device is made up of four basic circuit blocks:

1. Drivers
2. Receivers
3. The Exar proprietary charge pump, and
4. **AUTO ON-LINE®** circuitry.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is ±5.4V with no load and ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232-F and all previous RS-232 versions.

The drivers can guarantee a data rate of 250kbps fully loaded with 3kΩ in parallel with 1000pF, ensuring compatibility with PC-to-PC communication software. All unused drivers inputs should be connected to GND or V_{CC}.

The slew rate of the driver output is internally limited to a maximum of 30V/µs in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

Figure 7 shows a loopback test circuit used to test the RS-232 drivers. Figure 8 shows the test results of the loopback circuit with all five drivers active at 120kbps with typical RS-232 loads in parallel with 1000pF capacitors. Figure 9 shows the test results where one driver was active at 250kbps and all five drivers loaded with an RS-232 receiver in parallel with a 1000pF capacitor. A solid RS-232 data transmission rate of 120kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

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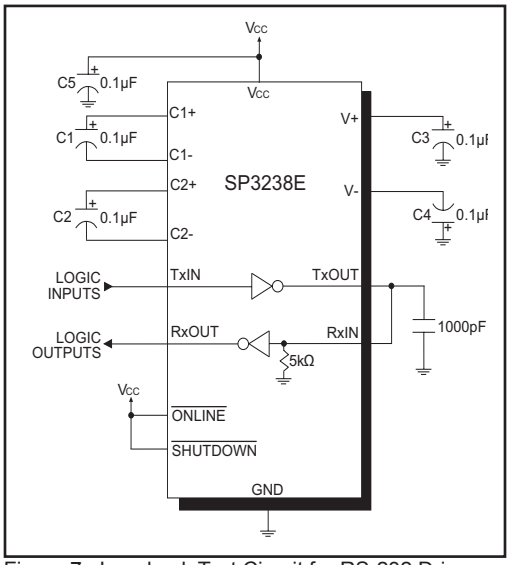

Figure 7. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

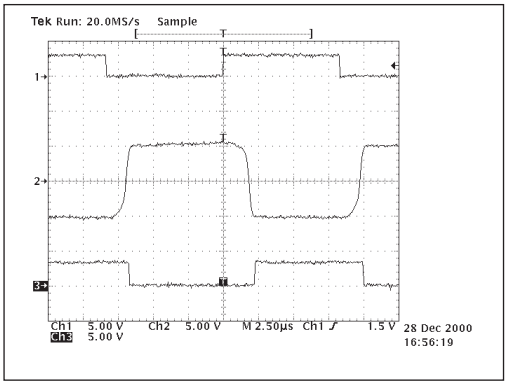

Figure 8. Loopback Test results at 120kbps (All Drivers Fully Loaded)

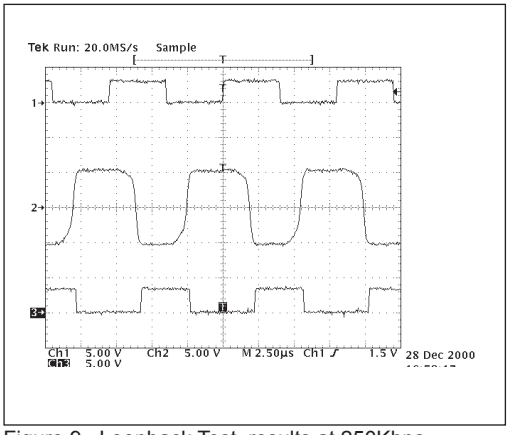

Figure 9. Loopback Test results at 250Kbps (All Drivers Fully Loaded)

Receivers

The receivers convert ±5.0V EIA/TIA-232 levels to TTL or CMOS logic output levels. Receivers are High-Z when the AUTO ON-LINE® circuitry is enabled or when in shutdown.

The SP3238E includes an additional non-inverting receiver with an output $\overline{R_1OUT}$. $\overline{R_1OUT}$ is an extra output that remains active and monitors activity while the other receiver outputs are forced into high impedance. This allows a Ring Indicator (RI) signal from a peripheral to be monitored without forward biasing the TTL/CMOS inputs of the other devices connected to the receiver outputs.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5kΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump is an Exar–patented design (U.S. 5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

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The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC}, in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 500kHz. The external capacitors can be as low as 0.1µF with a 16V breakdown voltage rating.

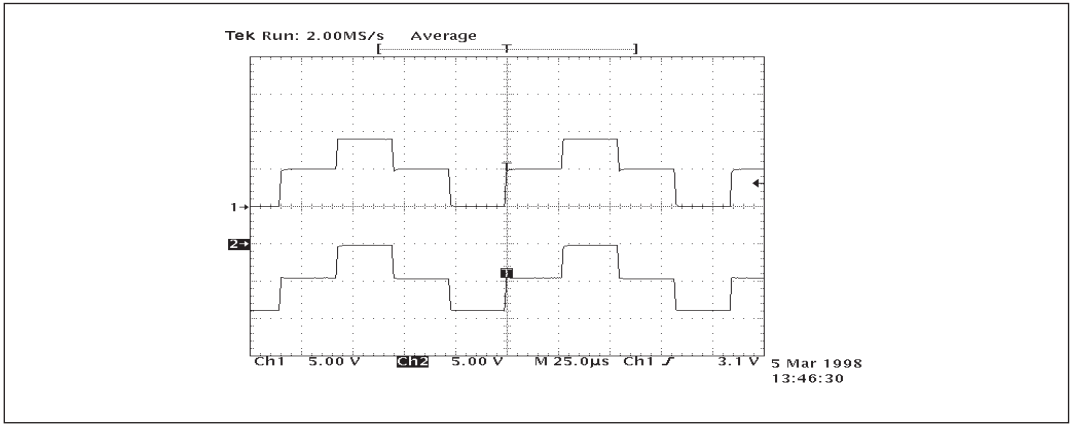

Figure 10. Charge Pump Waveform

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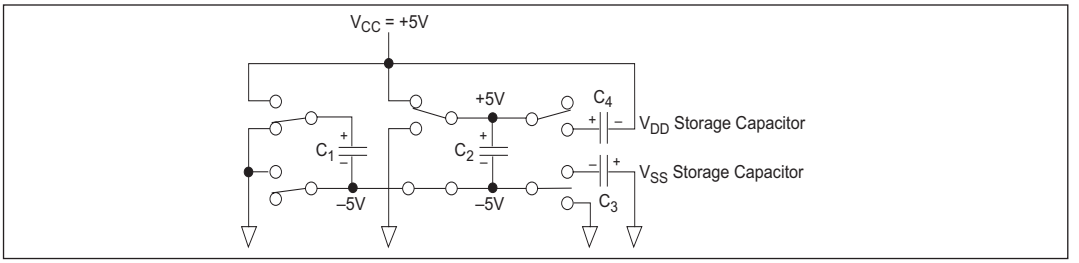

Figure 11. Charge Pump — Phase 1

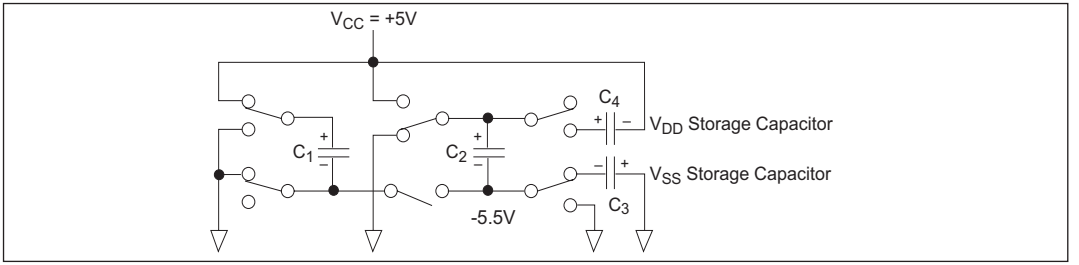

Figure 12. Charge Pump — Phase 2

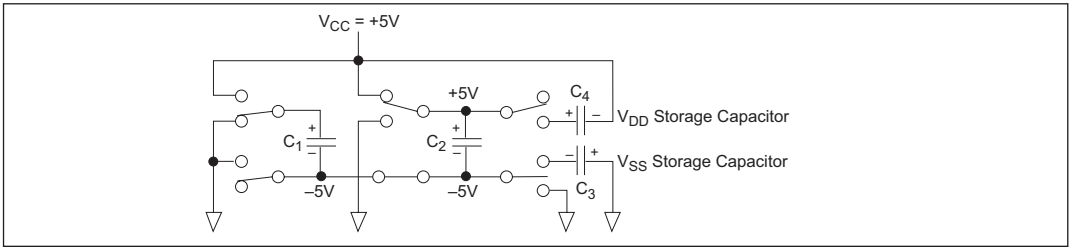

Figure 13. Charge Pump — Phase 3

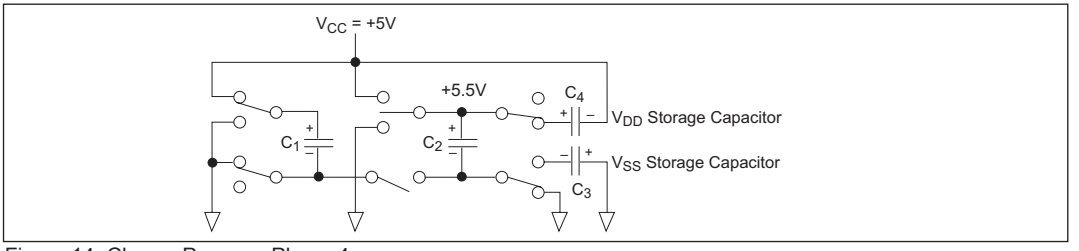

Figure 14. Charge Pump — Phase 4

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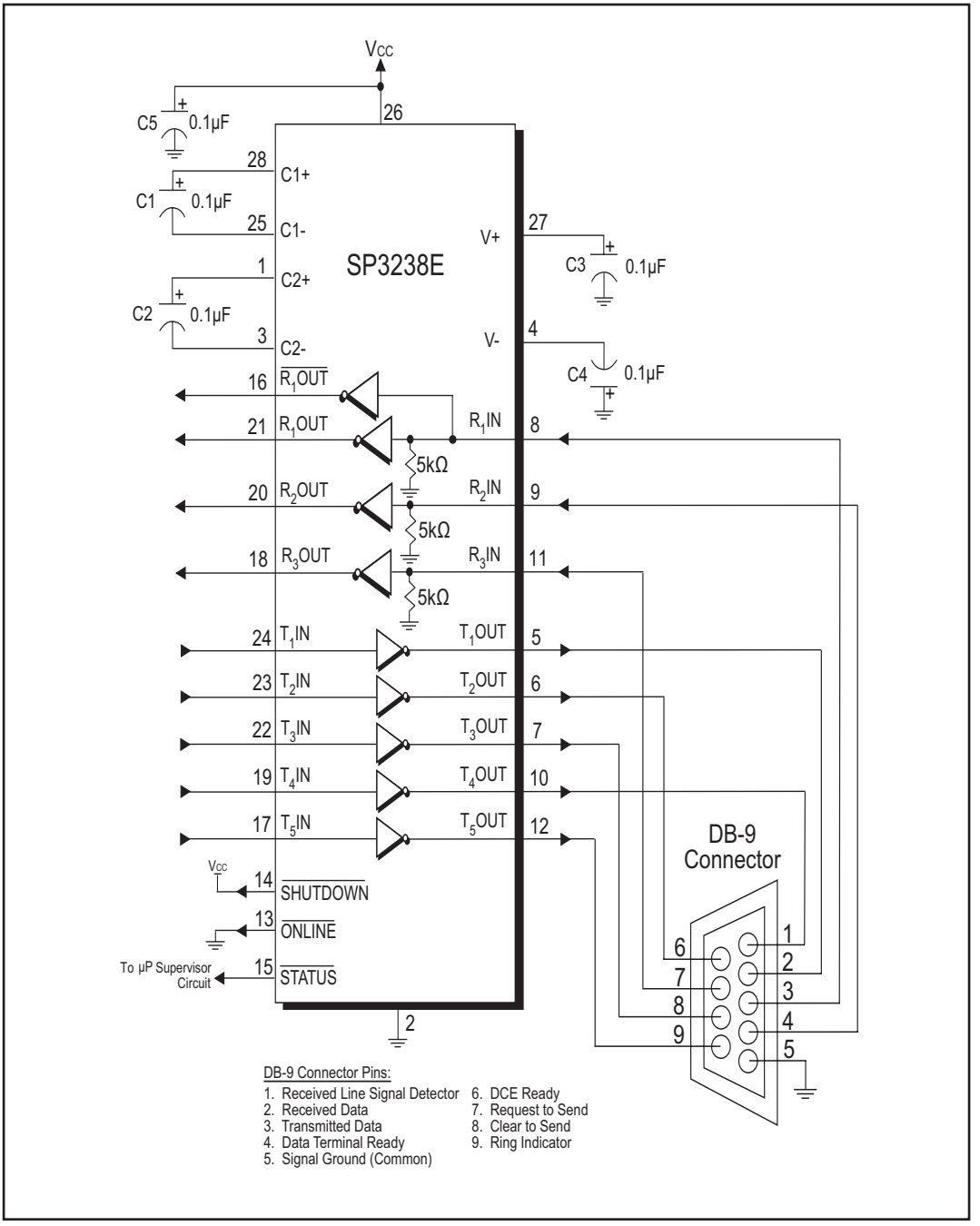

Figure 15. Circuit for the connectivity of the SP3238E with a DB-9 connector

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The SP3238E device has a patent pending **AUTO ON-LINE®** circuitry on board that saves power in applications such as laptop computers, palmtop (PDA) computers and other portable systems.

The SP3238E device incorporates an **AUTO ON-LINE®** circuit that automatically enables itself when the external transmitters are enabled and the cable is connected. Conversely, the **AUTO ON-LINE®** circuit also disables most of the internal circuitry when the device is not being used and goes into a standby mode where the device typically draws 1µA. This function is externally controlled by the $\overline{\text{ONLINE}}$ pin. When this pin is tied to a logic LOW, the **AUTO ON-LINE®** function is active. Once active, the device is enabled until there is no activity on the receiver inputs. The receiver input typically sees at least ±3V, which are generated from the transmitters at the other end of the cable with a ±5V minimum. When the external transmitters are disabled or the cable is disconnected, the receiver inputs will be pulled down by their internal 5kΩ resistors to ground. When this occurs over a period of time, the internal transmitters will be disabled and the device goes into a shutdown or standby mode. When $\overline{\text{ONLINE}}$ is HIGH, the **AUTO ON-LINE®** mode is disabled.

The **AUTO ON-LINE®** circuit has two stages:

1) Inactive Detection
2) Accumulated Delay

The first stage, shown in Figure 17, detects an inactive input. A logic HIGH is asserted on R_XINACT if the cable is disconnected or the external transmitters are disabled. Otherwise, R_XINACT will be at a logic LOW. This circuit is duplicated for each of the other receivers.

The second stage of the **AUTO ON-LINE®** circuitry, shown in Figure 18, processes all the receiver's R_XINACT signals with an accumulated delay that disables the device to a 1µA supply current. The $\overline{\text{STATUS}}$ pin goes to a logic LOW when the cable is disconnected, the external transmitters are disabled, or the $\overline{\text{SHUTDOWN}}$ pin is invoked. The typical accumulated delay is around 20µs. When the SP3238E drivers or internal charge pump are disabled, the supply current is reduced to 1µA. This can commonly occur in handheld or portable applications where the RS-232 cable is disconnected or the RS-232 drivers of the connected peripheral are turned off.

The **AUTO ON-LINE®** mode can be disabled by the $\overline{\text{SHUTDOWN}}$ pin. If this pin is a logic LOW, the **AUTO ON-LINE®** function will not operate regardless of the logic state of the $\overline{\text{ONLINE}}$ pin. *Table 3* summarizes the logic of the **AUTO ON-LINE®** operating modes.

The $\overline{\text{STATUS}}$ pin outputs a logic LOW signal if the device is shutdown. This pin goes to a logic HIGH when the external transmitters are enabled and the cable is connected.

When the SP3238E device is shutdown, the charge pumps are turned off. V+ charge pump output decays to V_{CC}, the V- output decays to GND. The decay time will depend on the size of capacitors used for the charge pump. Once in shutdown, the time required to exit the shut down state and have valid V+ and V- levels is typically 200ms.

For easy programming, the $\overline{\text{STATUS}}$ can be used to indicate DTR or a Ring Indicator signal. Tying $\overline{\text{ONLINE}}$ and $\overline{\text{SHUTDOWN}}$ together will bypass the **AUTO ON-LINE®** circuitry so this connection acts like a shutdown input pin

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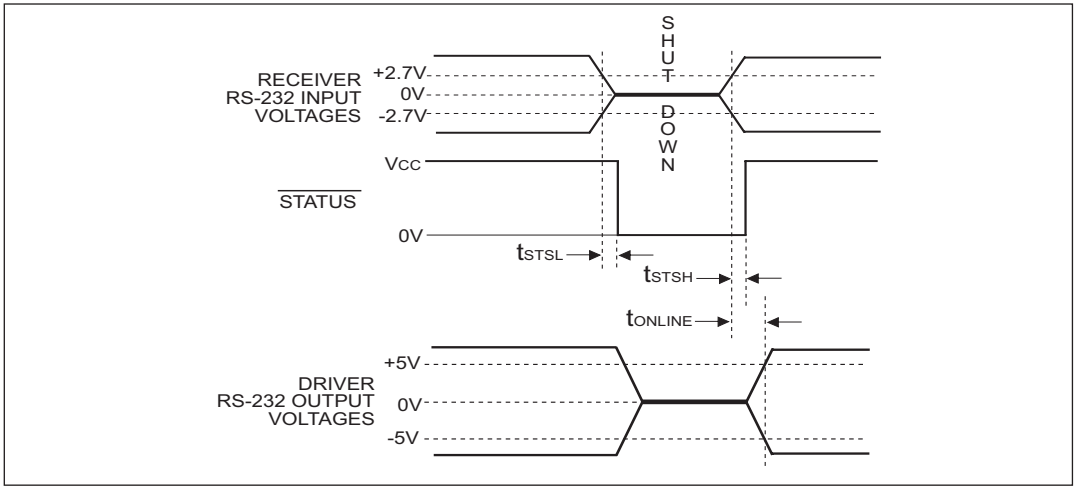

Figure 16. **AUTO ON-LINE®** Timing Waveforms

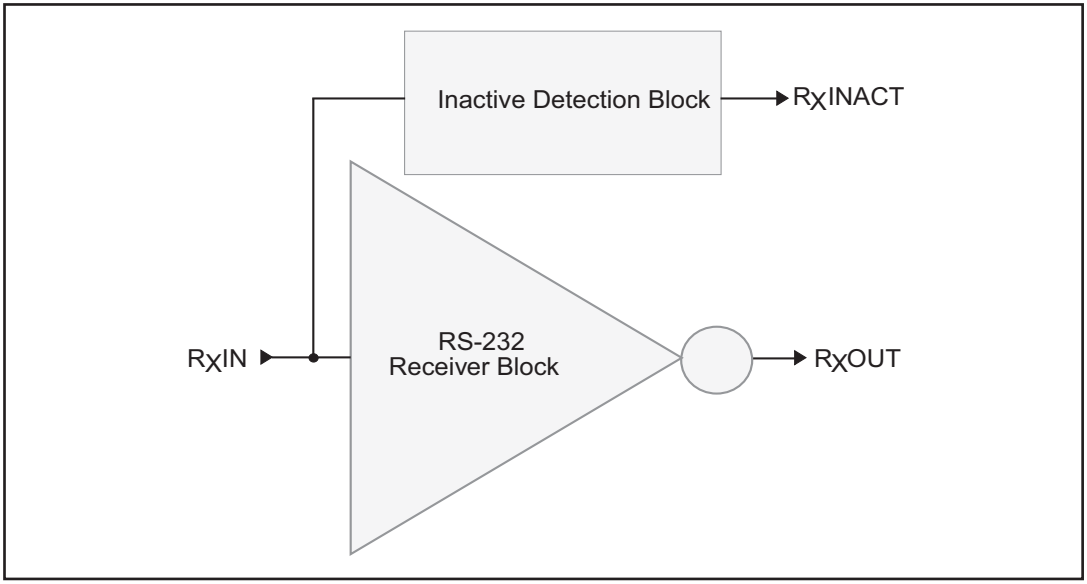

Figure 17. Stage I of **AUTO ON-LINE®** Circuitry

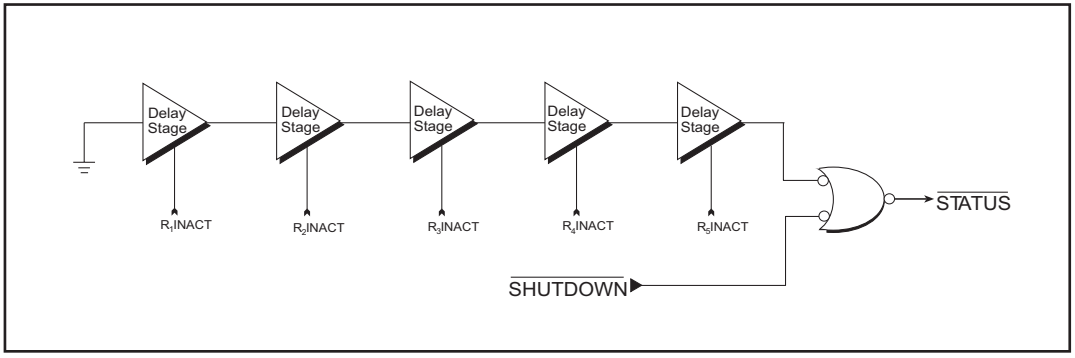

Figure 18. Stage II of **AUTO ON-LINE®** Circuitry

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$\overline{\text{SHUTDOWN}}$ **INPUT**	$\overline{\text{ONLINE}}$ **INPUT**	RS-232 SIGNAL AT **RECEIVER INPUT**	$\overline{\text{STATUS}}$ **OUTPUT**	T_XOUT	R_XOUT	$\overline{R_1}$OUT	TRANSCEIVER **STATUS**
HIGH	-	YES	HIGH	Active	Active	Active	Normal Operation
HIGH	HIGH	NO	LOW	Active	Active	Active	Normal Operation
HIGH	LOW	NO (>100µs)	LOW	High-Z	Active	Active	Shutdown (Auto-Online)
LOW	-	YES	HIGH	High-Z	High-Z	Active	Shutdown
LOW	-	NO	LOW	High-Z	High-Z	Active	Shutdown

Table 2. AUTO ON-LINE® Logic

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ESD TOLERANCE

The SP3238E device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV without damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC61000-4-2 Air-Discharge
c) IEC61000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semi-conductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 19. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the IC's tend to be handled frequently.

The IEC-61000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC61000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC61000-4-2 is shown on Figure 20. There are two methods within IEC61000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

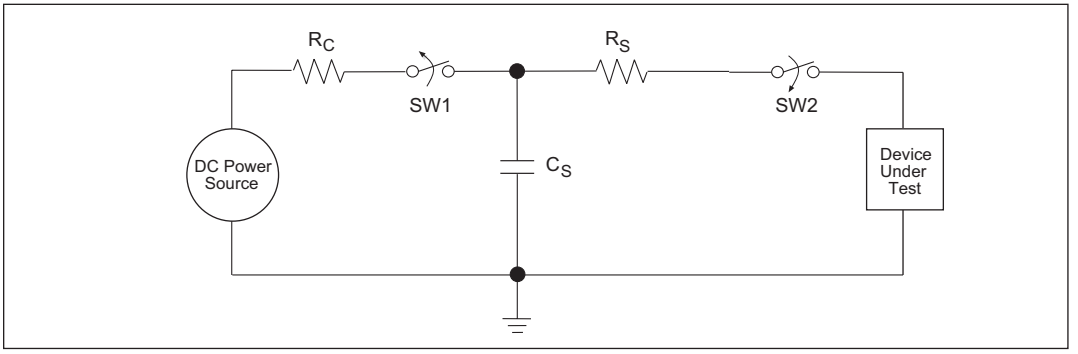

Figure 19. ESD Test Circuit for Human Body Model

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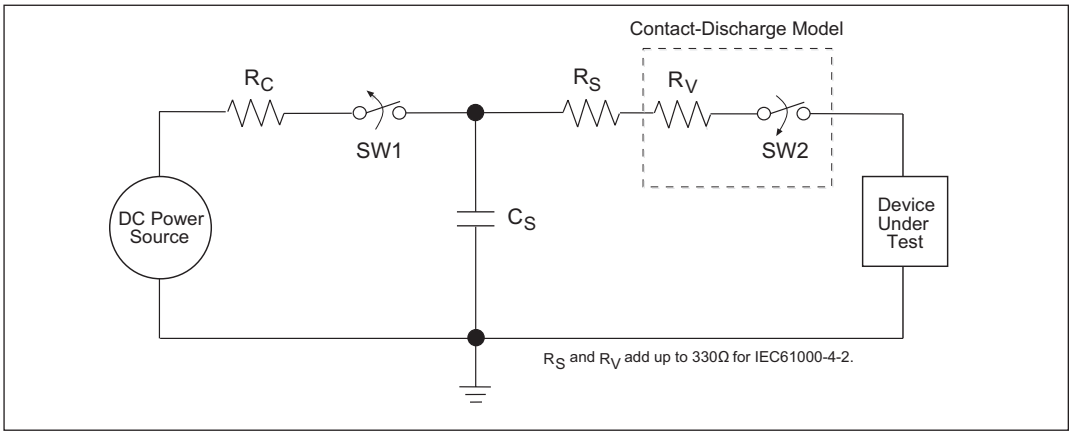

Figure 20. ESD Test Circuit for IEC61000-4-2

The circuit models in Figures 19 and 20 represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For IEC-61000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

The higher C_S value and lower R_S value in the IEC61000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

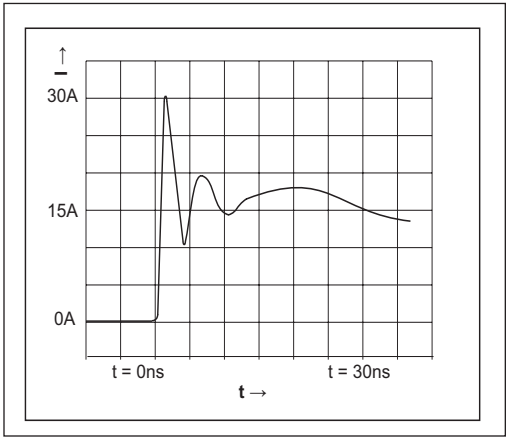

Figure 21. ESD Test Waveform for IEC61000-4-2

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC61000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

Table 3. Transceiver ESD Tolerance Levels

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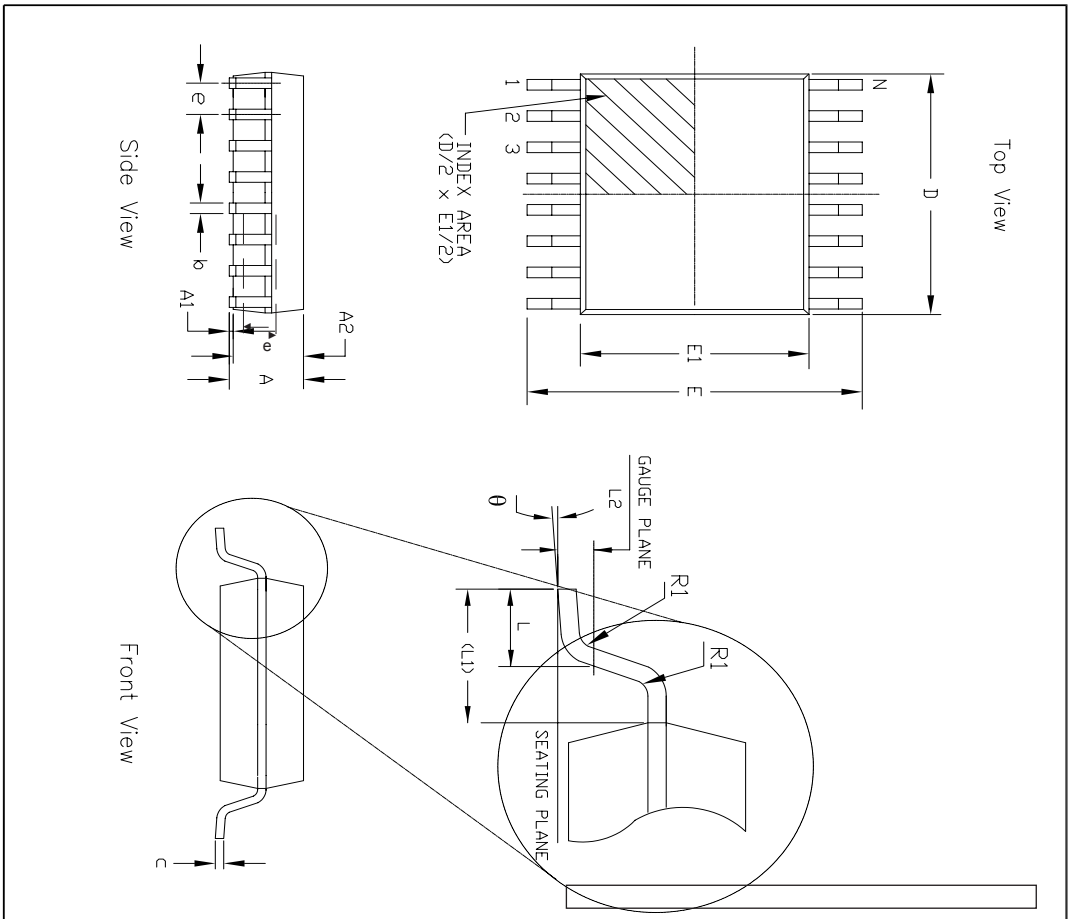

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	04/24/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/28/07	JL

28 Pin SSOP JEDEC MO-150 Variation AH

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e		0.65 BSC			0.026 BSC	
L	0.55	0.75	0.95	0.022	0.030	0.037
L1		1.25 REF			0.049 REF	
L2		0.25 BSC			0.010 BSC	
R1	0.09	—	—	0.004	—	—
θ	0°	4°	8°	0°	4°	8°
D	9.90	10.20	10.50	0.390	0.402	0.413
N	28			28		

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28 PIN SSOP PACKAGE OUTLINE

Packaging Approval:	Drawing No:	28-PIN SSOP
By: JL / Date: 11/28/07	Revision: B	Sheet: 1 OF 1

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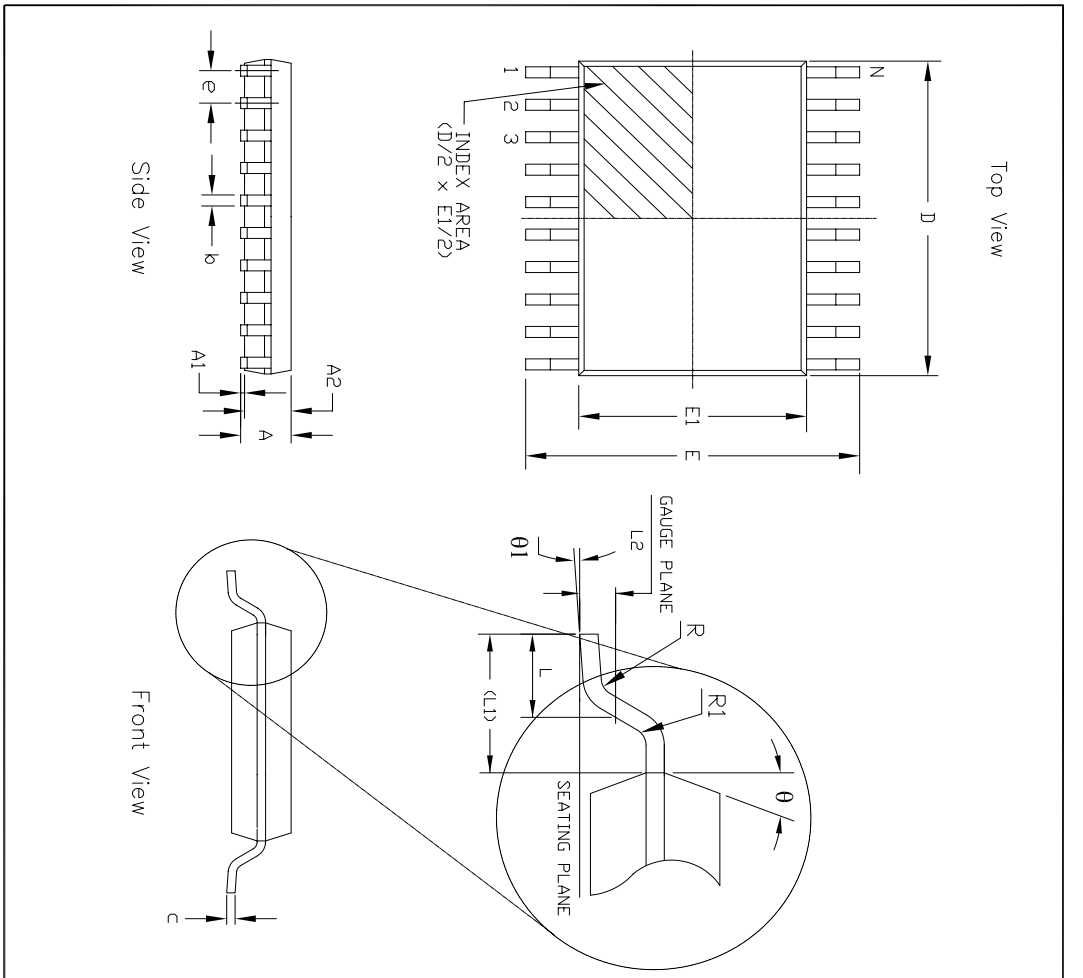

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORGINATION	04/19/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/28/07	JL

28 Pin TSSOP JEDEC MO-153 Variation AE

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
c	0.09	—	0.20	0.004	—	0.008
E		6.40 BSC			0.252 BSC	
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65 BSC			0.026 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF			0.039 REF	
L2		0.25 BSC			0.010 BSC	
R	0.09	—	—	0.035	—	—
R1	0.09	—	—	0.035	—	—
θ		12° REF			12° REF	
θ1	0°	—	8°	0°	—	8°
D	9.60	9.70	9.80	0.378	0.382	0.386
N		28			28	

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28 PIN TSSOP PACKAGE OUTLINE

Packaging Approval:		Drawing No:	28-PIN TSSOP
By: JL	Date: 11/28/07	Revision: B	Sheet: 1 OF 1

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Part Number	Temp. Range	Package
SP3238ECA-L	0C to +70C	28 Pin SSOP
SP3238ECA-L/TR	0C to +70C	28 Pin SSOP
SP3238ECY-L	0C to +70C	28 Pin TSSOP
SP3238ECY-L/TR	0C to +70C	28 Pin TSSOP
SP3238EEA-L	-40C to +85C	28 Pin SSOP
SP3238EEA-L/TR	-40C to +85C	28 Pin SSOP
SP3238EEY-L	-40C to +85C	28 Pin TSSOP
SP3238EEY-L/TR	-40C to +85C	28 Pin TSSOP

For Tape and Reel option add "/TR", Example: SP3238ECA-L/TR.

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REVISION HISTORY

DATE	REVISION	DESCRIPTION
03/04/05	--	Legacy Sipex Datasheet
02/01/11	1.0.0	Convert to Exar Format, Update ordering information and change ESD specification to IEC61000-4-2

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