Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Max	Units
Input Voltage	V_{IN}	7	V
Power Dissipation	P_D	Internally Limited	W
Thermal Resistance Junction to Ambient SOIC-8EDP(1)	θ_{JA}	36	°C/W
Thermal Resistance Junction to Case SOIC-8EDP(1)	θ_{JC}	5.5	°C/W
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-40 to +150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	V_{ESD}	4	kV

Note: (1) 1 square inch of FR-4, double sided, 1 oz. minimum copper weight.

Electrical Characteristics

Unless specified: $V_{EN} = V_{IN}$. Adjustable Option ($V_{ADJ} > V_{TH(ADJ)}$): V_{IN} = 2.2V to 5.5V and I_O = 10µA to 1A.
Fixed Options (V_{ADJ} = GND): $V_{IN} = (V_O + 0.5V)$ to 5.5V and I_O = 0A to 1A. Values in **bold** apply over T_J = -40°C to 125°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VIN						
Operating Voltage Range	V_{IN}		**2.2**		**5.5**	V
Quiescent Current	I_Q	V_{IN} = 3.3V		0.75	**1.75**	mA
		V_{IN} = 5.5V, V_{EN} = 0V		10	**35**	µA
VO						
Output Voltage(1)	V_O	I_O = 10mA	-1%	V_O	+1%	V
(Internal Fixed Voltage)			**-2%**		**+2%**	
Line Regulation(1)	$REG_{(LINE)}$	I_{OUT} = 10mA		0.035	**0.3**	%
Load Regulation(1)	$REG_{(LOAD)}$	I_{OUT} = 10mA to 1A		0.2	**0.4**	%
Dropout Voltage(1)(2)	V_D	I_O = 10mA		2.5	10	mV
					20	
		I_O = 500mA		90	300	mV
					400	
		I_O = 1A		180	400	mV
					500	

Electrical Characteristics (Cont.)

Unless specified: $V_{EN} = V_{IN}$. Adjustable Option ($V_{ADJ} > V_{TH(ADJ)}$): V_{IN} = 2.2V to 5.5V and I_O = 10µA to 1A.
Fixed Options (V_{ADJ} = GND): $V_{IN} = (V_O + 0.5V)$ to 5.5V and I_O = 0A to 1A. Values in **bold** apply over T_J = -40°C to 125°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VO (Cont.)						
Minimum Load Current(3)	I_O			1	**10**	µA
Current Limit	I_{CL}		**1.6**	1.33	**3.5**	A
ADJ						
Reference Voltage(1)	V_{REF}	V_{IN} = 2.2V, $V_{ADJ} = V_{OUT}$, I_O = 10mA	1.188	1.200	1.212	V
			1.176		**1.224**	
Adjust Pin Current(4)	I_{ADJ}	$V_{ADJ} = V_{REF}$		30	**200**	nA
Adjust Pin Threshold(5)	$V_{TH(ADJ)}$		**0.05**	0.20	**0.40**	V
EN						
Enable Pin Current	I_{EN}	V_{EN} = 0V, V_{IN} = 3.3V		1.5	**10**	µA
Enable Pin Threshold	V_{IH}	V_{IN} = 3.3V	**1.6**			V
	V_{IL}	V_{IN} = 3.3V			**0.4**	
Over Temperature Protection						
High Trip level	T_{HI}			170		°C
Hysteresis	T_{HYST}			20		°C

Notes:
(1) Low duty cycle pulse testing with Kelvin connections required.
(2) Defined as the input to output differential at which the output voltage drops to 1% below the value measured at a differential of 0.7V.
(3) Required to maintain regulation. Voltage set resistors R1 and R2 are usually utilized to meet this requirement. Adjustable versions only.
(4) Guaranteed by design.
(5) When V_{ADJ} exceeds this threshold, the “Sense Select” switch disconnects the internal feedback chain from the error amplifier and connects V_{ADJ} instead.

Ordering Information

Part Number	Package	Temp. Range (T_A)
SC4205IS-X.XTR(1)(2)	SOIC-8EDP	-40 to +85 °C
SC4205IS-X.XTRT(1)(2)(3)		
SC4205EVB	Evaluation Board	

Notes:

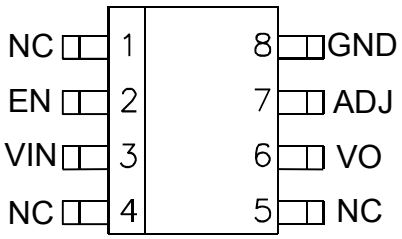
(1) Where -X.X denotes voltage options. Available voltages are: 2.5V and 1.8V. Output voltage can be adjusted using external resistors, see Pin Descriptions on page 5.

(2) Only available in tape and reel packaging. A reel contains 2500 devices.

(3) Lead free product

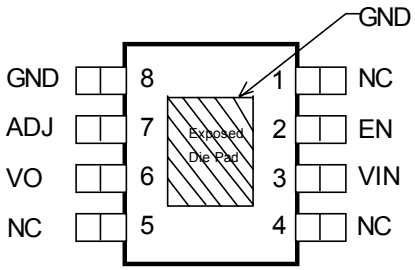
Pin Configuration

Top View



SOIC-8EDP

Bottom View

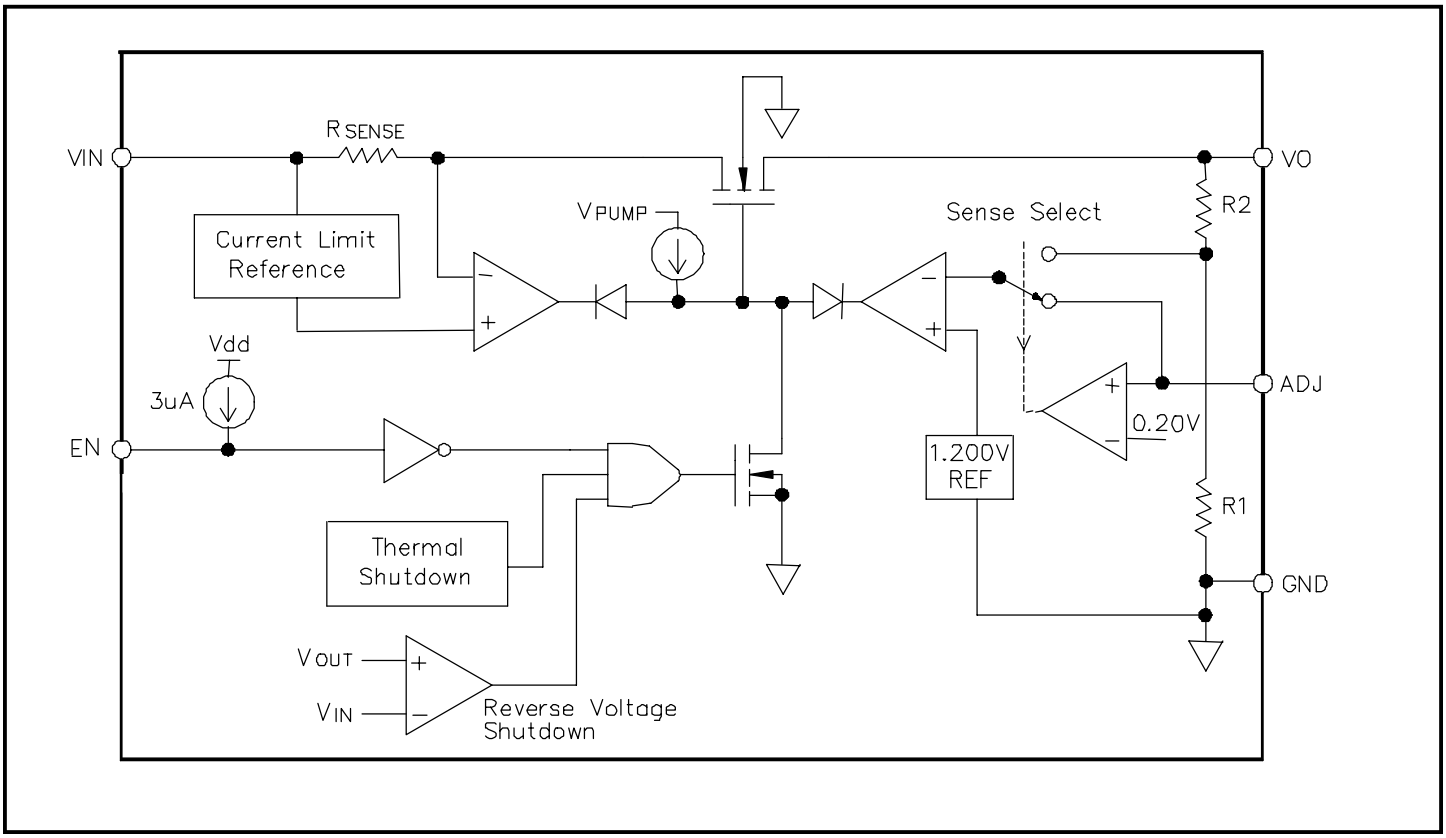


SOIC-8EDP

Pin Descriptions

Pin Name	Pin Desciption
ADJ	This pin, when grounded, sets the output voltage to that set by the internal feedback resistors. If external feedback resistors are used, the output voltage will be (See Application Circuits on page 1): $VO = \frac{1.200\ (R1 + R2)}{R2}$ Volts
EN	Enable Input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be enabled if this pin is left open. Connect to VIN if not being used.
GND	Reference ground. Note: The GND pin and the exposed die pad must be connected together at the IC pin. Use the exposed die pad on the device for heatsinking.
VIN	Input voltage. For regulation at full load, the input to this pin must be between (VO + 0.5V) and 5.5V. Minimum VIN = 2.2V.
VO	The pin is the power output of the device.

Block Diagram



Applications Information

Introduction

The SC4205 is intended for applications such as graphics cards where high current capability and very low dropout voltage are required. It provides a very simple, low cost solution that uses very little pcb real estate. Additional features include an enable pin to allow for a very low power consumption standby mode, and a fully adjustable output.

Component Selection

Input capacitor: a 4.7µF ceramic capacitor is recommended. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, input droop due to load transients is reduced, improving load transient response. Additional capacitance may be added if required by the application.

Output capacitor: a minimum bulk capacitance of 2.2µF, along with a 0.1µF ceramic decoupling capacitor is recommended. Increasing the bulk capacitance will improve the overall transient response. The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors, the SC4205 is extremely tolerant of output capacitor ESR values and thus will also work comfortably with tantalum output capacitors. For reference, the phase-margin contour of Figure 1 can be used to choose an appropriate output capacitor for a given stability requirement.

Noise immunity: in very electrically noisy environments, it is recommended that 0.1µF ceramic capacitors be placed from IN to GND and OUT to GND as close to the device pins as possible.

External voltage selection resistors: the use of 1% resistors, and designing for a current flow ≥ 10µA is recommended to ensure a well regulated output (thus R2 ≤ 120kΩ).

Thermal Considerations

The power dissipation in the SC4205 is approximately equal to the product of the output current and the input to output voltage differential:

$$P_D \approx (VIN - VOUT) \bullet I_O$$

The absolute worst-case dissipation is given by:

$$P_{D(MAX)} = (VIN_{(MAX)} - VOUT_{(MIN)}) \bullet I_{O(MAX)} + VIN_{(MAX)} \bullet I_{Q(MAX)}$$

For a typical scenario, V_{IN} = 3.3V ± 5%, V_{OUT} = 2.8V and I_O = 1A, therefore:

$V_{IN(MAX)}$ = 3.465V, $V_{OUT(MIN)}$ = 2.744V and $I_{Q(MAX)}$ = 1.75mA,

Thus $P_{D(MAX)}$ = 727mW.

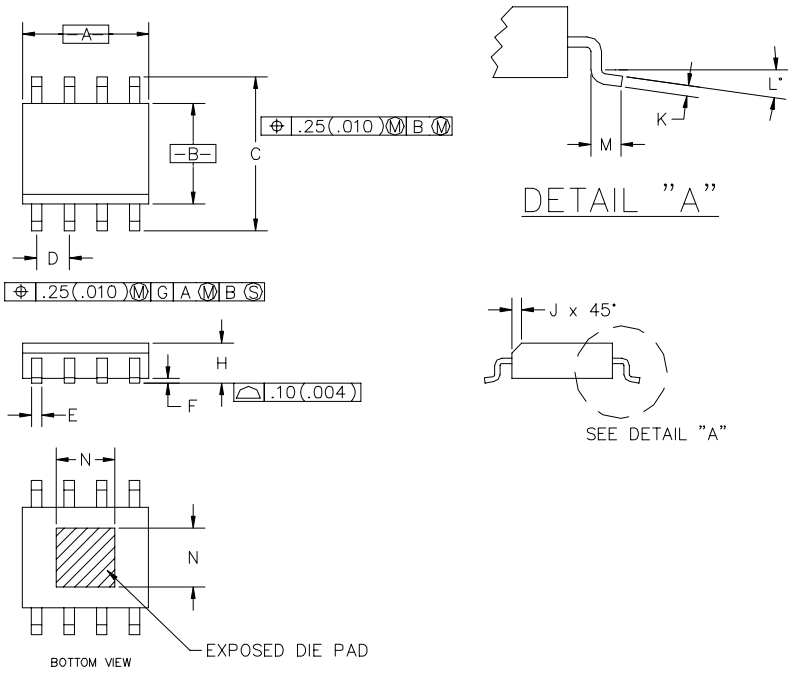
Using this figure, and assuming $T_{A(MAX)}$ = 70°C, we can calculate the maximum thermal impedance allowable to maintain $T_J \leq$ 150°C:

$$R_{TH(J-A)(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{P_{D(MAX)}} = \frac{(150-70)}{.727} = 110°C/W$$

This should be achievable for the SOIC-8EDP package using pcb copper area to aid in conducting the heat away, such as one square inch of copper connected to the pins of the device. Internal ground/power planes and air flow will also assist in removing heat. For higher ambient temperatures it may be necessary to use additional copper area.

POWER MANAGEMENT

Outline Drawing - SOIC-8EDP



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.189	.195	4.80	4.95	2
B	.152	.157	3.86	4.00	3
C	.230	.244	5.84	6.20	
D	.050	BSC	1.27	BSC	
E	.014	.020	0.35	0.51	
F	.001	.005	.025	.127	
H	.056	.066	1.42	1.68	
J	.010	.016	0.25	0.41	
K	.007	.010	0.19	0.25	
L	0°	8°	0°	8°	
M	.016	.035	0.41	0.89	
N	.086	.094	2.19	2.39	4

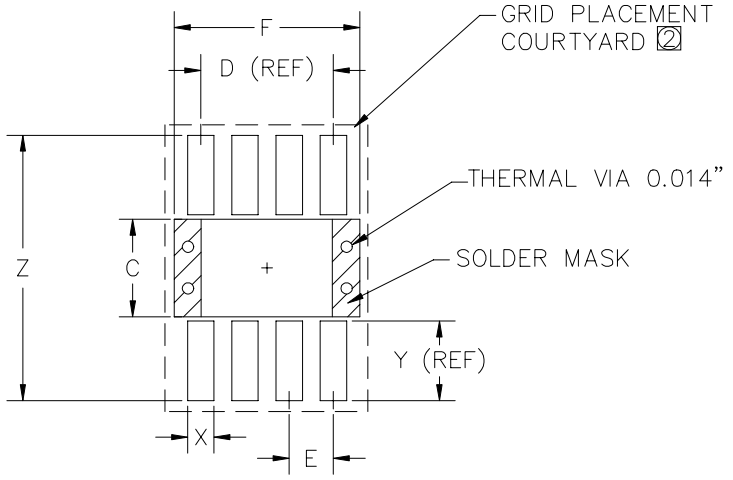
[4] END USER SHOULD VERIFY ACTUAL SIZE OF EXPOSED THERMAL DIE PAD FOR SPECIFIC DEVICE APPLICATION.

[3] DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTUSIONS. INTER-LEAD FLASH AND PROTUSIONS SHALL NOT EXCEED .25 mm (.010") PER SIDE.

[2] DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTUSIONS OR GATE BURRS. MOLD FLASH, PROTUSIONS AND GATE BURRS SHALL NOT EXCEED .15 mm (.010") PER SIDE.

[1] CONTROLLING DIMENSION : MILLIMETER

Land Pattern - SOIC-8EDP



DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	.095	.100	2.41	2.54	–
D	–	.150	–	3.81	REF
E	–	.050	–	1.27	BSC
F	.200	.210	5.08	5.33	–
X	.025	.030	0.64	0.80	–
Y	.070	.075	1.78	1.91	REF
Z	.310	.320	7.87	8.13	–

[2] GRID PLACEMENT COURTYARD IS 12 X 16 ELEMENTS (6mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Contact Information

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