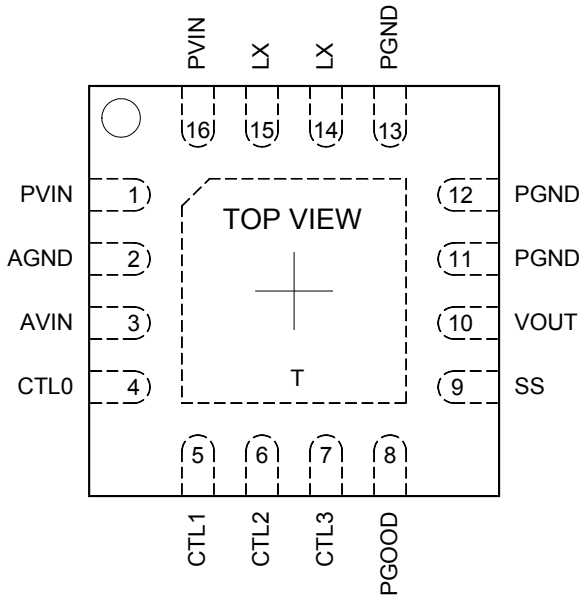
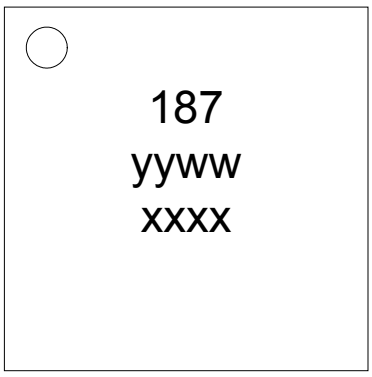
Pin Configuration



3 x 3 x 0.6 (mm) MLPQ-UT16
θ_{JA} = 40°C/W; θ_{JC} = 7°C/W

Marking Information



yyww = Date Code
XXXX = Semtech Lot number

Ordering Information

Device	Package
SC187ULTRT(1)(2)	3 x 3 x 0.6 (mm) MLPQ-UT16
SC187EVB(2)	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Device is lead-free, Halogen free, and RoHS/WEEE compliant.

Table 1 – Output Voltage Settings

CTL3	CTL2	CTL1	CTL0	Output Voltage
0	0	0	0	Shutdown
0	0	0	1	0.8
0	0	1	0	1.00
0	0	1	1	1.025
0	1	0	0	1.05
0	1	0	1	1.20
0	1	1	0	1.25
0	1	1	1	1.30
1	0	0	0	1.50
1	0	0	1	1.80
1	0	1	0	2.20
1	0	1	1	2.50
1	1	0	0	2.60
1	1	0	1	2.80
1	1	1	0	3.00
1	1	1	1	3.30

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Absolute Maximum Ratings

PVIN and AVIN Supply Voltages (V) ..... -0.3 to +6.0
LX (V) [1] ..... -0.3 to PVIN +0.3V, 6V Max
VOUT (V) ..... -0.3 to AVIN + 0.3
CTLx pins (V) ..... -0.3 to AVIN + 0.3
VOUT Short Circuit Duration ..... Continuous
ESD Protection Level [2] (kV) 3

Recommended Operating Conditions

PVIN and AVIN Supply (V) ..... 2.9 to +5.5
Maximum Output Current (A) 4.0
Input Capacitor (µF) 22
Output Capacitor (µF) ..... 47 or 2 x 22
Output Inductor (µH) 1.0

Thermal Information

Thermal Resistance, Junction to Ambient [3] (°C/W) 40
Thermal Resistance, Junction to Case (°C/W) 7
Operating Junction Temperature (°C) ..... -40 to +125
Maximum Junction Temperature (°C) .....+150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the absolute maximum ratings may result in permanent damage to the device and/or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Notes:
(1) Due to parasitic board inductance, the transient LX pin voltage at the point of measurement may appear larger than that which exists on silicon. The device is designed to tolerate the short duration transient voltages that will appear on the LX pin due to the deadtime diode conduction, for inductor currents up to the current limit setting of the device.
(2) Tested according to JEDEC standard JESD22-A114-B.
(3) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: PVIN = AVIN = 5.0V, VOUT = 1.50V, C_{IN} = 22µF, C_{OUT} = 2 x 22µF; L = 1.0µH; -40°C≤ T_J ≤ +125 °C; Unless otherwise noted typical values are T_A = +25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Under-Voltage Lockout	UVLO	Rising AVIN, PVIN=AVIN	2.70	2.80	2.90	V
		Hysteresis		300		mV
Output Voltage Tolerance [1]	ΔV_{OUT}	PVIN= AVIN= 2.9 to 5.5V; I_{OUT}=1A	-1.5		+1.5	%
Current Limit	I_{LIMIT}	Peak LX current	5.0	6.0	7.0	A
Supply Current	I_Q	I_{OUT} = 0A		12		mA
Shutdown Current	I_{SHDN}	CTL3-0 = AGND		1	10	µA
High Side Switch Resistance [2]	R_{DSON_P}	I_{LX}= 100mA, T_J= 25 °C		50		mΩ
Low Side Switch Resistance [2]	R_{DSON_N}	I_{LX}= -100mA, T_J= 25 °C		35		
L_X Leakage Current [2]	$I_{LK(LX)}$	PVIN= AVIN= 5.5V; LX= 0V; CTL3-0 = AGND		1	10	µA
		PVIN= AVIN= 5.5V; LX= 5.0V; CTL3-0 = AGND	-20	-1		
Load Regulation	$\Delta V_{LOAD-REG}$	PVIN= AVIN= 5.0V, I_{OUT}=800mA to 4A		±0.3		%

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Electrical Characteristics (continued)

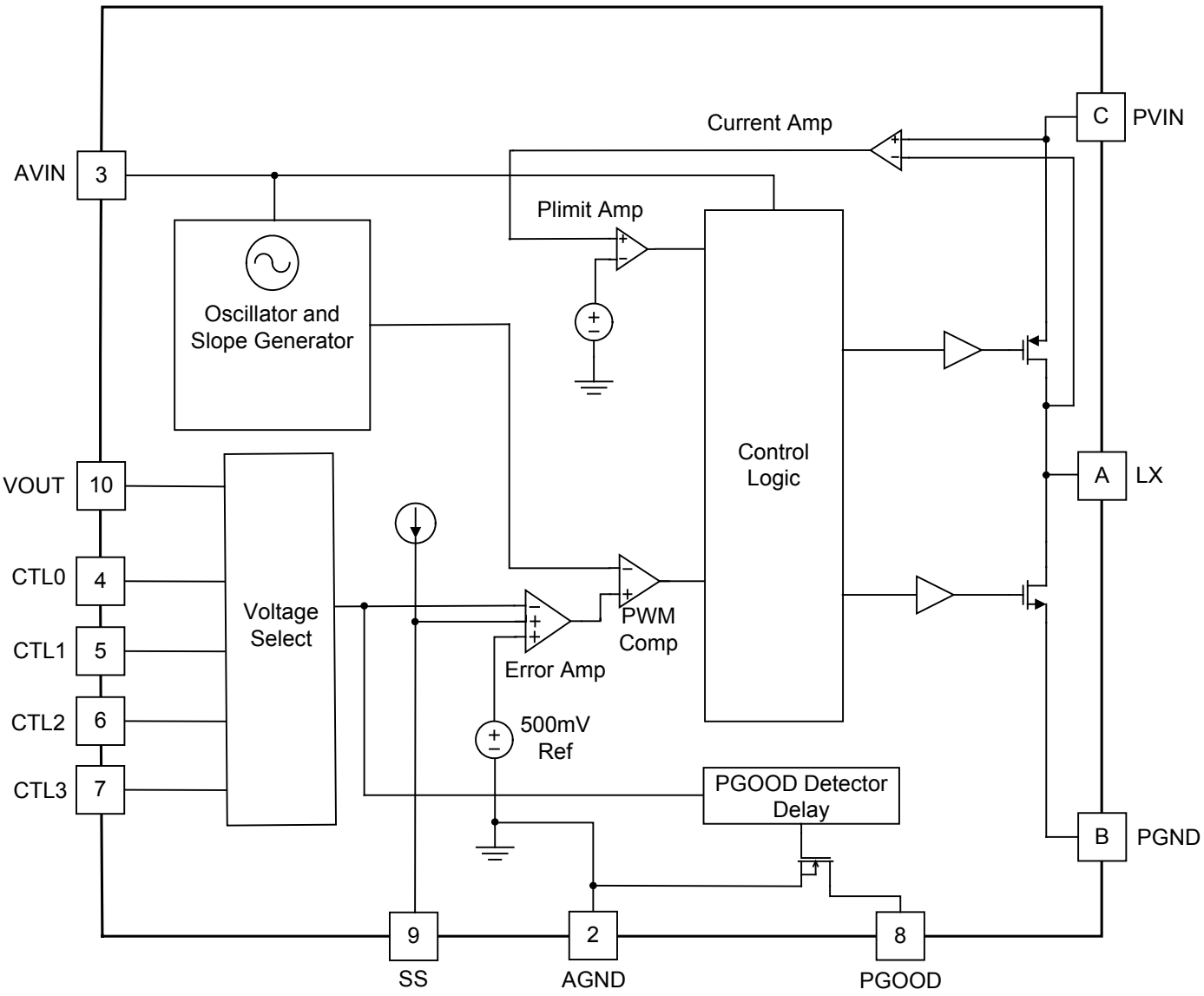
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Oscillator Frequency	f_{OSC}		1.8	2.2	2.6	MHz
Soft-Start Charging Current(2)	I_{SS}			+5		µA
Foldback Holding Current	I_{CL_HOLD}	Average LX Current		1		A
Impedence of PGOOD Low	R_{PGOOD_LO}			10		Ω
PGOOD Threshold	V_{PG_TH}	VOUT rising		90		%
PGOOD Delay	V_{PG_DLY}	Asserted		2		ms
		PGOOD= Low		20		µs
CTL_X Delay	t_{EN_DLY}	From CTL_X Input High to SS starts rising		50		µs
CTL_X Input Current(2)	I_{CTLx}	CTL_X=AVIN or AGND	-2.0		2.0	µA
CTL_X Input High Threshold	V_{CTLx_HI}		1.2			V
CTL_X Input Low Threshold	V_{CTLX_LO}				0.4	V
V_{OUT} Over Voltage Protection	V_{OVP}		110	115	120	%
Thermal Shutdown Temperature	T_{SD}			160		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}			10		°C

Notes:
(1) The "Output Voltage Tolerance" includes output voltage accuracy, voltage drift over temperature and the line regulation.
(2) A negative current means the current flows into the pin and a positive current means the current flows out from the pin.

Pin Descriptions

Pin #	Pin Name	Pin Function
1, 16	PVIN	Input supply voltage for the converter power stage
2	AGND	Ground connection for the internal circuitry — AGND needs to be connected to PGND directly.
3	AVIN	Power supply for the internal circuitry — AVIN is required to be connected to PVIN through an R-C filter of 1Ω and 10nF.
4, 5, 6, 7	CTLx	Control bit — see Table 1 for decoding. These pins have 500kΩ internal pull-down resistors which are switched in circuit whenever CTLx is low or when the part is in under-voltage lockout.
8	PGOOD	Power good indicator — when the output voltage reaches the PGOOD threshold, this pin will be open-drain (after the PGOOD delay), otherwise, it is pulled low internally.
9	SS	Soft Start — Connect a soft-start capacitor to program the soft start time. There is a 5µA charging current flowing out of the pin.
10	VOUT	Output voltage sense pin
11,12,13	PGND	Ground connection for converter power stage
14,15	LX	Switching node — connect an inductor between this pin and the output capacitor.
T	Thermal Pad	Thermal pad for heat sinking purposes — recommend to connect to PGND. It is not connected internally.

Block Diagram

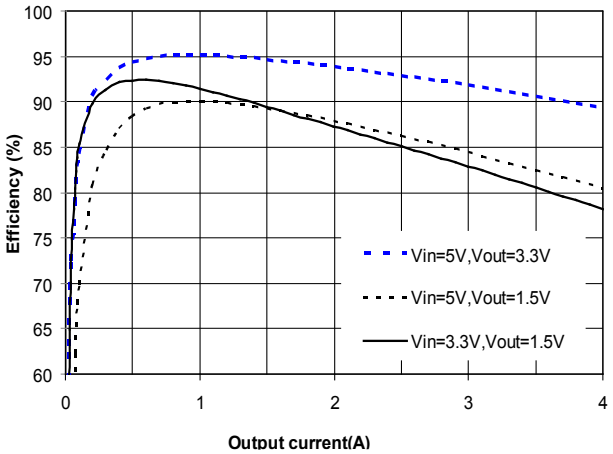


NOTES:
A = Pins 14,15
B = Pins 11, 12, 13
C = 1, 16

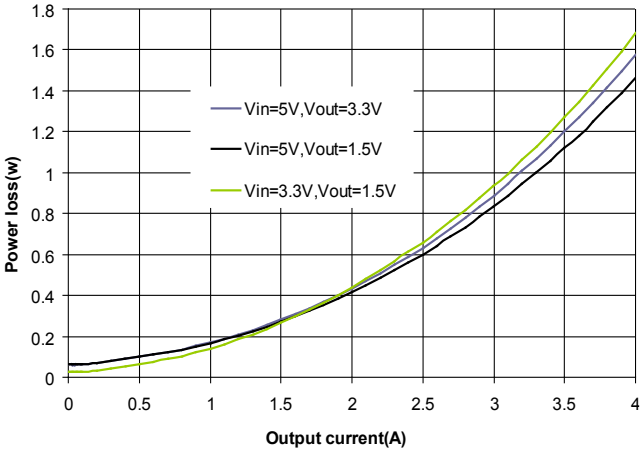
Typical Characteristics

Circuit Conditions: C_{IN} = 22µF/6.3V, C_{OUT} = 2 x 22µF/6.3V, C_{SS} = 10nF. Unless otherwise noted, L = 1.0µH (TOKO: FDV0530S-1R0).

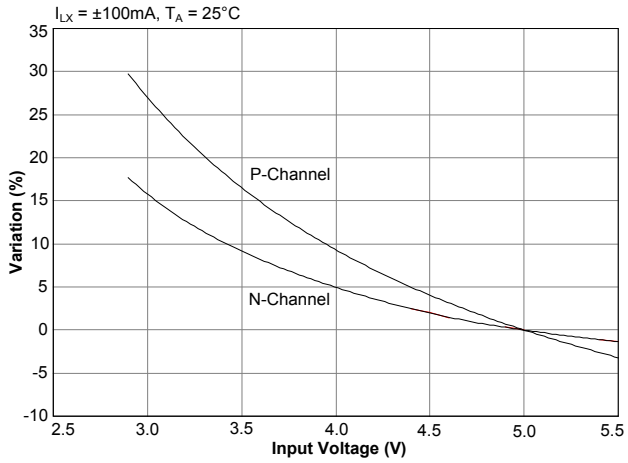
Efficiency



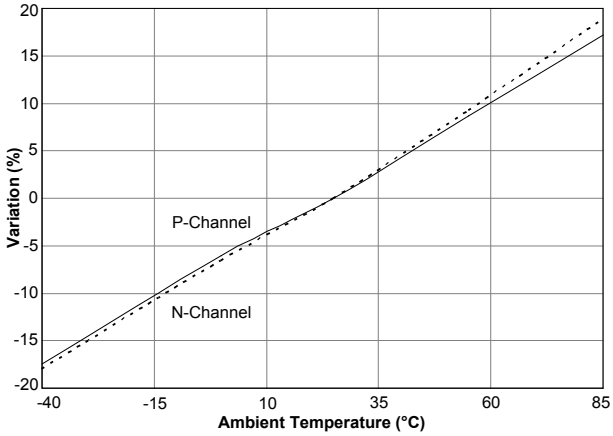
Total Loss



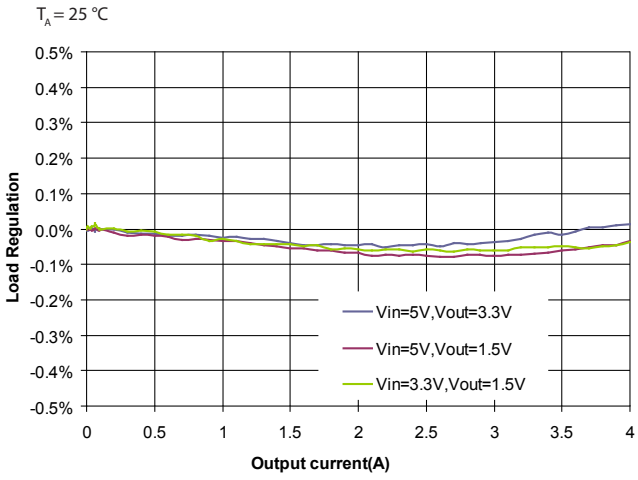
$R_{DS(ON)}$ Variation vs. Input Voltage



$R_{DS(ON)}$ Variation vs. Temperature



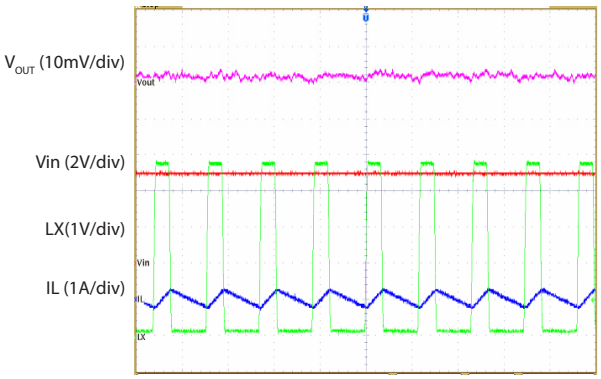
Load Regulation



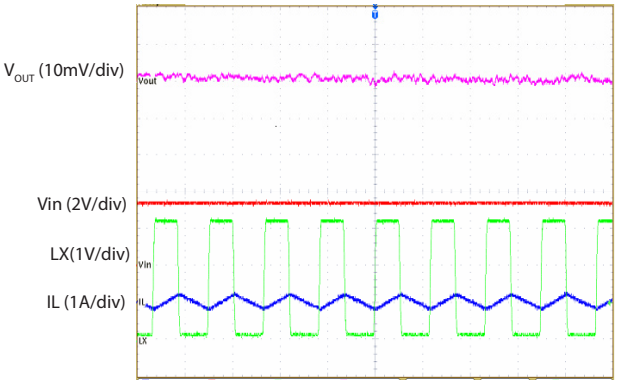
Typical Characteristics (continued)

Circuit Conditions: C_{IN} = 22µF/6.3V, C_{OUT} = 2 x 22µF/6.3V, C_{SS} = 10nF. Unless otherwise noted, L = 1.0µH (TOKO: FDV0530S-1R0).

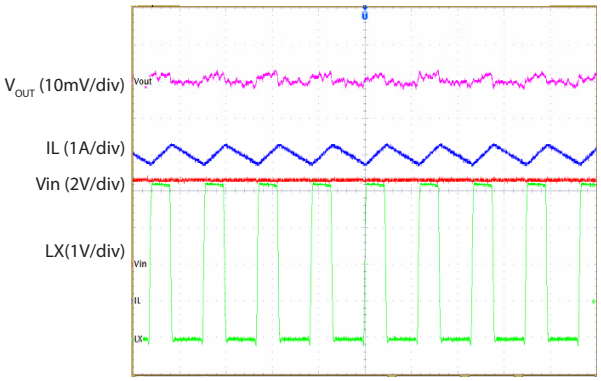
Vout Ripple (Vin=5V, V_{OUT}=1.5V) @0A Load



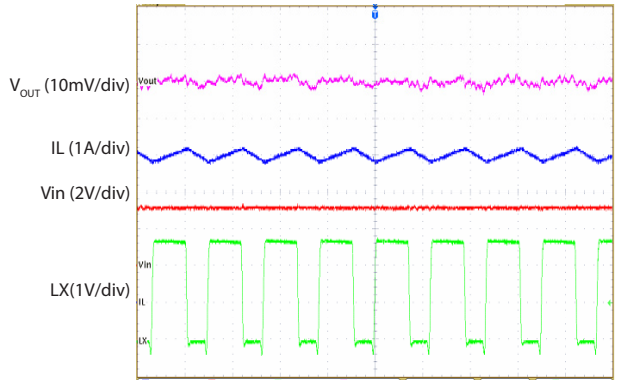
Vout Ripple (Vin=3.3V, V_{OUT}=1.5V)@ 0A Load



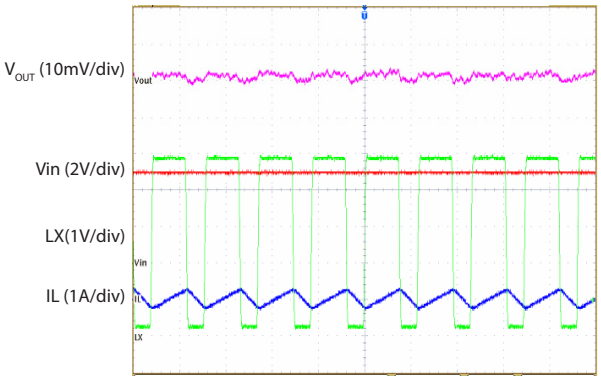
Vout Ripple (Vin=5V, V_{OUT}=1.5V) @ Full Load



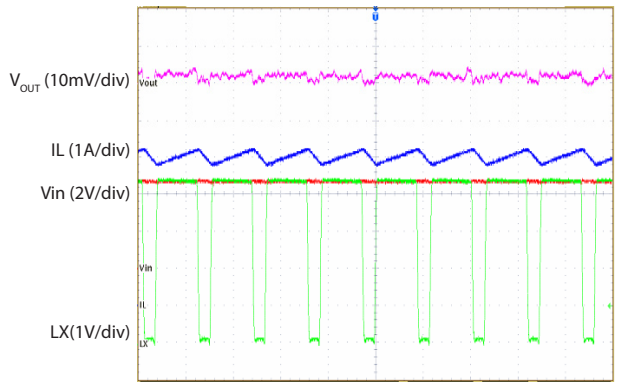
Vout Ripple (Vin=3.3V, V_{OUT}=1.5V) @ Full Load



Vout Ripple (Vin=5V, V_{OUT} = 3.3V) @ No Load



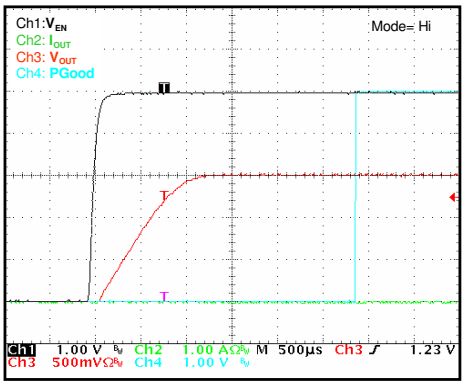
Vout Ripple (Vin=5V, V_{OUT} = 3.3V) @ Full Load



Typical Characteristics (continued)

Circuit Conditions: C_{IN} = 22µF/6.3V, C_{OUT} = 2 x 22µF/6.3V, C_{SS} = 10nF. Unless otherwise noted, L = 1.0µH (TOKO: FDV0530S-1R0).

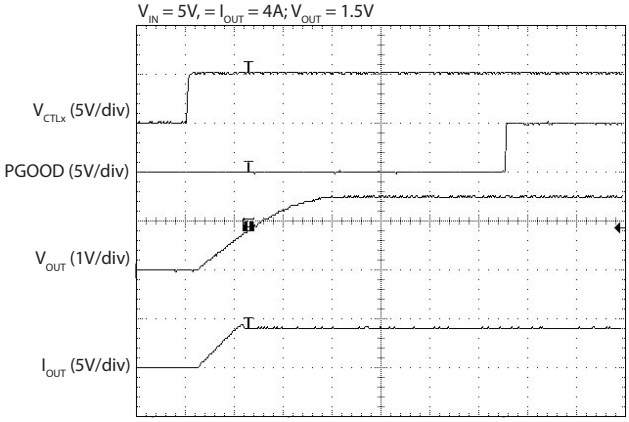
Start Up (CTL_x) — No Load



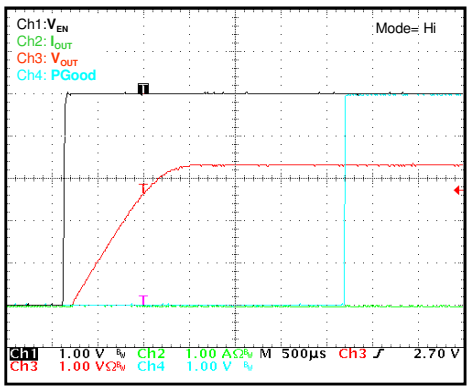
V_{IN} = 5.0V
I_{OUT} = 0A

Start Up (CTL_x) — Full Load

V_{IN} = 5V, = I_{OUT} = 4A; V_{OUT} = 1.5V



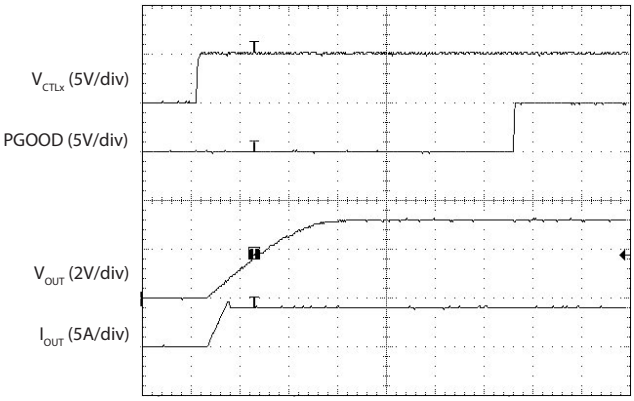
Start Up (CTL_x) — No Load



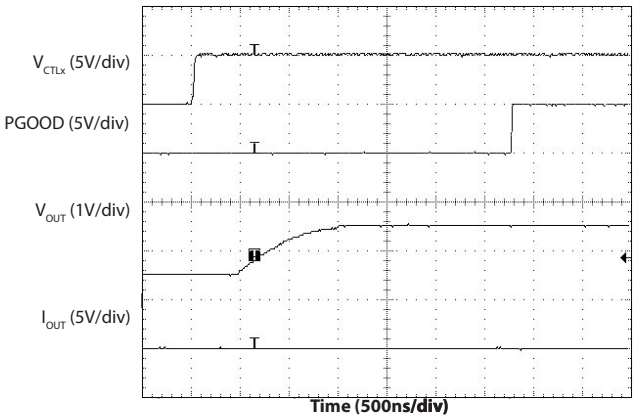
V_{IN} = 5.0V
I_{OUT} = 0A

Start Up (CTL_x) — Full Load

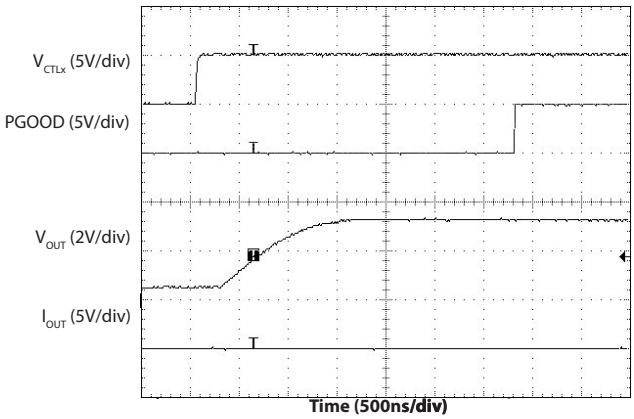
V_{IN} = 5V, = I_{OUT} = 0; V_{OUT} = 3.3V



Start Up into Pre-Biased Output (V_{OUT}=1.5V)



Start Up into Pre-Biased Output (V_{OUT}=3.3V)

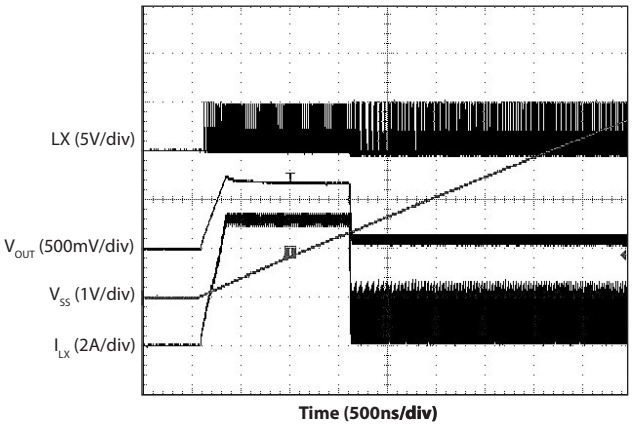


Typical Characteristics (continued)

Circuit Conditions: C_{IN} = 22µF/6.3V, C_{OUT} = 2 x 22µF/6.3V, C_{SS} = 10nF. Unless otherwise noted, L = 1.0µH (TOKO: FDV0530S-1R0).

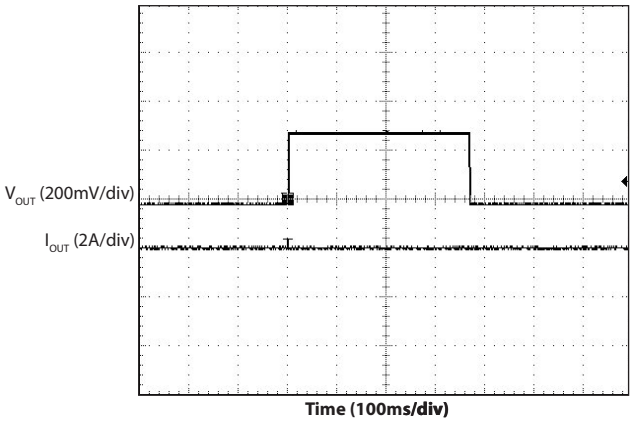
Start Up into Output Short Circuit

V_{IN} = 5V



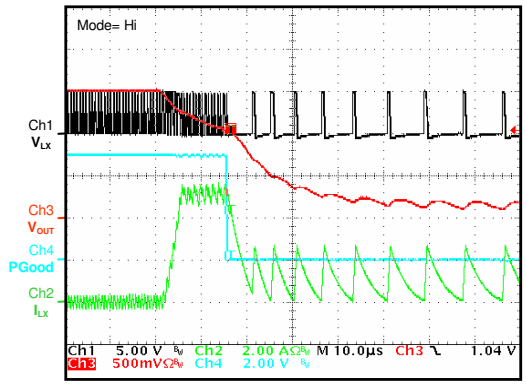
VID Transition — Full Load

V_{IN} = 5V; V_{OUT} = 1.5V to 1.8V to 1.5V



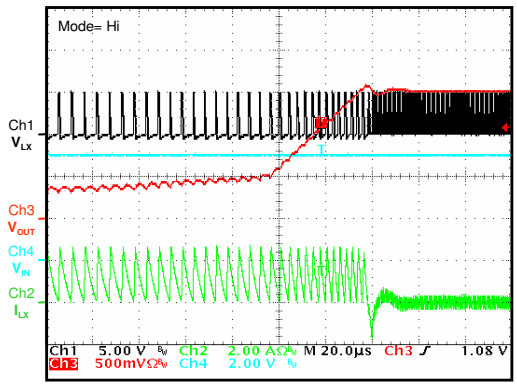
Output Short Circuit

V_{IN} = 5V; V_{OUT} = 1.5V



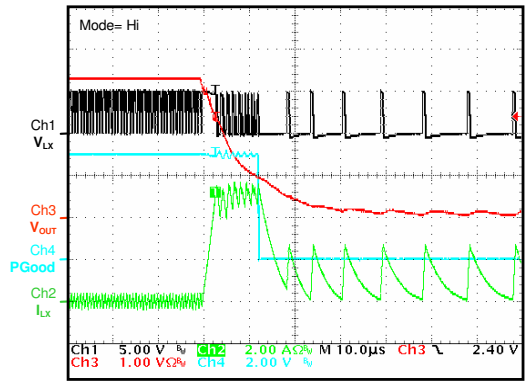
Recovery from Short Circuit

V_{IN} = 5V; V_{OUT} = 1.5V



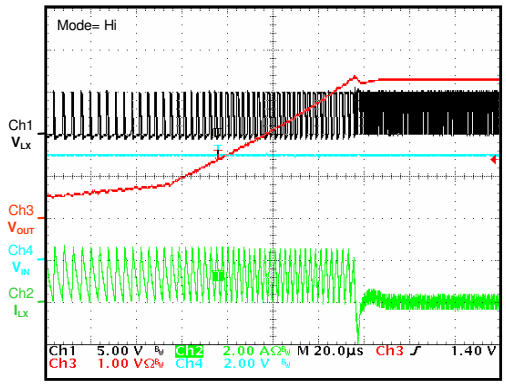
Output Short Circuit

V_{IN} = 5V; V_{OUT} = 3.3V



Recovery from Short Circuit

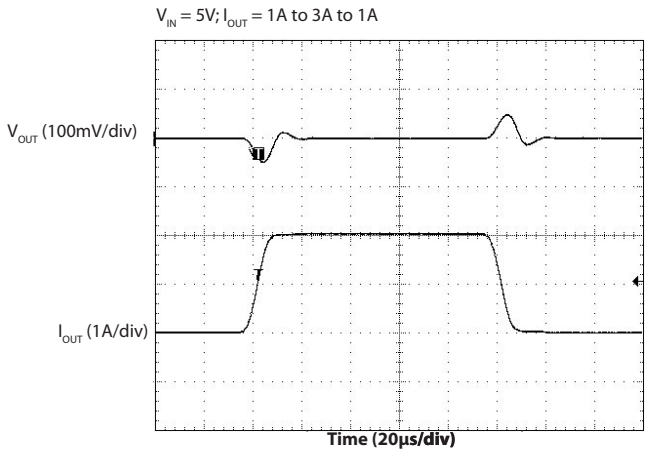
V_{IN} = 5V; V_{OUT} = 3.3V



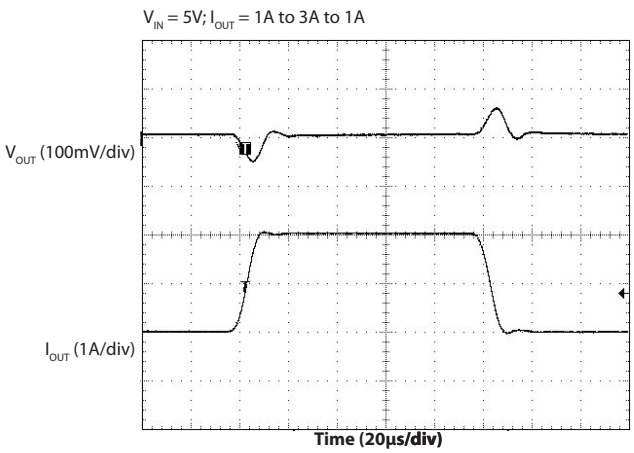
Typical Characteristics (continued)

Circuit Conditions: C_{IN} = 22µF/6.3V, C_{OUT} = 2 x 22µF/6.3V, C_{SS} = 10nF. Unless otherwise noted, L = 1.0µH (TOKO: FDV0530S-1R0).

Transient Response (V_{OUT}=1.5V, I_{STEP}=2A)



Transient Response (V_{OUT}=3.3V, I_{STEP}=2A)



Applications Information

Detailed Description

The SC187 is a synchronous step-down PWM (Pulse Width Modulated) DC-DC converter utilizing a 2.2MHz fixed-frequency voltage mode architecture. The device is designed to operate in fixed-frequency PWM mode. The switching frequency is chosen to minimize the size of the external inductor and capacitors while maintaining high efficiency.

Operation

During normal operation, the PMOS MOSFET is activated on each rising edge of the internal oscillator. The period is set by the onboard oscillator. The device has an internal synchronous NMOS rectifier and does not require a Schottky diode on the LX pin. The device operates as a buck converter in PWM mode with a fixed frequency of 2.2MHz.

Protection Features

The SC187 provides the following protection features:

- Current Limit
- Over-Voltage Protection
- Soft-Start Operation
- Thermal Shutdown

Current Limit & OCP

The internal PMOS power device in the switching stage is protected by a current limit feature. If the inductor current is above the PMOS current limit for 16 consecutive cycles, the part enters foldback current limit mode and the output current is limited to the current limit holding current (I_{CL_HOLD}) which is approximately 1A. Under this condition, the output voltage will be the product of I_{CL_HOLD} and the load resistance. The SC187 is capable of sustaining an indefinite short circuit without damage. During the soft start, if current limit has occurred before the SS voltage has reached 400mV, the part enters foldback current limit mode. Foldback current limit mode will be disabled during soft-start after the SS voltage is higher than 400mV.

Over-Voltage Protection

In the event of a 15% over-voltage on the output, the PWM drive is disabled with the LX pin floating. Switching does not resume until the output voltage falls below the nominal V_{OUT} regulation voltage.

Programmable Output Voltage

The SC187 has fifteen pre-determined output voltage values which can be individually selected by programming the CTL input pins (see Table 1 — Output Voltage Settings). Each CTL pin has an active 500kΩ internal pull-down resistor. The 500kΩ resistor is switched in circuit whenever the CTL input voltage is below the input threshold, or when the part is in under voltage lockout. It is recommended to tie all high CTL pins together and use an external pull-up resistor to AVIN if there is no enable signal or if the enable input is an open drain/collector signal. The CTL pins may be driven by a microprocessor to allow dynamic voltage adjustment for systems that reduce the supply voltage when entering sleep states. Avoid all zeros being present on the CTL pins when changing programmable output voltages as this would disable the device.

SC187 is also capable of regulating a different (higher) output voltage, which is not shown in the Table 1, via an external resistor divider. There will be a typical 2µA current flowing into the VOUT pin. The typical schematic for an adjustable output voltage option from the standard 1.0V with CTLx=[0010], is shown in Figure 2. RFB1 and RFB2 are used to adjust the desired output voltage. If the RFB2 current is such that the 2µA VOUT pin current can be ignored, then RFB1 can be found using the next equation. RFB2 needs to be low enough in value for the current through the resistor chain to be at least 20µA in order to ignore the VOUT pin current.

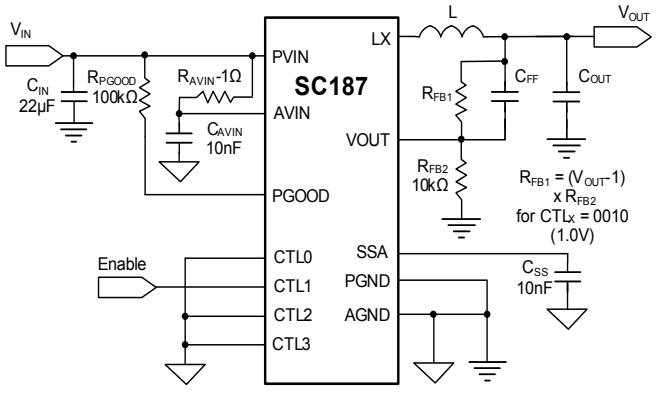


Figure 1 — Output Voltage Programming

Applications Information (continued)

$$R_{FB1} = \frac{V_{OUT} - V_{OSTD}}{V_{OSTD}} \times R_{FB2}$$

where V_{OSTD} is the pre-determined output voltage via the CTL pins.

C_{FF} is needed to maintain good transient response performance. The correct value of C_{FF} can be found using the following equation.

$$C_{FF}[nF] = 2.5 \times \frac{(V_{OUT} - 0.5)^2}{R_{FB1}[k\Omega] \times (V_{OUT} - V_{OSTD})} \times \left(\frac{V_{OSTD}}{V_{OSTD} - 0.5}\right)$$

To simplify the design, it is recommended to program the desired output voltage from a standard 1.0V as shown in Figure 2 with a proper C_{FF} calculated from Equation 2. For programming the output voltage from other standard voltages, R_{FB1}, R_{FB2} and C_{FF} need to be adjusted to conform to the previous equations.

Shut Down

When all CTL pins are low, the device will run in shutdown mode, drawing less than 1µA from the input power supply. The internal switches and band-gap voltage will be immediately turned off.

Thermal Shutdown

The device has a thermal shutdown feature to protect the SC187 if the junction temperature exceeds 160°C. During thermal shutdown, the on-chip power devices are disabled, floating the LX output. When the temperature drops by 10°C, it will initiate a soft start cycle to resume normal operation.

Under-Voltage Lockout

Under-Voltage Lockout (UVLO) is enabled when the input voltage drops below the UVLO threshold. This prevents the device from entering an ambiguous state in which regulation cannot be maintained. Hysteresis of approximately 300mV is included to prevent chattering near the threshold. When the AVIN voltage rises back to the turn-on threshold and CTL_X is high, the soft-start mode is resumed.

Power Good

The power good (PGOOD) is an open-drain output. When the output voltage drops below 10% of nominal voltage, the PGOOD pin is pulled low after a 20µs delay. During start-up, PGOOD will be asserted 2ms (typ.) after the output voltage reaches 90% of the final regulation voltage. The faults of over voltage, fold-back current limit mode and thermal shutdown will force PGOOD low after a 20µs delay. When recovering from a fault, PGOOD will be asserted 1.8ms (typ.) after Vout reaches 90% of the final regulation voltage.

Soft-Start

The soft-start mode is activated after AVIN reaches it's UVLO voltage threshold and CTL_X is set high to enable the part. A thermal shutdown event will also activate the soft start sequence. The soft-start mode controls the slew-rate of the output voltage during start-up thus limiting in-rush current on the input supply. During start-up, the reference voltage for the error amplifier is clamped by the voltage on the SS pin. The output voltage slew rate during soft-start is determined by the value of the external capacitor connected to the SS pin and the internal 5µA charging current. The device requires a minimum soft-start time from enable to final regulation in the order of 200µs, including the 50µs enable delay. As a result the soft start capacitor, Css, should be higher than 1.5nF.

100% Duty-Cycle Operation

SC187 is capable of operating at 100% duty-cycle. When the difference between the input voltage and output voltage is less than the minimum dropout voltage, the PMOS switch is completely on, operating in 100% duty-cycle. The minimum dropout voltage is the output current multiplied by the on-resistance of the internal PMOS switch and the DC-resistance of the inductor when PMOS switch is on continuously.

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Applications Information (continued)

Output L-C filter Selection

SC187 has fixed internal loop-gain compensation. It is optimized for X5R or X7R ceramic output capacitors and an output L-C filter corner frequency of less than 34kHz. The output L-C corner frequency can be determined by Equation 2.

$$f_C = \frac{1}{2\pi \sqrt{L \times C_{OUT}}}$$

In general, the inductor is chosen to set the inductor ripple current to approximately 30% of the maximum output current. It is recommended to use a typical inductor value of 1µH to 2.2µH with output ceramic capacitors of 44µF or higher capacitance. Lower inductance should be considered in applications where faster transient response is required. More output capacitance will reduce the output deviation for a particular load transient. When using low inductance, the maximum peak inductor current at any condition (normal operation and start up) can not exceed 5A which is the guaranteed minimum current limit. The saturation current rating of the inductor needs to be at least larger than the peak inductor current which is the maximum output current plus half of inductor ripple current.

Applications Information (continued)

PCB Layout Considerations

The layout diagram in Figure 2 shows a recommended top-layer PCB for the SC187 and supporting components. Figure 3 shows the bottom layer for this PCB. Fundamental layout rules must be followed since the layout is critical for achieving the performance specified in the Electrical Characteristics table. Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

The following guidelines are recommended when developing a PCB layout:

1. The input capacitor, C_{IN} should be placed as close to the PVIN and PGND pins as possible. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to connect as closely to the IC as possible. This will minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. Keep the LX pin traces as short as possible to minimize pickup of high frequency switching edges to other parts of the circuit. C_{OUT} and L should be connected as close as possible between the LX and PGND pins, with a direct return to the PGND pin from C_{OUT}.
3. Route the output voltage feedback/sense path away from the inductor and LX node to minimize noise and magnetic interference.
4. Use a ground plane referenced to the SC187 PGND pin. Use several vias to connect to the component side ground to further reduce noise and interference on sensitive circuit nodes.
5. If possible, minimize the resistance from the VOUT and PGND pins to the load. This will reduce the voltage drop on the ground plane and improve the load regulation. And it will also improve the overall efficiency by reducing the copper losses on the output and ground planes.

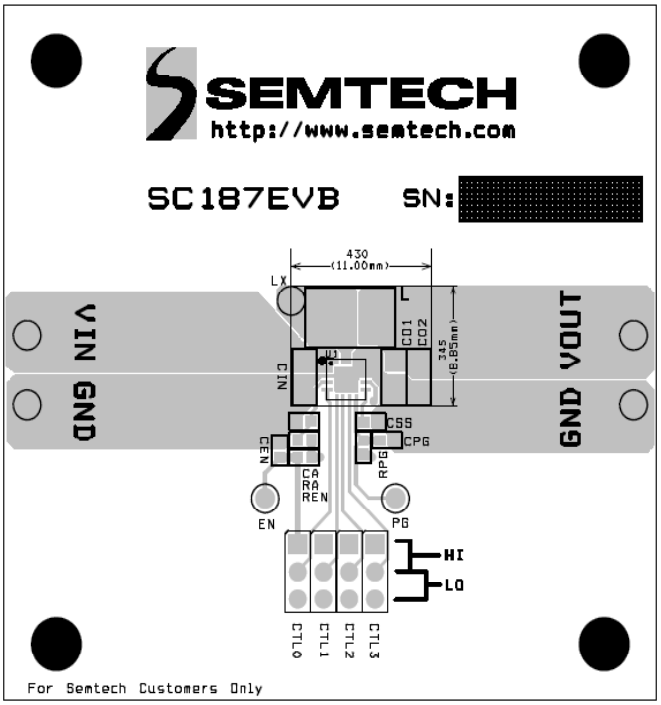


Figure 2 — Recommended PCB Layout (Top Layer)

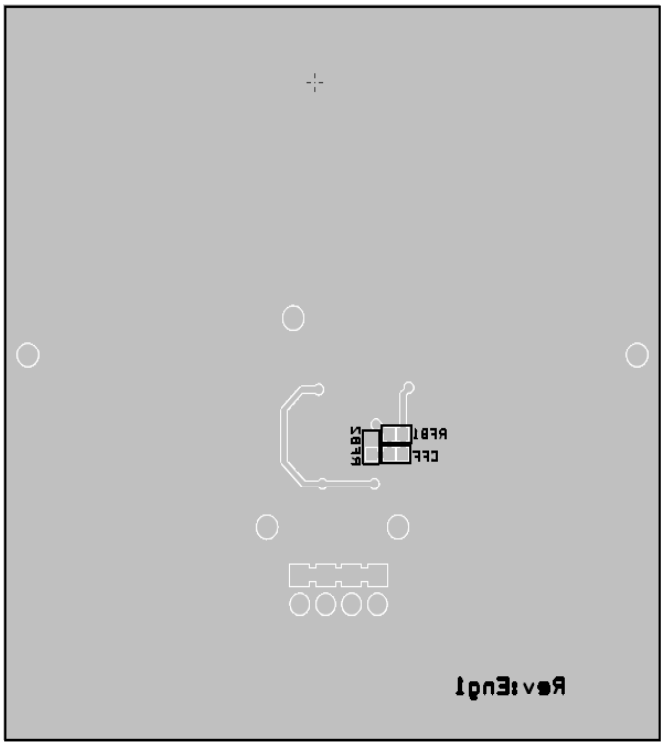
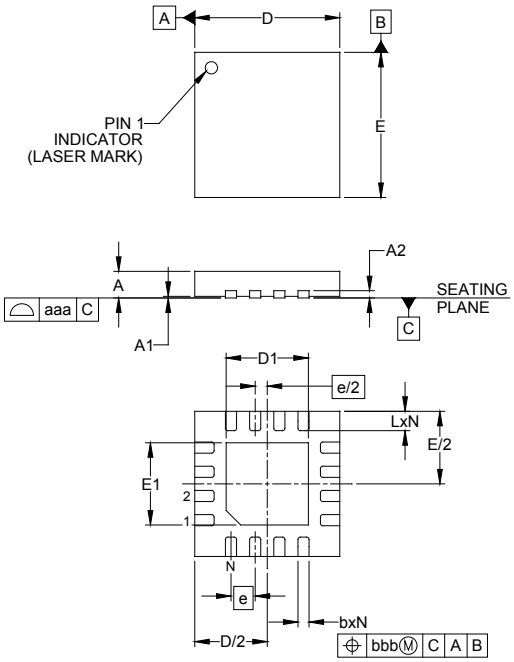


Figure 3 — Bottom Layer Detail

Outline Drawing – 3x3 MLPQ-UT16

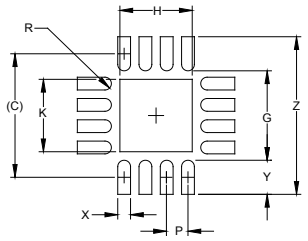


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.152)	
b	.007	.009	.012	0.18	0.23	0.30
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	16			16		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

Land Pattern – 3x3 MLPQ-UT16



DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.020	0.50
R	.006	0.15
X	.012	0.30
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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