

## Typical Application Circuit

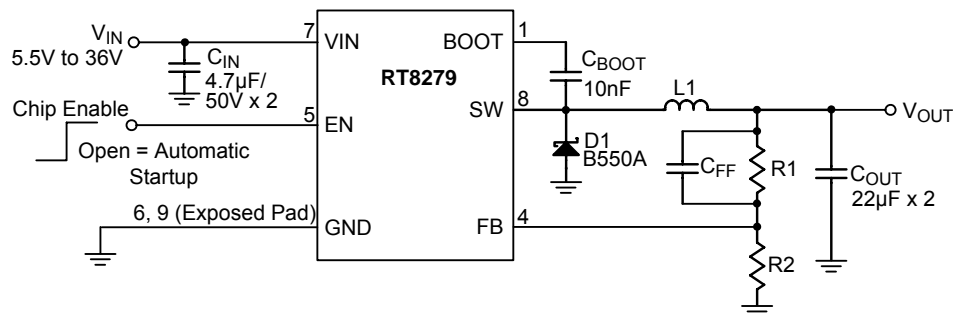


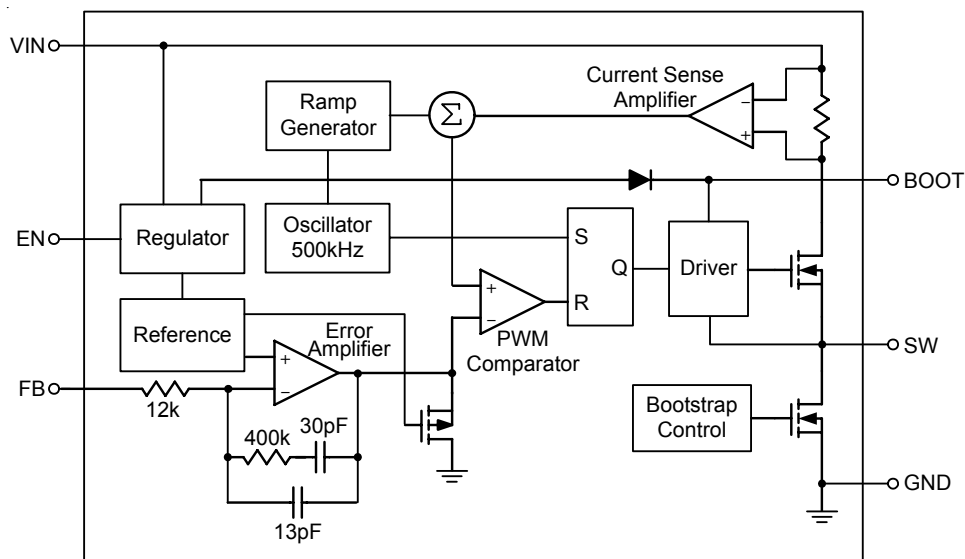
Table 1. Recommended Component Selection

V <sub>OUT</sub> (V)	R1 (kΩ)	R2 (kΩ)	C <sub>FF</sub> (pF)	L (μH)	C <sub>OUT</sub> (μF)
2.5	100	100	82	6.8	22 x 2
3.3	100	58.6	82	10	22 x 2
5	100	31.6	82	15	22 x 2
8	100	18	82	22	22 x 2

## Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	High Side Gate Drive Boost Input. BOOT supplies the drive for the high side N-MOSFET switch. Connect a 10nF or greater capacitor from SW to BOOT to power the high side switch.
2, 3	NC	No Internal Connection.
4	FB	Feedback Input. The feedback threshold is 1.222V.
5	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN higher than 1.4V to turn on the regulator, lower than 0.4V to turn it off. For automatic startup, leave EN unconnected.
6, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
7	VIN	Power Input. A suitable large capacitor should be bypassed from VIN to GND to eliminate noise on the input to the IC.
8	SW	Power Switching Output. Note that a capacitor is required from SW to BOOT to power the high side switch.

## Function Block Diagram



**Absolute Maximum Ratings** (Note 1)

Supply Voltage, $V_{IN}$	-----	-0.3V to 40V
Switching Voltage, $V_{SW}$	-----	-0.3V to $V_{IN} + 0.3V$
BOOT Voltage	-----	$(V_{SW} - 0.3V)$ to $(V_{SW} + 6V)$
The Other Pins	-----	-0.3V to 6V
Power Dissipation, $P_D$ @ $T_A = 25^\circ C$		
SOP-8 (Exposed Pad)	-----	1.333W
Package Thermal Resistance (Note 2)		
SOP-8 (Exposed Pad), $\theta_{JA}$	-----	75°C/W
SOP-8 (Exposed Pad), $\theta_{JC}$	-----	15°C/W
Junction Temperature	-----	150°C
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Storage Temperature Range	-----	-65°C to 150°C
ESD Susceptibility (Note 3)		
HBM (Human Body Mode)	-----	2kV
MM (Machine Mode)	-----	200V

**Recommended Operating Conditions** (Note 4)

Supply Voltage, $V_{IN}$	-----	5.5V to 36V
Junction Temperature Range	-----	-40°C to 125°C
Ambient Temperature Range	-----	-40°C to 85°C

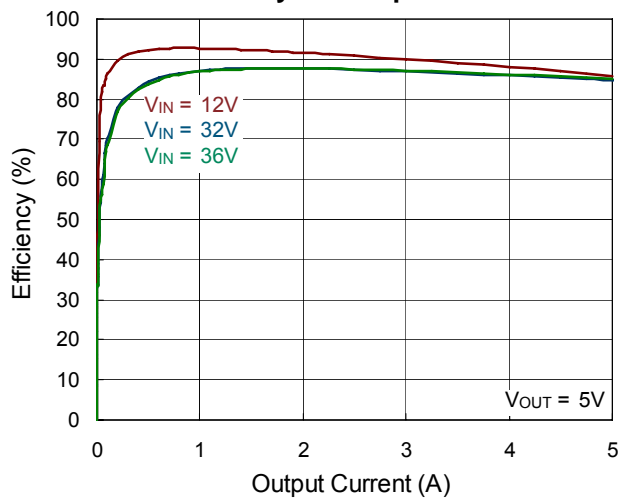
**Electrical Characteristics**(V<sub>IN</sub> = 12V, T<sub>A</sub> = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage		V <sub>REF</sub>	5.5V ≤ V <sub>IN</sub> ≤ 36V	1.202	1.222	1.239	V
High Side Switch-On Resistance		R <sub>DS(ON)1</sub>		--	110	160	mΩ
Low Side Switch-On Resistance		R <sub>DS(ON)2</sub>		--	10	15	Ω
High Side Switch Leakage			V <sub>EN</sub> = 0V, V <sub>SW</sub> = 0V	--	--	10	μA
Current Limit		I <sub>LIM</sub>	Duty = 90%, V <sub>BOOT-SW</sub> = 4.8V	6	7.5	9	A
Oscillator Frequency		f <sub>OSC</sub>		425	500	575	kHz
Short Circuit Frequency			V <sub>FB</sub> = 0V	--	150	--	kHz
Maximum Duty Cycle		D <sub>MAX</sub>	V <sub>FB</sub> = 0.8V	85	90	95	%
Minimum On-Time		t <sub>ON</sub>		--	100	150	ns
Under Voltage Lockout Threshold Rising				3.8	4.2	4.5	V
Under Voltage Lockout Threshold Hysteresis				--	315	--	mV
EN Threshold Voltage	Logic-High	V <sub>IH</sub>	EN_hys = 350mV	1.4	--	--	V
	Logic-Low	V <sub>IL</sub>		--	--	0.4	
Enable Pull Up Current				--	1	--	μA
Shutdown Current		I <sub>SHDN</sub>	V <sub>EN</sub> = 0V	--	25	45	μA
Quiescent Current		I <sub>Q</sub>	V <sub>EN</sub> = 2V, V <sub>FB</sub> = 1.5V	--	0.6	1	mA
Soft-Start Period			C <sub>SS</sub> = 0.1μF	3	5	8.2	ms
Thermal Shutdown		T <sub>SD</sub>		--	150	--	°C

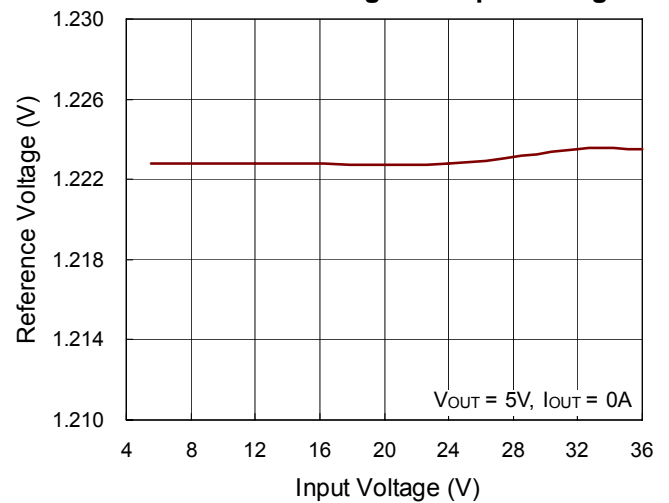
- Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
- Note 2.**  $\theta_{JA}$  is measured at  $T_A = 25^\circ\text{C}$  on a high effective thermal conductivity four-layer test board per JEDEC 51-7.  $\theta_{JC}$  is measured at the exposed pad of the package.
- Note 3.** Devices are ESD sensitive. Handling precaution is recommended.
- Note 4.** The device is not guaranteed to function outside its operating conditions.

## Typical Operating Characteristics

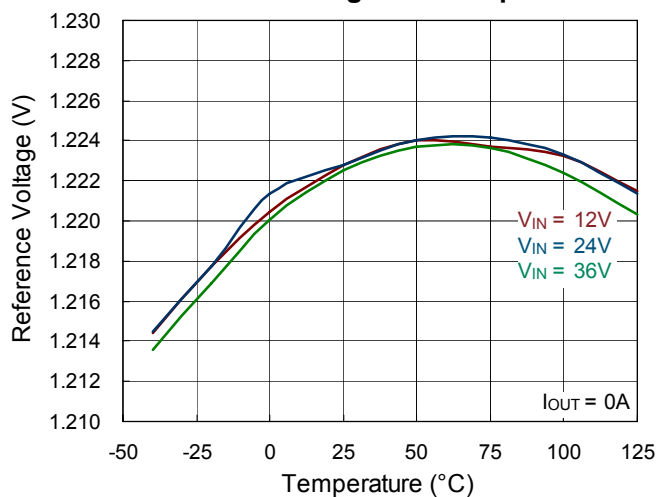
Efficiency vs. Output Current



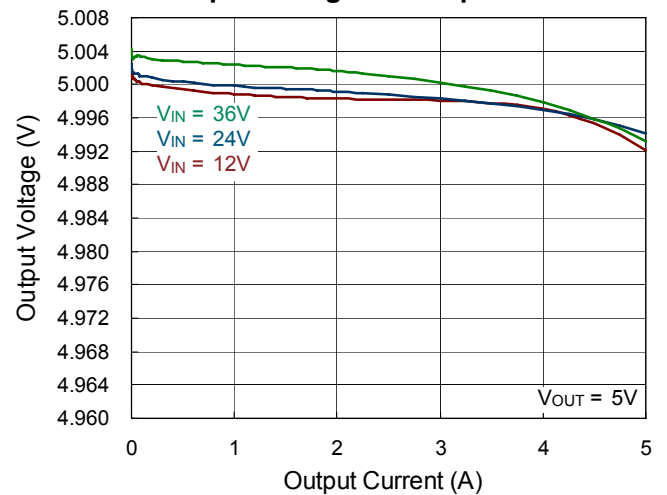
Reference Voltage vs. Input Voltage



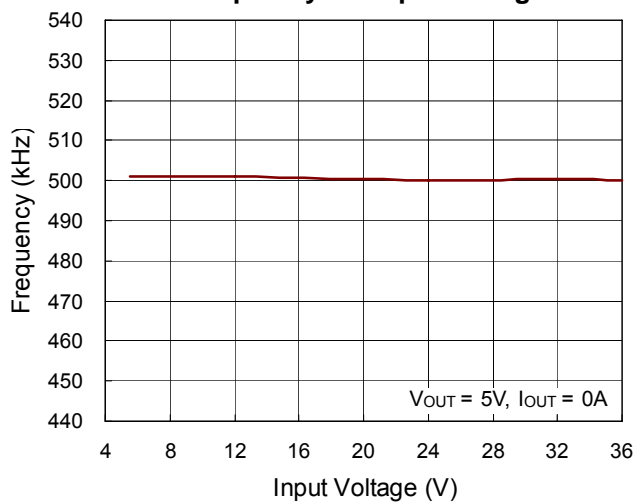
Reference Voltage vs. Temperature



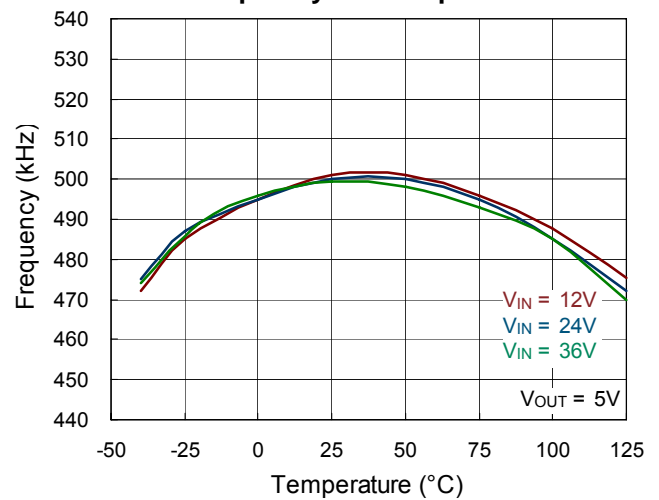
Output Voltage vs. Output Current



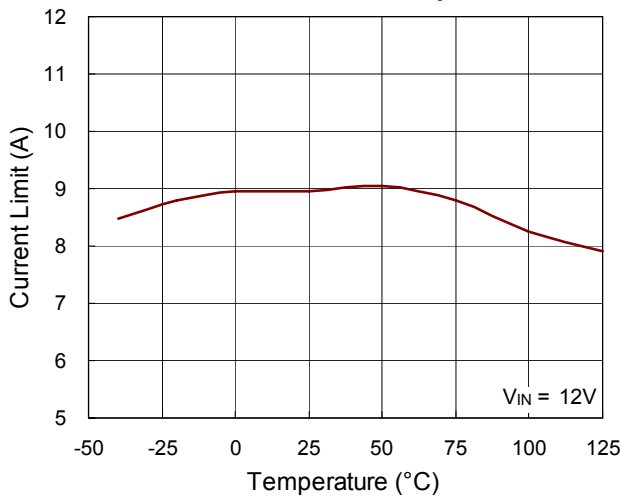
Frequency vs. Input Voltage



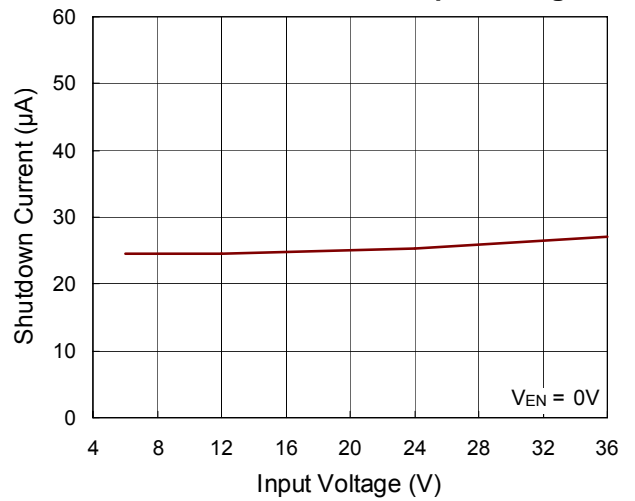
Frequency vs. Temperature



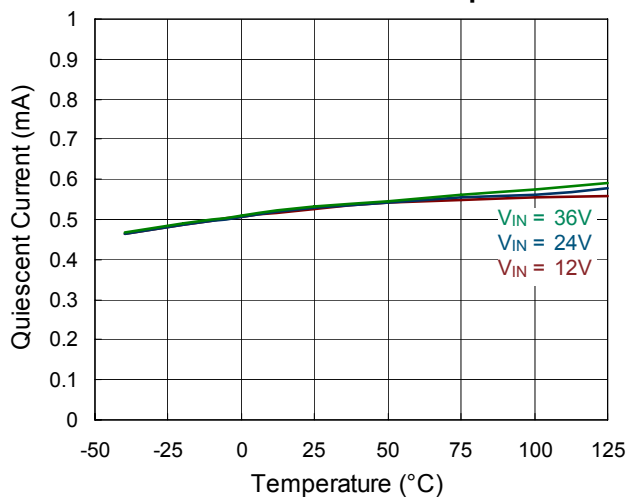
Current Limit vs. Temperature



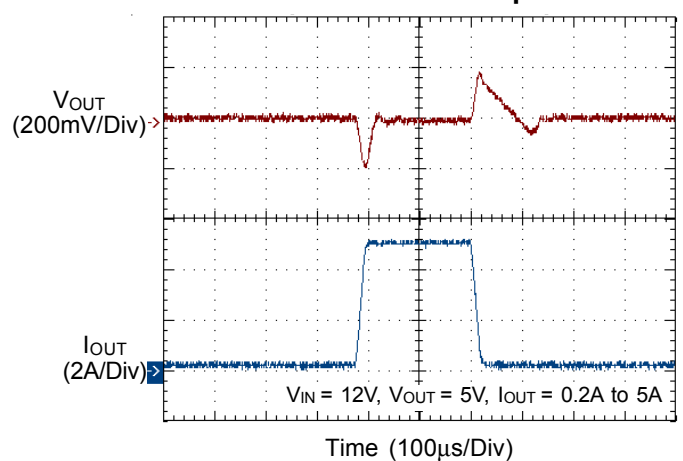
Shutdown Current vs. Input Voltage



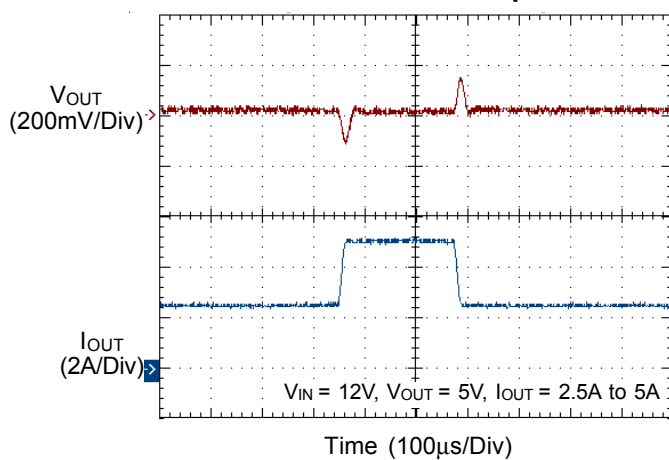
Quiescent Current vs. Temperature



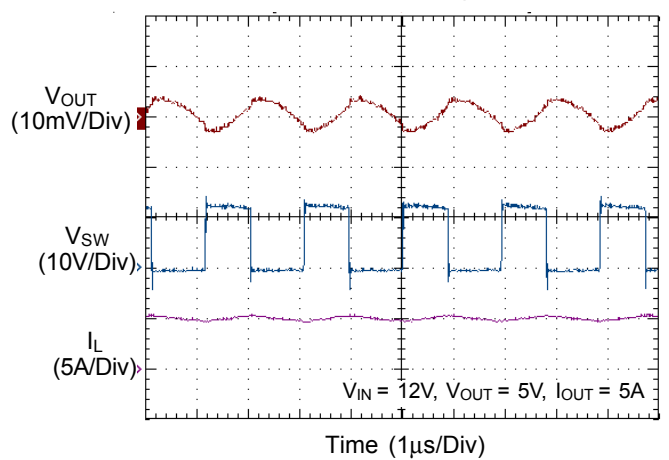
Load Transient Response



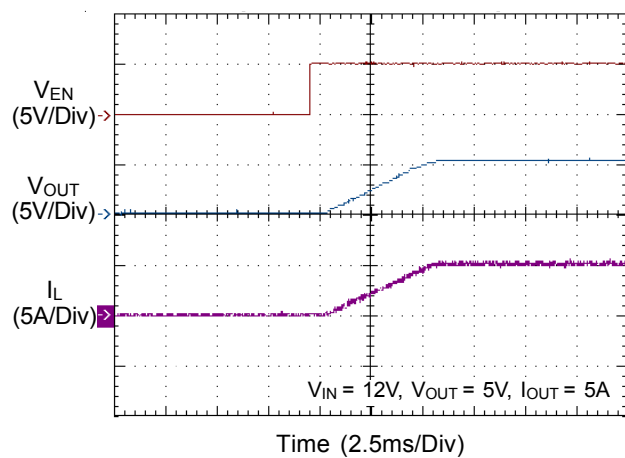
Load Transient Response



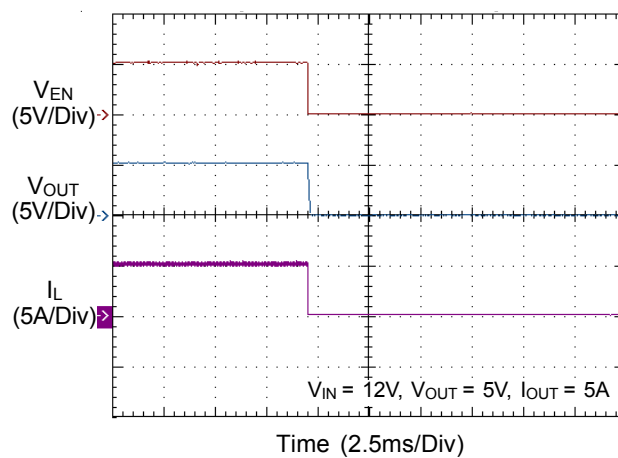
Switching



Power On from EN



Power Off from EN



## Application Information

The RT8279 is an asynchronous high voltage buck converter that can support the input voltage range from 5.5V to 32V and the output current can be up to 5A.

### Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

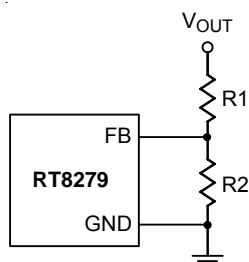


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF} \left( 1 + \frac{R1}{R2} \right)$$

Where  $V_{REF}$  is the reference voltage (1.222V typ.).

Where  $R1 = 100k\Omega$ .

### External Bootstrap Diode

Connect a 10nF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT8279.

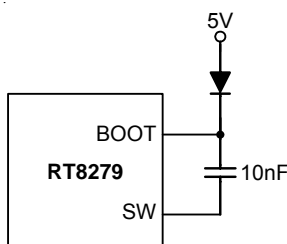


Figure 2. External Bootstrap Diode

### Soft-Start

The RT8279 contains an internal soft-start clamp that gradually raises the output voltage. The typical soft-start time is 5ms.

### Chip Enable Operation

The EN pin is the chip enable input. Pull the EN pin low (<0.4V) will shutdown the device. During shutdown mode, the RT8279 quiescent current drops to lower than 25μA. Drive the EN pin to high (>1.4V, <5.5V) will turn on the device again. If the EN pin is open, it will be pulled to high by internal circuit. For external timing control (e.g.RC),the EN pin can also be externally pulled to High by adding a 100kΩ or greater resistor from the VIN pin (see Figure 3).

### Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current  $\Delta I_L$  increases with higher  $V_{IN}$  and decreases with higher inductance.

$$\Delta I_L = \left[ \frac{V_{OUT}}{f \times L} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of  $\Delta I_L = 0.2(I_{MAX})$  will be a reasonable starting point. The largest ripple current occurs at the highest  $V_{IN}$ . To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[ \frac{V_{OUT}}{f \times \Delta I_L(MAX)} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.



**Table 2. Suggested Inductors for Typical Application Circuit**

Component Supplier	Series	Dimensions (mm)
TAIYO YUDEN	NR10050	10 x 9.8 x 5
TDK	SLF12565	12.5 x 12.5 x 6.5

### Diode Selection

When the power switch turns off, the path for the current is through the diode connected between the switch output and ground. This forward biased diode must have a minimum voltage drop and recovery times. Schottky diode is recommended and it should be able to handle those current. The reverse voltage rating of the diode should be greater than the maximum input voltage, and current rating should be greater than the maximum load current. For more detail please refer to Table 4.

### C<sub>IN</sub> and C<sub>OUT</sub> Selection

The input capacitance, C<sub>IN</sub>, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V<sub>IN</sub> = 2V<sub>OUT</sub>, where I<sub>RMS</sub> = I<sub>OUT</sub>/2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor, two 4.7μF low ESR ceramic capacitors are recommended. For the recommended capacitor, please refer to table 3 for more detail.

The selection of C<sub>OUT</sub> is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C<sub>OUT</sub> selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV<sub>OUT</sub>, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since ΔI<sub>L</sub> increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V<sub>IN</sub>. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V<sub>IN</sub> large enough to damage the part.

### Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V<sub>OUT</sub> immediately shifts by an amount equal to ΔI<sub>LOAD</sub> (ESR) also begins to charge or discharge C<sub>OUT</sub> generating a feedback error signal for the regulator to return V<sub>OUT</sub> to its steady-state value. During this

recovery time,  $V_{OUT}$  can be monitored for overshoot or ringing that would indicate a stability problem.

### EMI Consideration

Since parasitic inductance and capacitance effects in PCB circuitry would cause a spike voltage on SW pin when high side MOSFET is turned-on/off, this spike voltage on SW may impact on EMI performance in the system. In order to enhance EMI performance, there are two methods to suppress the spike voltage. One is to place an R-C

snubber between SW and GND and make them as close as possible to the SW pin (see Figure 3). Another method is to add a resistor in series with the bootstrap capacitor,  $C_{BOOT}$ . But this method will decrease the driving capability to the high side MOSFET. It is strongly recommended to reserve the R-C snubber during PCB layout for EMI improvement. Moreover, reducing the SW trace area and keeping the main power in a small loop will be helpful on EMI performance. For detailed PCB layout guide, please refer to the section of Layout Consideration.

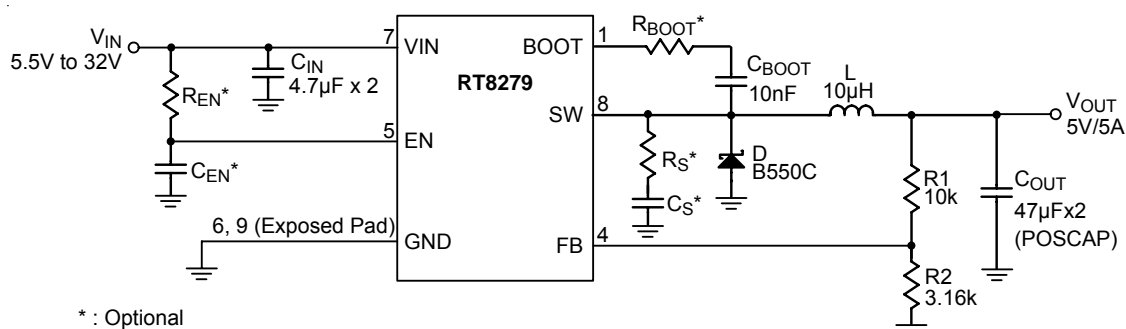


Figure 3. Reference Circuit with Snubber and Enable Timing Control

### Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where  $T_{J(MAX)}$  is the maximum operation junction temperature,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8279, the maximum junction temperature is 125°C. The junction to ambient thermal resistance  $\theta_{JA}$  is layout dependent. For PSOP-8 package, the thermal resistance  $\theta_{JA}$  is 75°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (75^\circ\text{C/W}) = 1.333\text{W} \text{ (min.copper area PCB layout)}$$

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (49^\circ\text{C/W}) = 2.04\text{W} \text{ (70mm}^2 \text{ copper area PCB layout)}$$

The thermal resistance  $\theta_{JA}$  of SOP-8 (Exposed Pad) is determined by the package architecture design and the PCB layout design. However, the package architecture design had been designed. If possible, it's useful to increase thermal performance by the PCB layout copper design. The thermal resistance  $\theta_{JA}$  can be decreased by adding copper area under the exposed pad of SOP-8 (Exposed Pad) package.

As shown in Figure 4, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 4a),  $\theta_{JA}$  is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 4.b) reduces the  $\theta_{JA}$  to 64°C/W. Even further, increasing the copper area of pad to 70mm<sup>2</sup> (Figure 4.e) reduces the  $\theta_{JA}$  to 49°C/W.

The maximum power dissipation depends on operating ambient temperature for fixed  $T_J$  (MAX) and thermal resistance  $\theta_{JA}$ . For the RT8279, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

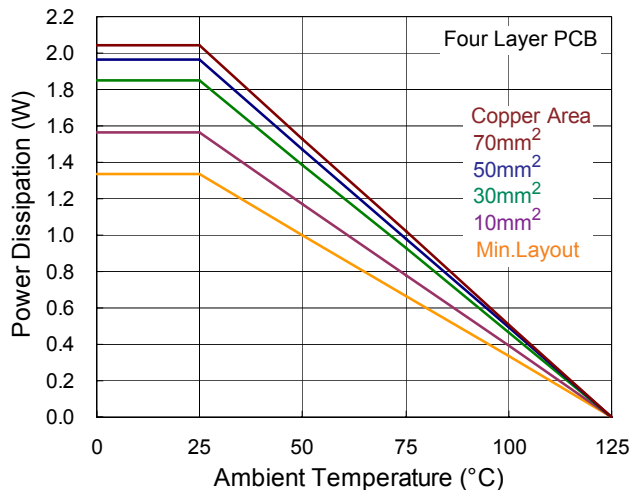
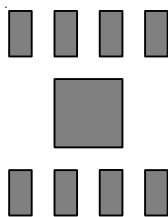
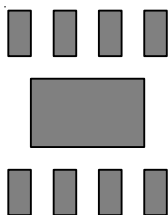


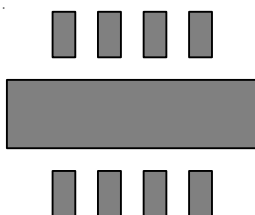
Figure 5. Derating Curves for RT8279 Package



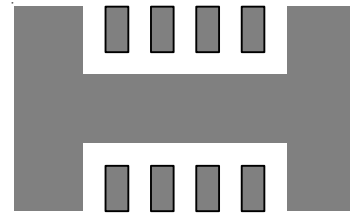
(a) Copper Area = (2.3 x 2.3) mm²,  $\theta_{JA}$  = 75°C/W



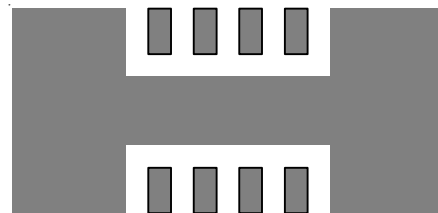
(b) Copper Area = 10mm²,  $\theta_{JA}$  = 64°C/W



(c) Copper Area = 30mm²,  $\theta_{JA}$  = 54°C/W



(d) Copper Area = 50mm²,  $\theta_{JA}$  = 51°C/W



(e) Copper Area = 70mm²,  $\theta_{JA}$  = 49°C/W

Figure 4. Thermal Resistance vs. Copper Area Layout Design

## Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT8279.

- ▶ Keep the traces of the main current paths as short and wide as possible.
- ▶ Put the input capacitor as close as possible to the device pins (VIN and GND).
- ▶ SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pick-up.
- ▶ Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8279.
- ▶ Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.
- ▶ An example of PCB layout guide is shown in Figure 6 for reference.

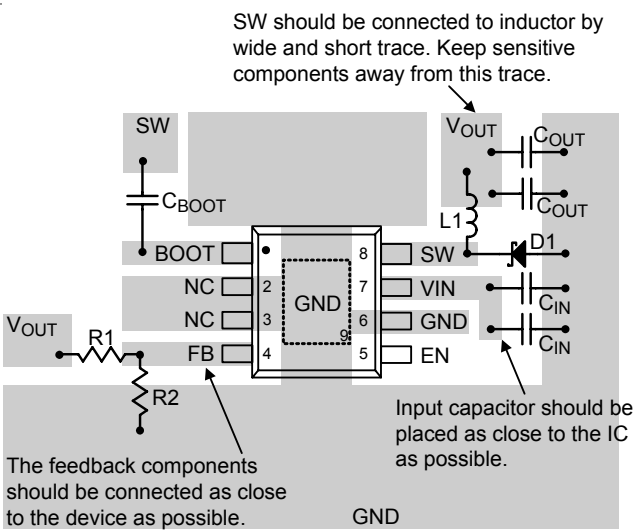


Figure 6. PCB Layout Guide

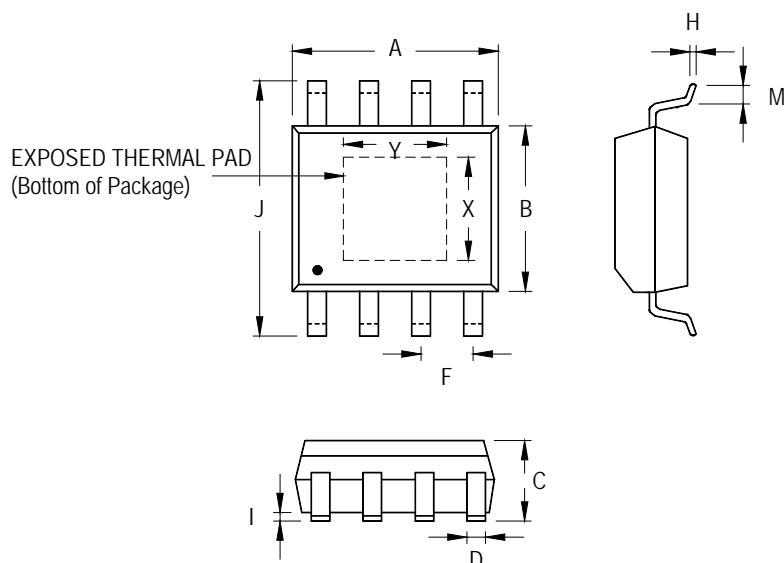
Table 3. Suggested Capacitors for C<sub>IN</sub> and C<sub>OUT</sub>

Location	Component Supplier	Part No.	Capacitance (μF)	Case Size
C <sub>IN</sub>	MURATA	GRM32ER71H475K	4.7	1206
C <sub>IN</sub>	TAIYO YUDEN	UMK325BJ475MM-T	4.7	1206
C <sub>OUT</sub>	MURATA	GRM31CR60J476M	47	1206
C <sub>OUT</sub>	TDK	C3225X5R0J476M	47	1210
C <sub>OUT</sub>	MURATA	GRM32ER71C226M	22	1210
C <sub>OUT</sub>	TDK	C3225X5R1C22M	22	1210

Table 4. Suggested Diode

Component Supplier	Series	V <sub>RRM</sub> (V)	I <sub>OUT</sub> (A)	Package
DIODES	B550C	50	5	SMC
PANJIT	SK55	50	5	SMC

## Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

**8-Lead SOP (Exposed Pad) Plastic Package**

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