

Pinout Table

Pin#	Pin Name	Type	Description
2, 3	SRC & SRC#	Input	0.7V Differential SRC input from PI6C410 clock synthesizer
8, 21	OE_0 & OE_3	Input	3.3V LVTTL input for enabling outputs, active high. OE_0 for OUT0 / OUT0# OE_3 for OUT3 / OUT3#
25	OE_INV	Input	3.3V LVTTL input for inverting the OE, SRC_STOP# and PWRDWN# pins. When 0 = same stage When 1 = OE_0, OE_3, SRC_STOP#, PWRDWN# inverted.
6, 7, 9, 10, 19, 20, 22, 23	OUT[0:3] & OUT[0:3]#	Output	0.7V Differential outputs
12	PLL/BYPASS#	Input	3.3V LVTTL input for selecting fan-out of PLL operation.
13	SCLK	Input	SMBus compatible SCLOCK input
14	SDA	I/O	SMBus compatible SDATA
26	IREF	Input	External resistor connection to set the differential output current
16	SRC_STOP#	Input	3.3V LVTTL input for SRC stop, active low
17	PLL_BW#	Input	3.3V LVTTL input for selecting the PLL bandwidth
15	PWRDWN#	Input	3.3V LVTTL input for Power Down operation, active low
1, 5, 11, 18, 24	V _{DD}	Power	3.3V Power Supply for Outputs
4	VSS	Ground	Ground for Outputs
27	VSS_A	Ground	Ground for PLL
28	VDD_A	Power	3.3V Power Supply for PLL

Serial Data Interface (SMBus)

This part is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	1	0	0/1

Data Protocol

1 bit	7 bits	1	1	8 bits	1	8 bits	1	8 bits	1		8 bits	1	1 bit
Start bit	Slave Addr	R/W	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	...	Data Byte N - 1	Ack	Stop bit

Notes:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

Data Byte 0: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Source Pin
0	Outputs Mode 0 = Divide by 2 1 = Normal	RW	1 = Normal	OUT[0:3], OUT[0:3]#	NA
1	PLL/BYPASS# 0 = Fanout 1 = PLL	RW	1 = PLL	OUT[0:3], OUT[0:3]#	NA
2	PLL Bandwidth 0 = High Bandwidth, 1 = Low Bandwidth	RW	1 = Low	OUT[0:3], OUT[0:3]#	NA
3	Reserved				NA
4	Reserved				NA
5	Reserved				NA
6	SRC_STOP# 0 = Driven when stopped 1 = Tristate	RW	0 = Driven when stopped	OUT[0:3], OUT[0:3]#	NA
7	PWRDWN# 0 = Driven when stopped 1 = Tristate	RW	0 = Driven when stopped	OUT[0:3], OUT[0:3]#	NA

Data Byte 1: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Source Pin
0	Reserved				NA
1	OUTPUTS enable	RW	1 = Enabled	OUT0, OUT0#	NA
2	1 = Enabled 0 = Disabled	RW	1 = Enabled	OUT1, OUT1#	NA
3	Reserved				NA
4	Reserved				NA
5	OUTPUTS enable	RW	1 = Enabled	OUT2, OUT2#	NA
6	1 = Enabled 0 = Disabled	RW	1 = Enabled	OUT3, OUT3#	NA
7	Reserved				NA

Data Byte 2: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Source Pin
0	Reserved				NA
1	Allow control of OUTPUTS with assertion of SRC_STOP# 0 = Free running 1 = Stopped with SRC_Stop#	RW	0 = Free running	OUT0, OUT0#	NA
2		RW	0 = Free running	OUT1, OUT1#	NA
3	Reserved				NA
4	Reserved				NA
5	Allow control of OUTPUTS with assertion of SRC_STOP# 0 = Free running 1 = Stopped with SRC_Stop#	RW	0 = Free running	OUT2, OUT2#	NA
6		RW	0 = Free running	OUT3, OUT3#	NA
7	Reserved				NA

Data Byte 3: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Source Pin
0	Reserved	RW			
1		RW			
2		RW			
3		RW			
4		RW			
5		RW			
6		RW			
7		RW			

Data Byte 3: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	Pericom ID	R	0	NA	NA
1		R	0	NA	NA
2		R	0	NA	NA
3		R	0	NA	NA
4		R	0	NA	NA
5		R	1	NA	NA
6		R	0	NA	NA
7		R	0	NA	NA

Functionality

PWRDWN#	OUT	OUT#	SRC_Stop#	OUT	OUT#
1	Normal	Normal	1	Normal	Normal
0	$I_{REF} \times 2$ or Float	Low	0	$I_{REF} \times 6$ or Float	Low

Power Down (PWRDWN# assertion)

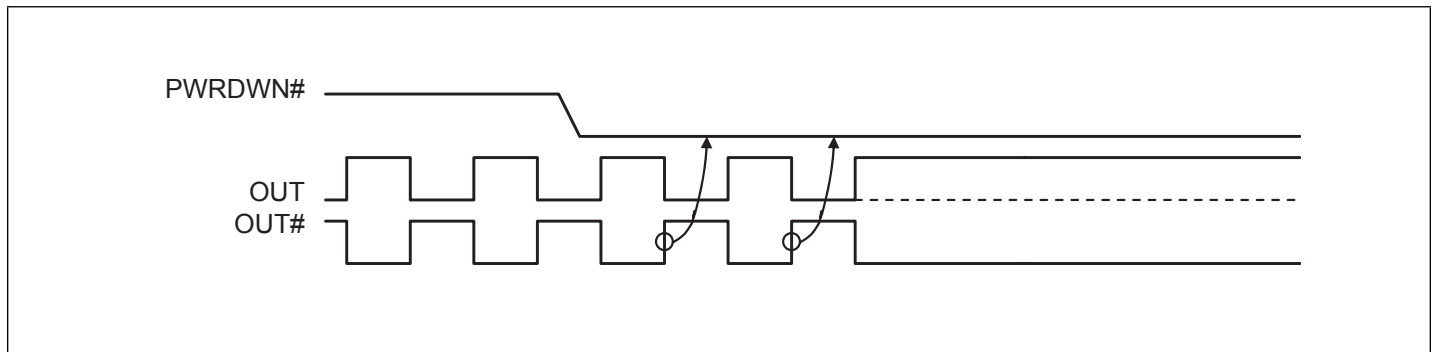


Figure 1. Power down sequence

Power Down (PWRDWN# De-assertion)

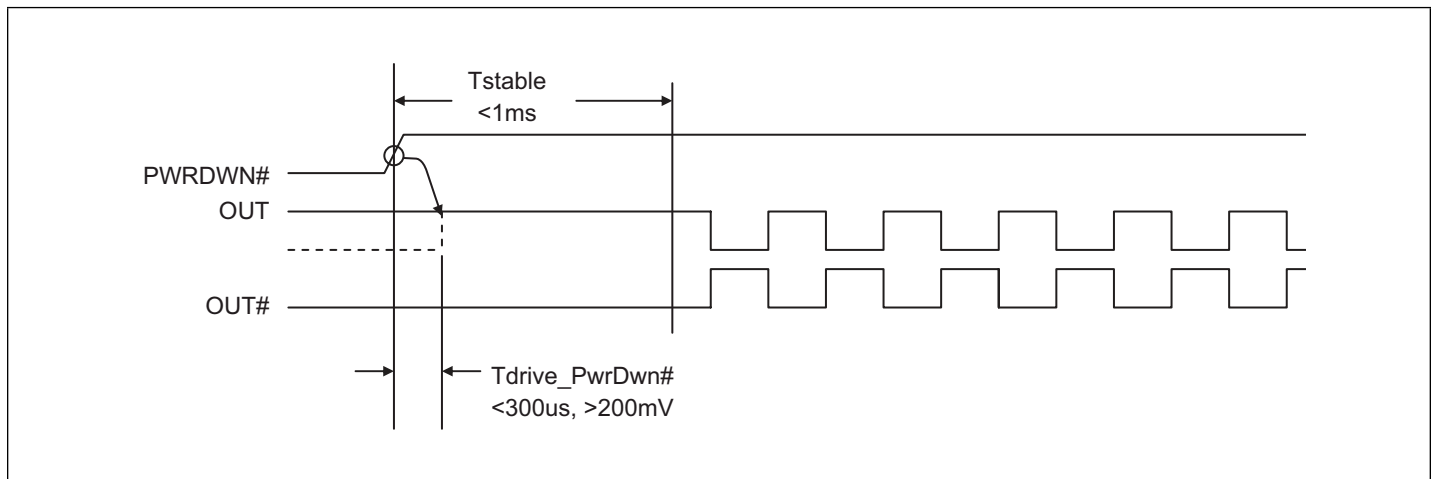
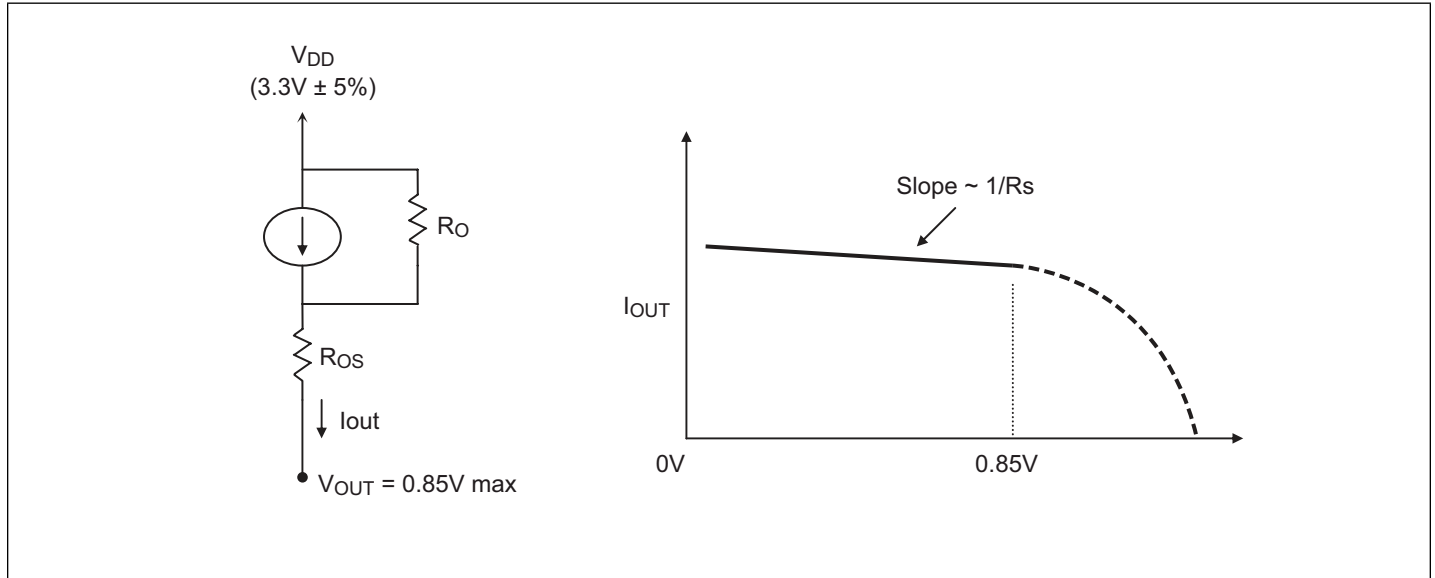


Figure 2. Power down de-assert sequence

Current-mode output buffer characteristics of OUT[0:3], OUT[0:3]#



Differential Clock Buffer characteristics

Symbol	Minimum	Maximum
R_O	3000 Ω	N/A
R_{OS}	unspecified	unspecified
V_{OUT}	N/A	850mV

Current Accuracy

Symbol	Conditions	Configuration	Load	Min.	Max.
I_{OUT}	$V_{DD} = 3.30 \pm 5\%$	$R_{REF} = 475\Omega$ 1% $I_{REF} = 2.32mA$	Nominal test load for given configuration	-12% $I_{NOMINAL}$	+12% $I_{NOMINAL}$

Note:

1. $I_{NOMINAL}$ refers to the expected current based on the configuration of the device.

Differential Clock Output Current

Board Target Trace/Term Z	Reference R, $I_{ref} = V_{DD}/(3 \times R_r)$	Output Current	V_{OH} @ Z
100 Ω (100 Ω differential $\approx$ 15% coupling ratio)	$R_{REF} = 475\Omega$ 1%, $I_{REF} = 2.32mA$	$I_{OH} = 6 \times I_{REF}$	0.7V @ 50

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameters	Min.	Max.	Units
V_{DD_A}	3.3V Core Supply Voltage	-0.5	4.6	V
V_{DD}	3.3V I/O Supply Voltage	-0.5	4.6	
V_{IH}	Input High Voltage		4.6	
V_{IL}	Input Low Voltage	-0.5		
T_s	Storage Temperature	-65	150	°C
V_{ESD}	ESD Protection	2000		V

Note:

1. Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

DC Electrical Characteristics ($V_{DD} = 3.3 \pm 5\%$, $V_{DD_A} = 3.3 \pm 5\%$)

Symbol	Parameters	Condition	Min.	Max.	Units
V_{DD_A}	3.3V Core Supply Voltage		3.135	3.465	V
V_{DD}	3.3V I/O Supply Voltage		3.135	3.465	
V_{IH}	3.3V Input High Voltage	V_{DD}	2.0	$V_{DD} + 0.3$	
V_{IL}	3.3V Input Low Voltage		$V_{SS} - 0.3$	0.8	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{DD}$	-5	+5	μA
V_{OH}	3.3V Output High Voltage	$I_{OH} = -1mA$	2.4		V
V_{OL}	3.3V Output Low Voltage	$I_{OL} = 1mA$		0.4	
I_{OH}	Output High Current	$I_{OH} = 6 \times I_{REF}$ $I_{REF} = 2.32mA$	12.2	15.6	mA
C_{IN}	Input Pin Capacitance		3	5	
C_{OUT}	Output Pin Capacitance			6	pF
L_{PIN}	Pin Inductance			7	nH
$I_{DD(BYPASS)}$	Power Supply Current (PLL Bypass)	$V_{DD} = 3.465V$, $F_{CPU} = 100MHz$		90	mA
I_{DD}	Power Supply Current	$V_{DD} = 3.465V$	Bypass mode	100	
		$F_{CPU} = 100MHz$	PLL mode	130	
I_{SS}	Power Down Current	Driven outputs		40	
I_{SS}	Power Down Current	Tristate outputs		12	
T_A	Ambient Temperature		-40	85	°C

AC Switching Characteristics ($V_{DD} = 3.3 \pm 5\%$, $V_{DD_A} = 3.3 \pm 5\%$)

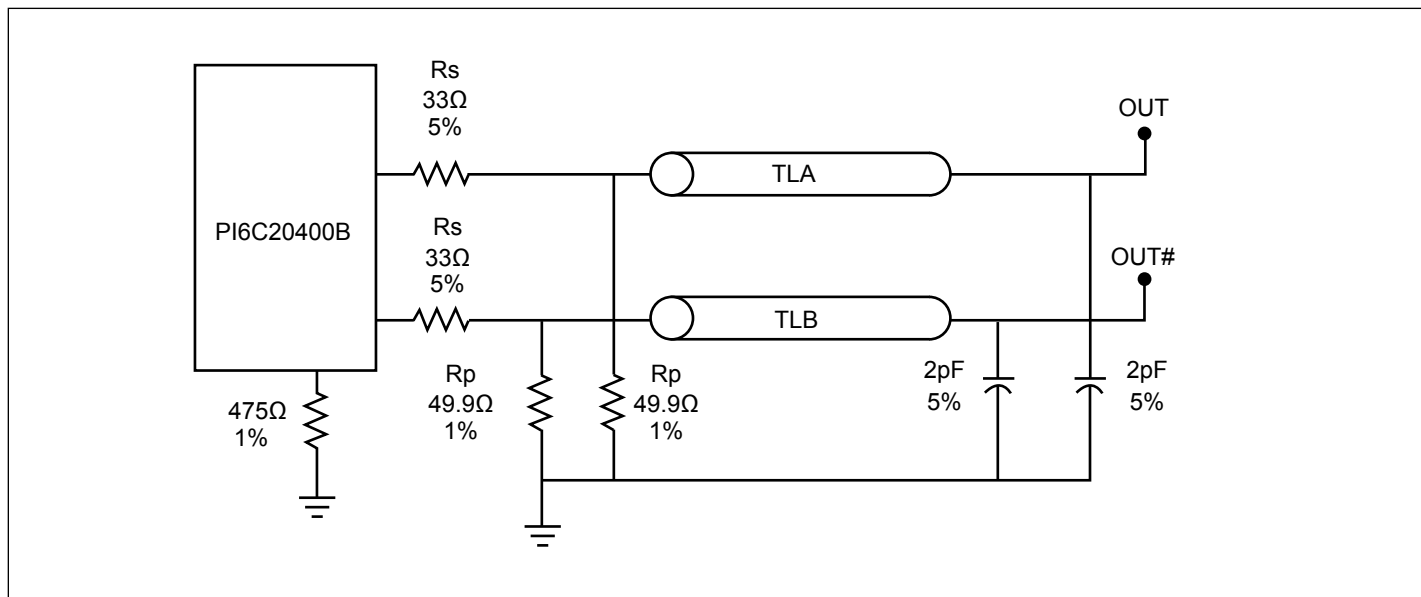
Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
F _{IN}	PLL Mode		95		105	MHz
	Bypass Mode		100		400	MHz
T _{rise} / T _{fall} ²	Rise and Fall Time (measured between 0.175V to 0.525V)		175		700	ps
DT _{rise} / DT _{fall} ²	Rise and Fall Time Variation				125	ps
T _{pd}	PLL Mode				±250	ps
	Non-PLL Mode		2.5		6.5	ns
T _{jitter} ^{3, 4}	Cycle – Cycle Jitter				50	ps
V _{HIGH} ²	Voltage High including overshoot		660		1150	mV
V _{LOW} ²	Voltage Low including undershoot		-300			mV
V _{cross} ²	Absolute crossing point voltages		250		550	mV
DV _{cross} ²	Total Variation of Vcross over all edges				140	mV
T _{DC} ³	Duty Cycle		45		55	%
t _{jphPCIeG1}	Phase Jitter, PLL Mode	PCIe Gen1		30	86	ps (p-p)
t _{jphPCIeG2}		PCIE_2_0_8MHz_1_5M_H3_STEP, Low Freq.		0.7	3	ps (rms)
		PCIE_2_0_8MHz_1_5M_H3_STEP, High Freq.		2	3.1	
t _{jphPCIeG3}		PCIE_3_0_2MHz_5M_H3_FIRST, Low Freq.		2	3	
		PCIE_3_0_2MHz_5M_H3_FIRST, High Freq.		0.47	1	
t _{jphPCIeG1}	Additive Phase Jitter, Bypass Mode	PCIe Gen1		0	0.001	ps (p-p)
t _{jphPCIeG2}		PCIE_2_0_8MHz_1_5M_H3_FIRST, Low Freq.		0	0.001	ps (rms)
		PCIE_2_0_8MHz_1_5M_H3_FIRST, High Freq.		0	0.001	
t _{jphPCIeG3}		PCIE_3_0_2MHz_5M_H3_FIRST, Low Freq.		0	0.001	
		PCIE_3_0_2MHz_5M_H3_FIRST, High Freq.		0	0.001	

Notes:

- Test configuration is $R_s = 33.2\Omega$, $R_p = 49.9\Omega$, and 2pF.
- Measurement taken from Single Ended waveform.
- Measurement taken from Differential waveform.
- Measurement taken using M1 data capture analysis tool.
- Additive jitter is calculated from input and output RMS phase jitter by using PCIe 2.0 filter. ($T_{jadd} = \sqrt{(\text{output jitter})^2 - (\text{input jitter})^2}$)

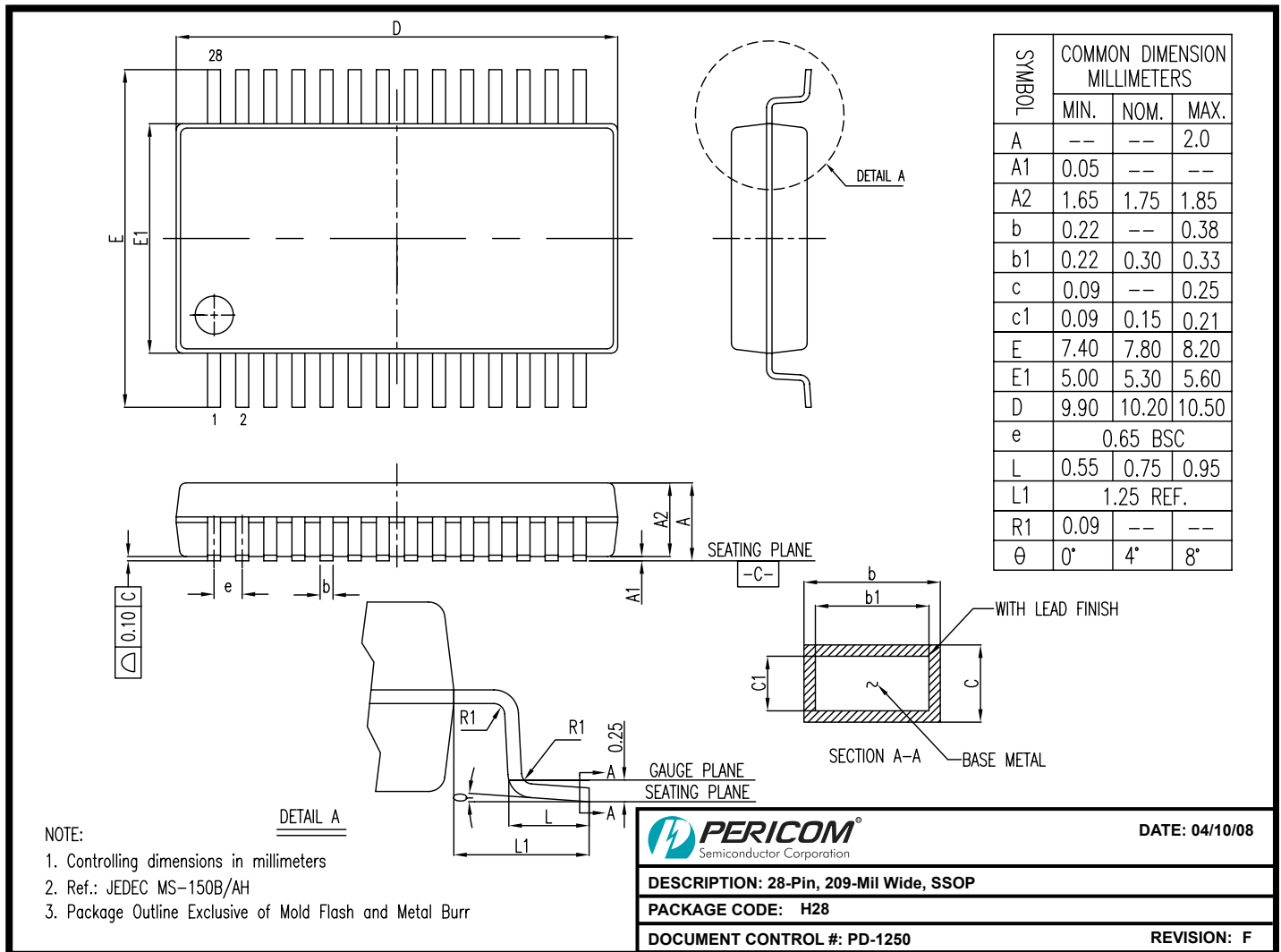
PI6C20400B

Configuration Test Load Board Termination

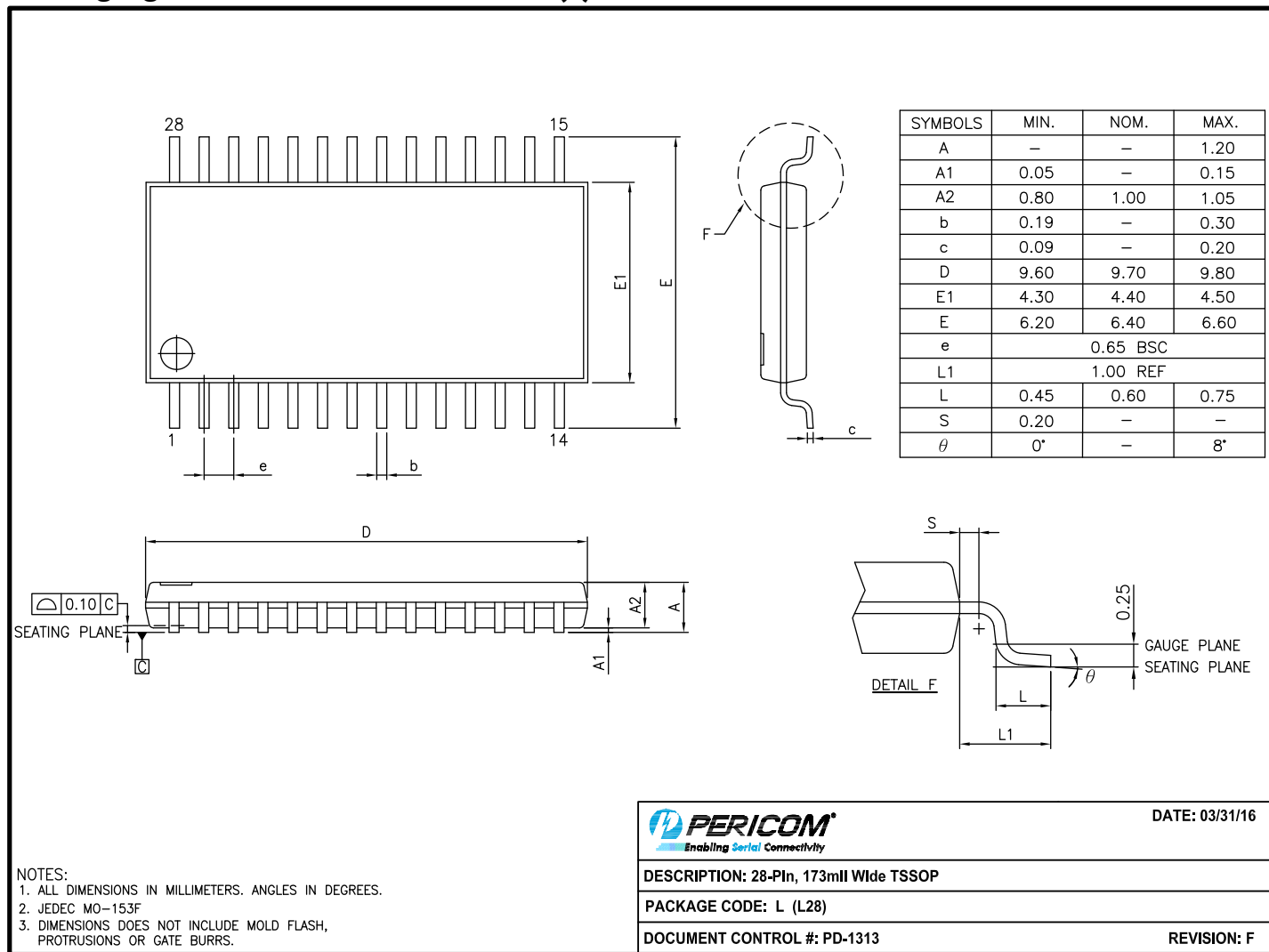


PI6C20400B

Packaging Mechanical: 28-Pin SSOP (H)



08-0143

PI6C20400B
Packaging Mechanical: 28-Pin TSSOP (L)


16-0076

 Note: For latest package info, please check: <http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/>
Ordering Information⁽¹⁻³⁾

Ordering Code	Package Code	Package Description
PI6C20400BHE	H	28-pin, 209-mil wide (SSOP)
PI6C20400BHEX	H	28-pin, 209-mil wide (SSOP), Tape & Reel
PI6C20400BLE	L	28-pin, 173-mil wide (TSSOP)
PI6C20400BLEX	L	28-pin, 173-mil wide (TSSOP), Tape & Reel

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

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