MACRONIX
INTERNATIONAL CO., LTD.

MX29LV640D T/B

64M-BIT [8M x 8/4M x 16] SINGLE VOLTAGE 3V ONLY FLASH MEMORY

The MX29LV640D T/B product family is not recommended for new designs. The MX29LV640E T/B family is the recommended replacement. Please refer to MX29LV640E T/B datasheet for full specifications and ordering information, or contact your local sales representative for additional support.

FEATURES

GENERAL FEATURES

- 8,388,608 x 8 / 4,194,304 x 16 switchable
- Sector Structure
  - 8KB(4KW) x 8 and 64KB(32KW) x 127
- Extra 128-word sector for security
  - Features factory locked and identifiable, and customer lockable
- Sector Groups Protection / Chip Unprotect
  - Provides sector group protect function to prevent program or erase operation in the protected sector group
  - Provides chip unprotect function to allow code changing
  - Provides temporary sector group unprotect function for code changing in previously protected sector groups
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to 1.5 x Vcc
- Low Vcc write inhibit : Vcc ≤ Vlko
- Compatible with JEDEC standard
  - Pinout and software compatible to single power supply Flash

PERFORMANCE

- High Performance
  - Fast access time: 90ns
  - Fast program time: 11us/word (typical)
  - Fast erase time: 0.7s/sector, 45s/chip (typical)
- Low Power Consumption
  - Low active read current: 9mA (typical) at 5MHz
  - Low standby current: 5uA (typical)
- 100,000 erase/program cycle (typical)
- 20 years data retention

SOFTWARE FEATURES

- Erase Suspend/ Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data# Polling & Toggle bits provide detection of program and erase operation completion
- Support Common Flash Interface (CFI)

HARDWARE FEATURES

- Ready/Busy# (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input

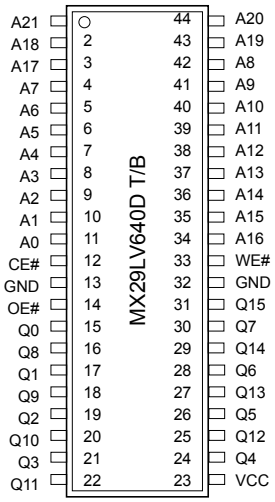
- Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input pin
  - Provides accelerated program capability

PACKAGE

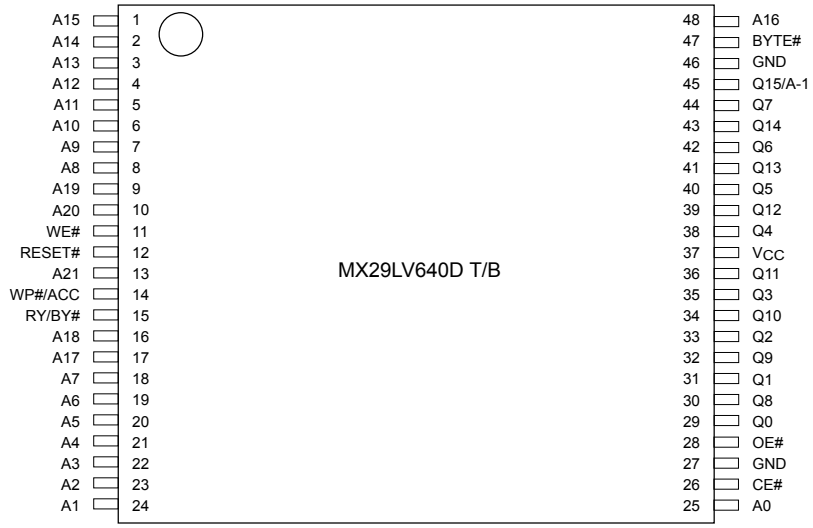
- 44-Pin SOP
- 48-Pin TSOP
- 48-Ball LFBGA
- **All Pb-free devices are RoHS Compliant**

PIN CONFIGURATION

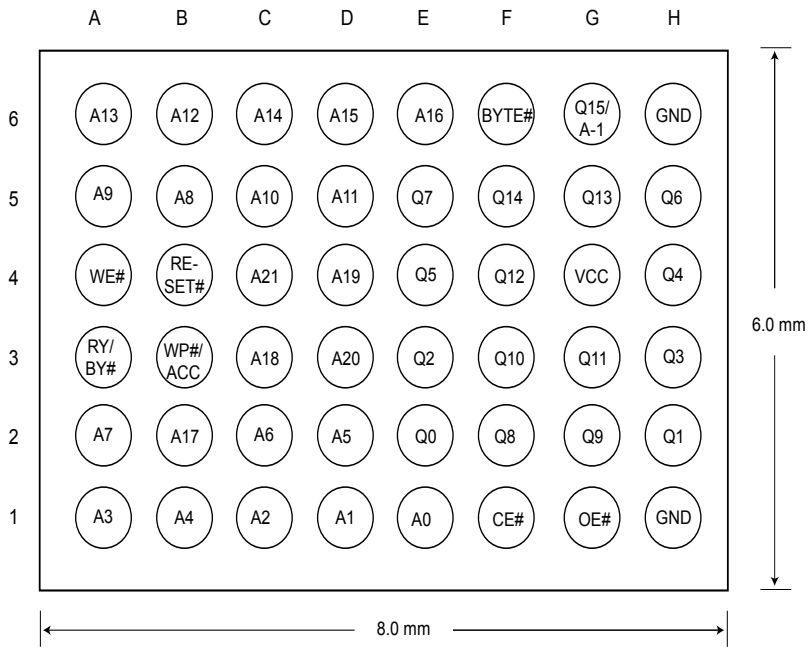
44 SOP



48 TSOP



48-Ball LFBGA 6mm x 8mm (Ball Pich=0.8mm), Top View, Balls Facing Down

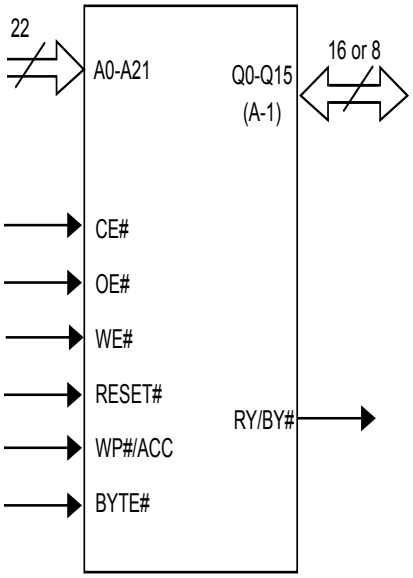


PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A21	Address Input
Q0~Q14	Data Inputs/Outputs
Q15/A-1	Q15(Word Mode)/LSB addr(Byte Mode)
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
RESET#	Hardware Reset Pin, Active Low
BYTE#	Word/Byte Selection Input
WP#/ACC	Hardware Write Protect/Programming Acceleration Input
RY/BY#	Read/Busy Output
VCC	+3.0V single power supply
GND	Device Ground
NC	Pin Not Connected Internally

Note: If customer does not need WP#/ACC, please connect WP#/ACC pin to VCC or let it float. The WP#/ACC has an internal pull-up when unconnected WP#/ACC is at Vih.

LOGIC SYMBOL



BLOCK DIAGRAM

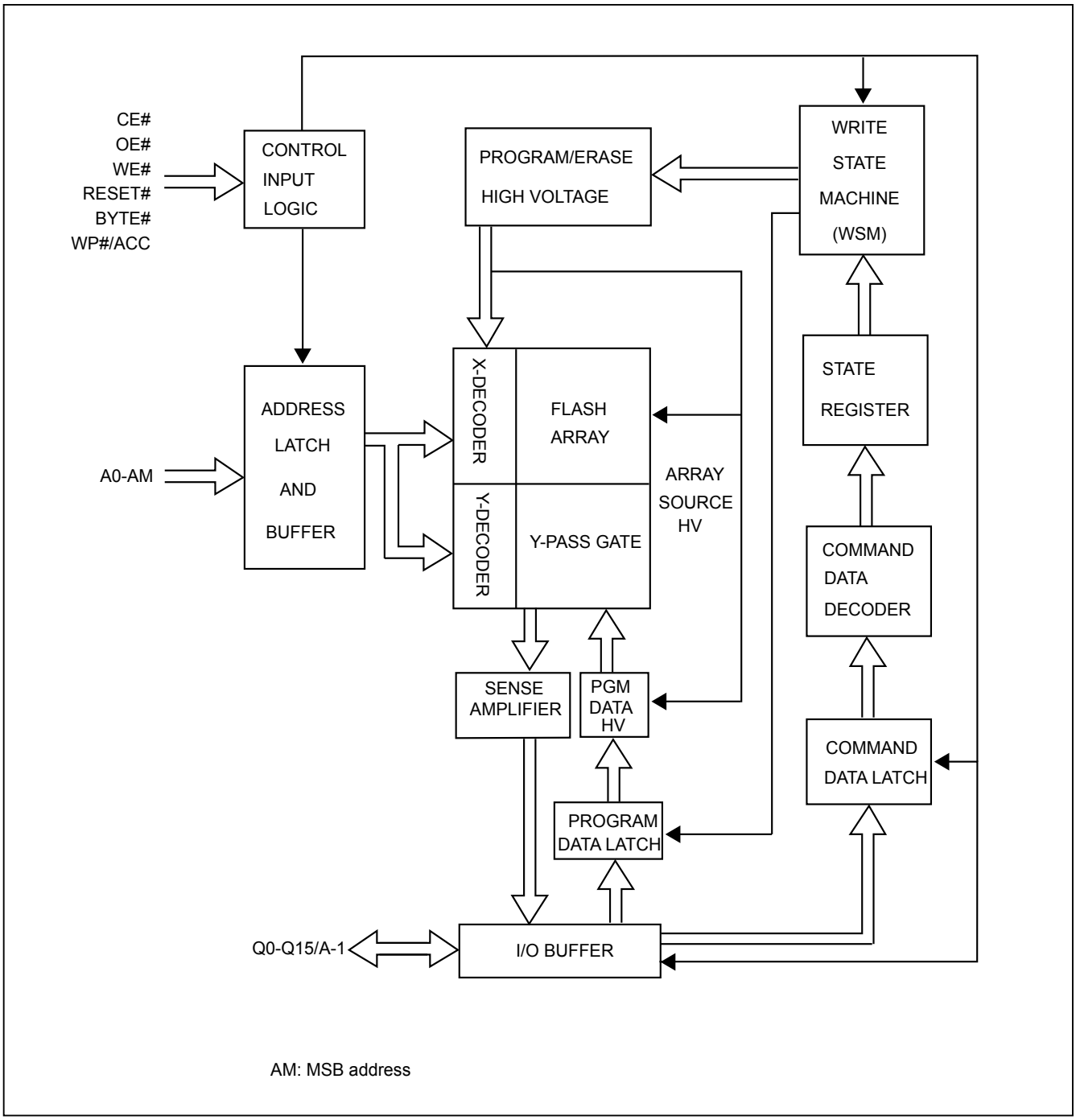


Table 1. BLOCK STRUCTURE

MX29LV640DT SECTOR GROUP ARCHITECTURE

Sector Group	Sector Size		Sector	Sector Address A21-A12	Address Range	
	Byte Mode (Kbytes)	Word Mode (Kwords)			Byte Mode (x8)	Word Mode (x16)
1	64	32	SA0	0000000xxx	000000h-00FFFFh	000000h-07FFFh
1	64	32	SA1	0000001xxx	010000h-01FFFFh	008000h-0FFFFh
1	64	32	SA2	0000010xxx	020000h-02FFFFh	010000h-17FFFh
1	64	32	SA3	0000011xxx	030000h-03FFFFh	018000h-01FFFFh
2	64	32	SA4	0000100xxx	040000h-04FFFFh	020000h-027FFFh
2	64	32	SA5	0000101xxx	050000h-05FFFFh	028000h-02FFFFh
2	64	32	SA6	0000110xxx	060000h-06FFFFh	030000h-037FFFh
2	64	32	SA7	0000111xxx	070000h-07FFFFh	038000h-03FFFFh
3	64	32	SA8	0001000xxx	080000h-08FFFFh	040000h-047FFFh
3	64	32	SA9	0001001xxx	090000h-09FFFFh	048000h-04FFFFh
3	64	32	SA10	0001010xxx	0A0000h-0AFFFFh	050000h-057FFFh
3	64	32	SA11	0001011xxx	0B0000h-0BFFFFh	058000h-05FFFFh
4	64	32	SA12	0001100xxx	0C0000h-0CFFFFh	060000h-067FFFh
4	64	32	SA13	0001101xxx	0D0000h-0DFFFFh	068000h-06FFFFh
4	64	32	SA14	0001110xxx	0E0000h-0EFFFFh	070000h-077FFFh
4	64	32	SA15	0001111xxx	0F0000h-0FFFFFh	078000h-07FFFFh
5	64	32	SA16	0010000xxx	100000h-10FFFFh	080000h-087FFFh
5	64	32	SA17	0010001xxx	110000h-11FFFFh	088000h-08FFFFh
5	64	32	SA18	0010010xxx	120000h-12FFFFh	090000h-097FFFh
5	64	32	SA19	0010011xxx	130000h-13FFFFh	098000h-09FFFFh
6	64	32	SA20	0010100xxx	140000h-14FFFFh	0A0000h-0A7FFFh
6	64	32	SA21	0010101xxx	150000h-15FFFFh	0A8000h-0AFFFFh
6	64	32	SA22	0010110xxx	160000h-16FFFFh	0B0000h-0B7FFFh
6	64	32	SA23	0010111xxx	170000h-17FFFFh	0B8000h-0BFFFFh
7	64	32	SA24	0011000xxx	180000h-18FFFFh	0C0000h-0C7FFFh
7	64	32	SA25	0011001xxx	190000h-19FFFFh	0C8000h-0CFFFFh
7	64	32	SA26	0011010xxx	1A0000h-1AFFFFh	0D0000h-0D7FFFh
7	64	32	SA27	0011011xxx	1B0000h-1BFFFFh	0D8000h-0DFFFFh
8	64	32	SA28	0011100xxx	1C0000h-1CFFFFh	0E0000h-0E7FFFh
8	64	32	SA29	0011101xxx	1D0000h-1DFFFFh	0E8000h-0EFFFFh
8	64	32	SA30	0011110xxx	1E0000h-1EFFFFh	0F0000h-0F7FFFh
8	64	32	SA31	0011111xxx	1F0000h-1FFFFFh	0F8000h-0FFFFFh
9	64	32	SA32	0100000xxx	200000h-20FFFFh	100000h-107FFFh
9	64	32	SA33	0100001xxx	210000h-21FFFFh	108000h-10FFFFh
9	64	32	SA34	0100010xxx	220000h-22FFFFh	110000h-117FFFh
9	64	32	SA35	0100011xxx	230000h-23FFFFh	118000h-11FFFFh
10	64	32	SA36	0100100xxx	240000h-24FFFFh	120000h-127FFFh
10	64	32	SA37	0100101xxx	250000h-25FFFFh	128000h-12FFFFh
10	64	32	SA38	0100110xxx	260000h-26FFFFh	130000h-137FFFh
10	64	32	SA39	0100111xxx	270000h-27FFFFh	138000h-13FFFFh

Sector Group	Sector Size		Sector	Sector Address A21-A12	Address Range	
	Byte Mode (Kbytes)	Word Mode (Kwords)			Byte Mode (x8)	Word Mode (x16)
11	64	32	SA40	0101000xxx	280000h-28FFFFh	140000h-147FFFh
11	64	32	SA41	0101001xxx	290000h-29FFFFh	148000h-14FFFFh
11	64	32	SA42	0101010xxx	2A0000h-2AFFFFh	150000h-157FFFh
11	64	32	SA43	0101011xxx	2B0000h-2BFFFFh	158000h-15FFFFh
12	64	32	SA44	0101100xxx	2C0000h-2CFFFFh	160000h-167FFFh
12	64	32	SA45	0101101xxx	2D0000h-2DFFFFh	168000h-16FFFFh
12	64	32	SA46	0101110xxx	2E0000h-2EFFFFh	170000h-177FFFh
12	64	32	SA47	0101111xxx	2F0000h-2FFFFFh	178000h-17FFFFh
13	64	32	SA48	0110000xxx	300000h-30FFFFh	180000h-187FFFh
13	64	32	SA49	0110001xxx	310000h-31FFFFh	188000h-18FFFFh
13	64	32	SA50	0110010xxx	320000h-32FFFFh	190000h-197FFFh
13	64	32	SA51	0110011xxx	330000h-33FFFFh	198000h-19FFFFh
14	64	32	SA52	0110100xxx	340000h-34FFFFh	1A0000h-1A7FFFh
14	64	32	SA53	0110101xxx	350000h-35FFFFh	1A8000h-1AFFFFh
14	64	32	SA54	0110110xxx	360000h-36FFFFh	1B0000h-1B7FFFh
14	64	32	SA55	0110111xxx	370000h-37FFFFh	1B8000h-1BFFFFh
15	64	32	SA56	0111000xxx	380000h-38FFFFh	1C0000h-1C7FFFh
15	64	32	SA57	0111001xxx	390000h-39FFFFh	1C8000h-1CFFFFh
15	64	32	SA58	0111010xxx	3A0000h-3AFFFFh	1D0000h-1D7FFFh
15	64	32	SA59	0111011xxx	3B0000h-3BFFFFh	1D8000h-1DFFFFh
16	64	32	SA60	0111100xxx	3C0000h-3CFFFFh	1E0000h-1E7FFFh
16	64	32	SA61	0111101xxx	3D0000h-3DFFFFh	1E8000h-1EFFFFh
16	64	32	SA62	0111110xxx	3E0000h-3EFFFFh	1F0000h-1F7FFFh
16	64	32	SA63	0111111xxx	3F0000h-3FFFFFh	1F8000h-1FFFFFh
17	64	32	SA64	1000000xxx	400000h-40FFFFh	200000h-207FFFh
17	64	32	SA65	1000001xxx	410000h-41FFFFh	208000h-20FFFFh
17	64	32	SA66	1000010xxx	420000h-42FFFFh	210000h-217FFFh
17	64	32	SA67	1000011xxx	430000h-43FFFFh	218000h-21FFFFh
18	64	32	SA68	1000100xxx	440000h-44FFFFh	220000h-227FFFh
18	64	32	SA69	1000101xxx	450000h-45FFFFh	228000h-22FFFFh
18	64	32	SA70	1000110xxx	460000h-46FFFFh	230000h-237FFFh
18	64	32	SA71	1000111xxx	470000h-47FFFFh	238000h-23FFFFh
19	64	32	SA72	1001000xxx	480000h-48FFFFh	240000h-247FFFh
19	64	32	SA73	1001001xxx	490000h-49FFFFh	248000h-24FFFFh
19	64	32	SA74	1001010xxx	4A0000h-4AFFFFh	250000h-257FFFh
19	64	32	SA75	1001011xxx	4B0000h-4BFFFFh	258000h-25FFFFh
20	64	32	SA76	1001100xxx	4C0000h-4CFFFFh	260000h-247FFFh
20	64	32	SA77	1001101xxx	4D0000h-4DFFFFh	268000h-24FFFFh
20	64	32	SA78	1001110xxx	4E0000h-4EFFFFh	270000h-277FFFh
20	64	32	SA79	1001111xxx	4F0000h-4FFFFFh	278000h-27FFFFh

Sector Group	Sector Size		Sector	Sector Address A21-A12	Address Range	
	Byte Mode (Kbytes)	Word Mode (Kwords)			Byte Mode (x8)	Word Mode (x16)
21	64	32	SA80	1010000xxx	500000h-50FFFFh	280000h-287FFFh
21	64	32	SA81	1010001xxx	510000h-51FFFFh	288000h-28FFFFh
21	64	32	SA82	1010010xxx	520000h-52FFFFh	290000h-297FFFh
21	64	32	SA83	1010011xxx	530000h-53FFFFh	298000h-29FFFFh
22	64	32	SA84	1010100xxx	540000h-54FFFFh	2A0000h-2A7FFFh
22	64	32	SA85	1010101xxx	550000h-55FFFFh	2A8000h-2AFFFFh
22	64	32	SA86	1010110xxx	560000h-56FFFFh	2B0000h-2B7FFFh
22	64	32	SA87	1010111xxx	570000h-57FFFFh	2B8000h-2BFFFFh
23	64	32	SA88	1011000xxx	580000h-58FFFFh	2C0000h-2C7FFFh
23	64	32	SA89	1011001xxx	590000h-59FFFFh	2C8000h-2CFFFFh
23	64	32	SA90	1011010xxx	5A0000h-5AFFFFh	2D0000h-2D7FFFh
23	64	32	SA91	1011011xxx	5B0000h-5BFFFFh	2D8000h-2DFFFFh
24	64	32	SA92	1011100xxx	5C0000h-5CFFFFh	2E0000h-2E7FFFh
24	64	32	SA93	1011101xxx	5D0000h-5DFFFFh	2E8000h-2EFFFFh
24	64	32	SA94	1011110xxx	5E0000h-5EFFFFh	2F0000h-2F7FFFh
24	64	32	SA95	1011111xxx	5F0000h-5FFFFFh	2F8000h-2FFFFFh
25	64	32	SA96	1100000xxx	600000h-60FFFFh	300000h-307FFFh
25	64	32	SA97	1100001xxx	610000h-61FFFFh	308000h-30FFFFh
25	64	32	SA98	1100010xxx	620000h-62FFFFh	310000h-317FFFh
25	64	32	SA99	1100011xxx	630000h-63FFFFh	318000h-31FFFFh
26	64	32	SA100	1100100xxx	640000h-64FFFFh	320000h-327FFFh
26	64	32	SA101	1100101xxx	650000h-65FFFFh	328000h-32FFFFh
26	64	32	SA102	1100110xxx	660000h-66FFFFh	330000h-337FFFh
26	64	32	SA103	1100111xxx	670000h-67FFFFh	338000h-33FFFFh
27	64	32	SA104	1101000xxx	680000h-68FFFFh	340000h-347FFFh
27	64	32	SA105	1101001xxx	690000h-69FFFFh	348000h-34FFFFh
27	64	32	SA106	1101010xxx	6A0000h-6AFFFFh	350000h-357FFFh
27	64	32	SA107	1101011xxx	6B0000h-6BFFFFh	358000h-35FFFFh
28	64	32	SA108	1101100xxx	6C0000h-6CFFFFh	360000h-347FFFh
28	64	32	SA109	1101101xxx	6D0000h-6DFFFFh	368000h-34FFFFh
28	64	32	SA110	1101110xxx	6E0000h-6EFFFFh	370000h-377FFFh
28	64	32	SA111	1101111xxx	6F0000h-6FFFFFh	378000h-37FFFFh
29	64	32	SA112	1110000xxx	700000h-70FFFFh	380000h-387FFFh
29	64	32	SA113	1110001xxx	710000h-71FFFFh	388000h-38FFFFh
29	64	32	SA114	1110010xxx	720000h-72FFFFh	390000h-397FFFh
29	64	32	SA115	1110011xxx	730000h-73FFFFh	398000h-39FFFFh
30	64	32	SA116	1110100xxx	740000h-74FFFFh	3A0000h-3A7FFFh
30	64	32	SA117	1110101xxx	750000h-75FFFFh	3A8000h-3AFFFFh
30	64	32	SA118	1110110xxx	760000h-76FFFFh	3B0000h-3B7FFFh
30	64	32	SA119	1110111xxx	770000h-77FFFFh	3B8000h-3BFFFFh

Sector Group	Sector Size		Sector	Sector Address A21-A12	Address Range	
	Byte Mode (Kbytes)	Word Mode (Kwords)			Byte Mode (x8)	Word Mode (x16)
31	64	32	SA120	1111000xxx	780000h-78FFFFh	3C0000h-3C7FFFh
31	64	32	SA121	1111001xxx	790000h-79FFFFh	3C8000h-3CFFFFh
31	64	32	SA122	1111010xxx	7A0000h-7AFFFFh	3D0000h-3D7FFFh
31	64	32	SA123	1111011xxx	7B0000h-7BFFFFh	3D8000h-3DFFFFh
32	64	32	SA124	1111100xxx	7C0000h-7CFFFFh	3E0000h-3E7FFFh
32	64	32	SA125	1111101xxx	7D0000h-7DFFFFh	3E8000h-3EFFFFh
32	64	32	SA126	1111110xxx	7E0000h-7EFFFFh	3F0000h-3F7FFFh
33	8	4	SA127	1111111000	7F0000h-7F1FFFh	3F8000h-3FFFFFh
34	8	4	SA128	1111111001	7F2000h-7F3FFFh	3F9000h-3F9FFFh
35	8	4	SA129	1111111010	7F4000h-7F5FFFh	3FA000h-3FAFFFh
36	8	4	SA130	1111111011	7F6000h-7F7FFFh	3FB000h-3FBFFFh
37	8	4	SA131	1111111100	7F8000h-7F9FFFh	3FC000h-3FCFFFh
38	8	4	SA132	1111111101	7FA000h-7FBFFFh	3FD000h-3FDFFFh
39	8	4	SA133	1111111110	7FC000h-7FDFFFh	3FE000h-3FEFFFh
40	8	4	SA134	1111111111	7FE000h-7FFFFFh	3FF000h-3FFFFFh

Top Boot Security Sector Addresses

Sector Size		Sector Address A21~A12	Address Range	
Byte Mode (Kbytes)	Word Mode (Kwords)		Byte Mode (x8)	Word Mode (x16)
256	128	1111111111	7FFF00h-7FFFFFh	3FFF80h-3FFFFFh

MX29LV640DB SECTOR GROUP ARCHITECTURE

Sector Group	Sector Size		Sector	Sector Address A21-A12	Address Range	
	Byte Mode (Kbytes)	Word Mode (Kwords)			Byte Mode (x8)	Word Mode (x16)
1	8	4	SA0	0000000000	000000h-001FFFh	000000h-000FFFh
2	8	4	SA1	0000000001	002000h-003FFFh	001000h-001FFFh
3	8	4	SA2	0000000010	004000h-005FFFh	002000h-002FFFh
4	8	4	SA3	0000000011	006000h-007FFFh	003000h-003FFFh
5	8	4	SA4	0000000100	008000h-009FFFh	004000h-004FFFh
6	8	4	SA5	0000000101	00A000h-00BFFFh	005000h-005FFFh
7	8	4	SA6	0000000110	00C000h-00DFFFh	006000h-006FFFh
8	8	4	SA7	0000000111	00E000h-00FFFFh	007000h-007FFFh
9	64	32	SA8	0000001xxx	010000h-01FFFFh	008000h-00FFFFh
9	64	32	SA9	0000010xxx	020000h-02FFFFh	010000h-017FFFh
9	64	32	SA10	0000011xxx	030000h-03FFFFh	018000h-01FFFFh
10	64	32	SA11	0000100xxx	040000h-04FFFFh	020000h-027FFFh
10	64	32	SA12	0000101xxx	050000h-05FFFFh	028000h-02FFFFh
10	64	32	SA13	0000110xxx	060000h-06FFFFh	030000h-037FFFh
10	64	32	SA14	0000111xxx	070000h-07FFFFh	038000h-03FFFFh
11	64	32	SA15	0001000xxx	080000h-08FFFFh	040000h-047FFFh
11	64	32	SA16	0001001xxx	090000h-09FFFFh	048000h-04FFFFh
11	64	32	SA17	0001010xxx	0A0000h-0AFFFFh	050000h-057FFFh
11	64	32	SA18	0001011xxx	0B0000h-0BFFFFh	058000h-05FFFFh
12	64	32	SA19	0001100xxx	0C0000h-0CFFFFh	060000h-067FFFh
12	64	32	SA20	0001101xxx	0D0000h-0DFFFFh	068000h-06FFFFh
12	64	32	SA21	0001110xxx	0E0000h-0EFFFFh	070000h-077FFFh
12	64	32	SA22	0001111xxx	0F0000h-0FFFFFh	078000h-07FFFFh
13	64	32	SA23	0010000xxx	100000h-10FFFFh	080000h-087FFFh
13	64	32	SA24	0010001xxx	110000h-11FFFFh	088000h-08FFFFh
13	64	32	SA25	0010010xxx	120000h-12FFFFh	090000h-097FFFh
13	64	32	SA26	0010011xxx	130000h-13FFFFh	098000h-09FFFFh
14	64	32	SA27	0010100xxx	140000h-14FFFFh	0A0000h-0A7FFFh
14	64	32	SA28	0010101xxx	150000h-15FFFFh	0A8000h-0AFFFFh
14	64	32	SA29	0010110xxx	160000h-16FFFFh	0B0000h-0B7FFFh
14	64	32	SA30	0010111xxx	170000h-17FFFFh	0B8000h-0BFFFFh
15	64	32	SA31	0011000xxx	180000h-18FFFFh	0C0000h-0C7FFFh
15	64	32	SA32	0011001xxx	190000h-19FFFFh	0C8000h-0CFFFFh
15	64	32	SA33	0011010xxx	1A0000h-1AFFFFh	0D0000h-0D7FFFh
15	64	32	SA34	0011011xxx	1B0000h-1BFFFFh	0D8000h-0DFFFFh
16	64	32	SA35	0011100xxx	1C0000h-1CFFFFh	0E0000h-0E7FFFh
16	64	32	SA36	0011101xxx	1D0000h-1DFFFFh	0E8000h-0EFFFFh
16	64	32	SA37	0011110xxx	1E0000h-1EFFFFh	0F0000h-0F7FFFh
16	64	32	SA38	0011111xxx	1F0000h-1FFFFFh	0F8000h-0FFFFFh

Sector Group	Sector Size		Sector	Sector Address A21-A12	Address Range	
	Byte Mode (Kbytes)	Word Mode (Kwords)			Byte Mode (x8)	Word Mode (x16)
17	64	32	SA39	0100000xxx	200000h-20FFFFh	100000h-107FFFh
17	64	32	SA40	0100001xxx	210000h-21FFFFh	108000h-10FFFFh
17	64	32	SA41	0100010xxx	220000h-22FFFFh	110000h-117FFFh
17	64	32	SA42	0100011xxx	230000h-23FFFFh	118000h-11FFFFh
18	64	32	SA43	0100100xxx	240000h-24FFFFh	120000h-127FFFh
18	64	32	SA44	0100101xxx	250000h-25FFFFh	128000h-12FFFFh
18	64	32	SA45	0100110xxx	260000h-26FFFFh	130000h-137FFFh
18	64	32	SA46	0100111xxx	270000h-27FFFFh	138000h-13FFFFh
19	64	32	SA47	0101000xxx	280000h-28FFFFh	140000h-147FFFh
19	64	32	SA48	0101001xxx	290000h-29FFFFh	148000h-14FFFFh
19	64	32	SA49	0101010xxx	2A0000h-2AFFFFh	150000h-157FFFh
19	64	32	SA50	0101011xxx	2B0000h-2BFFFFh	158000h-15FFFFh
20	64	32	SA51	0101100xxx	2C0000h-2CFFFFh	160000h-167FFFh
20	64	32	SA52	0101101xxx	2D0000h-2DFFFFh	168000h-16FFFFh
20	64	32	SA53	0101110xxx	2E0000h-2EFFFFh	170000h-177FFFh
20	64	32	SA54	0101111xxx	2F0000h-2FFFFFh	178000h-17FFFFh
21	64	32	SA55	0110000xxx	300000h-30FFFFh	180000h-187FFFh
21	64	32	SA56	0110001xxx	310000h-31FFFFh	188000h-18FFFFh
21	64	32	SA57	0110010xxx	320000h-32FFFFh	190000h-197FFFh
21	64	32	SA58	0110011xxx	330000h-33FFFFh	198000h-19FFFFh
22	64	32	SA59	0110100xxx	340000h-34FFFFh	1A0000h-1A7FFFh
22	64	32	SA60	0110101xxx	350000h-35FFFFh	1A8000h-1AFFFFh
22	64	32	SA61	0110110xxx	360000h-36FFFFh	1B0000h-1B7FFFh
22	64	32	SA62	0110111xxx	370000h-37FFFFh	1B8000h-1BFFFFh
23	64	32	SA63	0111000xxx	380000h-38FFFFh	1C0000h-1C7FFFh
23	64	32	SA64	0111001xxx	390000h-39FFFFh	1C8000h-1CFFFFh
23	64	32	SA65	0111010xxx	3A0000h-3AFFFFh	1D0000h-1D7FFFh
23	64	32	SA66	0111011xxx	3B0000h-3BFFFFh	1D8000h-1DFFFFh
24	64	32	SA67	0111100xxx	3C0000h-3CFFFFh	1E0000h-1E7FFFh
24	64	32	SA68	0111101xxx	3D0000h-3DFFFFh	1E8000h-1EFFFFh
24	64	32	SA69	0111110xxx	3E0000h-3EFFFFh	1F0000h-1F7FFFh
24	64	32	SA70	0111111xxx	3F0000h-3FFFFFh	1F8000h-1FFFFFh
25	64	32	SA71	1000000xxx	400000h-40FFFFh	200000h-207FFFh
25	64	32	SA72	1000001xxx	410000h-41FFFFh	208000h-20FFFFh
25	64	32	SA73	1000010xxx	420000h-42FFFFh	210000h-217FFFh
25	64	32	SA74	1000011xxx	430000h-43FFFFh	218000h-21FFFFh
26	64	32	SA75	1000100xxx	440000h-44FFFFh	220000h-227FFFh
26	64	32	SA76	1000101xxx	450000h-45FFFFh	228000h-22FFFFh
26	64	32	SA77	1000110xxx	460000h-46FFFFh	230000h-237FFFh
26	64	32	SA78	1000111xxx	470000h-47FFFFh	238000h-23FFFFh

Sector Group	Sector Size		Sector	Sector Address A21-A12	Address Range	
	Byte Mode (Kbytes)	Word Mode (Kwords)			Byte Mode (x8)	Word Mode (x16)
27	64	32	SA79	1001000xxx	480000h-48FFFFh	240000h-247FFFh
27	64	32	SA80	1001001xxx	490000h-49FFFFh	248000h-24FFFFh
27	64	32	SA81	1001010xxx	4A0000h-4AFFFFh	250000h-257FFFh
27	64	32	SA82	1001011xxx	4B0000h-4BFFFFh	258000h-25FFFFh
28	64	32	SA83	1001100xxx	4C0000h-4CFFFFh	260000h-267FFFh
28	64	32	SA84	1001101xxx	4D0000h-4DFFFFh	268000h-26FFFFh
28	64	32	SA85	1001110xxx	4E0000h-4EFFFFh	270000h-277FFFh
28	64	32	SA86	1001111xxx	4F0000h-4FFFFFh	278000h-27FFFFh
29	64	32	SA87	1010000xxx	500000h-50FFFFh	280000h-287FFFh
29	64	32	SA88	1010001xxx	510000h-51FFFFh	288000h-28FFFFh
29	64	32	SA89	1010010xxx	520000h-52FFFFh	290000h-297FFFh
29	64	32	SA90	1010011xxx	530000h-53FFFFh	298000h-29FFFFh
30	64	32	SA91	1010100xxx	540000h-54FFFFh	2A0000h-2A7FFFh
30	64	32	SA92	1010101xxx	550000h-55FFFFh	2A8000h-2AFFFFh
30	64	32	SA93	1010110xxx	560000h-56FFFFh	2B0000h-2B7FFFh
30	64	32	SA94	1010111xxx	570000h-57FFFFh	2B8000h-2BFFFFh
31	64	32	SA95	1011000xxx	580000h-58FFFFh	2C0000h-2C7FFFh
31	64	32	SA96	1011001xxx	590000h-59FFFFh	2C8000h-2CFFFFh
31	64	32	SA97	1011010xxx	5A0000h-5AFFFFh	2D0000h-2D7FFFh
31	64	32	SA98	1011011xxx	5B0000h-5BFFFFh	2D8000h-2DFFFFh
32	64	32	SA99	1011100xxx	5C0000h-5CFFFFh	2E0000h-2E7FFFh
32	64	32	SA100	1011101xxx	5D0000h-5DFFFFh	2E8000h-2EFFFFh
32	64	32	SA101	1011110xxx	5E0000h-5EFFFFh	2F0000h-2F7FFFh
32	64	32	SA102	1011111xxx	5F0000h-5FFFFFh	2F8000h-2FFFFFh
33	64	32	SA103	1100000xxx	600000h-60FFFFh	300000h-307FFFh
33	64	32	SA104	1100001xxx	610000h-61FFFFh	308000h-30FFFFh
33	64	32	SA105	1100010xxx	620000h-62FFFFh	310000h-317FFFh
33	64	32	SA106	1100011xxx	630000h-63FFFFh	318000h-31FFFFh
34	64	32	SA107	1100100xxx	640000h-64FFFFh	320000h-327FFFh
34	64	32	SA108	1100101xxx	650000h-65FFFFh	328000h-32FFFFh
34	64	32	SA109	1100110xxx	660000h-66FFFFh	330000h-337FFFh
34	64	32	SA110	1100111xxx	670000h-67FFFFh	338000h-33FFFFh
35	64	32	SA111	1101000xxx	680000h-68FFFFh	340000h-347FFFh
35	64	32	SA112	1101001xxx	690000h-69FFFFh	348000h-34FFFFh
35	64	32	SA113	1101010xxx	6A0000h-6AFFFFh	350000h-357FFFh
35	64	32	SA114	1101011xxx	6B0000h-6BFFFFh	358000h-35FFFFh
36	64	32	SA115	1101100xxx	6C0000h-6CFFFFh	360000h-367FFFh
36	64	32	SA116	1101101xxx	6D0000h-6DFFFFh	368000h-36FFFFh
36	64	32	SA117	1101110xxx	6E0000h-6EFFFFh	370000h-377FFFh
36	64	32	SA118	1101111xxx	6F0000h-6FFFFFh	378000h-37FFFFh

Sector Group	Sector Size		Sector	Sector Address A21-A12	Address Range	
	Byte Mode (Kbytes)	Word Mode (Kwords)			Byte Mode (x8)	Word Mode (x16)
37	64	32	SA119	1110000xxx	700000h-70FFFFh	380000h-387FFFh
37	64	32	SA120	1110001xxx	710000h-71FFFFh	388000h-38FFFFh
37	64	32	SA121	1110010xxx	720000h-72FFFFh	390000h-397FFFh
37	64	32	SA122	1110011xxx	730000h-73FFFFh	398000h-39FFFFh
38	64	32	SA123	1110100xxx	740000h-74FFFFh	3A0000h-3A7FFFh
38	64	32	SA124	1110101xxx	750000h-75FFFFh	3A8000h-3AFFFFh
38	64	32	SA125	1110110xxx	760000h-76FFFFh	3B0000h-3B7FFFh
38	64	32	SA126	1110111xxx	770000h-77FFFFh	3B8000h-3BFFFFh
39	64	32	SA127	1111000xxx	780000h-78FFFFh	3C0000h-3C7FFFh
39	64	32	SA128	1111001xxx	790000h-79FFFFh	3C8000h-3CFFFFh
39	64	32	SA129	1111010xxx	7A0000h-7AFFFFh	3D0000h-3D7FFFh
39	64	32	SA130	1111011xxx	7B0000h-7BFFFFh	3D8000h-3DFFFFh
40	64	32	SA131	1111100xxx	7C0000h-7CFFFFh	3E0000h-3E7FFFh
40	64	32	SA132	1111101xxx	7D0000h-7DFFFFh	3E8000h-3EFFFFh
40	64	32	SA133	1111110xxx	7E0000h-7EFFFFh	3F0000h-3F7FFFh
40	64	32	SA134	1111111xxx	7F0000h-7FFFFFh	3F8000h-3FFFFFh

Bottom Boot Security Sector Addresses

Sector Size		Sector Address A21~A12	Address Range	
Byte Mode (Kbytes)	Word Mode (Kwords)		Byte Mode (x8)	Word Mode (x16)
256	128	0000000xxx	000000h-0000FFh	000000h-00007Fh

Table 2. BUS OPERATION--1

Mode Select	RE-SET#	CE#	WE#	OE#	Address	Data (I/O) Q0~Q7	Byte# Vil Q8~Q15	Byte# Vih Q8~Q15	WP#/ ACC
Device Reset	L	X	X	X	X	HighZ	HighZ	HighZ	L/H
Standby Mode	Vcc± 0.3V	Vcc± 0.3V	X	X	X	HighZ	HighZ	HighZ	H
Output Disable	H	L	H	H	X	HighZ	HighZ	HighZ	L/H
Read Mode	H	L	H	L	AIN	DOUT	Q8-Q14= HighZ, Q15=A-1	DOUT	L/H
Write(Note1)	H	L	L	H	AIN	DIN		DIN	Note3
Accelerate Program	H	L	L	H	AIN	DIN		DIN	Vhv
Temporary Sector-Group Unprotect	Vhv	X	X	X	AIN	DIN	HighZ	DIN	Note3
Sector-Group Protect (Note2)	Vhv	L	L	H	Sector Address, A6=L, A1=H, A0=L	DIN, DOUT	X	X	L/H
Chip Unprotect (Note2)	Vhv	L	L	H	Sector Address, A6=H, A1=H, A0=L	DIN, DOUT	X	X	Note3

Notes:
1. All sectors will be unprotected if WP#/ACC=Vhv.
2. The two outmost boot sectors are protected if WP#/ACC=Vil.
3. When WP#/ACC = Vih, the protection conditions of the two outmost boot sectors depend on previous protection conditions."Sector/Sector Block Protection and Unprotection" describes the protect and unprotect method.
4. Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.
5. In Word Mode (Byte#=Vih), the addresses are AM to A0.
   In Byte Mode (Byte#=Vil), the addresses are AM to A-1 (Q15).
6. AM: MSB of address.

BUS OPERATION--2

Item	Control Input			AM to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	Q0~Q7	Q8~Q15
	CE#	WE#	OE#										
Sector Lock Status Verification	L	H	L	SA	x	V_{hv}	x	L	x	H	L	01h or 00h (Note1)	x
Read Silicon ID Manufacturer Code	L	H	L	x	x	V_{hv}	x	L	x	L	L	C2h	x
Read Silicon ID MX29LV640DT	L	H	L	x	x	V_{hv}	x	L	x	L	H	C9h	22h(Word) XXh(Byte)
Read Silicon ID MX29LV640DB	L	H	L	x	x	V_{hv}	x	L	x	L	H	CBh	22h(Word) XXh(Byte)
Read Indicator Bit (Q7) For Security Sector	L	H	L	x	x	V_{hv}	x	L	x	H	H	(Note2)	x

Notes:
1. Sector unprotected code:00h. Sector protected code:01h.
2. Factory locked code: 88h.
   Factory unlocked code: 08h.
3. AM: MSB of address.

WRITE COMMANDS/COMMAND SEQUENCES

To write a command to the device, system must drive WE# and CE# to Vil, and OE# to Vih. In a command cycle, all address are latched at the later falling edge of CE# and WE#, and all data are latched at the earlier rising edge of CE# and WE#.

Figure 1 illustrates the AC timing waveform of a write command, and Table 3 defines all the valid command sets of the device. System is not allowed to write invalid commands not defined in this datasheet. Writing an invalid command will bring the device to an undefined state.

REQUIREMENTS FOR READING ARRAY DATA

Read array action is to read the data stored in the array. While the memory device is in powered up or has been reset, it will automatically enter the status of read array. If the microprocessor wants to read the data stored in the array, it has to drive CE# (device enable control pin) and OE# (Output control pin) as Vil, and input the address of the data to be read into address pin at the same time. After a period of read cycle (Tce or Taa), the data being read out will be displayed on output pin for microprocessor to access. If CE# or OE# is Vih, the output will be in tri-state, and there will be no data displayed on output pin at all.

After the memory device completes embedded operation (automatic Erase or Program), it will automatically return to the status of read array, and the device can read the data in any address in the array. In the process of erasing, if the device receives the Erase suspend command, erase operation will be stopped temporarily after a period of time no more than Tready and the device will return to the status of read array. At this time, the device can read the data stored in any address except the sector being erased in the array. In the status of erase suspend, if user wants to read the data in the sectors being erased, the device will output status data onto the output. Similarly, if program command is issued after erase suspend, after program operation is completed, system can still read array data in any address except the sectors to be erased.

The device needs to issue reset command to enable read array operation again in order to arbitrarily read the data in the array in the following two situations:

1. In program or erase operation, the programming or erasing failure causes Q5 to go high.

2. The device is in auto select mode or CFI mode.

In the two situations above, if reset command is not issued, the device is not in read array mode and system must issue reset command before reading array data.

ACCELERATED PROGRAM OPERATION

The accelerated program can improve programming performance compared with word/byte program. By applying Vhv on WP#/ACC pin, the device will enter accelerated program and draw current no more than Icp1 from WP#/ACC pin. Removing the Vhv from WP#/ACC pin will put the device back to normal operation (not accelerated).

RESET# OPERATION

Driving RESET# pin low for a period more than Trp will reset the device back to read mode. If the device is in program or erase operation, the reset operation will take at most a period of Tready for the device to return to read array mode. Before the device returns to read array mode, the RY/BY# pin remains low (busy status).

When RESET# pin is held at GND±0.3V, the device consumes standby current(Isb).However, device draws larger current if RESET# pin is held at Vil but not within GND±0.3V.

It is recommended that the system to tie its reset signal to RESET# pin of flash memory, so that the flash memory will be reset during system reset and allows system to read boot code from flash memory.

SECTOR GROUP PROTECT OPERATION

When a sector group is protected, program or erase operation will be disabled on these sectors. MX29LV640D T/B provides two methods for sector group protection.

Once the sector group is protected, the sector group remains protected until next chip unprotect, or is temporarily unprotected by asserting RESET# pin at Vhv. Refer to temporary sector group unprotect operation for further details.

The first method is by applying Vhv on RESET# pin. Refer to Figure 13 for timing diagram and Figure 14 for the algorithm for this method.

The other method is asserting Vhv on A9 and OE# pins, with A6 and CE# at Vil. The protection operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

CHIP UNPROTECT OPERATION

MX29LV640D T/B provides two methods for chip unprotect. The chip unprotect operation unprotects all sectors within the device. It is recommended to protect all sectors before activating chip unprotect mode. All sectors groups are unprotected when shipped from the factory.

The first method is by applying Vhv on RESET# pin. Refer to Figure 13 for timing diagram and Figure 14 for algorithm of the operation.

The other method is asserting Vhv on A9 and OE# pins, with A6 at Vih and CE# at Vil. The unprotect operation begins at the falling edge of WE# and terminates at the rising edge. Contact Macronix for details.

TEMPORARY SECTOR GROUP UNPROTECT OPERATION

System can apply RESET# pin at Vhv to place the device in temporary unprotect mode. In this mode, previously protected sectors can be programmed or erased just as it is unprotected. The devices returns to normal operation once Vhv is removed from RESET# pin and previously protected sectors are again protected.

WRITE PROTECT (WP#)

Another function of the WP#/ACC pin is to provide write protection function on the two outermost 8 Kbyte boot sectors. When ViL is asserted on WP#/ACC pin, the two boot sectors are protected regardless of the previous state of protection implemented by aforementioned Sector Group Protect/Chip Unprotect. For MX29LV640DT, the two outermost sectors are the two boot sectors of the highest addresses. For MX29LV640DB, the two outermost sectors are the two boot sectors of the lowest addresses.

Note that the WP#/ACC should be either Vhv, Vih, or Vil, and must not be floated or unconnected; otherwise the device may not function properly.

AUTOMATIC SELECT OPERATION

When the device is in Read array mode, erase-suspended read array mode or CFI mode, user can issue read silicon ID command to enter read silicon ID mode. After entering read silicon ID mode, user can query several silicon IDs continuously and does not need to issue read silicon ID mode again. When A0 is Low, device will output Macronix Manufacture ID C2H. When A0 is high, device will output Device ID. In read silicon ID mode, issuing reset command will reset device back to read array mode or erase-suspended read array mode.

Another way to enter read silicon ID is to apply high voltage on A9 pin with CE#, OE#, A6 and A1 at Vil. While the high voltage of A9 pin is discharged, device will automatically leave read silicon ID mode and go back to read array mode or erase-suspended read array mode. When A0 is Low, device will output Macronix Manufacture ID C2. When A0 is high, device will output Device ID.

VERIFY SECTOR GROUP PROTECT STATUS OPERATION

MX29LV640D T/B provides hardware sector protection against Program and Erase operation for protected sectors. The sector protect status can be read through Sector Protect Verify command. This method requires V_{hv} on A9 pin, Vih on WE# and A1 pins, Vil on CE#, OE#, A6 and A0 pins, and sector address on A12 to A21 pins. If the read out data is 01H, the designated sector is protected. Oppositely, if the read out data is 00H, the designated sector is not protected.

SECURITY SECTOR FLASH MEMORY REGION

The Security Sector region is an extra memory space of 128 words in length. The security sectors can be locked upon shipping from factory, or it can be locked by customer after shipping. Customer can issue Security Sector Factory Protect Verify and/or Security Sector Protect Verify to query the lock status of the device.

In factory-locked device, security sector region is protected when shipped from factory and the security silicon sector indicator bit is set to "1". In customer lockable device, security sector region is unprotected when shipped from factory and the security silicon indicator bit is set to "0".

Factory Locked: Security Sector Programmed and Protected at the Factory

In a factory locked device, the security silicon region is permanently locked after shipping from factory. The device will have a 16-byte (8-word) ESN in the security region. In bottom boot device : 000000h - 000007h (for MX29LV640DB).In Top boot device : 3FFF70h - 3FFF77h (for MX29LV640DT).

Customer Lockable: Security Sector NOT Programmed or Protected at the Factory

When the security feature is not required, the security region can act as an extra memory space.

Security silicon sector can also be protected by two methods. Note that once the security silicon sector is protected, there is no way to unprotect the security silicon sector and the content of it can no longer be altered.

The first method is to write a three-cycle command of Enter Security Region, and then follow the sector group protect algorithm as illustrated in Figure 14, except that RESET# pin may at either Vih or Vhv.

The other method is to write a three-cycle command of Enter Security Region, and then follow the alternate method of sector protect with A9, OE# at Vhv.

After the security silicon is locked and verified, system must write Exit Security Sector Region, go through a power cycle, or issue a hardware reset to return the device to read normal array mode.

DATA PROTECTION

To avoid accidental erasure or programming of the device, the device is automatically reset to read array mode during power up. Besides, only after successful completion of the specified command sets will the device begin its erase or program operation.

Other features to protect the data from accidental alternation are described as followed.

LOW VCC WRITE INHIBIT

The device refuses to accept any write command when Vcc is less than Vlko. This prevents data from spuriously altered. The device automatically resets itself when Vcc is lower than Vlko and write cycles are ignored until Vcc is greater than Vlko. System must provide proper signals on control pins after Vcc is larger than Vlko to avoid unintentional program or erase operation

WRITE PULSE "GLITCH" PROTECTION

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle.

LOGICAL INHIBIT

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. Write cycle is ignored when either CE# at Vih, WE# a Vih, or OE# at Vil.

POWER-UP SEQUENCE

Upon power up, MX29LV640D T/B is placed in read array mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

POWER-UP WRITE INHIBIT

When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

POWER SUPPLY DECOUPLING

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

TABLE 3. MX29LV640D T/B COMMAND DEFINITIONS

Command		Read Mode	Reset Mode	Automatic Select								Enter Security Sector Region Enable	
				Manifacture ID		Device ID		Sector Factory		Sector Protect Verify			
				Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte
1st Bus Cycle	Addr	Addr	XXX	555	AAA	555	AAA	555	AAA	555	AAA	555	AAA
	Data	Data	F0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
2nd Bus Cycle	Addr			2AA	555	2AA	555	2AA	555	2AA	555	2AA	555
	Data			55	55	55	55	55	55	55	55	55	55
3rd Bus Cycle	Addr			555	AAA	555	AAA	555	AAA	555	AAA	555	AAA
	Data			90	90	90	90	90	90	90	90	88	88
4th Bus Cycle	Addr			X00	X00	X01	X02	X03	X06	(Sector) X02	(Sector) X04		
	Data			C2h	C2h	ID	ID	88/08	88/08	00/01	00/01		
5th Bus Cycle	Addr												
	Data												
6th Bus Cycle	Addr												
	Data												

Command		Exit Security Sector		Program		Chip Erase		Sector Erase		CFI Read		Erase Suspend	Erase Resume
		Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Byte/ Word	Byte/ Word
1st Bus Cycle	Addr	555	AAA	555	AAA	555	AAA	555	AAA	55	AA	XXX	XXX
	Data	AA	AA	AA	AA	AA	AA	AA	AA	98	98	B0	30
2nd Bus Cycle	Addr	2AA	555	2AA	555	2AA	555	2AA	555				
	Data	55	55	55	55	55	55	55	55				
3rd Bus Cycle	Addr	555	AAA	555	AAA	555	AAA	555	AAA				
	Data	90	90	A0	A0	80	80	80	80				
4th Bus Cycle	Addr	XXX	XXX	Addr	Addr	555	AAA	555	AAA				
	Data	00	00	Data	Data	AA	AA	AA	AA				
5th Bus Cycle	Addr					2AA	555	2AA	555				
	Data					55	55	55	55				
6th Bus Cycle	Addr					555	AAA	Sector	Sector				
	Data					10	10	30	30				

RESET

In the following situations, executing reset command will reset device back to read array mode:

- Among erase command sequence (before the full command set is completed)
- Sector erase time-out period
- Erase fail (while Q5 is high)
- Among program command sequence (before the full command set is completed, erase-suspended program included)
- Program fail (while Q5 is high, and erase-suspended program fail is included)
- Read silicon ID mode
- Sector protect verify
- CFI mode

While device is at the status of program fail or erase fail (Q5 is high), user must issue reset command to reset device back to read array mode. While the device is in read silicon ID mode, sector protect verify or CFI mode, user must issue reset command to reset device back to read array mode.

When the device is in the progress of programming (not program fail) or erasing (not erase fail), device will ignore reset command.

AUTOMATIC SELECT COMMAND SEQUENCE

Automatic Select mode is used to access the manufacturer ID, device ID and to verify whether or not secured silicon is locked and whether or not a sector is protected. The automatic select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The reset command is necessary to exit the Automatic Select mode and back to read array. The following table shows the identification code with corresponding address.

		Address	Data (Hex)	Representation
Manufacturer ID	Word	X00	C2	
	Byte	X00	C2	
Device ID	Word	X01	22C9/22CB	Top/Bottom Boot Sector
	Byte	X02	C9/CB	Top/Bottom Boot Sector
Secured Silicon	Word	X03	88/08	Factory locked/unlocked
	Byte	X06	88/08	Factory locked/unlocked
Sector Protect Verify	Word	(Sector address) X 02	00/01	Unprotected/protected
	Byte	(Sector address) X 04	00/01	Unprotected/protected

There is an alternative method to that shown in Table 2, which is intended for EPROM programmers and requires Vhv on address bit A9.

AUTOMATIC PROGRAMMING

The MX29LV640D T/B can provide the user program function by the form of Byte-Mode or Word-Mode. As long as the users enter the right cycle defined in the Table.3 (including 2 unlock cycles and A0H), any data user inputs will automatically be programmed into the array.

Once the program function is executed, the internal write state controller will automatically execute the algorithms and timings necessary for program and verification, which includes generating suitable program pulse, verifying whether the threshold voltage of the programmed cell is high enough and repeating the program pulse if any of the cells does not pass verification. Meanwhile, the internal control will prohibit the programming to cells that pass verification while the other cells fail in verification in order to avoid over-programming. With the internal write state controller, the device requires the user to write the program command and data only.

Programming will only change the bit status from "1" to "0". That is to say, it is impossible to convert the bit status from "0" to "1" by programming. Meanwhile, the internal write verification only detects the errors of the "1" that is not successfully programmed to "0".

Any command written to the device during programming will be ignored except hardware reset, which will terminate the program operation after a period of time no more than Tready. When the embedded program algorithm is complete or the program operation is terminated by hardware reset, the device will return to the reading array data mode.

The typical chip program time at room temperature of the MX29LV640D T/B is less than 45 seconds.

When the embedded program operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	RY/BY#*2
In progress*1	Q7#	togging	0	0
Finished	Q7	Stop toggling	0	1
Exceed time limit	Q7#	Toggling	1	0

*1: The status "in progress" means both program mode and erase-suspended program mode.
*2: RY/BY# is an open drain output pin and should be weakly connected to VDD through a pull-up resistor.
*3: When an attempt is made to program a protected sector, Q7 will output its complement data or Q6 continues to toggle for about 1us or less and the device returns to read array state without programing the data in the protected sector.

CHIP ERASE

Chip Erase is to erase all the data with "1" and "0" as all "1". It needs 6 cycles to write the action in, and the first two cycles are "unlock" cycles, the third one is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle is the chip erase operation.

During chip erasing, all the commands will not be accepted except hardware reset or the working voltage is too low that chip erase will be interrupted. After Chip Erase, the chip will return to the state of Read Array.

When the embedded chip erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q2	RY/BY#
In progress	0	Togging	0	Toggling	0
Finished	1	Stop toggling	0	1	1
Exceed time limit	0	Toggling	1	Toggling	0

SECTOR ERASE

Sector Erase is to erase all the data in a sector with "1" and "0" as all "1". It requires six command cycles to issue. The first two cycles are "unlock cycles", the third one is a configuration cycle, the fourth and fifth are also "unlock cycles" and the sixth cycle is the sector erase command. After the sector erase command sequence is issued, there is a time-out period of 50us counted internally. During the time-out period, additional sector address and sector erase command can be written multiply. Once user enters another sector erase command, the time-out period of 50us is recounted. If user enters any command other than sector erase or erase suspend during time-out period, the erase command would be aborted and the device is reset to read array condition. The number of sectors could be from one sector to all sectors. After time-out period passing by, additional erase command is not accepted and erase embedded operation begins.

During sector erasing, all commands will not be accepted except hardware reset and erase suspend and user can check the status as chip erase.

When the embedded erase operation is on going, user can confirm if the embedded operation is finished or not by the following methods:

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#*2
Time-out period	0	Togging	0	0	Toggling	0
In progress	0	Togging	0	1	Toggling	0
Finished	1	Stop toggling	0	1	1	1
Exceed time limit	0	Toggling	1	1	Toggling	0

Note :

1. The status Q3 is the time-out period indicator. When Q3=0, the device is in time-out period and is acceptible to another sector address to be erased. When Q3=1, the device is in erase operation and only erase suspend is valid.

2. RY/BY# is open drain output pin and should be weakly connected to VDD through a pull-up resistor.
3. When an attempt is made to erase a protected sector, Q7 will output its complement data or Q6 continues to toggle for 100us or less and the device returned to read array status without erasing the data in the protected sector.
4. Q2 is a localized indicator showing a specified sector is undergoing erase operation or not. Q2 toggles when user reads at addresses where the sectors are actively being erased (in erase mode) or to be erased (in erase suspend mode). When a sector has been completely erased, Q2 stops toggling at the sector even when the device is still in erase operation for remaining selected sectors. At that circumstance, Q2 will still toggle when device is read at any other sector that remains to be erased.

SECTOR ERASE SUSPEND

During sector erasure, sector erase suspend is the only valid command. If user issue erase suspend command in the time-out period of sector erasure, device time-out period will be over immediately and the device will go back to erase-suspended read array mode. If user issue erase suspend command during the sector erase is being operated, device will suspend the ongoing erase operation, and after the Tready1 (<=20us) suspend finishes and the device will enter erase-suspended read array mode. User can judge if the device has finished erase suspend through Q6, Q7, and RY/BY#.

After device has entered erase-suspended read array mode, user can read other sectors not at erase suspend by the speed of Taa; while reading the sector in erase-suspend mode, device will output its status. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another erase command. The system can use the status register bits shown in the following table to determine the current state of the device:

Status	Q7	Q6	Q5	Q3	Q2	RY/BY#
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	toggle	1
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	1
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A	0

When the device has suspended erasing, user can execute the command sets except sector erase and chip erase, such as read silicon ID, sector protect verify, program, CFI query and erase resume.

SECTOR ERASE RESUME

Sector erase resume command is valid only when the device is in erase suspend state. After erase resume, user can issue another erase suspend command, but there should be a 4ms interval between erase resume and the next erase suspend. If user issue infinite suspend-resume loop, or suspend-resume exceeds 1024 times, the time for erasing will increase.

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LV640D T/B features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. The device enters the CFI Query mode when the system writes the CFI Query command, 98H, to address 55H/AAH (depending on Word/Byte mode) any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 4. A reset command is required to exit CFI mode and go back to ready array mode or erase suspend mode. The system can write the CFI Query command only when the device is in read mode, erase suspend, standby mode or automatic select mode. The CFI unused area is Macronix's reserved.

Table 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address (h) (Word Mode)	Address (h) (Byte Mode)	Data (h)
Query-unique ASCII string "QRY"	10	20	0051
	11	22	0052
	12	24	0059
Primary vendor command set and control interface ID code	13	26	0002
	14	28	0000
Address for primary algorithm extended query table	15	2A	0040
	16	2C	0000
Alternate vendor command set and control interface ID code	17	2E	0000
	18	30	0000
Address for alternate algorithm extended query table	19	32	0000
	1A	34	0000

Table 4-2. CFI Mode: System Interface Data Values

Description	Address (h) (Word Mode)	Address (h) (Byte Mode)	Data (h)
Vcc supply minimum program/erase voltage	1B	36	0027
Vcc supply maximum program/erase voltage	1C	38	0036
VPP supply minimum program/erase voltage	1D	3A	0000
VPP supply maximum program/erase voltage	1E	3C	0000
Typical timeout per single word/byte write, 2^n us	1F	3E	0004
Typical timeout for maximum-size buffer write, 2^n us	20	40	0000
Typical timeout per individual block erase, 2^n ms	21	42	000A
Typical timeout for full chip erase, 2^n ms	22	44	0000
Maximum timeout for word/byte write, 2^n times typical	23	46	0005
Maximum timeout for buffer write, 2^n times typical	24	48	0000
Maximum timeout per individual block erase, 2^n times typical	25	4A	0004
Maximum timeout for chip erase, 2^n times typical	26	4C	0000

Table 4-3. CFI Mode: Device Geometry Data Values

Description	Address (h) (Word Mode)	Address (h) (Byte Mode)	Data (h)
Device size = 2^n in number of bytes	27	4E	0017
Flash device interface description (02=asynchronous x8/x16)	28	50	0002
	29	52	0000
Maximum number of bytes in buffer write = 2^n (not support)	2A	54	0000
	2B	56	0000
Number of erase regions within device Index for Erase Bank Area 1 [2E,2D] = # of same-size sectors in region 1-1 [30, 2F] = sector size in multiples of 256-bytes	2C	58	0002
	2D	5A	0007
	2E	5C	0000
	2F	5E	0020
	30	60	0000
Index for Erase Bank Area 2	31	62	007E
	32	64	0000
	33	66	0000
	34	68	0001
Index for Erase Bank Area 3	35	6A	0000
	36	6C	0000
	37	6E	0000
	38	70	0000
Index for Erase Bank Area 4	39	72	0000
	3A	74	0000
	3B	76	0000
	3C	78	0000

Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h) (Word Mode)	Address (h) (Byte Mode)	Data (h)
Query - Primary extended table, unique ASCII string, PRI	40	80	0050
	41	82	0052
	42	84	0049
Major version number, ASCII	43	86	0031
Minor version number, ASCII	44	88	0031
Unlock recognizes address (0= recognize, 1= don't recognize)	45	8A	0000
Erase suspend (2= to both read and program)	46	8C	0002
Sector protect (N= # of sectors/group)	47	8E	0004
Temporary sector unprotect (1=supported)	48	90	0001
Sector protect/Chip unprotect scheme	49	92	0004
Simultaneous R/W operation (0=not supported)	4A	94	0000
Burst mode (0=not supported)	4B	96	0000
Page mode (0=not supported)	4C	98	0000
Minimum ACC (acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4D	9A	00B5
Maximum ACC (acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4E	9C	00C5
Top/Bottom boot block indicator 02h=bottom boot device 03h=top boot device	4F	9E	0002/0003

ABSOLUTE MAXIMUM STRESS RATINGS

Surrounding Temperature with Bias		-65°C to +125°C
Storage Temperature		-65°C to +150°C
Voltage Range	VCC	-0.5V to +4.0 V
	RESET#, A9 and OE#	-0.5V to +11.5 V
	The other pins	-0.5V to Vcc +0.5V
Output Short Circuit Current (less than one second)		200 mA

Note:
1. Minimum voltage may undershoot to -2V during transition and for less than 20ns during transitions.
2. Maximum voltage may overshoot to Vcc+2V during transition and for less than 20ns during transitions.

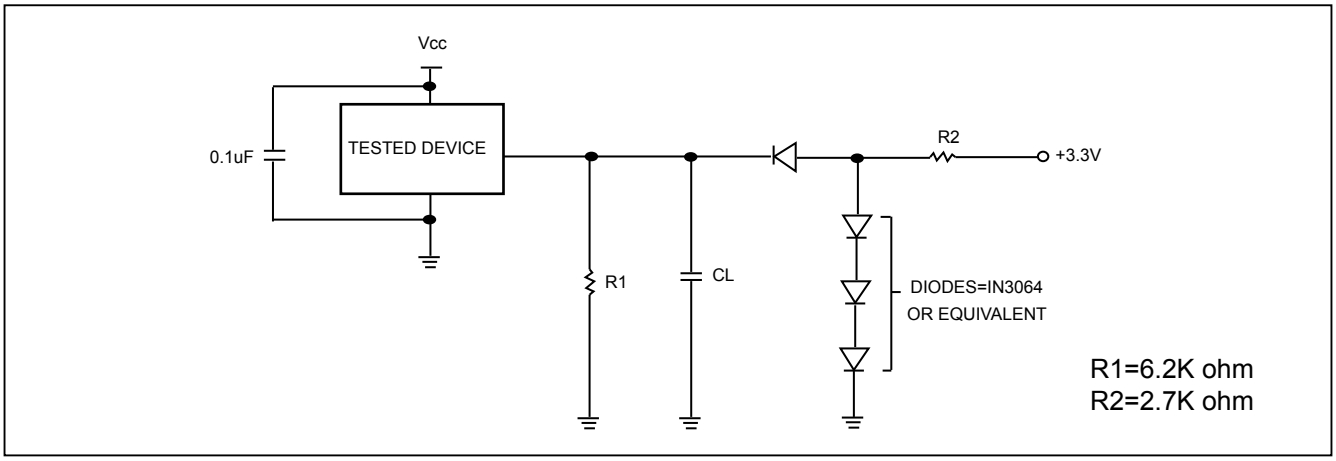
OPERATING TEMPERATURE AND VOLTAGE

Commercial (C) Grade	Surrounding Temperature (T_A)	0°C to +70°C
Industrial (I) Grade	Surrounding Temperature (T_A)	-40°C to +85°C
VCC Supply Voltages	VCC range	+2.7 V to 3.6 V

DC CHARACTERISTICS

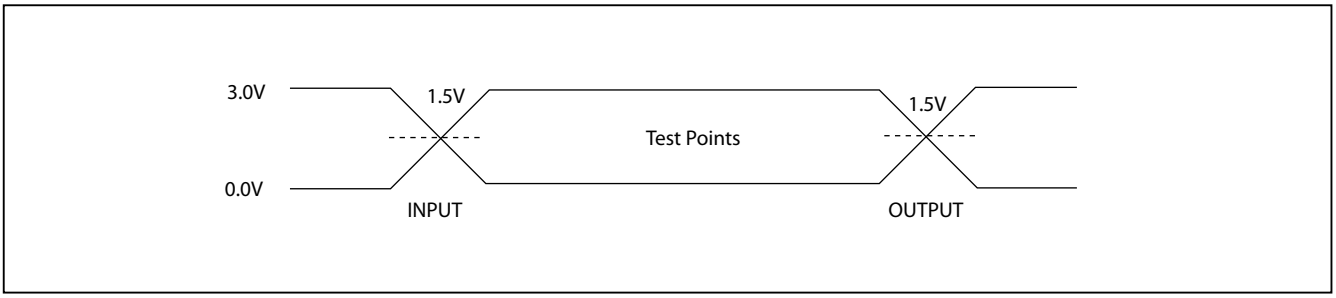
Symbol	Description	Min.	Typ.	Max.	Remark
Iilk	Input Leak			± 1.0uA	
Iilk9	A9 Leak			35uA	A9=10.5V
Iolk	Output Leak			± 1.0uA	
Icr1	Read Current(5MHz)		9mA	16mA	CE#=Vil, OE#=Vih
Icr2	Read Current(1MHz)		2mA	4mA	CE#=Vil, OE#=Vih
Icw	Write Current		26mA	30mA	CE#=Vil, OE#=Vih, WE#=Vil
Isb	Standby Current		5uA	15uA	Vcc=Vcc max, other pin disable
Isbr	Reset Current		5uA	15uA	Vcc=Vccmax, Reset# enable, other pin disable
Isbs	Sleep Mode Current		5uA	15uA	
Icp1	Accelerated Pgm Current, WP#/ACC pin (Word/Byte)		5mA	10mA	CE#=Vil, OE#=Vih,
Icp2	Accelerated Pgm Current, Vcc pin (Word/Byte)		15mA	30mA	CE#=Vil, OE#=Vih,
Vil	Input Low Voltage	-0.5V		0.8V	
Vih	Input High Voltage	0.7xVcc		Vcc+0.3V	
Vhv	Very High Voltage for hardware Protect/ Unprotect/Auto Select/Temporary Unprotect/Accelerated Program	9.5V		10.5V	
Vol	Output Low Voltage			0.45V	Iol=4.0mA
Voh1	Ouput High Voltage	0.85xVcc			Ioh1=-2mA
Voh2	Ouput High Voltage	Vcc-0.4V			Ioh2=-100uA
Vlko	Low Vcc Lock-out Voltage	2.3V		2.5V	

SWITCHING TEST CIRCUITS



Test Condition
Output Load : 1 TTL gate
Output Load Capacitance,CL : 30pF
Rise/Fall Times : 5ns
In/Out reference levels :1.5V

SWITCHING TEST WAVEFORMS

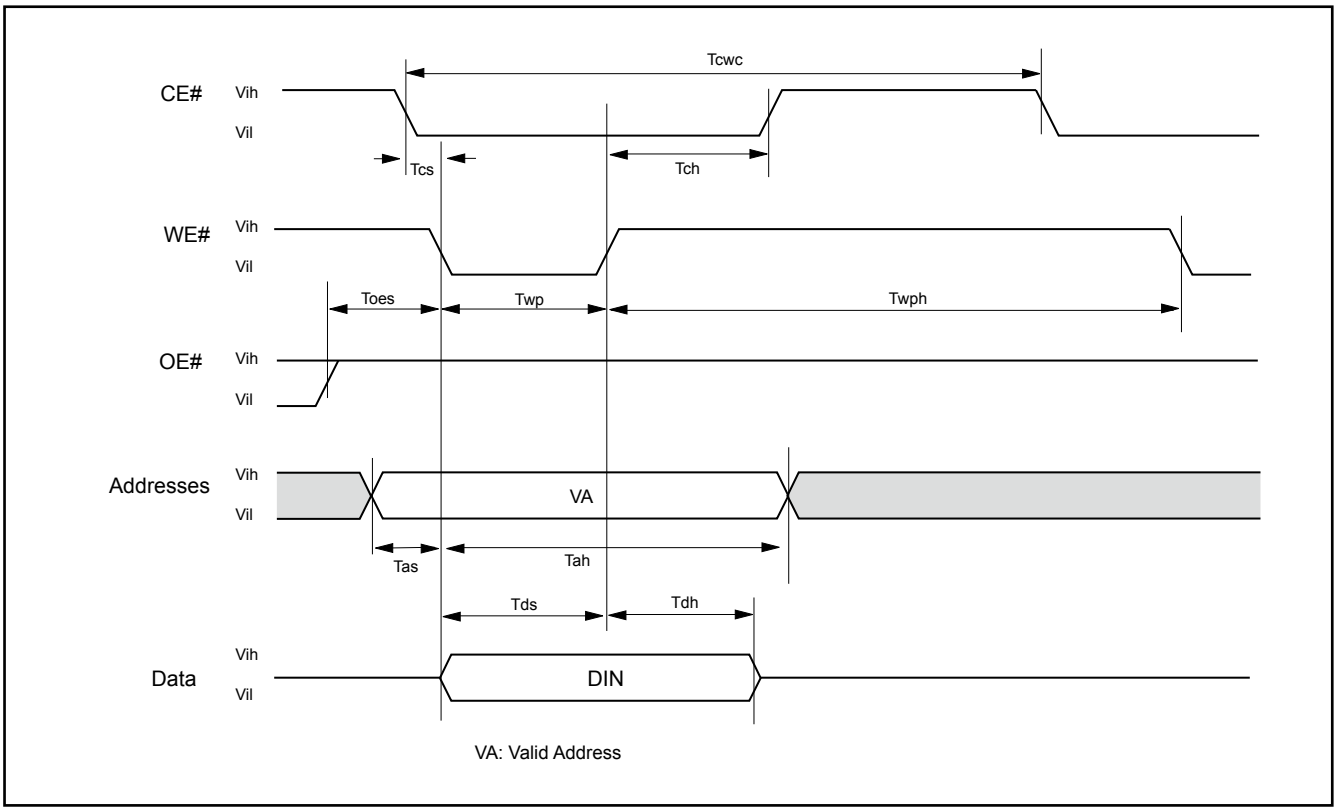


AC CHARACTERISTICS

Symbol	Description		Min.	Typ.	Max.	Unit
Taa	Valid data output after address				90	ns
Tce	Valid data output after CE# low				90	ns
Toe	Valid data output after OE# low				30	ns
Tdf	Data output floating after OE# high (*Note 1)				16	ns
Toh	Output hold time from the earliest rising edge of address, CE#, OE#		0			ns
Trc	Read period time		90			ns
Tsrw	Latency Between Read and Write operation (*Note 1)		45			ns
Twc	Write period time		90			ns
Tcwc	Command write period time		90			ns
Tas	Address setup time		0			ns
Tah	Address hold time		45			ns
Tds	Data setup time		45			ns
Tdh	Data hold time		0			ns
Tvcs	Vcc setup time		200			us
Tcs	Chip enable Setup time		0			ns
Tch	Chip enable hold time		0			ns
Toes	Output enable setup time		0			ns
Toeh	Output enable hold time	Read	0			ns
		Toggle & Data# Polling	10			ns
Tws	WE# setup time		0			ns
Twh	WE# hold time		0			ns
Tcep	CE# pulse width		45			ns
Tceph	CE# pulse width high		30			ns
Twp	WE# pulse width		35			ns
Twph	WE# pulse width high		30			ns
Tbusy	Program/Erase active time by RY/BY#				90	ns
Tghwl	Read recover time before write		0			ns
Tghel	Read recover time before write		0			ns
Twhwh1	Program operation	Byte		9		us
Twhwh1	Program operation	Word		11		us
Twhwh1	Acc Program operation(Word/Byte)			7		us
Twhwh2	Sector Erase Operation			0.7		sec
Tbal	Sector Add hold time				50	us

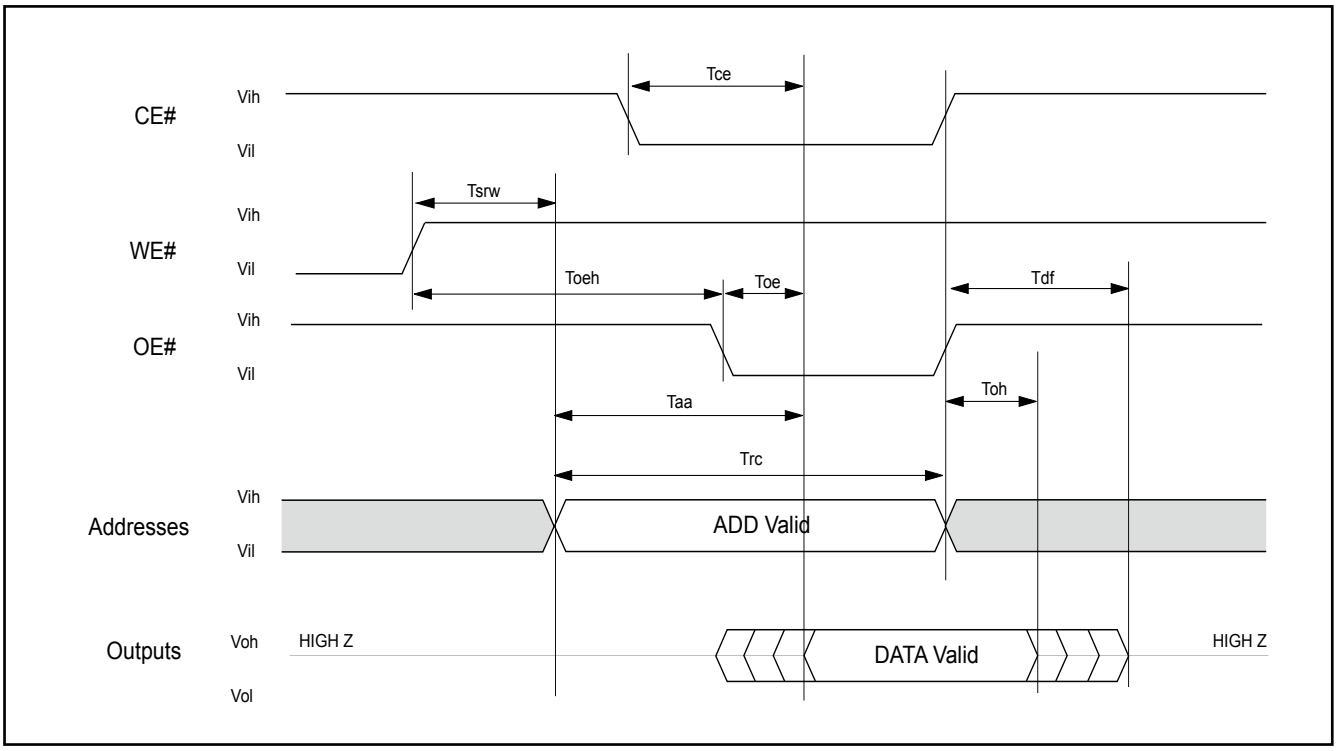
* Note 1: Sampled only, not 100% tested.

Figure 1. COMMAND WRITE OPERATION



READ/RESET OPERATION

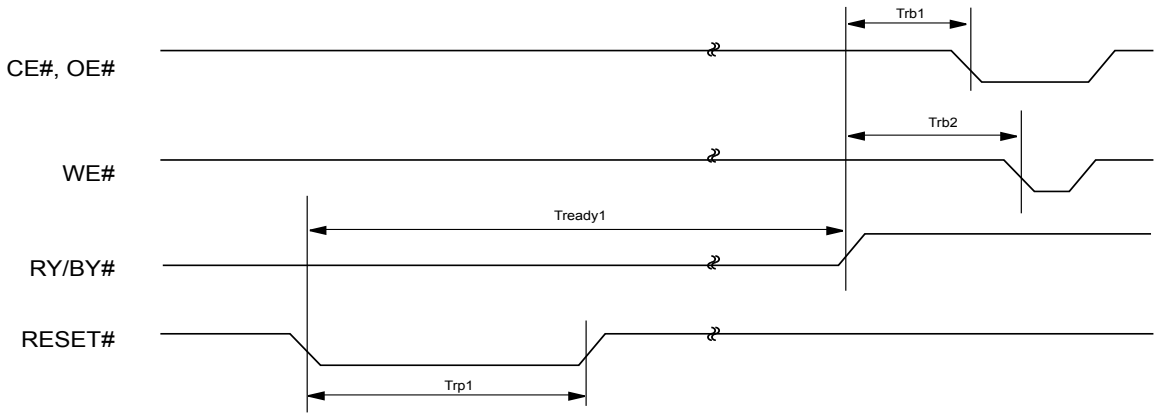
Figure 2. READ TIMING WAVEFORMS



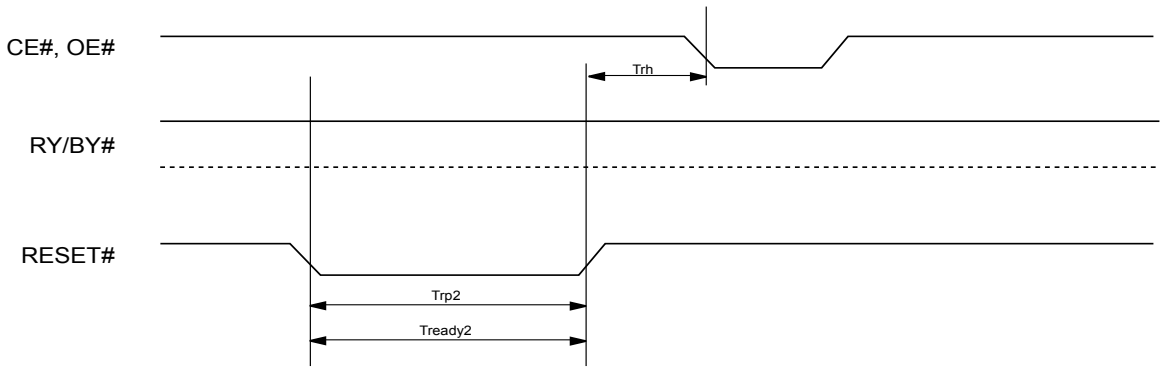
AC CHARACTERISTICS

Item	Description	Setup	Speed	Unit
Trp1	RESET# Pulse Width (During Automatic Algorithms)	MIN	10	us
Trp2	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
Trh	RESET# High Time Before Read	MIN	50	ns
Trb1	RY/BY# Recovery Time (to CE#, OE# go low)	MIN	0	ns
Trb2	RY/BY# Recovery Time (to WE# go low)	MIN	50	ns
Tready1	RESET# PIN Low (During Automatic Algorithms) to Read or Write	MAX	20	us
Tready2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write	MAX	500	ns

Figure 3. RESET# TIMING WAVEFORM



Reset Timing during Automatic Algorithms



Reset Timing NOT during Automatic Algorithms

ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC CHIP ERASE TIMING WAVEFORM

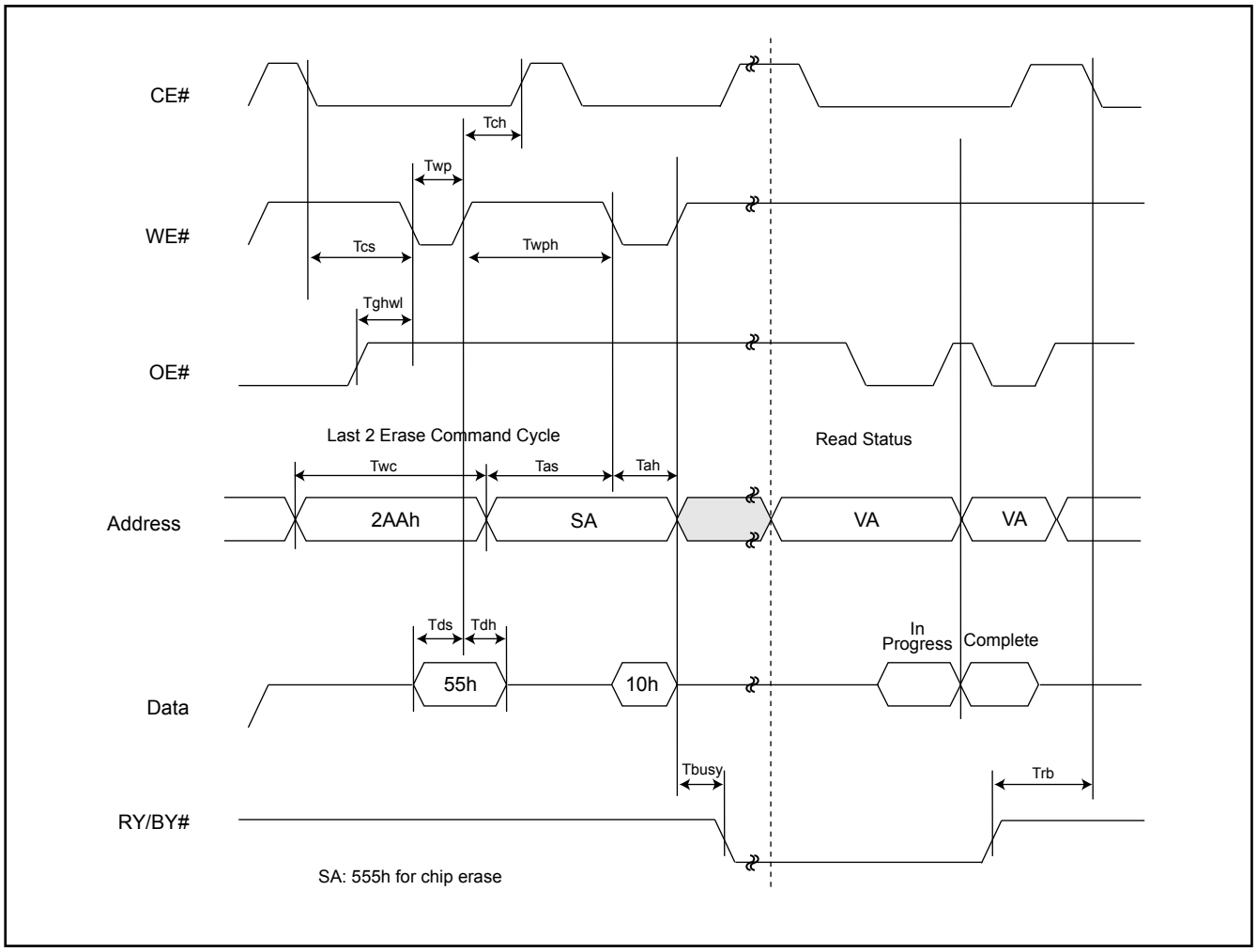


Figure 5. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

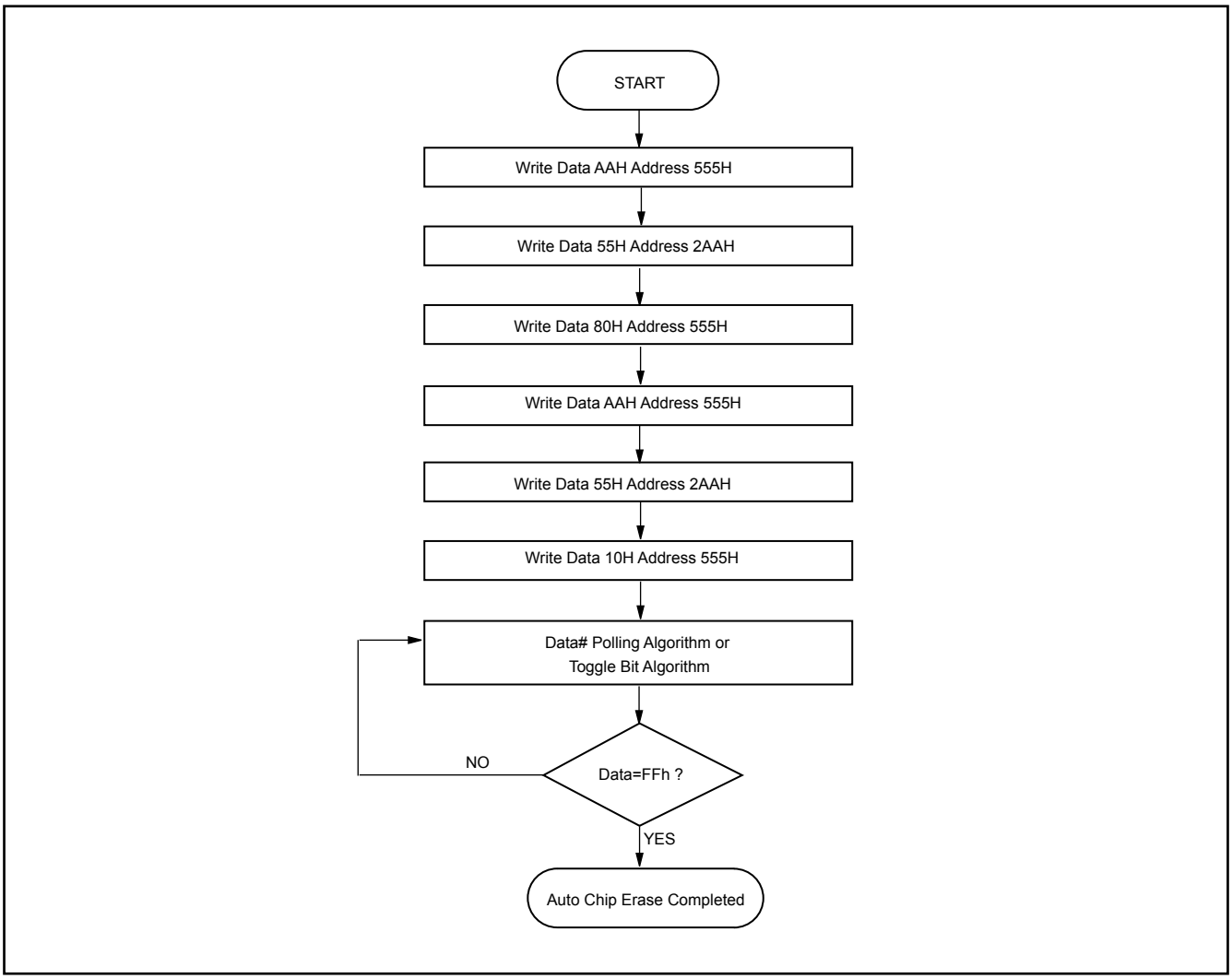


Figure 6. AUTOMATIC SECTOR ERASE TIMING WAVEFORM

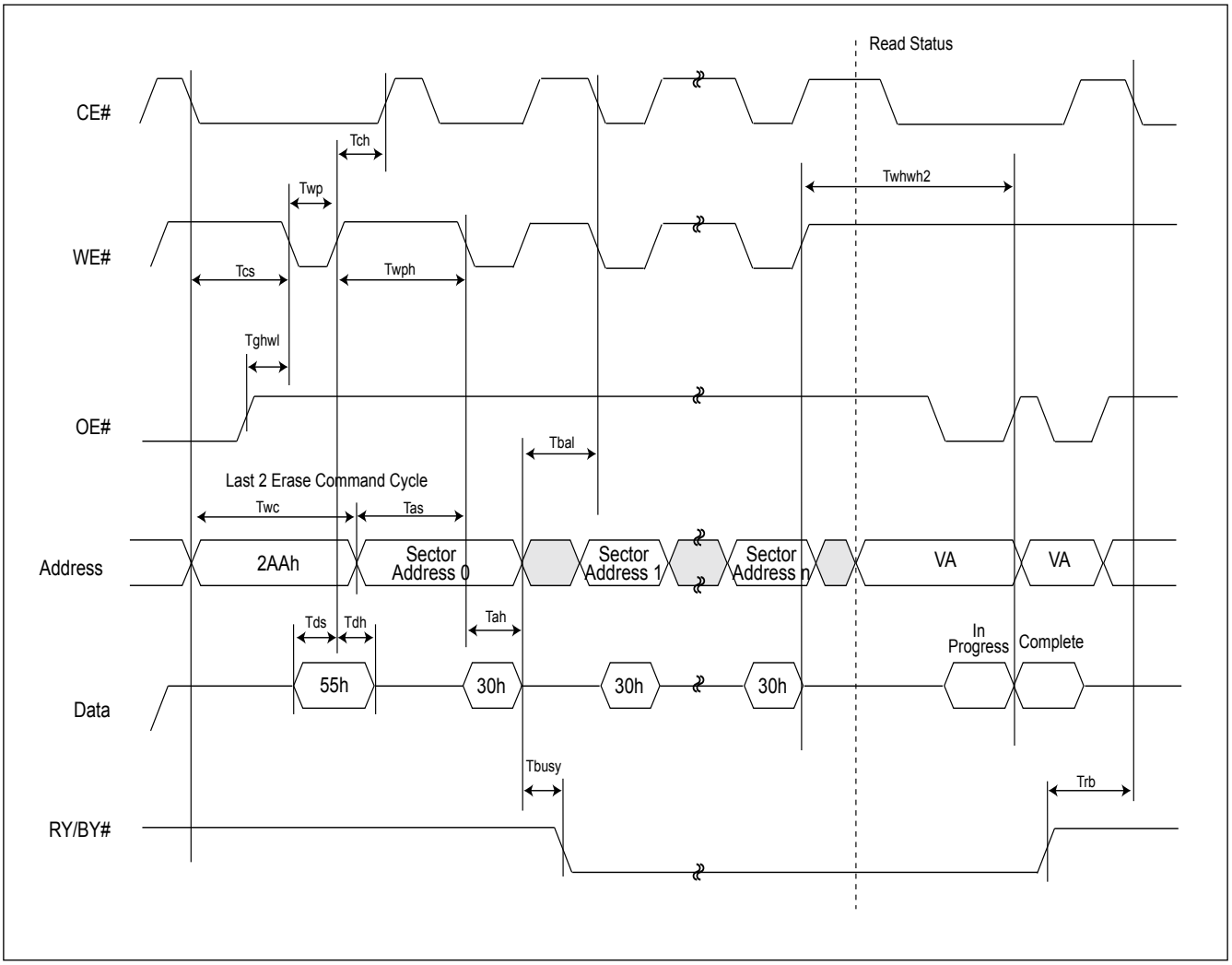


Figure 7. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

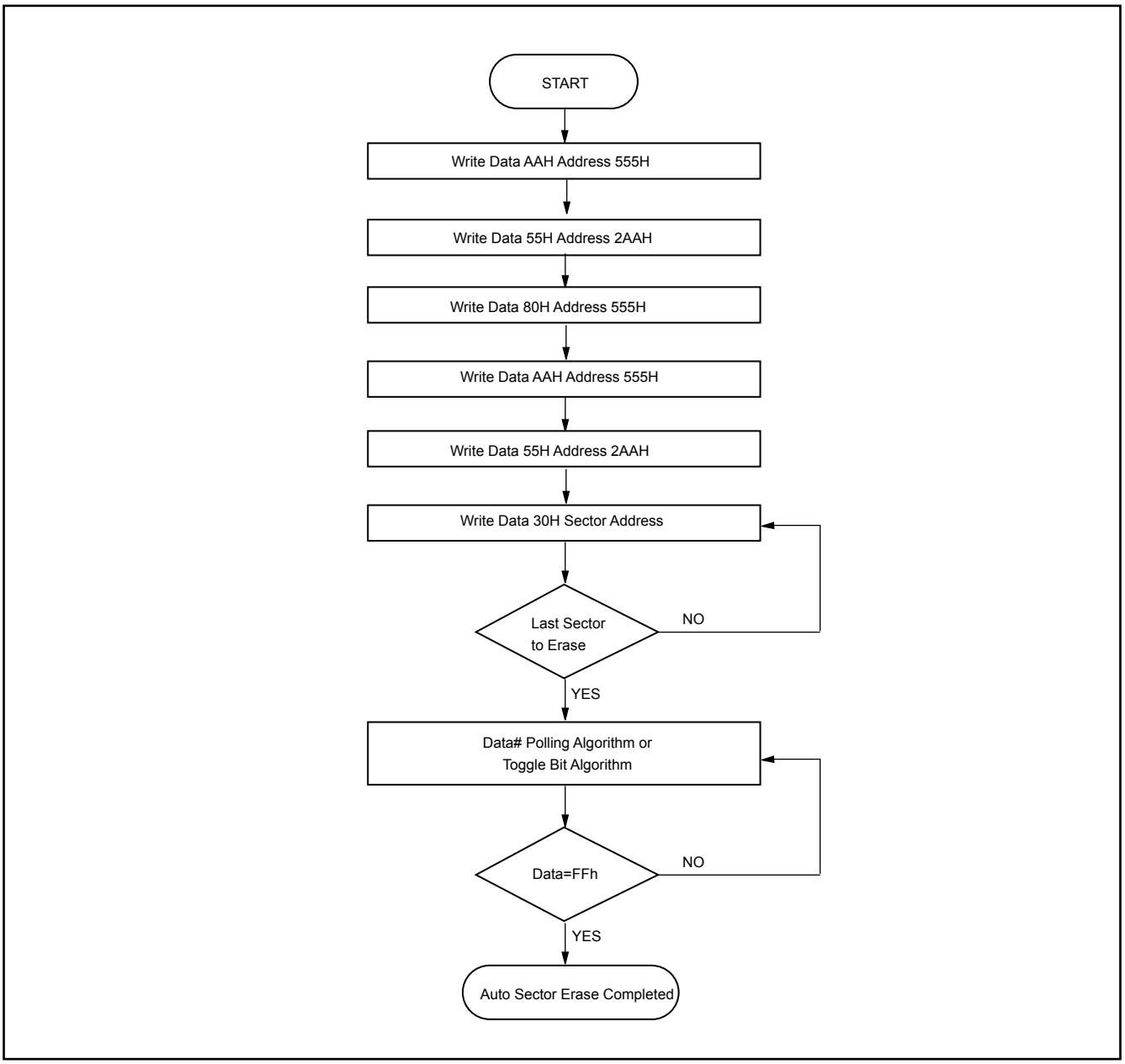


Figure 8. ERASE SUSPEND/RESUME FLOWCHART

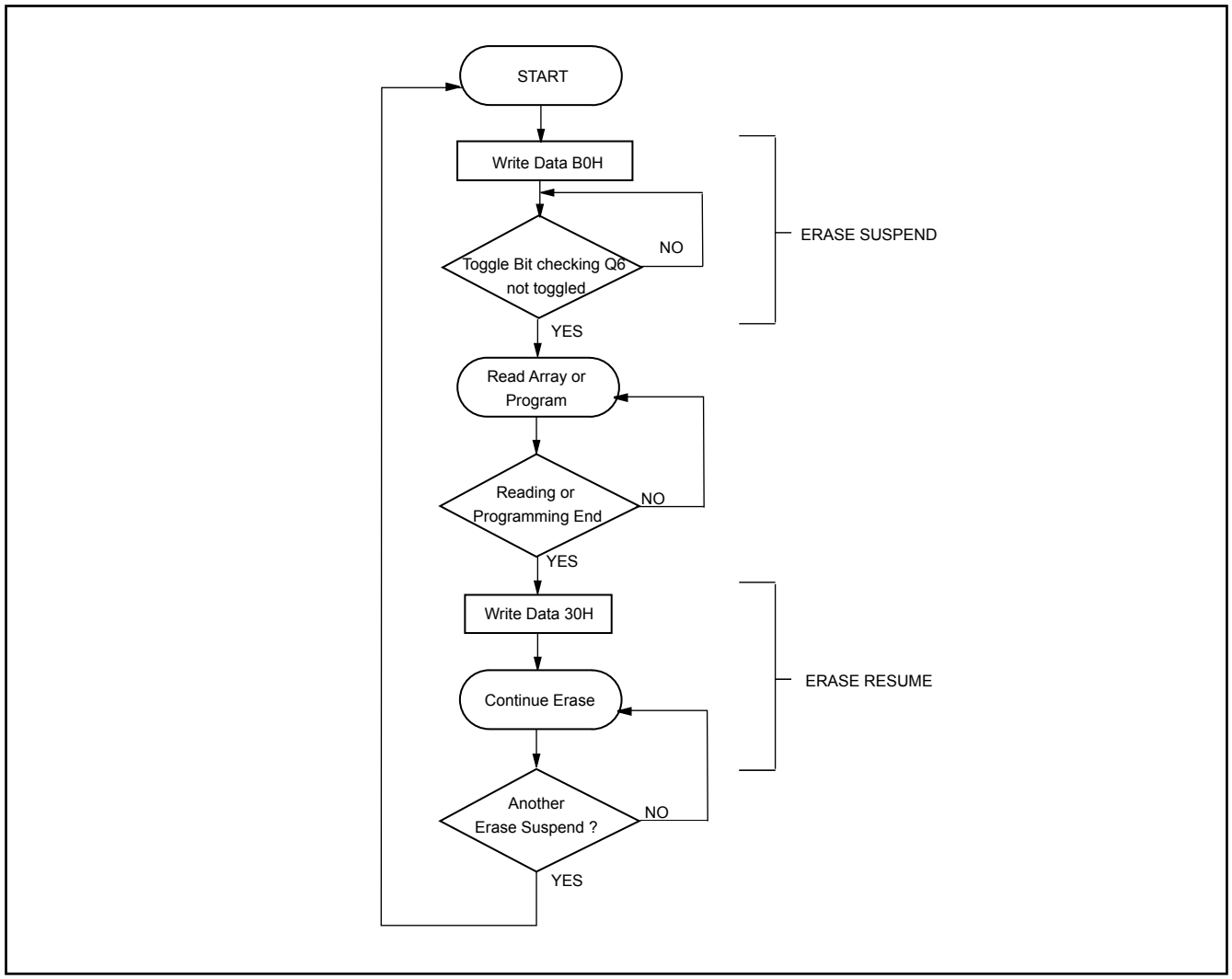


Figure 9. AUTOMATIC PROGRAM TIMING WAVEFORMS

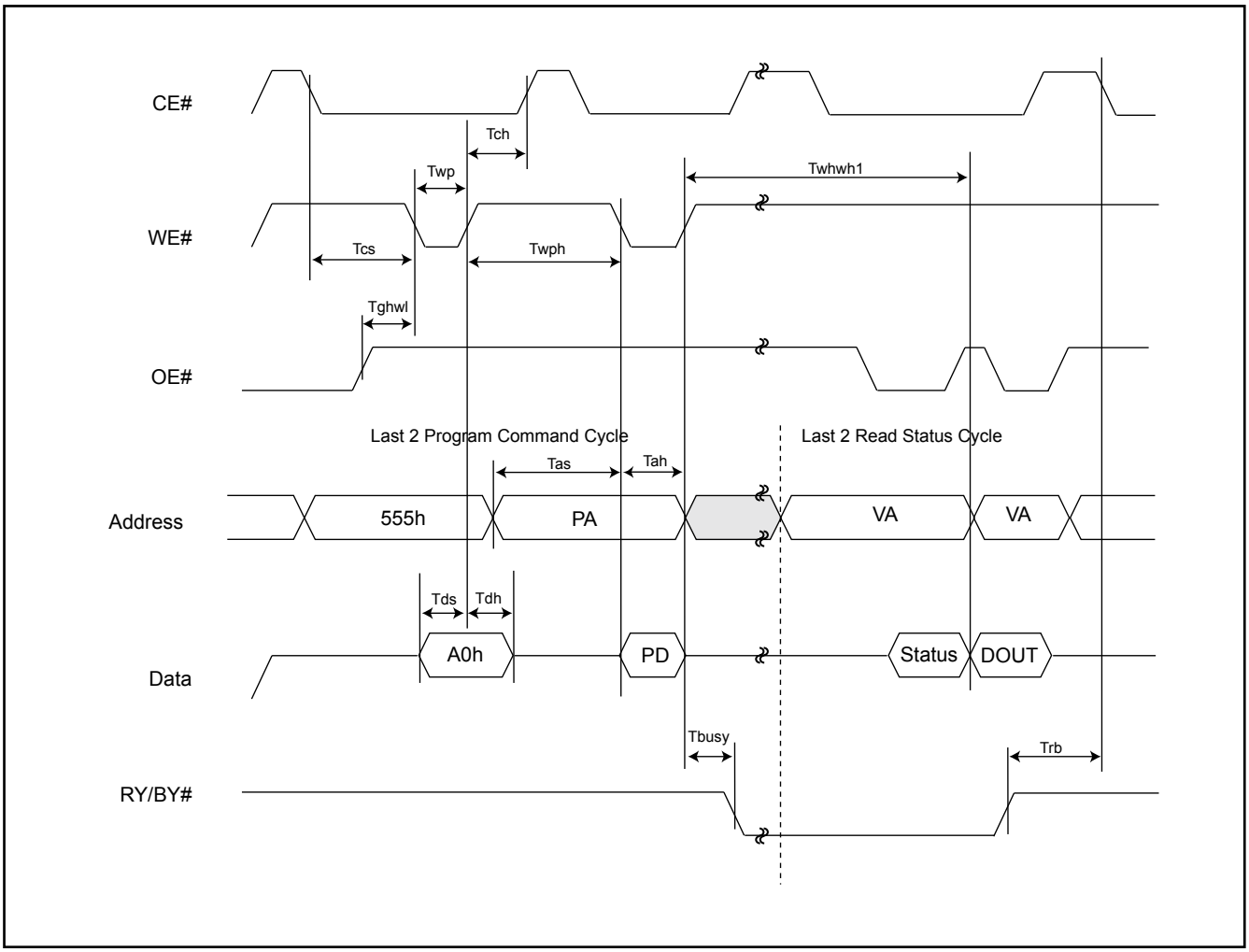


Figure 10. Accelerated Program Timing Diagram

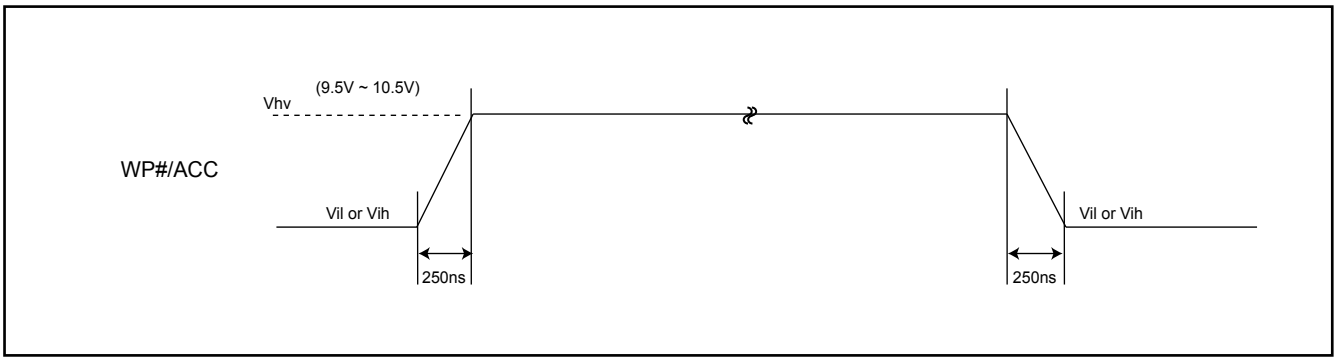


Figure 11. CE# CONTROLLED WRITE TIMING WAVEFORM

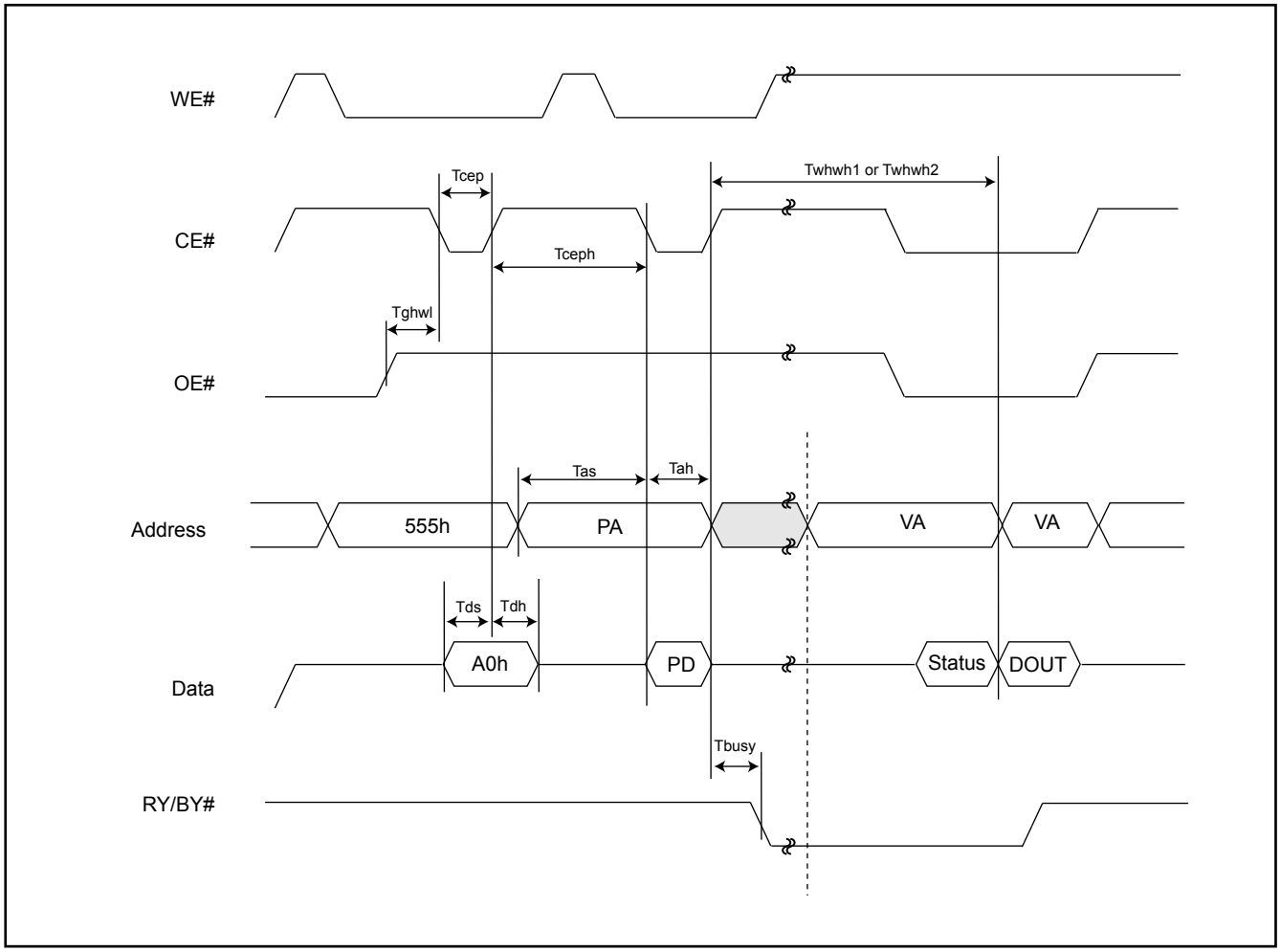
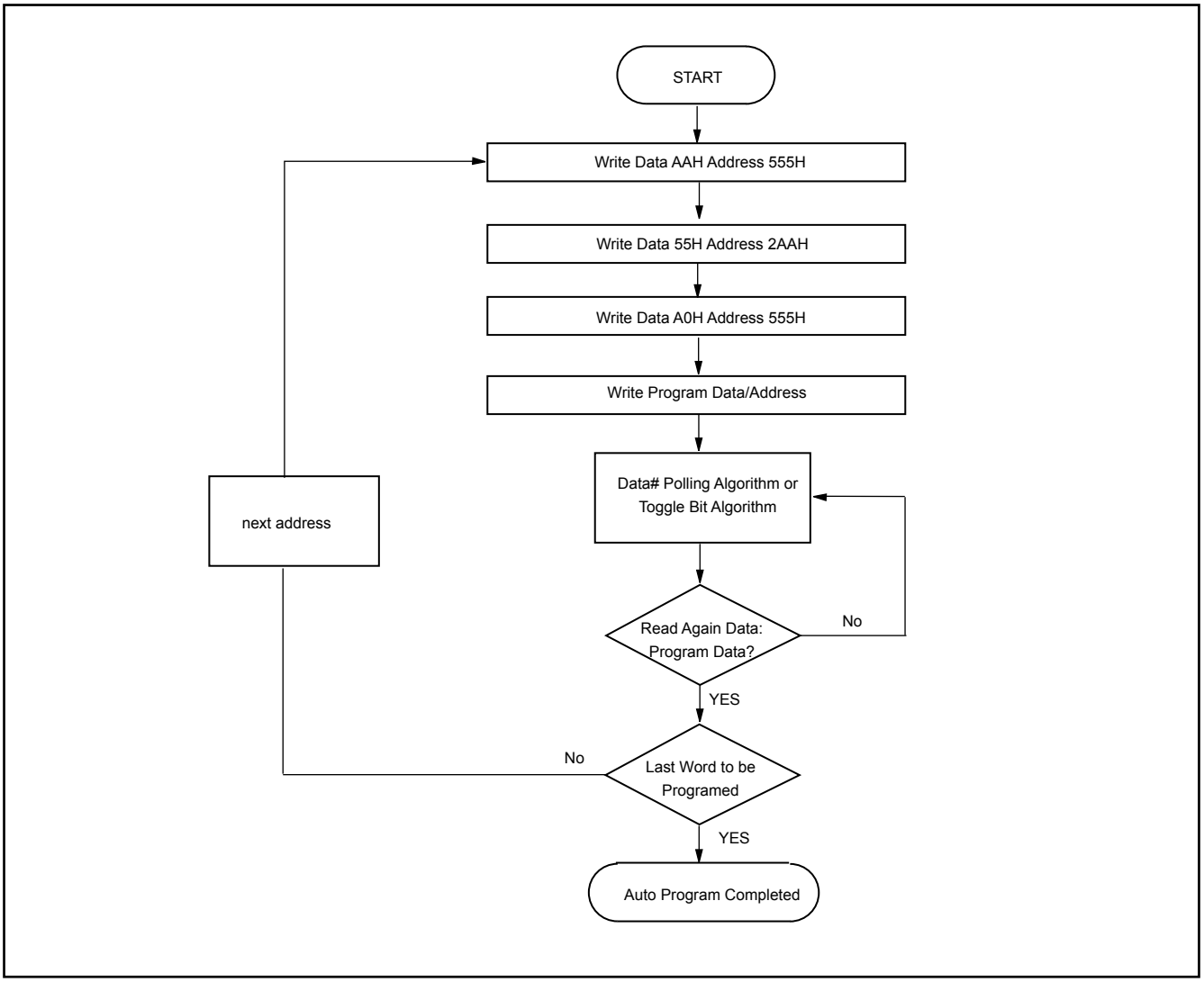


Figure 12. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



SECTOR GROUP PROTECT/CHIP UNPROTECT

Figure 13. SECTOR GROUP PROTECT/CHIP UNPROTECT WAVEFORM (RESET# Control)

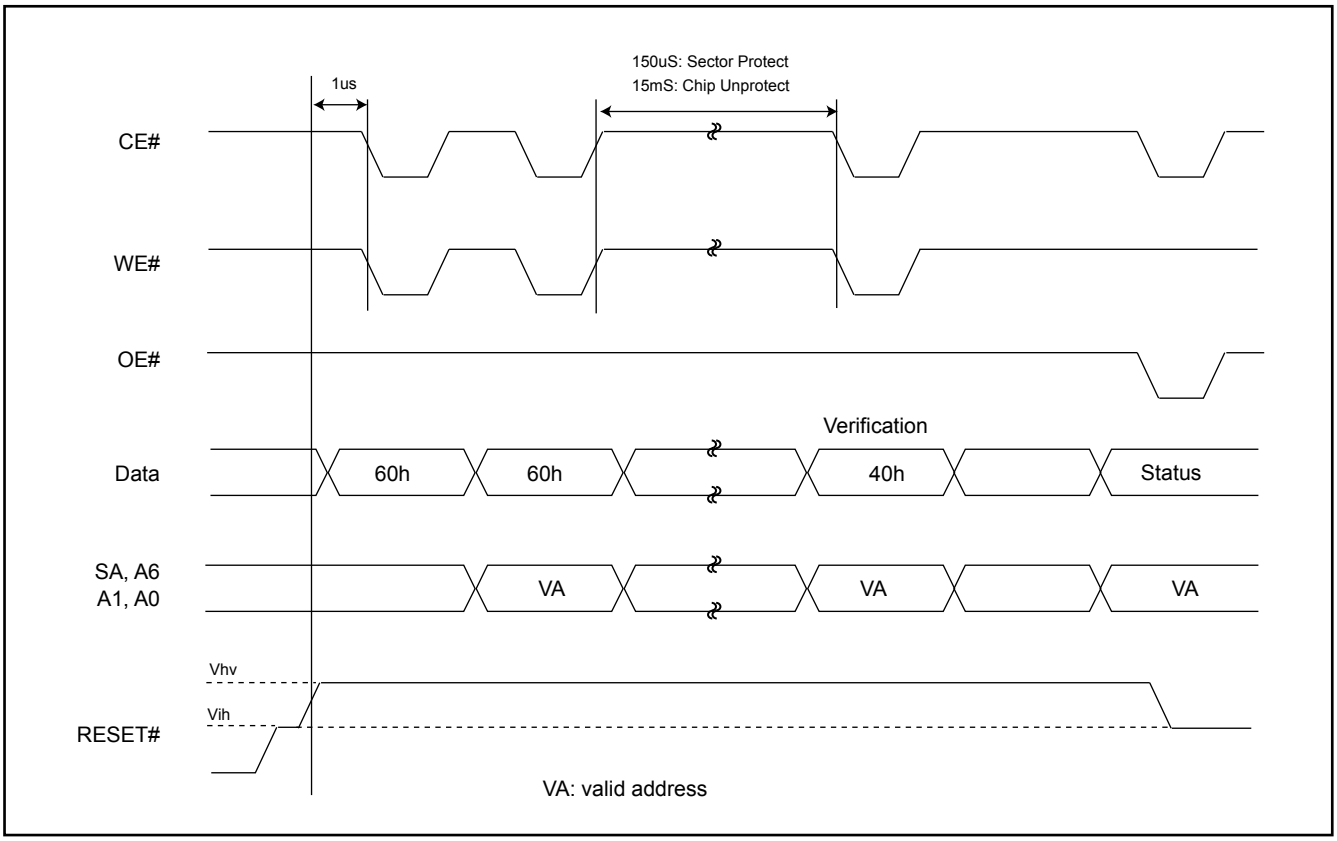


Figure 14-1. IN-SYSTEM SECTOR GROUP PROTECT WITH RESET#=Vhv

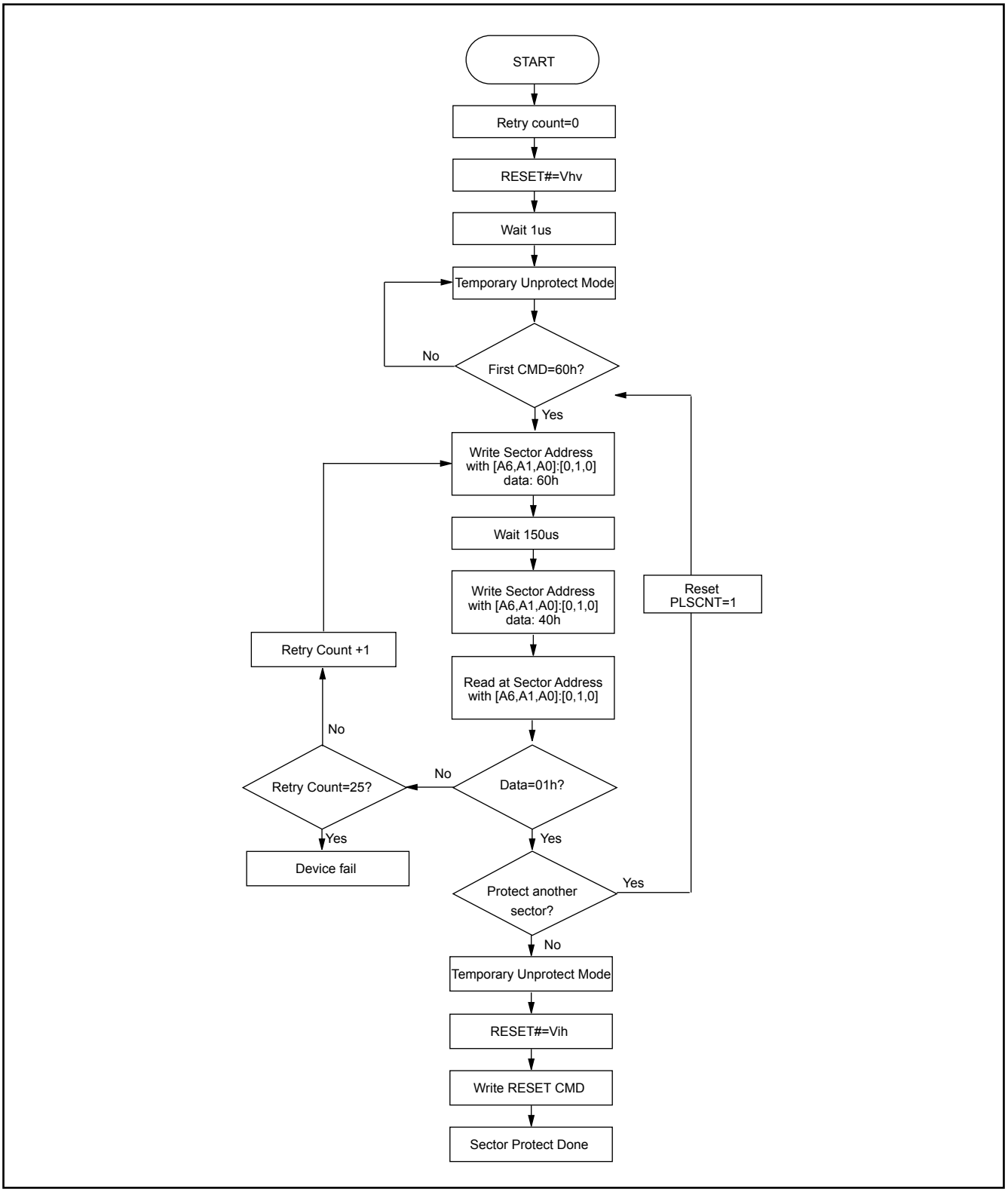


Figure 14-2. CHIP UNPROTECT ALGORITHMS WITH RESET#=Vhv

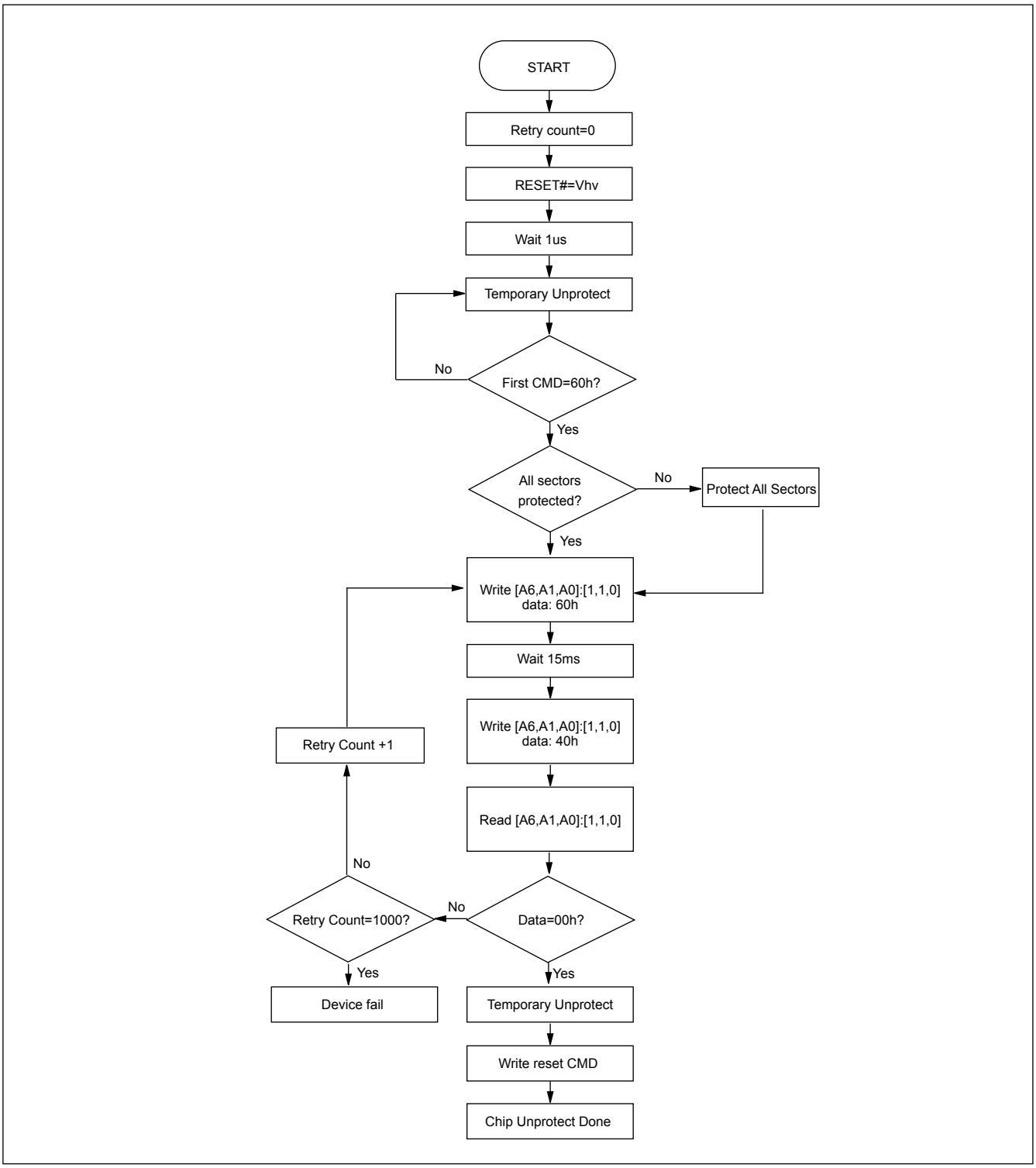


Table 5. TEMPORARY SECTOR GROUP UNPROTECT

Parameter	Alt	Description	Condition	Speed	Unit
Trpvhh	Tvidr	RESET# Rise Time to Vhv and Vhv Fall Time to RESET#	MIN	500	ns
Tvhhwl	Trsp	RESET# Vhv to WE# Low	MIN	4	us

Figure 15. TEMPORARY SECTOR GROUP UNPROTECT WAVEFORMS

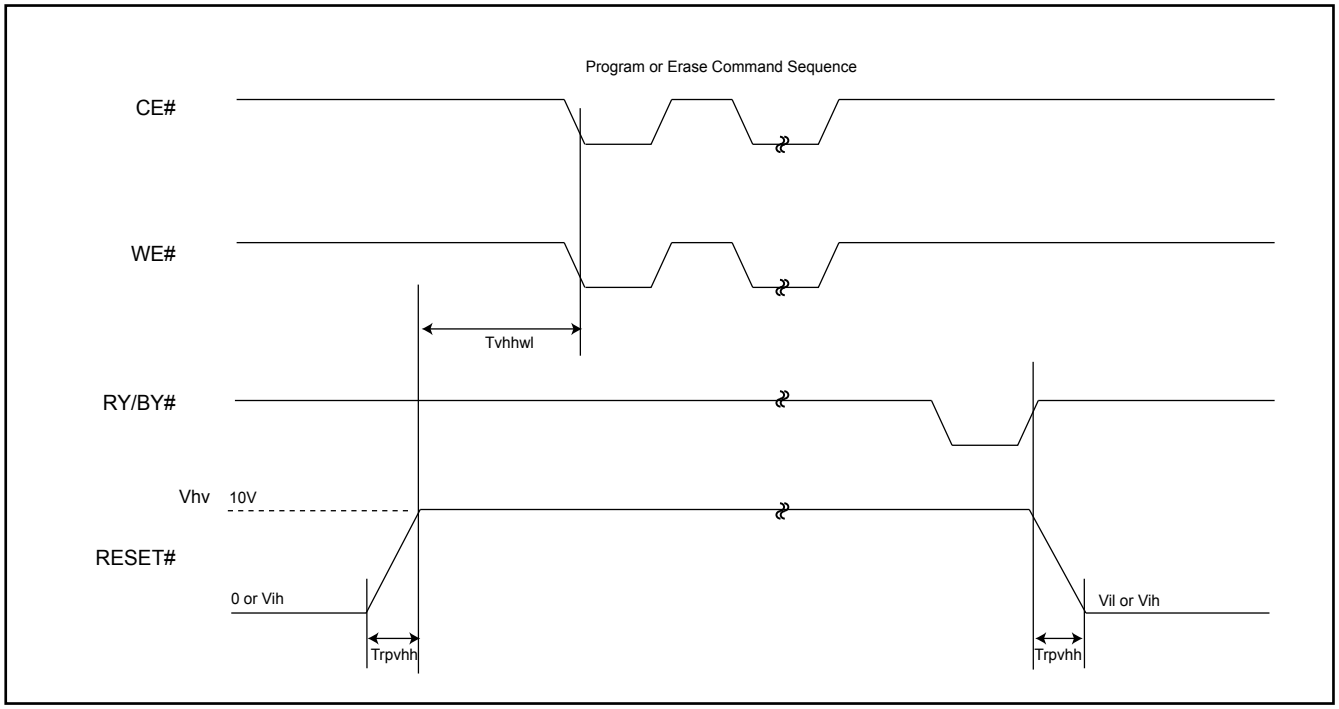
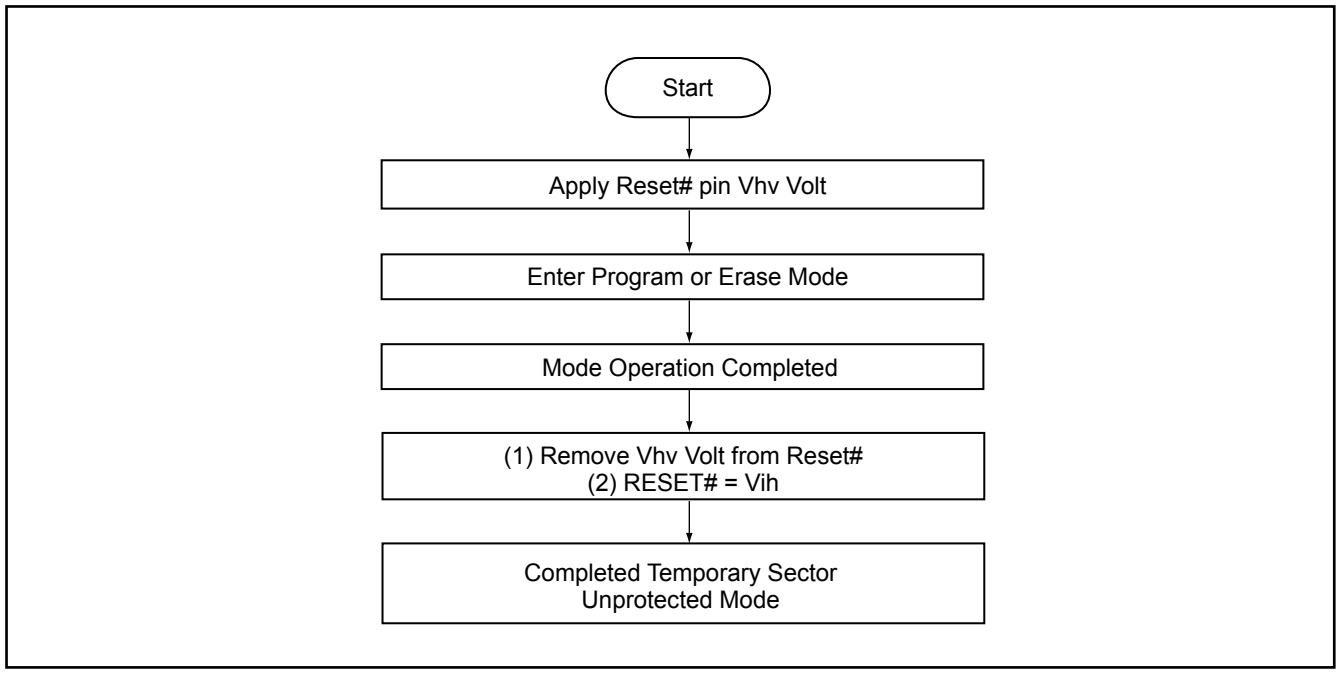
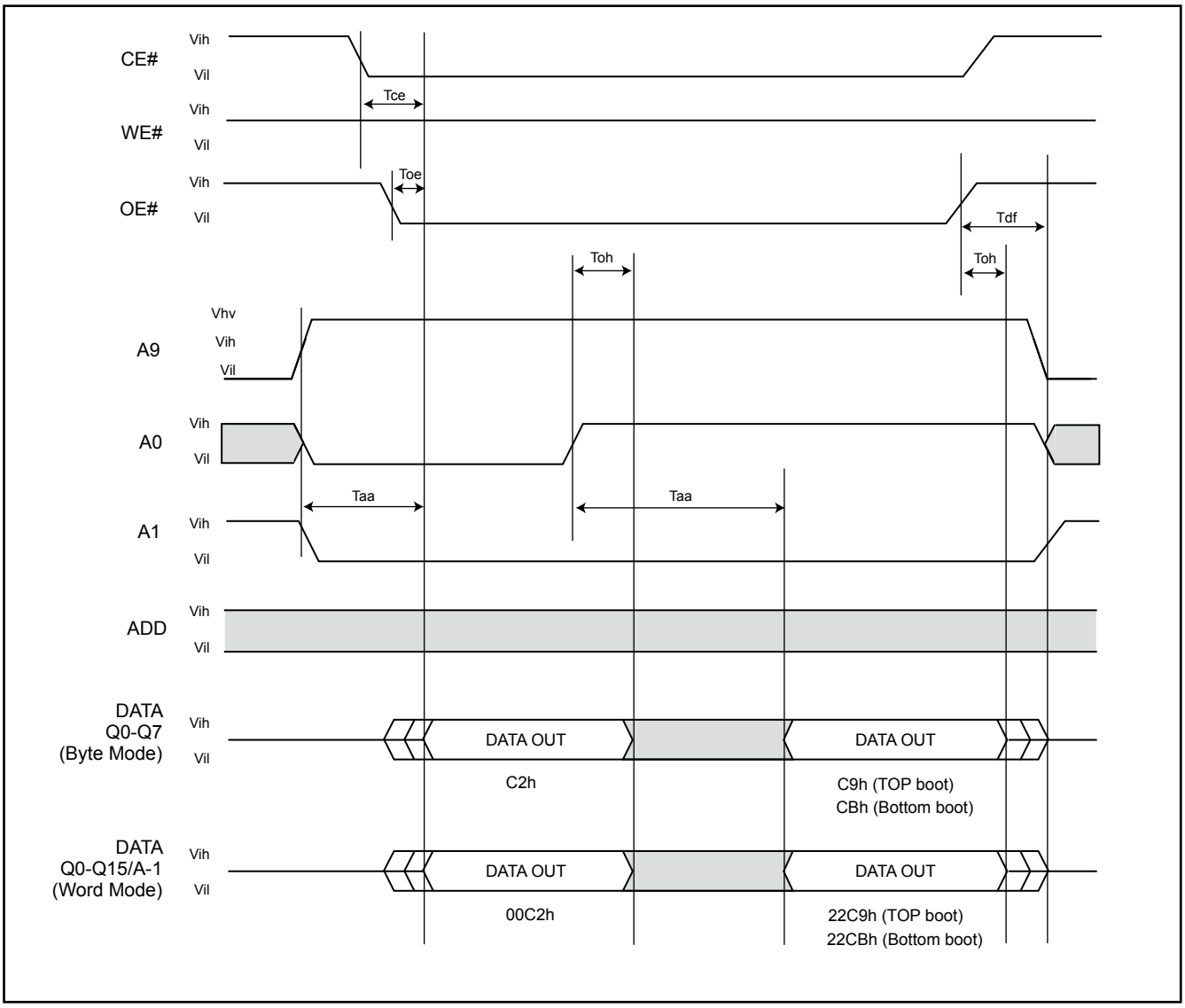


Figure 16. TEMPORARY SECTOR GROUP UNPROTECT FLOWCHART



Notes:
1. Temporary unprotect all protected sectors Vhv=9.5~10.5V.
2. After leaving temporary unprotect mode, the previously protected sectors are again protected.

Figure 17. SILICON ID READ TIMING WAVEFORM



WRITE OPERATION STATUS

Figure 18. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

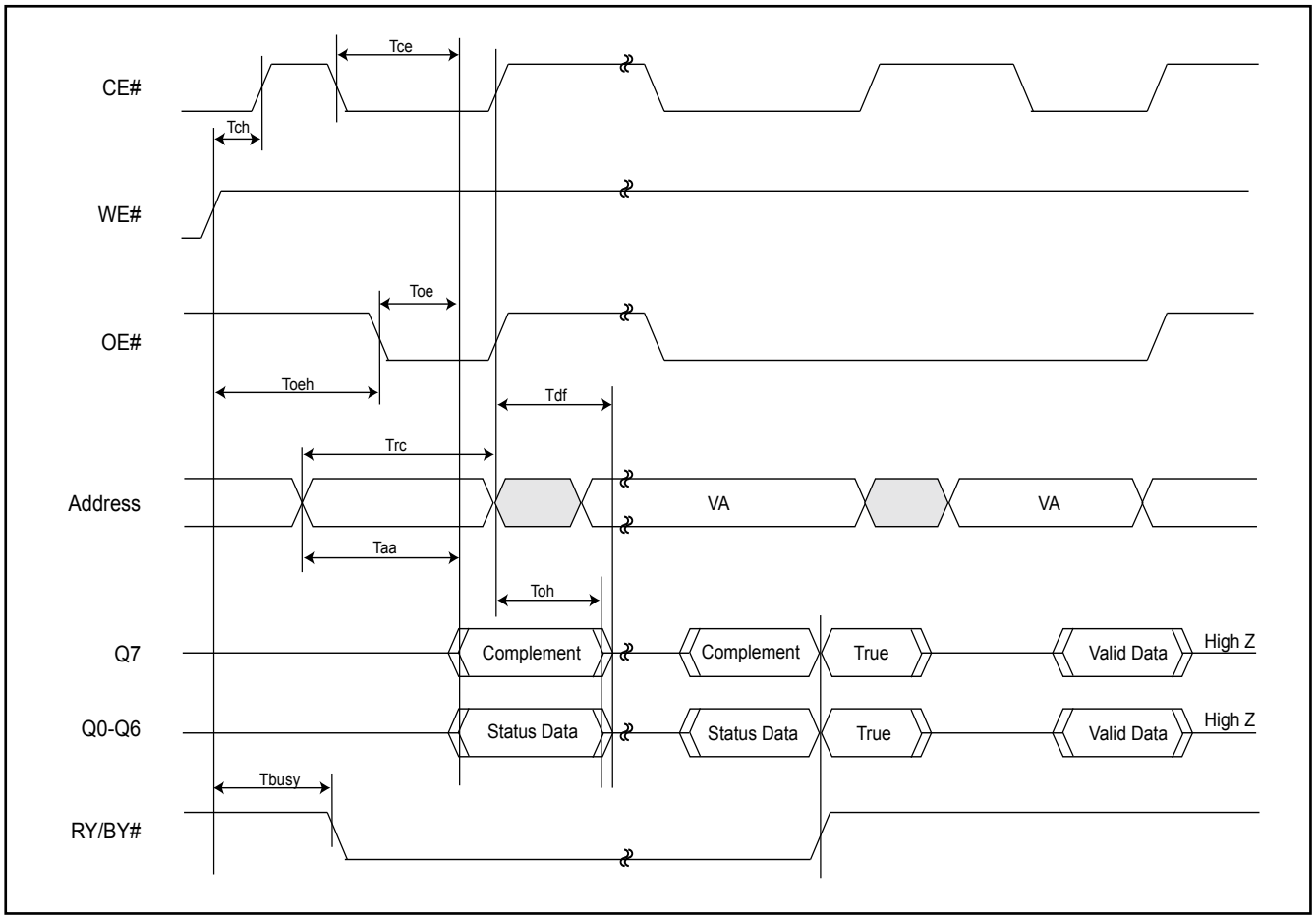
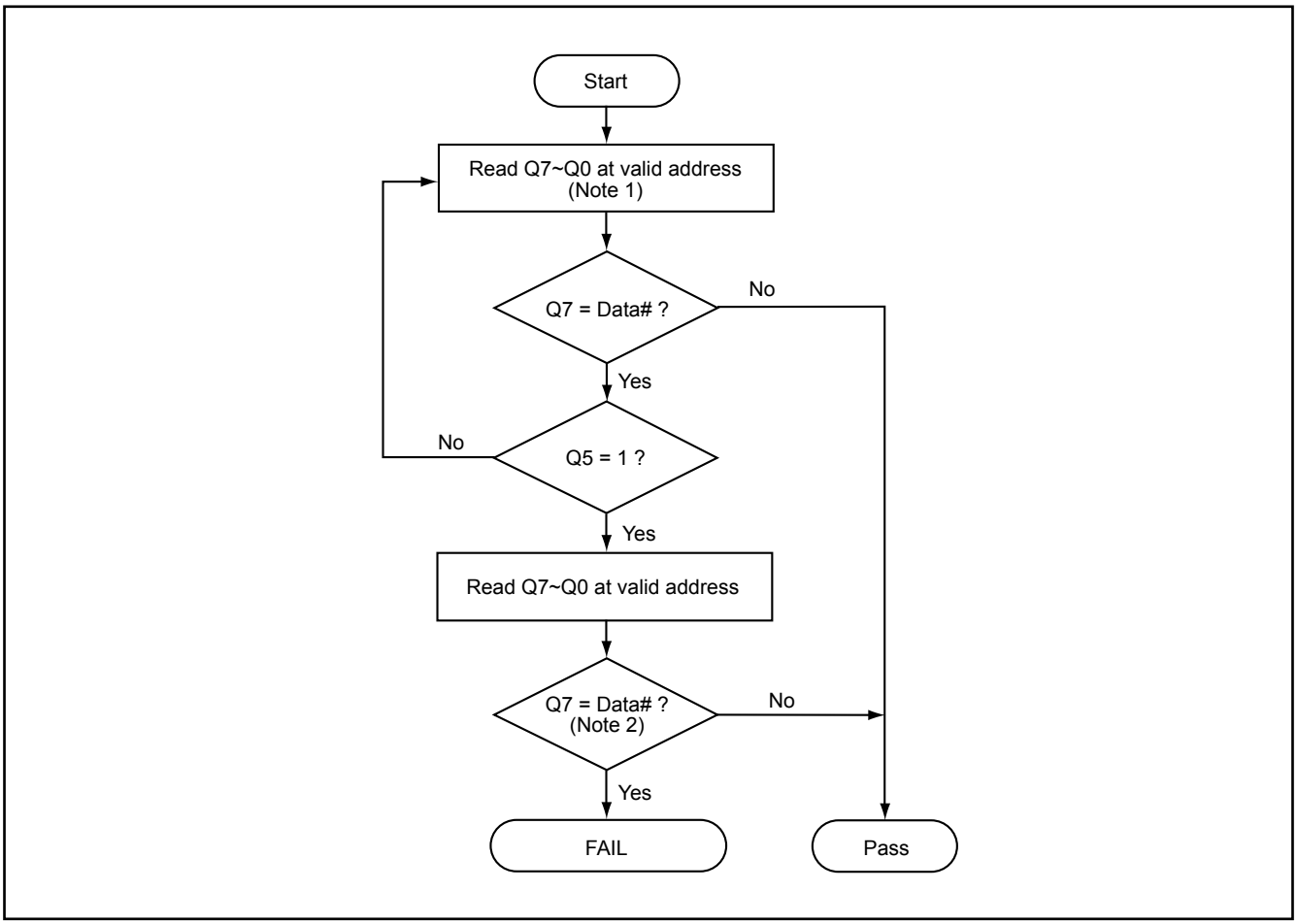


Figure 19. DATA# POLLING ALGORITHM



Notes:
1. For programming, valid address means program address.
   For erasing, valid address means erase sectors address.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 20. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)

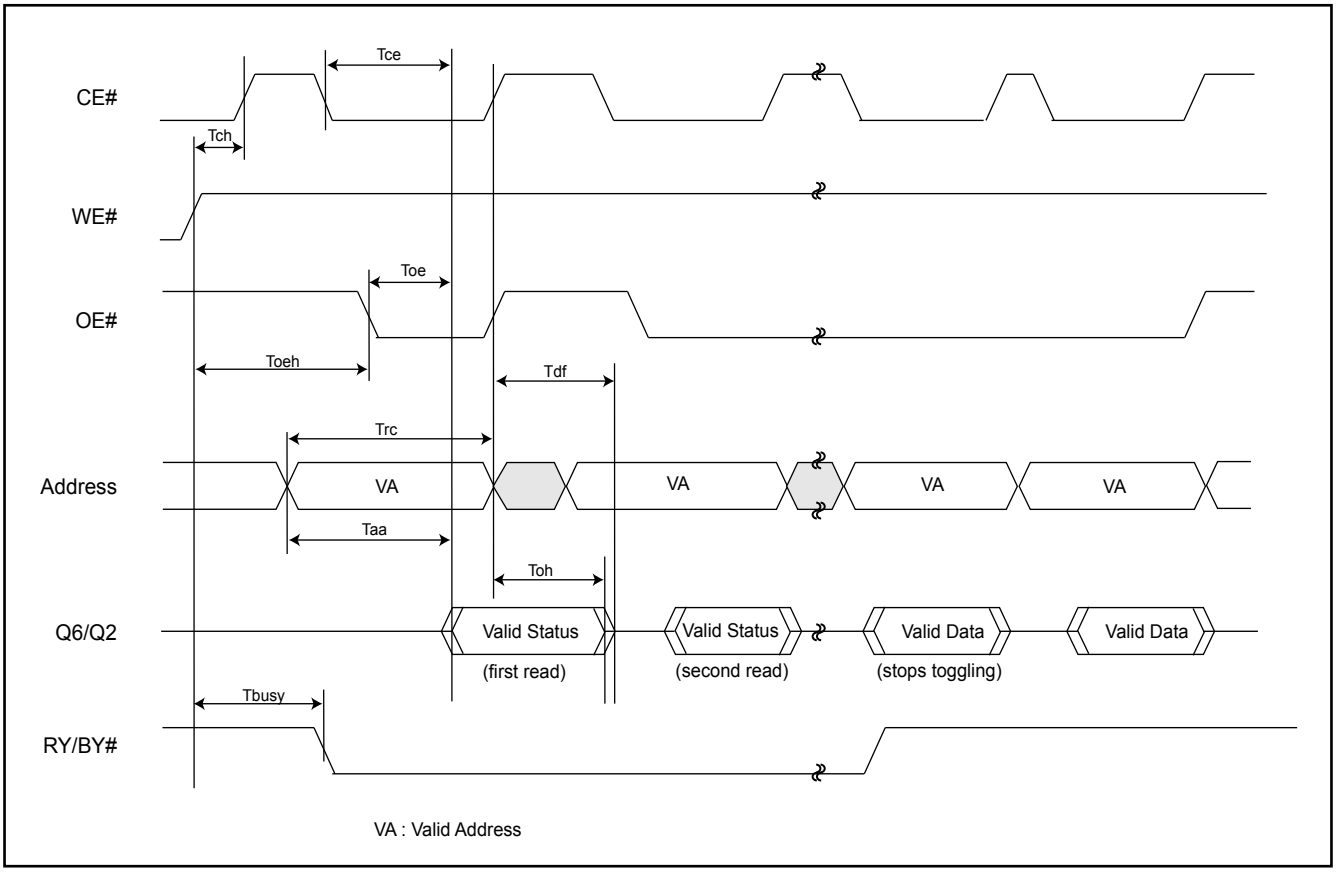
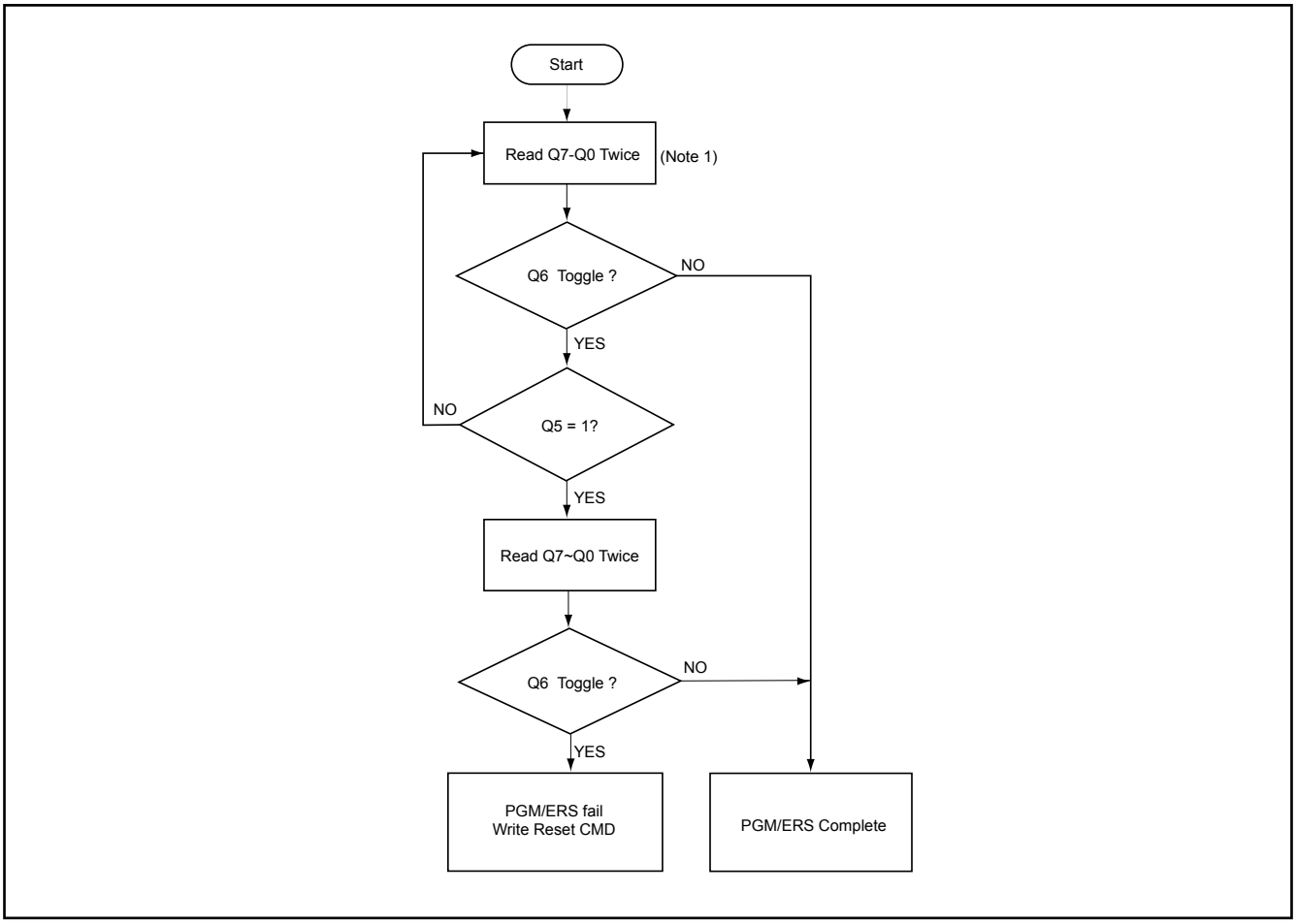


Figure 21. TOGGLE BIT ALGORITHM



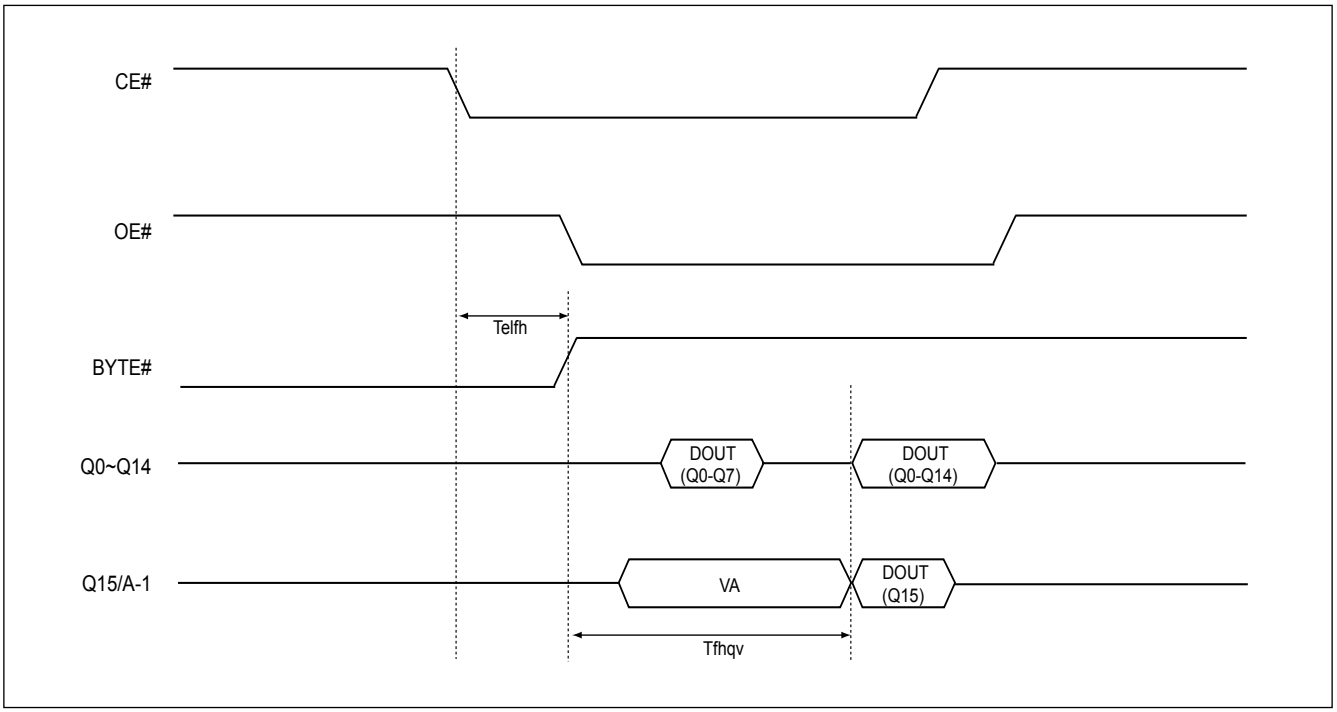
Notes:
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

AC CHARACTERISTICS

WORD/BYTE CONFIGURATION (BYTE#)

Parameter	Description		Speed	Unit
			90	
Telfl/Telfh	CE# to BYTE# from L/H	MAX	5	ns
Tflqz	BYTE# from L to Output Hiz	MAX	30	ns
Tfhqv	BYTE# from H to Output Active	MIN	90	ns

Figure 22. BYTE# TIMING WAVEFORM FOR READ OPERATIONS (BYTE# switching from byte mode to word mode)



RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

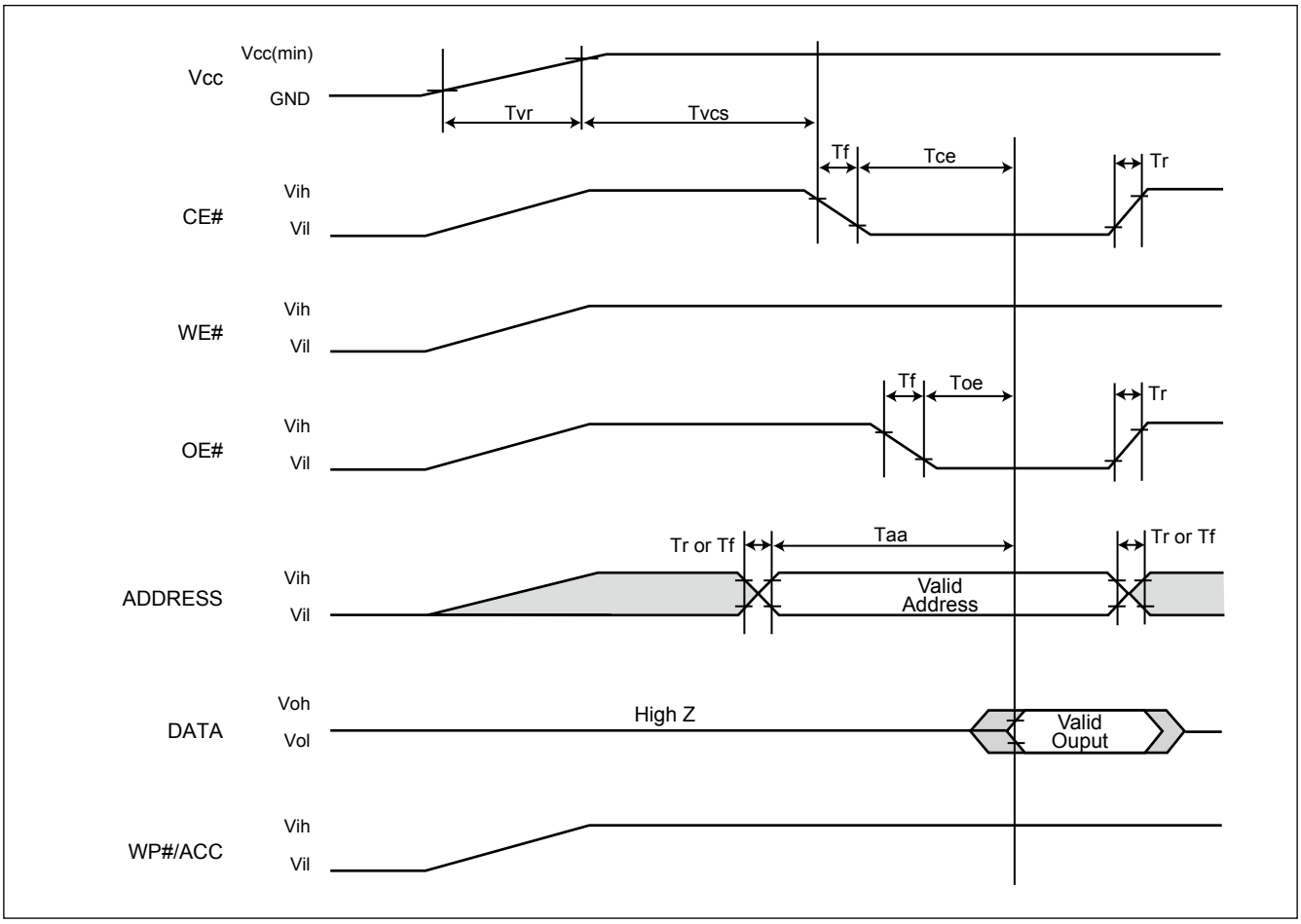


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Min.	Max.	Unit
Tvr	Vcc Rise Time	20	500000	us/V
Tr	Input Signal Rise Time		20	us/V
Tf	Input Signal Fall Time		20	us/V
Tvcs	Vcc Setup Time	200		us

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER		LIMITS			UNITS
		MIN.	TYP.	MAX.	
Chip Erase Time			45	65	sec
Sector Erase Time			0.7	2	sec
Erase/Program Cycles			100,000		Cycles
Chip Programming Time	Byte Mode		50	160	sec
	Word Mode		45	140	sec
Accelerated Byte/Word Program Time			7	210	us
Word Program Time			11	360	us
Byte Programming Time			9	300	us

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 3.0V VCC. Programming specifications assume checkboard data pattern.
2. Maximum values are measured at VCC = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.
4. Erase/Program cycles comply with JEDEC JESD-47 & 22-A117 standard.

Data Retention

PARAMETER	Condition	Min.	Max.	UNIT
Data retention	55˚C	20		years

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage difference with GND on WP#/ACC, A9, OE, Reset# pins	-1.0V	11.5V
Input Voltage difference with GND on all normal pins input	-1.0V	Vcc x 1.5V
Input Current Pulse	-100mA	+100mA
All pins included. Test conditions: Vcc = 3.0V, one pin per testing		

TSOP/SOP PIN CAPACITANCE

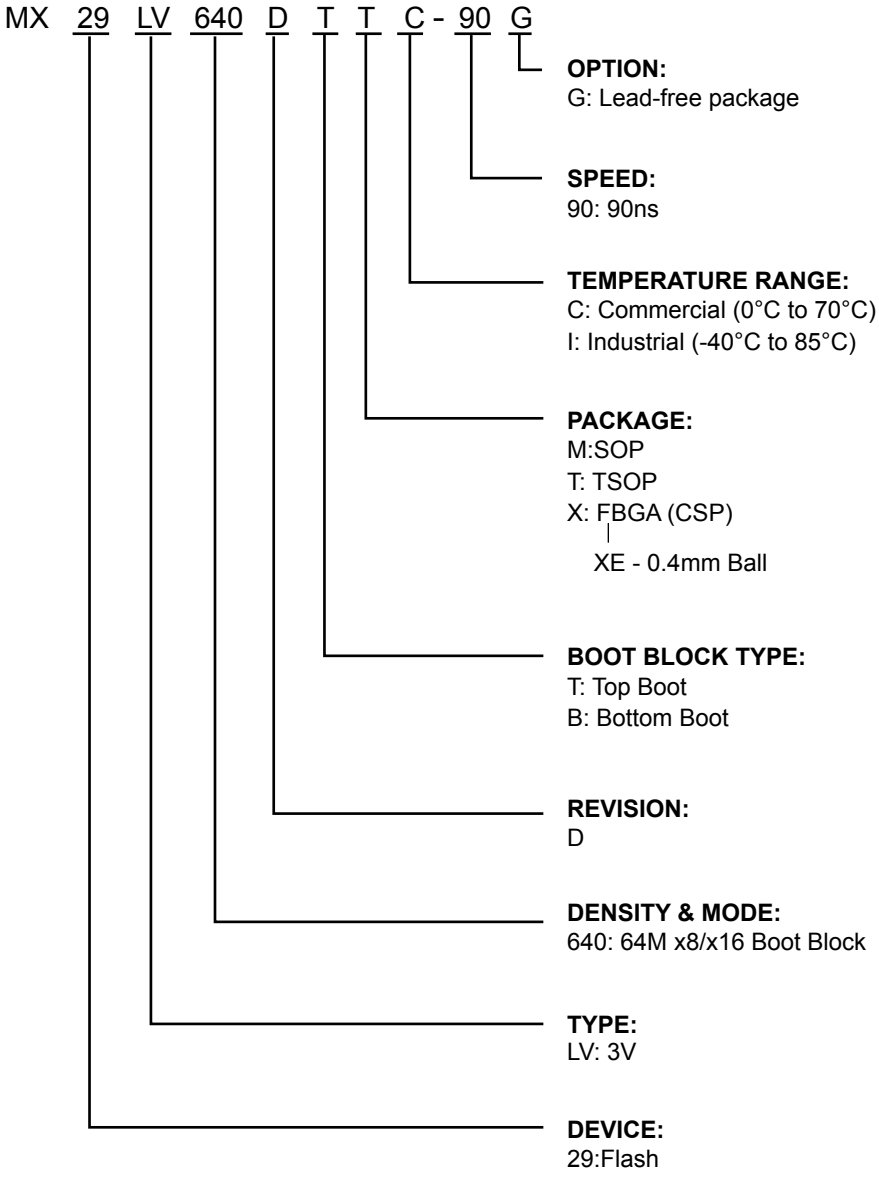
Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN2	Control Pin Capacitance	VIN=0	7.5	15	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN	Input Capacitance	VIN=0	6	7.5	pF

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	Ball Pitch/Ball size	PACKAGE	Remark
MX29LV640DTMC-90G	90		44 Pin SOP	Pb-free
MX29LV640DBMC-90G	90		44 Pin SOP	Pb-free
MX29LV640DTTC-90G	90		48 Pin TSOP(Normal Type)	Pb-free
MX29LV640DBTC-90G	90		48 Pin TSOP(Normal Type)	Pb-free
MX29LV640DTXEC-90G	90	0.8mm/0.4mm	48 Ball LFBGA	Pb-free
MX29LV640DBXEC-90G	90	0.8mm/0.4mm	48 Ball LFBGA	Pb-free
MX29LV640DTXEI-90G	90	0.8mm/0.4mm	48 Ball LFBGA	Pb-free
MX29LV640DBXEI-90G	90	0.8mm/0.4mm	48 Ball LFBGA	Pb-free
MX29LV640DTTI-90G	90		48 Pin TSOP(Normal Type)	Pb-free
MX29LV640DBTI-90G	90		48 Pin TSOP(Normal Type)	Pb-free

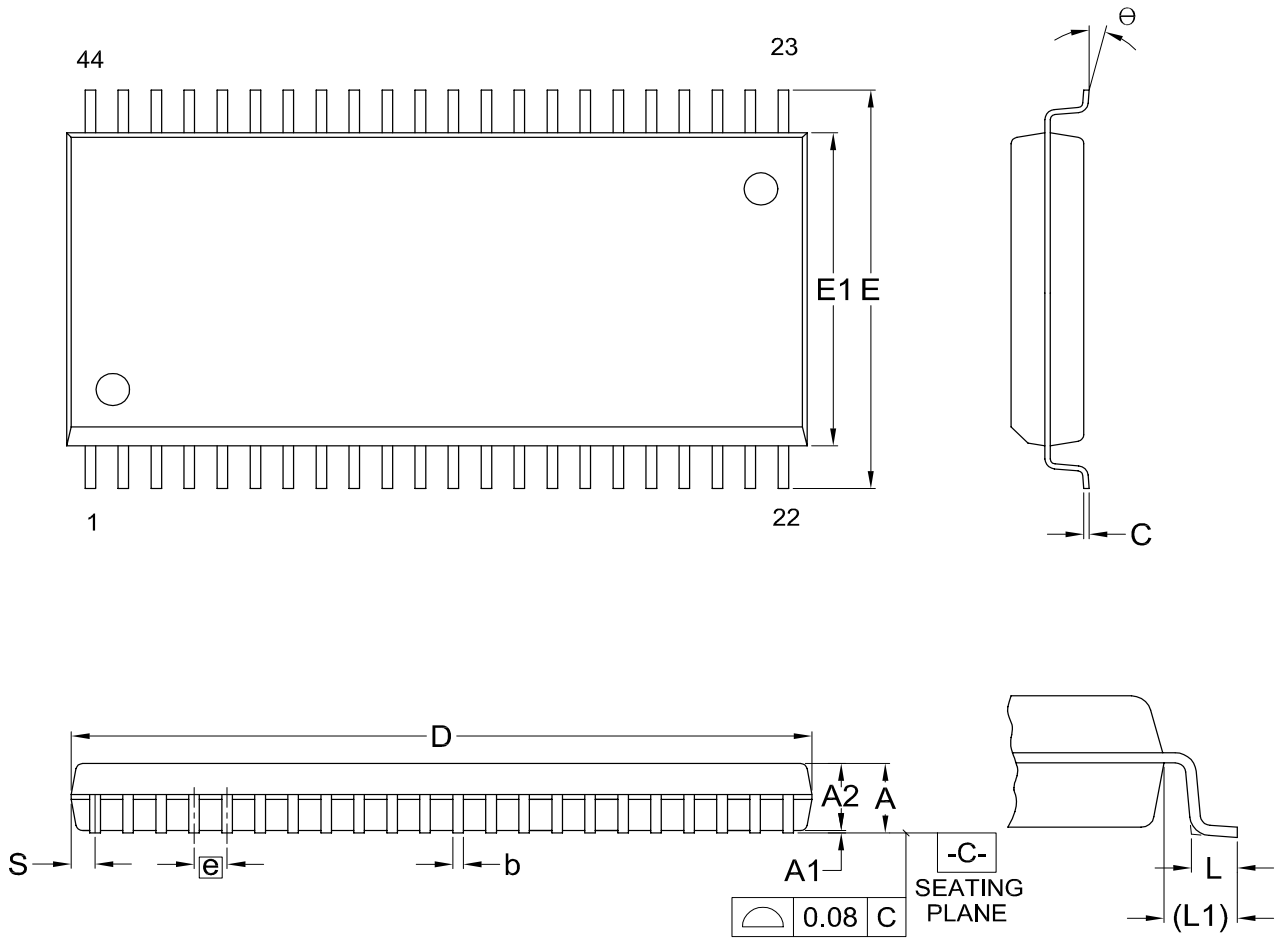
* 44-pin SOP is only for Pachinko Socket

PART NAME DESCRIPTION



PACKAGE INFORMATION

Doc. Title: Package Outline for SOP 44L (500MIL)

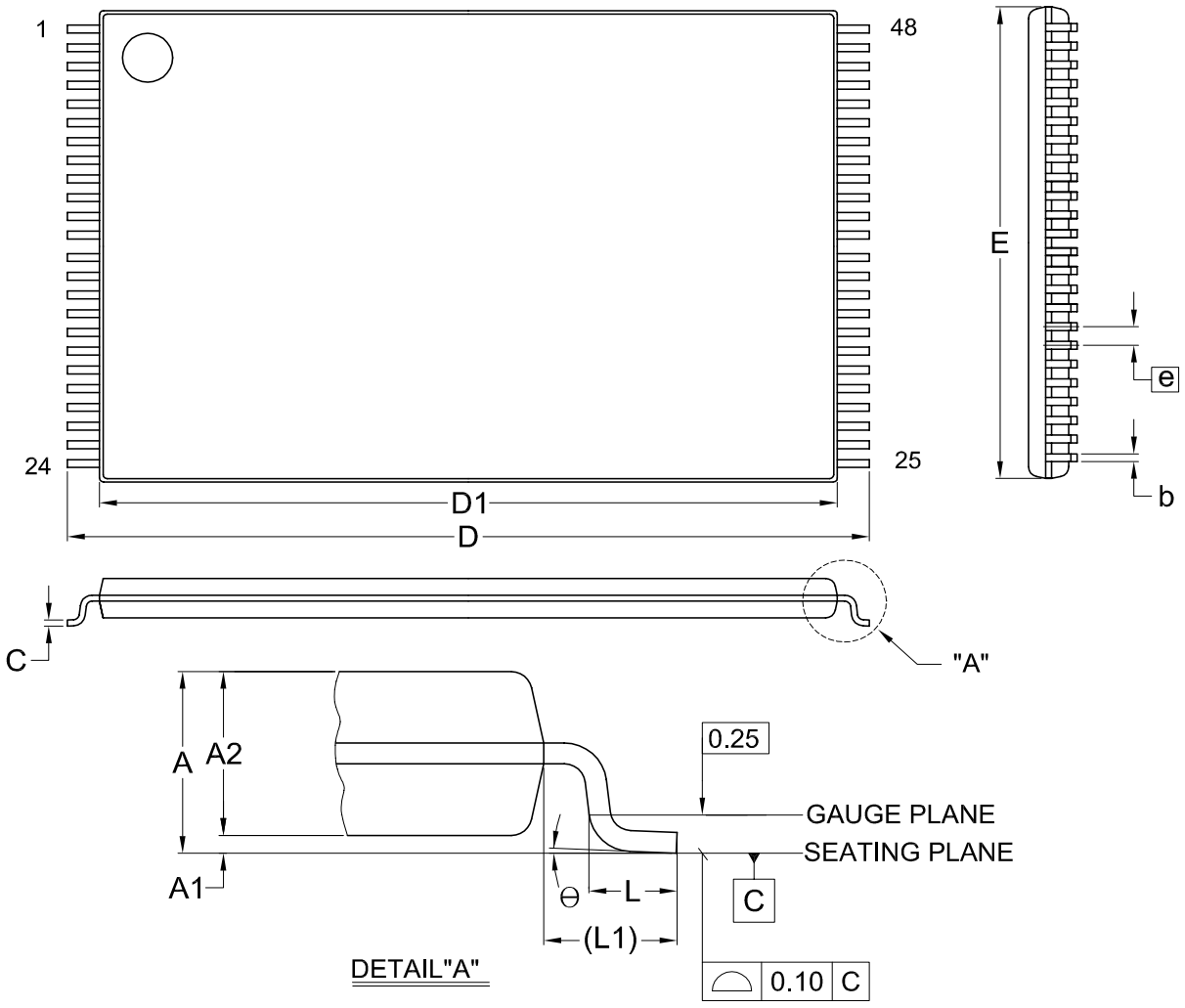


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.59	0.36	0.15	28.37	15.83	12.47	---	0.56	1.51	0.78	0
	Nom.	---	0.15	2.69	0.41	0.20	28.50	16.03	12.60	1.27	0.76	1.71	0.91	5
	Max.	3.00	0.20	2.80	0.51	0.25	28.63	16.23	12.73	---	0.96	1.91	1.04	10
Inch	Min.	---	0.004	0.102	0.014	0.006	1.117	0.623	0.491	---	0.022	0.059	0.031	0
	Nom.	---	0.006	0.106	0.016	0.008	1.122	0.631	0.496	0.050	0.030	0.067	0.036	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.127	0.639	0.501	---	0.038	0.075	0.041	10

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1405	7	MO-175			2008/02/18

Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM



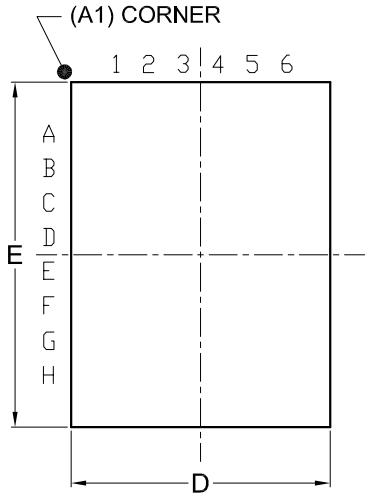
Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90	—	0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10	—	0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469	—	0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476	—	0.028	0.035	8

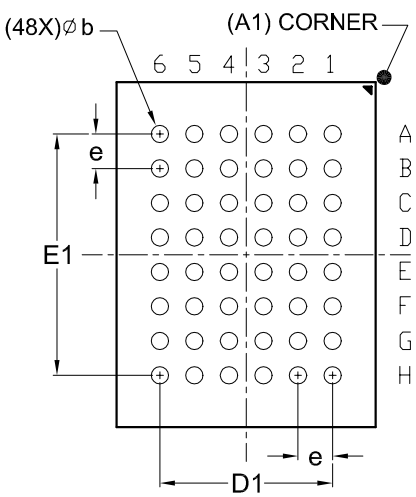
DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	8	MO-142			2007/08/03

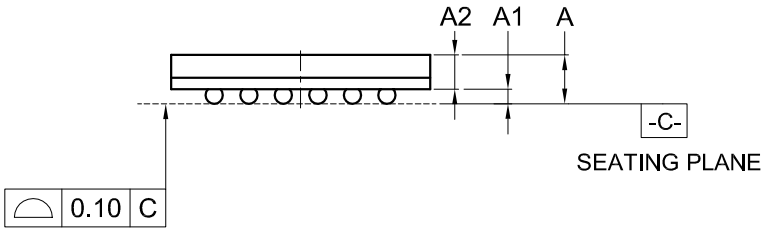
Title: **Package Outline for CSP 48BALL(6X8X1.3MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)**

TOP VIEW



BOTTOM VIEW





Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	5.90		7.90		
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	5.60	0.80
	Max.	1.30	0.35	---	0.45	6.10		8.10		
Inch	Min.	—	0.010	0.026	0.014	0.232		0.311		
	Nom.	—	0.012	—	0.016	0.236	0.157	0.315	0.220	0.031
	Max.	0.051	0.014	—	0.018	0.240		0.319		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4202	4	MO-219			12-12-'03

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Modified Tvcs from 50us(Min.) to 100us(Min.)	P31,54	MAY/02/2007
	2. Modified latch-up protected to 250mA→100mA	P1	
	3. Modified latch-up characteristics	P1,29,55	
	4. Modified sector erase resume section ...should be a 400us→4ms	P24	
	5. Modified "sector erase time" from 0.9s(typ)/15s(max) to 0.7s(typ)/2s(max)	P1, 31,55	
1.1	1. Erase/ Program test methodology comply with JEDEC standard	P1,55	SEP/03/2007
	2. Added Byte# mode and removed NC pin of the pin description table	P2	
	3. Added industrial grade information	P56,57	
1.2	1. Removed 44-sop package information	All	OCT/23/2007
	2. Modified figure 11. CE# controlled write timing waveform	P41	
	3. Modified Tvcs from 100us to 200us	P31,54	
	4. Added overshoot/undershoot information	P28	
1.3	1. Added 44-pin SOP package solution	P2,56,57	JAN/25/2008
	2. Corrected wrong security sector address	P8,12	
	3. Corrected wrong ID code data	P21	
	4. Redefined Trv (Vcc Rise Time) min. spec	P54	
	5. Revised Tdf spec from 30ns(max.) to 16ns(max.)	P31	
1.4	1. Changed Vhv spec from 10.5V~11.5V to 9.5V~10.5V	P29, P40,47	APR/08/2008
	2. Added note 1 of AC Characteristics	P31	
1.5	1. Modified DATA at Silicon ID Dead Timing Waveform	P48	MAY/29/2008
1.6	1. Renamed CSP package as LFBGA	P2,56	AUG/15/2008
1.7	1. Revised copyright page	P63	MAY/18/2009
	2. Added migration page	P1,2	
	3. Modified the data retention condition from 10 years to 20 years	P1,56	
	4. Added Tsrw parameter to read and erase/program operation table	P32,34	
1.8	1. Revised factory locked/unlocked code from 98/18 to 88/08	P15, P21~22	JUL/07/2009
1.9	1. Modified SA44/SA45 address	P7	OCT/02/2009
2.0	1. Modified CIN2(max.) from 9pF to 15pF	P56	NOV/26/2010

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