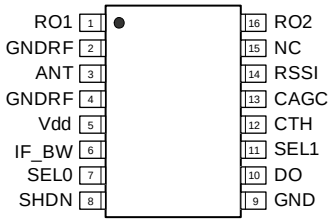
Ordering Information

Part Number	Temperature Range	Package
MICRF218AYQS	–40° to +85°C	16-Pin QSOP

Pin Configuration



MICRF218AYQS

Pin Description

16-Pin QSOP	Pin Name	Pin Function
1	RO1	Reference resonator input connection to Colpitts oscillator stage. May also be driven by external reference signal of 1.5V p-p amplitude maximum.
2	GNDRF	Negative supply connection associated with ANT RF input.
3	ANT	RF signal input from antenna. Internally AC-Coupled. It is recommended that a matching network with an inductor to RF ground is used to improve ESD protection.
4	GNDRF	Negative supply connection associated with ANT RF input.
5	VDD	Positive supply connection for all chip functions.
6	IF_BW	IF bandwidth control logic input. Use VDD for Wide IF Bandwidth or VSS for Narrow IF Bandwidth. This pin must not be left floating, must be tied to VDD or VSS.
7	SEL0	Logic control input with active internal pull-up. Used in conjunction with SEL1 to control the demodulator low pass filter bandwidth. (See filter table for SEL0 and SEL1 in application subsection)
8	SHDN	Shutdown logic control input. Active internal pull-up and must be pulled low for Normal Operation.
9	GND	Negative supply connection for all chip functions except RF input.
10	DO	Demodulated data output.
11	SEL1	Logic control input with active internal pull-up. Used in conjunction with SEL0 to control the demodulator low pass filter bandwidth. (See filter table for SEL0 and SEL1 in application subsection)
12	CTH	Demodulation threshold voltage integration capacitor. Capacitor to GND sets the settling time for the demodulation data slicing level. Values above 1nF are recommended and should be optimized for data rate and data profile.
13	CAGC	AGC filter capacitor. A capacitor, normally greater than 0.47uF, is connected from this pin to GND
14	RSSI	Received signal strength indication output. Output is from a buffer with 200 ohms typical output impedance.
15	NC	Not Connected
16	RO2	Reference resonator connection. 7pF in parallel with low resistance MOS switch to GND during normal operation. Driven by startup excitation circuit during the internal startup control sequence.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}) .....+5V
Input Voltage .....+5V
Junction Temperature .....+150°C
Lead Temperature (soldering, 10sec.) .....+260°C
Storage Temperature (T_S) .....-65ºC to +150°C
Maximum Receiver Input Power .....+10dBm
ESD Rating(3) 3kV

Operating Ratings[2]

Supply voltage (V_{DD}) ..... +3.0V to +3.6V
Ambient Temperature (T_A)..... –40°C to +85°C
Input Voltage (V_{IN}) .....3.6V (max.)
Maximum Input RF Power ..... –20dBm
Operating Frequency.....300MHz to 450MHz

Electrical Characteristics[4]

Specifications apply for VDD = 3.0V, VSS = 0V, CAGC = 4.7µF, CTH = 0.1µF, Bold values indicate –40°C - T_A +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DD}	MICRF218 Operating Supply Current	Continuous Operation, f_{RX} = 315MHz		4.0		mA
		20:1 Duty Cycle, f_{RX} = 315MHz		0.2		mA
		Continuous Operation, f_{RX} = 433.92MHz		5.5		mA
		20:1 Duty Cycle, f_{RX} = 433.92MHz		0.3		mA
Ishut	Shut down Current			1		µA
RF/IF Section						
	Image Rejection			20		dB
	1st IF Center Frequency	f_{RX} = 315MHz, Narrow IF		0.98		MHz
		f_{RX} = 433.92MHz, Narrow IF		1.4		MHz
	1st IF Center Frequency	f_{RX} = 315MHz, Wide IF		1.8		MHz
		f_{RX} = 433.92MHz, Wide IF		2.4		MHz
	Receiver Sensitivity @ 1kbps	f_{RX} = 315MHz, Narrow IF (50Ω)		-108		dBm
		f_{RX} = 433.92MHz, Narrow IF (50Ω)		-108		dBm
	Receiver Sensitivity @ 1kbps	f_{RX} = 315MHz, Wide IF (50Ω)		-106		dBm
		f_{RX} = 433.92MHz, Wide IF (50Ω)		-106		dBm
	IF Bandwidth	f_{RX} = 315MHz, Narrow IF		400		kHz
		f_{RX} = 433.92MHz, Narrow IF		550		kHz
		f_{RX} = 315MHz, Wide IF		1000		kHz
		f_{RX} = 433.92MHz, Wide IF		1500		kHz
	Antenna Input Impedance	f_{RX} = 315MHz		16-j211		Ω
		f_{RX} = 433.92MHz		9.54-j152		Ω
	Receive Modulation Duty Cycle	Note 6	20		80	%

Electrical Characteristics[4] (Continued)

Specifications apply for VDD = 3.0V, VSS = 0V, CAGC = 4.7µF, CTH = 0.1µF, Bold values indicate –40°C - T_A +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
	AGC Attack / Decay Ratio	t_{ATTACK} / t_{DECAY}		0.1		
	AGC pin leakage current	T_A = 25ºC		± 2		nA
		T_A = +85ºC		± 800		nA
	AGC Dynamic Range @ fRX = 433.92MHz	RFIN @ -50dBm		1.13		V
		RFIN @ -110dBm		1.70		V
Reference Oscillator						
	Frequency	f_{RX} = 315MHz, Narrow IF, IF_BW = VSS Crystal Load Cap = 10pF		9.8131		MHz
		f_{RX} = 315MHz, Wide IF, IF_BW = VDD Crystal Load Cap = 10pF		9.78823		MHz
		f_{RX} = 433.92MHz Narrow IF, IF_BW = VSS Crystal Load Cap = 10pF		13.5178		MHz
		f_{RX} = 433.92MHz Wide IF , IF_BW = VDD Crystal Load Cap = 10pF		13.48352		MHz
	Input Impedance			300		kΩ
	Input Range		0.2		1.5	Vp-p
	Source Current	V(REFOSC) = 0V		3.5		µA
Demodulator						
	CTH Source Impedance	f_{REFOSC} = 9.8131MHz, 315MHz, Note 8		165		kΩ
	CTH Leakage Current	TA = 25ºC		± 2		nA
		TA = +85ºC		± 800		
	Demodulator Filter Bandwidth @ 315 MHz	SEL0=0, SEL1=0		1180		Hz
		SEL0=0, SEL1=1		2360		Hz
		SEL0=1, SEL1=0		4720		Hz
		SEL0=1, SEL1=1		9420		Hz
	CTH Source Impedance	f_{REFOSC} = MHz, 433.92MHz, note 8		120		kΩ
	CTH Leakage Current	TA = 25ºC		± 2		nA
		TA = +85ºC		± 800		
	Demodulator Filter Bandwidth @ 433.92 MHz	SEL0=0, SEL1=0		1625		Hz
		SEL0=0, SEL1=1		3250		Hz
		SEL0=1, SEL1=0		6500		Hz
		SEL0=1, SEL1=1		13000		Hz

Electrical Characteristics[4] (Continued)

Specifications apply for VDD = 3.0V, VSS = 0V, CAGC = 4.7µF, CTH = 0.1µF, Bold values indicate –40°C - T_A +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Digital / Control Functions						
	Input High Voltage	Pins DO (As input), SHDN	**$0.8V_{DD}$**			V
	Input Low Voltage	Pins DO (As input), SHDN			**$0.2V_{DD}$**	V
	DO pin output current	Source @ 0.8 Vdd		260		µA
		Sink @ 0.2 Vdd		600		
	Output rise and fall times	Cl = 15 pF, pin DO, 10-90%		2		µsec
RSSI						
	RSSI DC Output Voltage Range			0.22 to 2		V
	RSSI response slope	-90dBm to -40dBm		35		mV/ dBm
	RSSI Output Current			±1.5		mA
	RSSI Output Impedance			200		Ω
	RSSI Response Time	50% data duty cycle, input power to Antenna = -20 dBm		0.3		Sec

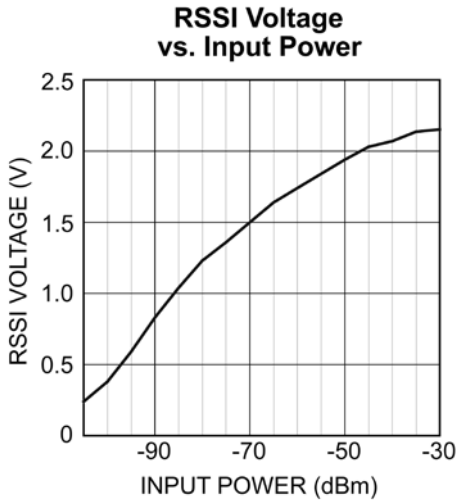
Notes:

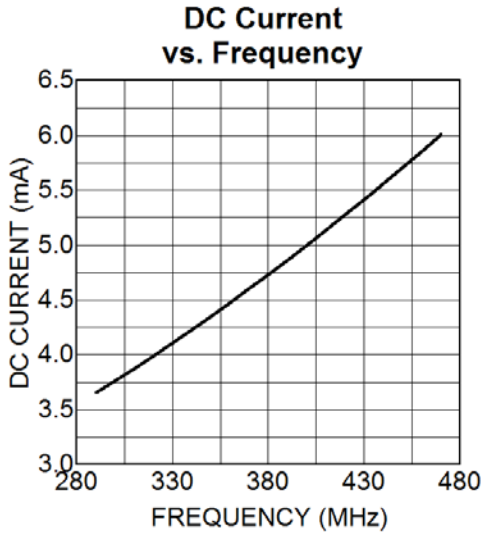
1. **Exceeding the absolute maximum rating may damage the device.**
2. **The device is not guaranteed to function outside its operating rating.**
3. **Device are ESD sensitive. Use appropriate ESD precaution. Exceeding the absolute maximum rating may damage the device.**
4. **Sensitivity is defined as the average signal level measured at the input necessary to achieve 10-2 BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (Manchester encoded) at a data rate of 1kBPS. Conductive measurement is performed using 50 ohm test circuit .**
5. **Spurious reverse isolation represents the spurious component that appear on the RF input pin (ANT) measured into 50 Ohms with an input RF matching network.**
6. **When data burst does not contain preamble, the duty cycle is then defined as total duty cycle, including any "quiet" time between data bursts. When data bursts contain preamble sufficient to charge the slice level on capacitor Cth, then duty cycle is the effective duty cycle of the burst alone. [For example, 100msec burst with 50% duty cycle, and 100msec "quiet" time between bursts. If burst includes preamble, duty cycle is $T_{ON}/(T_{ON} + t_{OFF})$ = 50%; without preamble, duty cycle is $T_{ON}/(T_{ON} + T_{OFF} + T_{QUIET})$ = 50msec/(200msec) = 25%. T_{ON} is the (Average number of 1's/burst) × bit time, and $T_{OFF} = T_{BURST} – T_{ON}$.)**
7. **Parameter scales linearly with reference oscillator frequency f_T. For any reference oscillator frequency other than one of the tabulated frequencies (called F_{TAB}), compute new parameter value as the ratio:**

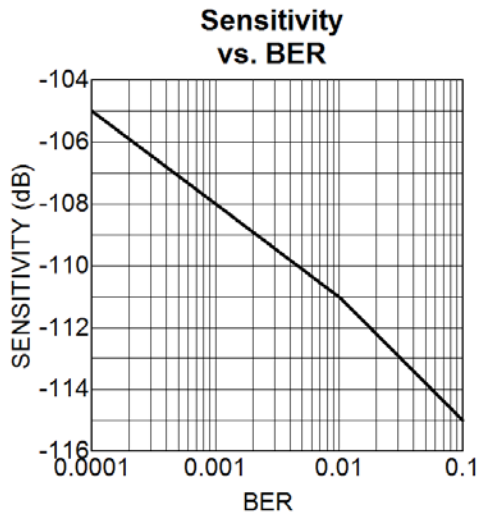
   Parameter at f_{REFOSC}MHz = (f_{REFOSC}MHz /F_{TAB}) × (parameter at F_{TAB}MHz)
8. **Parameter scales inversely with reference oscillator frequency fT. For any reference oscillator frequency other than one of the tabulated frequencies (called F_{TAB}), compute new parameter value as the ratio:**

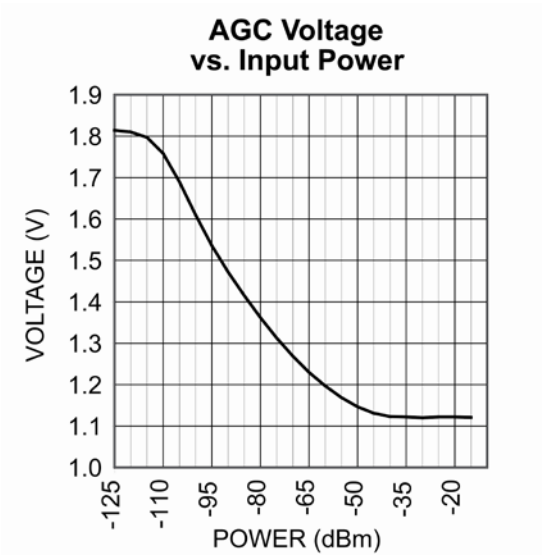
   Parameter at f_{REFOSC}MHz = (F_{TAB} / f_{REFOSC}MHz) × (parameter at F_{TAB}MHz)

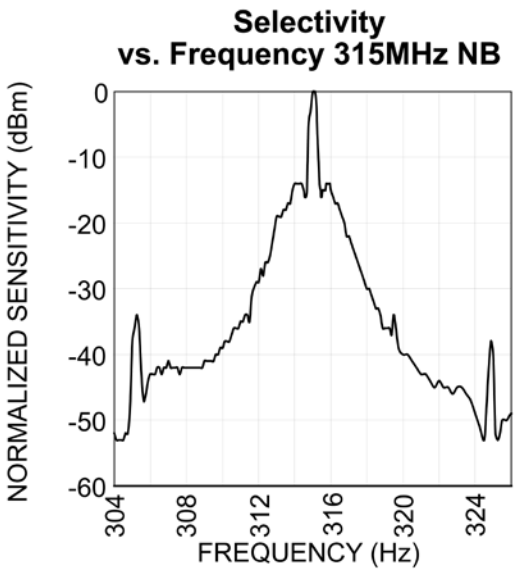
Typical Characteristics

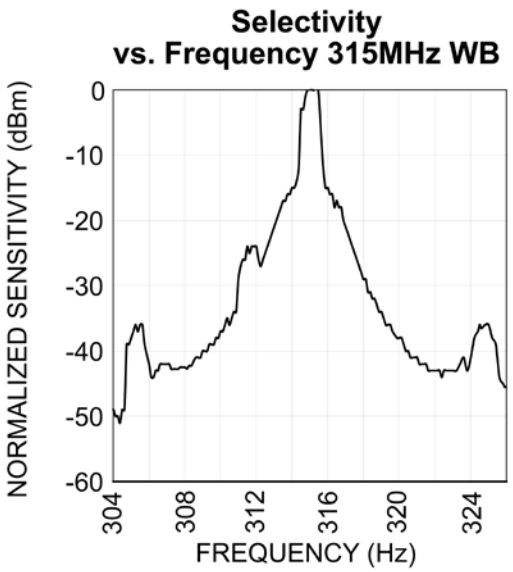


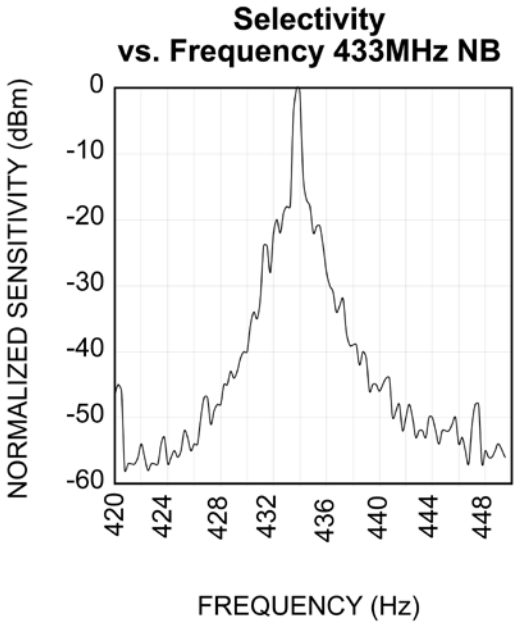


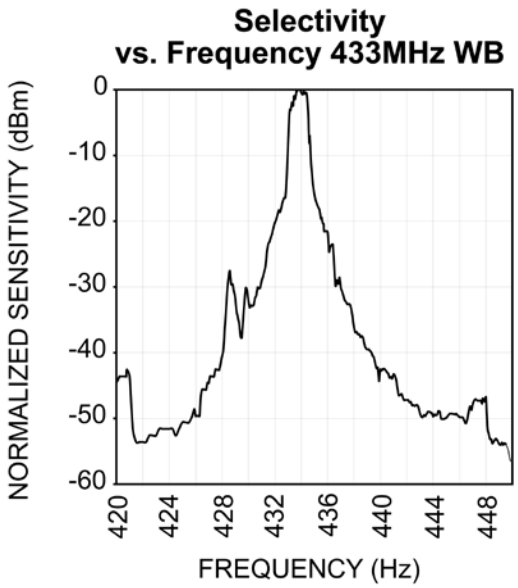




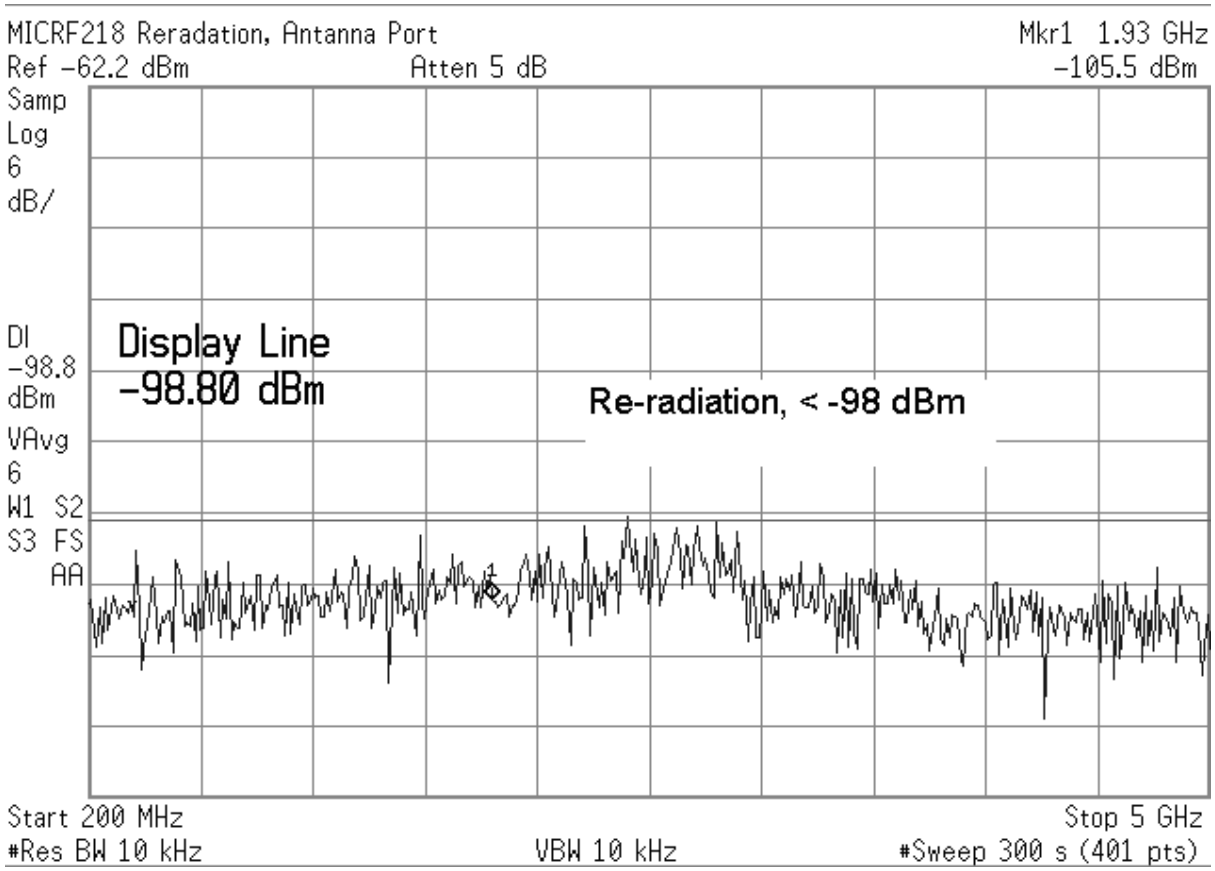








LO Leakage in RF Port



Re-radiation from MICRF218 Antenna Port

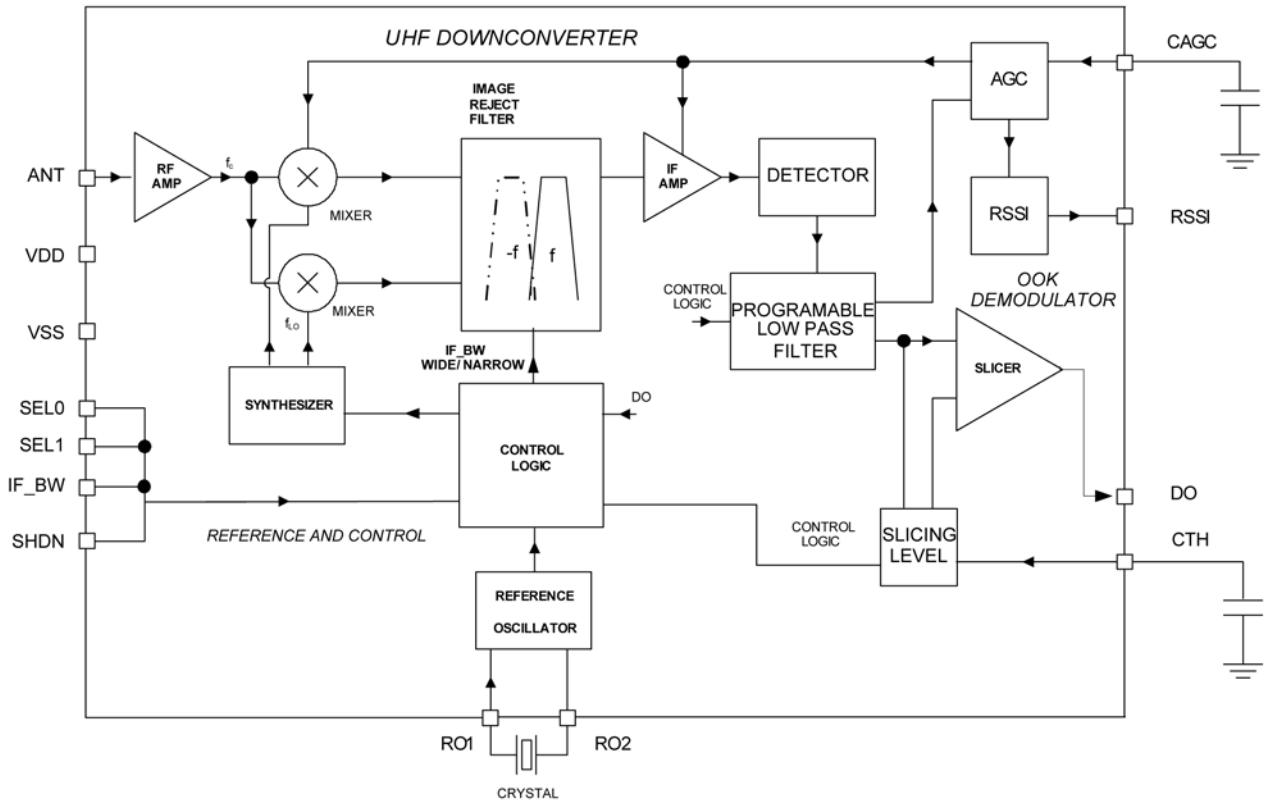


Figure 1 Simplified Block Diagram

Functional Description

Figure 1 illustrates the basic structure of the MICRF218. It is composed of three sub-blocks; Image Rejection UHF Down-converter with Switch-able Dual IF Bandwidths, the OOK Demodulator, and Reference and Control Logics.

Outside the device, the MICRF218 requires only three components to operate: two capacitors (CTH, and CAGC) and the reference frequency device, usually a quartz crystal.

Additional five components may be used to improve performance. These are: low cost linear regulator decoupling capacitor, two components for the matching network, and two components for the pre-selector band pass filter.

Receiver Operation

LNA

The RF input signal is AC-coupled into the gate circuit of the grounded source LNA input stage. The LNA is a Cascoded NMOS.

Mixers and Synthesizer

The LO ports of the Mixers are driven by quadrature local oscillator outputs from the synthesizer block. The local oscillator signal from the synthesizer is placed on the low side of the desired RF signal to allow suppression of the image frequency at twice the IF frequency below the wanted signal. The local oscillator is set to 32 times the crystal reference frequency via a phase-locked loop synthesizer with a fully integrated loop filter.

Image Reject Filter and IF Band-Pass Filter

The IF ports of the mixer produce quadrature down converted IF signals. These IF signals are low-pass filtered to remove higher frequency products prior to

the image reject filter where they are combined to reject the image frequencies. The IF signal then passes through a third order band pass filter. The IF Band-Pass filters are fully integrated inside the MICRF218. After filtering, four active gain controlled amplifier stages enhance the IF signal to proper level for demodulation.

IF Bandwidth General Description

The MICRF218 has IF filters which may be configured for operation in a narrow band or wide band mode using the IF_BW pin. This pin must not be left floating; it must be tied to VDD or VSS. With the use of a 13.4835MHz crystal and the IF_BW = VDD (wide mode) the IF frequency is set to 2.4MHz with a bandwidth of 1500kHz. With the use of a 13.5178MHz crystal and the IF_BW = VSS (narrow mode) the IF frequency is set to 1.4MHz with a bandwidth of 550kHz at 433.92MHz.

The crystal frequency for Wide Bandwidth IF operation is given by:

$$\text{REFOSC} = \frac{\text{Operating Freq}}{(32 + \frac{2.178}{12})}\text{MHz} \qquad \text{Eq. 1}$$

The crystal frequency for Narrow Bandwidth IF operation is given by:

$$\text{REFOSC} = \frac{\text{Operating Freq}}{(32 + \frac{1.198}{12})}\text{MHz} \qquad \text{Eq. 2}$$

Note: The IF frequency, IF bandwidth, and IF separation between IF_BW modes using a single crystal will scale linearly and can be calculated as follows:

$$\text{IF\_Parameter} = \text{IF\_Parameter}_{@\,433.92\,\text{MHz}} * \left(\frac{\text{Operating Freq (MHz)}}{433.92(\text{MHz})}\right) \qquad \text{Eq. 3}$$

Switched Crystal Application Operation

Appropriate choice of two crystal frequencies and IF_BW mode switching allows operation at two different frequencies; one with low bandwidth operation and the other with high bandwidth operation. Either the lower or higher reception frequency may use the wider IF bandwidth by utilizing the appropriate equation (1) or (2) for each crystal frequency.

The following circuit, Figure 4, is an example of switched crystal operation. The IF Bandwidth Control and REF-OSC Control allow switching between two operating frequencies with either a narrow bandwidth or a wide bandwidth. In this case, the logic control switches between 390MHz in Wide Band Mode and 315MHz in Narrow Bandwidth Mode. The advantage of this circuit is when a RF interferer is at one frequency, the receiver can go to another frequency to get clear reception.

Figure 5 shows PCB layout for MICRF218 with switched crystal operation. Please contact the Micrel RF Application Group for detailed document.

Dual Frequency Configuration Examples:

Scenario 1:

- Frequency 1 - 315MHz Narrow Bandwidth
- Frequency 2 - 433.92MHz Wide Bandwidth

A 9.81314MHz crystal switched in circuit during narrow IF mode, combined with a 13.48352MHz crystal, allows operation at 315MHz with 400kHz IF bandwidth, and at 433.92MHz with 1500kHz bandwidth.

Scenario 2:

- Frequency 1 - 315MHz Wide Bandwidth
- Frequency 2 - 433.92MHz Narrow Bandwidth

A 9.78823MHz crystal switched in circuit during Wide IF mode, combined with a 13.51783MHz crystal, allows operation at 315MHz with 1000kHz IF bandwidth, and 433.92MHz with 550kHz IF bandwidth.

Scenario 3:

- Frequency 1 - 315MHz Narrow Bandwidth
- Frequency 2 - 433.92MHz Narrow Bandwidth

A 9.8131MHz crystal switched in circuit, combined with a 13.51783MHz crystal during narrow IF mode, allows operation at 315MHz with 400kHz IF bandwidth, and at 433.92MHz with 550kHz bandwidth.

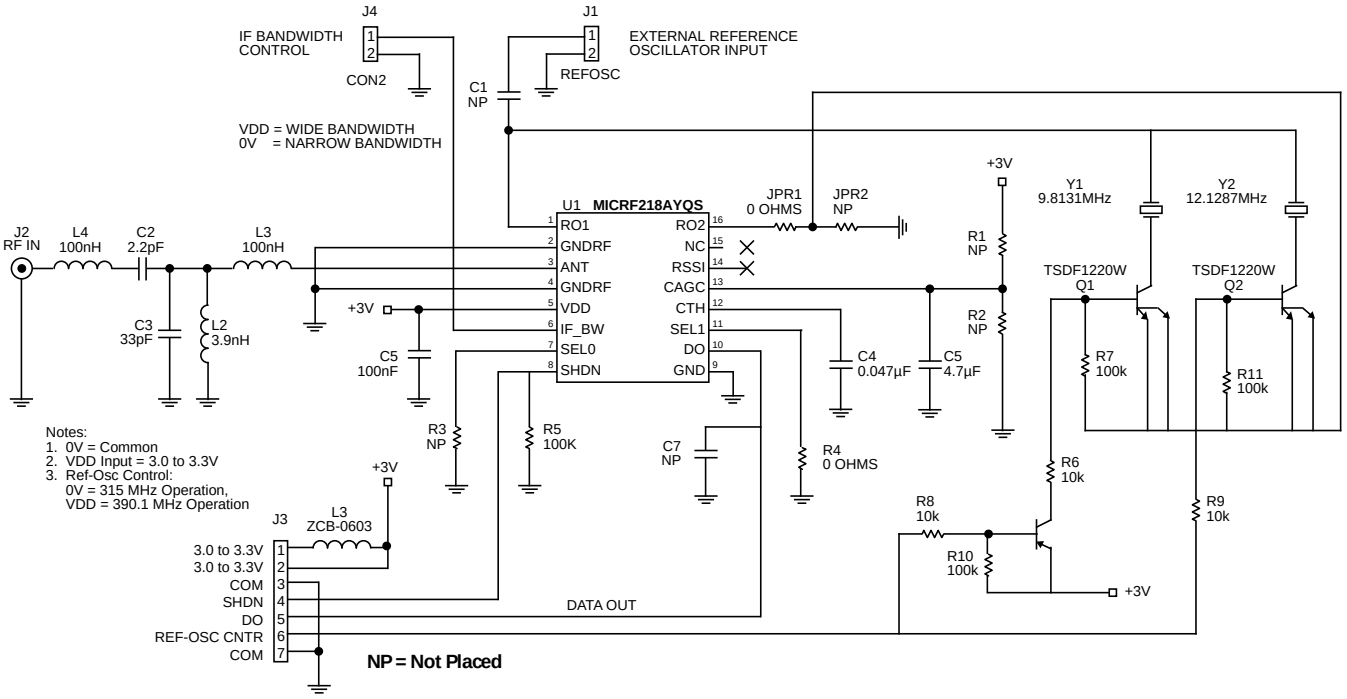


Figure 4. Dual Frequency QR218BP_SWREF, 315 MHz and 390 MHz

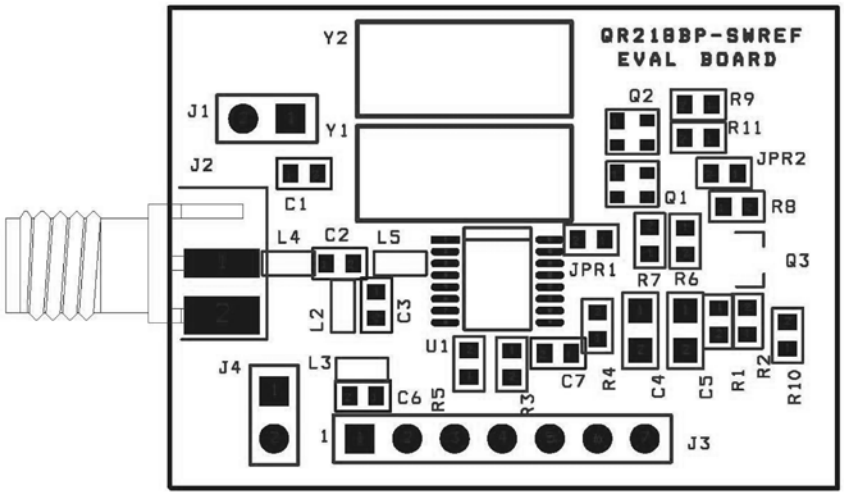


Figure 5. MICR218 Dual Frequency Evaluation Board

Single Crystal Operation for Dual Frequency Operation

When using a single crystal, the IF_BW function may be used to switch between two operating frequencies.

Bandwidth will scale directly with operating frequency (equation 3). Higher operating frequency will have the wider IF bandwidth.

Given one operating frequency, the other frequency can be determined.:

$$Freq2_{\text{Narrow Bandwidth}} = Freq1_{\text{Wide Bandwidth}} * \frac{(384+1.198)}{(384-2.178)}$$

Eq. 4

$$Freq2_{\text{Wide Bandwidth}} = Freq1_{\text{Narrow Bandwidth}} * \frac{(384+2.178)}{(384-1.198)}$$

Eq. 5

OOK Demodulator

The following section discusses the demodulator which is comprised of Detector, Programmable Low Pass Filter, Slicer, and AGC comparator.

Detector and Programmable Low-Pass Filter

The demodulation starts with the detector removing the carrier from the IF signal. Post detection, the signal becomes baseband information. The programmable low-pass filter further enhances the baseband information through the use of SEL0 and SEL1. There are four programmable low-pass filter BW settings for 433.92MHz operation, see Table 1. Low pass filter BW will vary with RF Operating Frequency. Filter BW values can be easily calculated by direct scaling. See equation below for filter BW calculation:

$$BW_{\text{Operating Freq}} = BW_{@433.92MHz} * \frac{(\text{Operating Freq})}{433.92}$$

Eq. 6

It is very important to choose the filter setting that best fits the intended data rate to minimize data distortion.

Demod BW is set at 13000Hz @ 433.92MHz as default (assuming both SEL0 and SEL1 pins are floating). The low pass filter can be hardware set by external pins SEL0 and SEL1.

SEL0	SEL1	Demod BW (@ 434MHz)
0	0	1625Hz
1	0	3250Hz
0	1	6500Hz
1	1	13000Hz - default

Table 1. Demodulation BW Selection

Slicer and Slicing Level

The signal prior to slicer is still linear demodulated AM. Data slicer converts this signal into digital “1”s and “0”s by comparing with the threshold voltage built up on the CTH capacitor. This threshold is determined by detecting the positive and negative peaks of the data signal and storing the mean value. Slicing threshold is at 50%. After the slicer, the signal is now digital OOK data.

During long periods of “0”s or no data period, threshold voltage on the CTH capacitor may be very low. Large random noise spikes during this time may cause erroneous “1”s at DO pin.

AGC Comparator

The AGC comparator monitors the signal amplitude from the output of the programmable low-pass filter. When the output signal is less than 750mV, the threshold 1.5µA current is sourced into the external CAGC capacitor. When the output signal is greater than 750mV, a 15µA current sink discharges the CAGC capacitor. The voltage developed on the CAGC capacitor acts to adjust the gain of the mixer and the IF amplifier to compensate for RF input signal level variation.

Reference Control

There are two components in Reference and Control sub-block: 1) Reference Oscillator and 2) Control Logic through parallel Inputs: SEL0, SEL1, SHDN and IF_BW.

Reference Oscillator

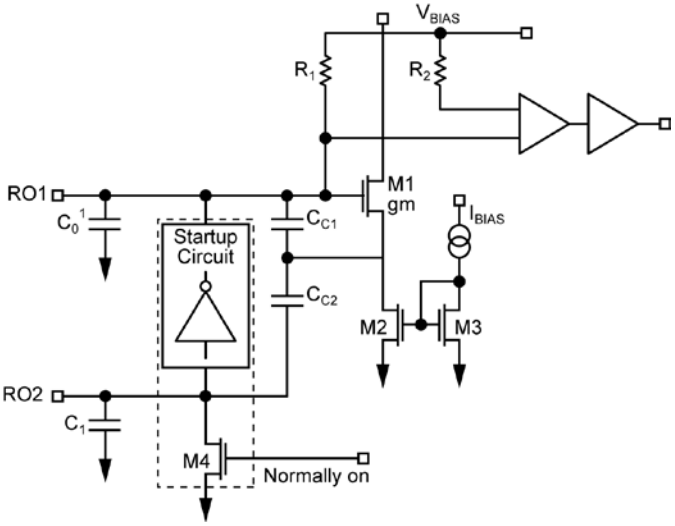


Figure 6. Reference Oscillator Circuit

The reference oscillator in the MICRF218 (Figure 6) uses a basic Colpitts crystal oscillator configuration with MOS transconductor to provide negative resistance. All capacitors shown in Figure 6 are integrated inside the MICRF218. R01 and R02 are external pins of MICRF218. User only needs to connect reference oscillation crystal.

See equation (1) and (2) to calculate reference oscillator crystal frequency for either narrow or wide bandwidth.

Crystal Parameters

To operate the MICRF218 with minimum offset, crystal frequencies should be specified with 10pF loading capacitance. Please contact Micrel RF Applications department for crystal parameters.

Application Information

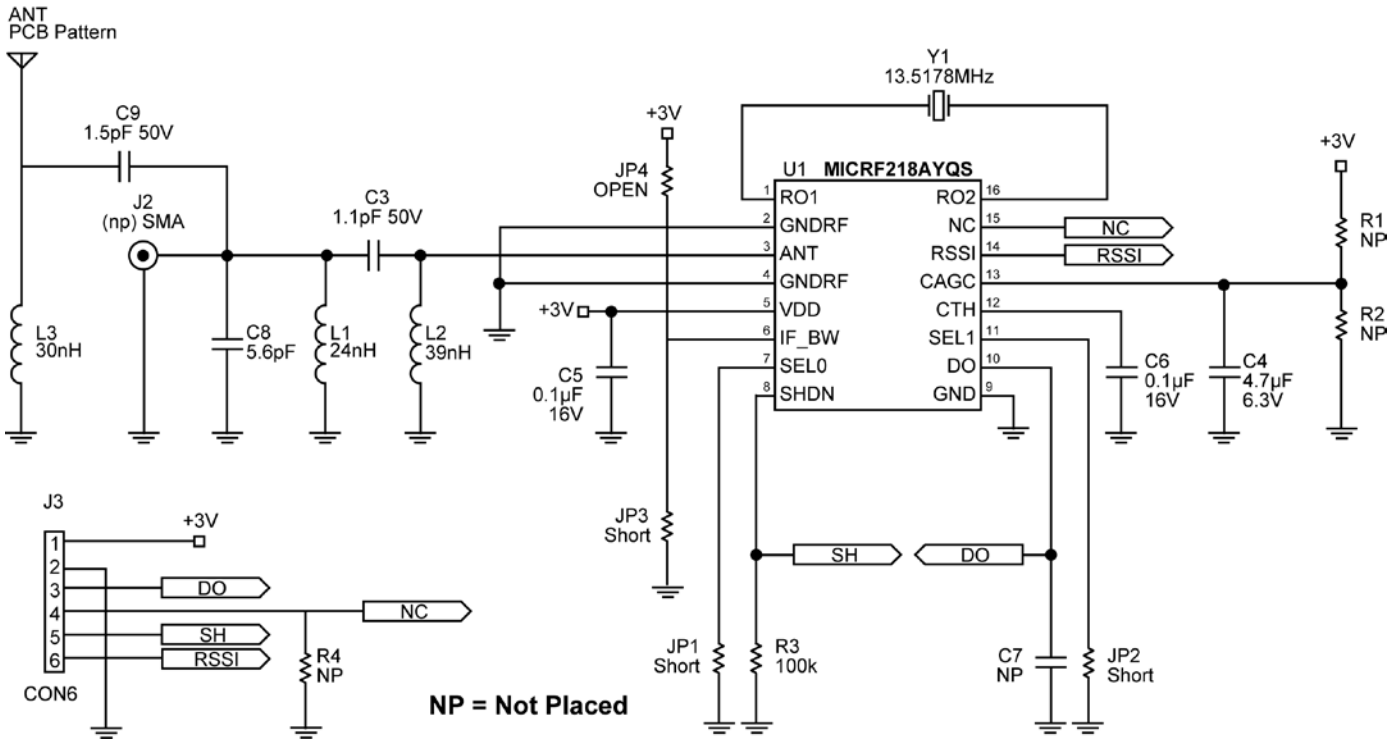


Figure 7. QR218HE1 Application Example, 433.92 MHz, Narrow Band

The MICRF218 can be fully tested by using one of many evaluation boards designed at Micrel for this device. As simple demonstrator, the QR218HE1 (Figure 7) offers a good start for most applications. It has a helical PCB antenna with its matching network, a bandpass-filter front-end as a pre-selector filter, matching network and the minimum components required to make the device work, which are a crystal, Cagc, and Cth capacitors.

The matching network of the helical PCB antenna (C9 and L3) can be removed and a whip antenna (ANT2) or a RF connector (J2) can be used instead. Figure 7 shows the entire schematic of it for 433.92MHz. Other frequencies can be used. Matching network values for other frequencies are listed in the tables below.

Capacitor C9 and inductor L3 are the passive elements for the helical PCB matching network. Tight tolerance is recommended for these devices, like 2% for the inductor and 0.1pF for the capacitor. PCB variations may require different component values and optimization.

Table 2 shows the matching elements for the device frequency range. For additional information look for Small PCB Antennas for Micrel RF Products application note.

Freq (MHz)	C9 (pF)	L3(nH)
315.0	**1.2**	75
390.0	**1.2**	43
418.0	**1.2**	36
433.92	1.5	30

Table 2. Matching Values for the Helical PCB Antenna

If whip antenna is used, remove C9 and place the whip antenna in the hole provided in the PCB. Also, RF signal can be injected there (add RF connector).

L1 and C8 form the pass-band-filter front-end. Its purpose is to attenuate undesired outside band noise which reduces the receiver performance. It is calculated by the parallel resonance equation:

$$f = \frac{1}{(2 * \pi \sqrt{L1 * C8})}$$

Table 3 shows the most used frequency values.

Freq (MHz)	C8 (pF)	L1(nH)
315.0	**6.8**	39
390.0	**6.8**	24
418.0	**6.0**	24
433.92	5.6	24

Table 3. Band-Pass-Filter Front-End Values

There is no need for the bandpass-filter front-end for applications where it is proven that the outside band noise does not cause a problem. The MICRF218 has image reject mixers which improve significantly the selectivity and rejection of outside band noise.

Capacitor C3 and inductor L2 form the L-shape matching network. The capacitor provides additional attenuation for low frequency outside band noise, and the inductor provides additional ESD protection for the antenna pin. Two methods can be used to find these values, which are matched close to 50Ω. One method is done by calculating the values using the equations below, and the other method uses a Smith chart. The latter is made easier by using software that plots the values of the components C8 and L1, like WinSmith by Noble Publishing.

To calculate the matching values, one needs to know the input impedance of the device. Table 4 4 shows the input impedance of the MICRF218 and suggested matching values for the most used frequencies. These suggested values may be different if the layout is not exactly the same as the one made here.

Freq (MHz)	C3 (pF)	L2(nH)	Z device (Ω)
315.0	1.5	68	16.3 -j210.8
390.0	1.2	47	8.26 – j163.9
418.0	1.2	43	11.1 – j161.9
433.92	1.1	39	9.54 – j152.3

Table 4. Matching values for the most used frequencies

For the frequency of 433.92MHz, the input impedance is Z = 9.54 – j152.3Ω. The matching components are calculated by:

Equivalent parallel = B = 1/Z = 0.410 + j6.54 msiemens

Rp = 1 / Re (B); Xp = 1 / Im (B)

Rp = 2.44kΩ; Xp = 345.8Ω

Q = SQRT (Rp/50 + 1)

Q = 7.06

Xm = Rp / Q

Xm = 345.8Ω

Resonance Method For L-shape Matching Network:

Lc = Xp / (2×Pi×f); Lp = Xm / (2×Pi×f)

L2 = (Lc×Lp) / (Lc + Lp); C3 = 1 / (2×Pi×f×Xm)

L2 = 38.9nH

C3 = 1.06pF

Doing the same calculation example with the Smith Chart, it would appear as follows,

First, the input impedance of the device is plotted, (Z = 9.54 – j152)Ω @ 433.92MHz.(Figure 8).

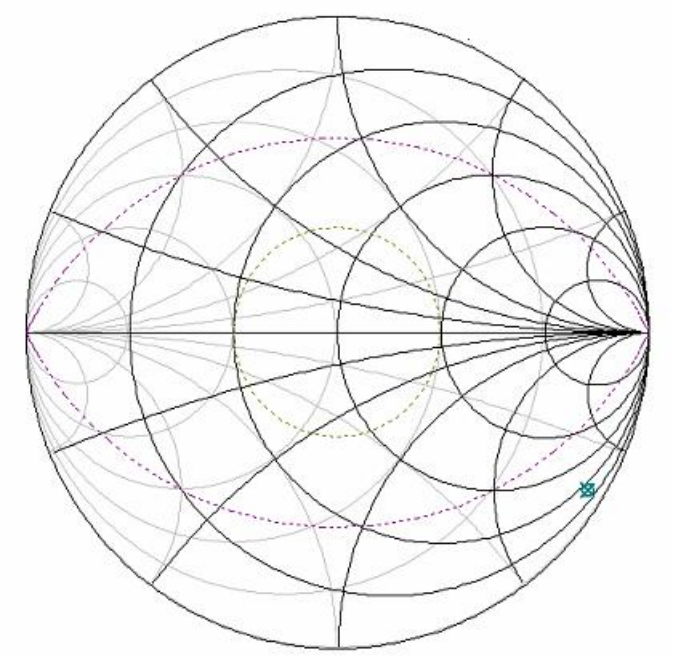


Figure 8. Device's Input Impedance, Z = 9.54-j152Ω

Second, the shunt inductor (39nH) and the series capacitor (1.1pF) for the desired input impedance are plotted (Figure 9). One can see the matching leading to the center of the Smith Chart or close to 50Ω.

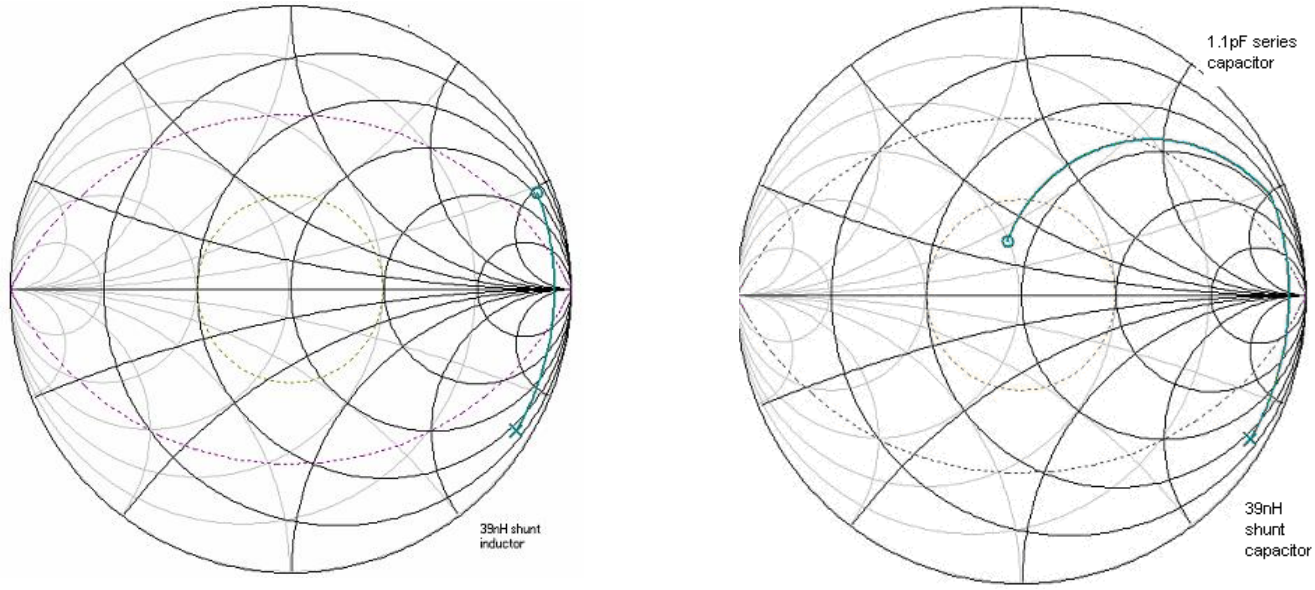


Figure 9. Plotting the Shunt Inductor and Series Capacitor

Crystal Y1 may be either SMT or leaded. It is the reference clock for all the device internal circuits. Crystal characteristics of 10pF load capacitance, 30ppm, ESR < 50Ω, -40ºC to +85ºC temperature range are desired. Table 5 shows the crystal frequencies for WB or NB and one of Micrel's approved crystal manufacturers (www.hib.com.br).

REFOSC (MHz)	Carrier (MHz)	HIB Part Number
9.813135, NB	315	SA-9.813135-F-10-G-30-30-X
12.149596, NB	390.0	SA-12.149596-F-10-G-30-30-X
13.021874, NB	418.0	SA-13.021874-F-10-G-30-30-X
13.517827, NB	433.92	SA-13.517827-F-10-G-30-30-X
9.788232, WB	315	SA-9.788232-F-10-G-30-30-X
12.118764, WB	390.0	SA-12.118764-F-10-G-30-30-X
12.988829, WB	418.0	SA-12.988829-F-10-G-30-30-X
13.483523, WB	433.92	SA-13.483523-F-10-G-30-30-X

Table 5. Crystal Frequency and Vendor Part Number

The oscillator of the MICRF218 is Colpitts in configuration. It is very sensitive to stray capacitance loads. Thus, very good care must be taken when laying out the printed circuit board. Avoid long traces and ground plane on the top layer close to the REFOSC pins RO1 and RO2. When care is not taken in the layout, and crystals from other vendors are used, the oscillator may take longer times to start as well as the time to good data in the DO pin to show up. In some cases, if the stray capacitance is too high (> 20pF), the oscillator may not start at all.

Refer to Equations 1 and 2 for crystal frequency calculations. The local oscillator is low side injection (32 × 13.51783MHz = 432.571MHz), that is, its frequency is below the RF carrier frequency and the image frequency is below the LO frequency. See Figure 10. The product of the incoming RF signal and local oscillator signal will yield the IF frequency, which will be demodulated by the detector of the device.

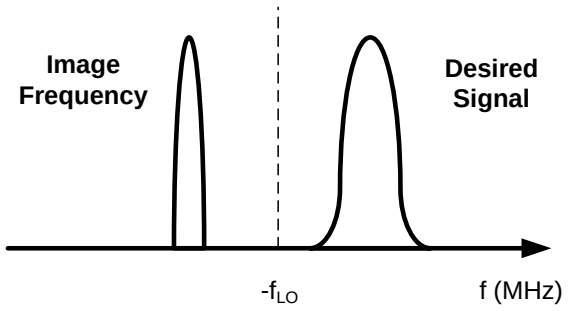


Figure 10. Low Side Injection Local Oscillator

Narrow and Wide Band Crystal Part Numbers,

WB = IF Wide Band, NB = IF Narrow Band

JP1 and JP2 are the bandwidth selection for the demodulator bandwidth. To set it correctly, it is necessary to know the shortest pulse width of the encoded data sent in the transmitter. Similar to the example of the data profile in the Figure 11 below, PW2 is shorter than PW1, so PW2 should be used for the demodulator bandwidth calculation which is found by 0.65/shortest pulse width. After this value is found, the setting should be done according to Table 6. For example, if the pulse period is 100µsec, 50% duty cycle, the pulse width will be 50µsec (PW = (100µsec × 50%) / 100). So, a bandwidth of 13kHz would be necessary (0.65 / 50µsec). However, if this data stream had a pulse period with 20% duty cycle, then the bandwidth required would be 32.5kHz (0.65 / 20µsec), which exceeds the maximum bandwidth of the demodulator circuit. If one tries to exceed the maximum bandwidth, the pulse would appear stretched or wider.

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	Shortest Pulse (µsec)	Maximum baud rate for 50% Duty Cycle (hertz)
Short	Short	1625	400	1250
Open	Short	3250	200	2500
Short	Open	6500	100	5000
Open	Open	13000	50	10000

Table 6. JP1 and JP2 setting, 433.92 MHz

Other frequencies will have different demodulator bandwidth limits, which are derived from the reference oscillator frequency. Table 7 and 8 below shows the limits for the other two most used frequencies.

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	Shortest Pulse (µsec)	Maximum baud rate for 50% Duty Cycle (hertz)
Short	Short	1565	416	1204
Open	Short	3130	208	2408
Short	Open	6261	104	4816
Open	Open	12523	52	9633

Table 7. JP1 and JP2 setting, 418.0 MHz

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	Shortest Pulse (µsec)	Maximum baud rate for 50% Duty Cycle (Hertz)
Short	Short	1460	445	1123
Open	Short	2921	223	2246
Short	Open	5842	111	4493
Open	Open	11684	56	8987

Table 8. JP1 and JP2 setting, 390.0 MHz

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	Shortest Pulse (µsec)	Maximum baud rate for 50% Duty Cycle (Hertz)
Short	Short	1180	551	908
Open	Short	2360	275	1815
Short	Open	4720	138	3631
Open	Open	9400	69	7230

Table 9. JP1 and JP2 setting, 315.0 MHz.

Selection of CTH and CAGC Capacitors

Capacitors C6 and C4, Cth and Cagc respectively provide time-based reference for the data pattern received. These capacitors are selected according to data profile, pulse duty cycle, dead time between two received data packets, and if the data pattern has or does not have a preamble. See Figure 11 for an example of a data profile.

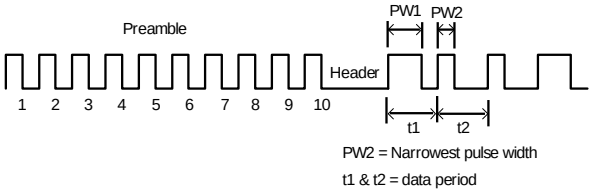


Figure 11. Example of a Data Profile

For best results, the capacitors should always be optimized for the data pattern used. As the baud rate increases, the capacitor values decrease. Table 10 shows suggested values for Manchester Encoded data, 50% duty cycle.

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	Cth (C6)	Cagc (Cagc)
Short	Short	1625	100nF	4.7µF
Open	Short	3250	47nF	2.2µF
Short	Open	6500	22nF	1µF
Open	Open	13000	10nF	0.47µF

Table 10. Suggested Cth and Cagc Values.

Other components used include C5, which is a decoupling capacitor for the Vdd line; R4 reserved for future use and not needed for the evaluation board; R3 for the shutdown pin (SHDN = 0, device is operation), which can be removed if that pin is connected to a microcontroller or an external switch, and R1 and R2 which form a voltage divider for the AGC pin. One can force a voltage in this AGC pin to purposely decrease the device sensitivity. Special care is needed when doing this operation, as an external control of the AGC voltage may vary from lot to lot and may not work the same for several devices.

DO, RSSI and Shutdown Functions

Three other pins are worthy of comment. They are the DO, RSSI, and shut down pins. The DO pin has a driving capability of 0.6mA. This drive current is good enough for most of the logic family ICs in the market today. The RSSI pin provides a transfer function of the RF signal intensity vs. voltage. It is very useful to determine the signal to noise ratio of the RF link, crude range estimate from the transmitter source and AM demodulation, which requires a low Cagc capacitor value.

Shut Down Control

The shut down pin (SHDN) is useful to save energy. When its level close to Vdd (SHDN = 1), the device is not in operation. Its DC current consumption is less than 1µA (do not forget to remove R3). When toggling from high to low, there will be a time required for the device to come to steady state mode, and a time for data to show up in the DO pin. This time will be dependent upon many things such as temperature, choice of crystal used, and if the there is an external oscillator with faster startup time. Normally, with the crystal vendors suggested, the data will show up in the DO pin around 1msec time, and 2msec over the temperature range of the device. See Figures 12.

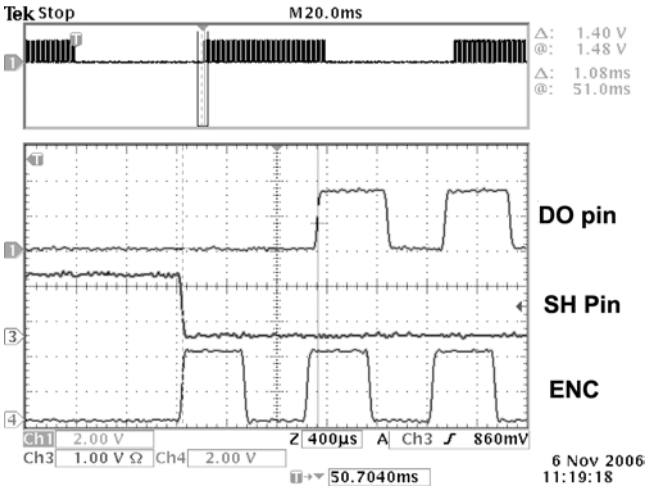
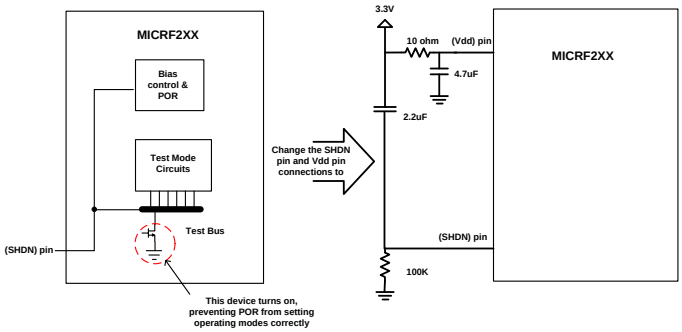


Figure 12. Time-to-Good Data After Shut Down Cycle, Room Temperature

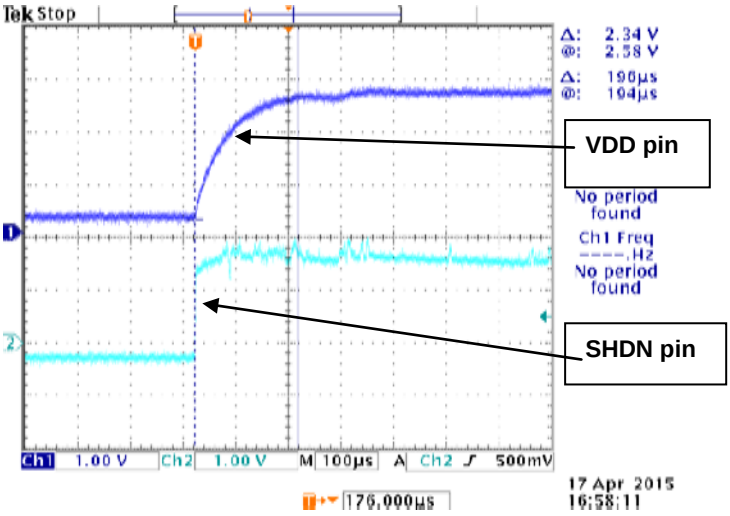
Important Note

A few customers have reported that some MICRF218 receiver do not start up correctly. When the issue occurs, DO either chatters or stays at low voltage level. An unusual operating current is observed and the part cannot receive or demodulate data even when a strong OOK signal is present.

Micrel has confirmed that this is the symptom of incorrect power on reset (POR) of internal register bits. The MICRF218 is designed to start up in shutdown mode (SHDN pin must be in logic high during VDD ramp up). When the SHDN pin is tied to GND, and if the supply is ramped up slowly, a “test bus pull down” circuit may be activated. Once the chip enters this mode, the POR does not have the chance to set register bits (and hence operating modes) correctly. The test bus pull down acts on the SHDN pin, and can be illustrated in the following diagram.



To prevent the erroneous startup, a simple RC network is recommended. The 10Ω resistor and the 4.7µF capacitor provide a delay of about 200µs between VDD and SHDN during power up, thus ensuring the part enters the shutdown stage before the part is actually turned on. The 2.2µF capacitor bootstraps the voltage on SHDN, ensuring that SHDN voltage leads the supply voltage on VDD during power up. This gives the POR circuit time to set internal register bits. The SHDN pin can be brought low to turn the chip on once the initialization is completed. The 2.2µF and 100kΩ network form a RC delay of about 200ms before the SHDN pin is brought to low again. The 100kΩ resistor discharges the SHDN pin to turn the chip on.



The suggestion provided above will generally serve to prevent the startup issue from happening to the MICRF218 series ASK receiver. However, exact values of the RC network depend on the ramp rate of the supply voltage, and should be determined on a case-by-case basis.

PCB Considerations and Layout

Figures 14 to 17 show top, bottom and silkscreen layers of printed circuit board for the QR218HE1 board. Gerber files are provided and are downloadable from Micrel Website: www.micrel.com, to fabricate this board. Keep traces as short as possible. Long traces will alter the matching network, and the values suggested will not be valid. Suggested Matching Values may vary due to PCB variations. A PCB trace 100 mills (2.5mm) long has about 1.1nH inductance. Optimization should always be done with exhaustive range tests. Make individual ground connections to the ground plane with a via for each ground connection. Do not share vias with ground connections. Each ground connection = 1 via or more vias. Ground plane must be solid and possibly without interruptions. Avoid ground plane on top next to the matching elements. It normally adds additional stray capacitance which changes the matching. Do not use phenolic material. Use only FR4 or better materials. Phenolic material is conductive above 200MHz. RF path should be as straight as possible avoiding loops and unnecessary turns. Separate ground and Vdd lines from other circuits (microcontroller, etc). Known sources of noise should be laid out as far as possible from the RF circuits. Avoid thick traces, the higher the frequency, the thinner the trace should be in order to minimize losses in the RF path.

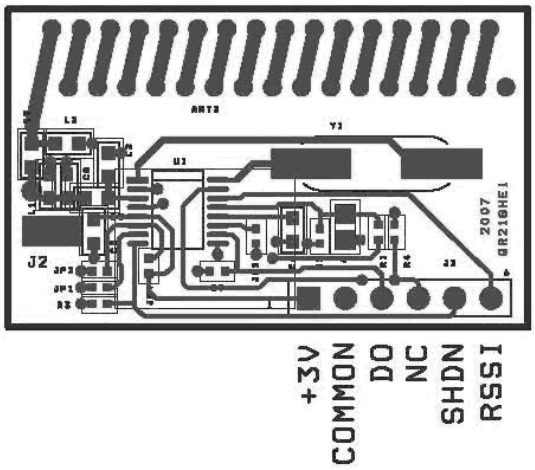


Figure 14. QR218HE1 Top Layer.

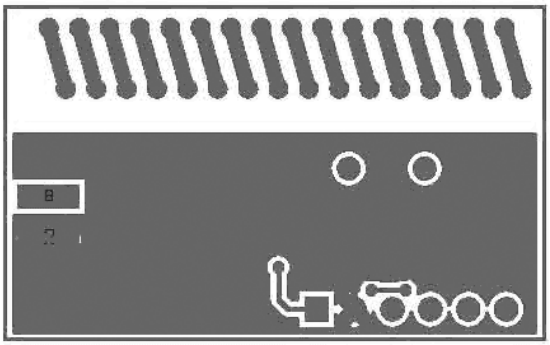


Figure15. QR218HE1 Bottom Layer, Mirror Image.

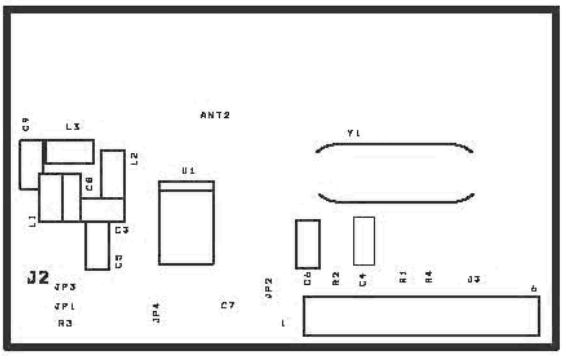


Figure 16. QR218HE1 Top Silkscreen Layer.

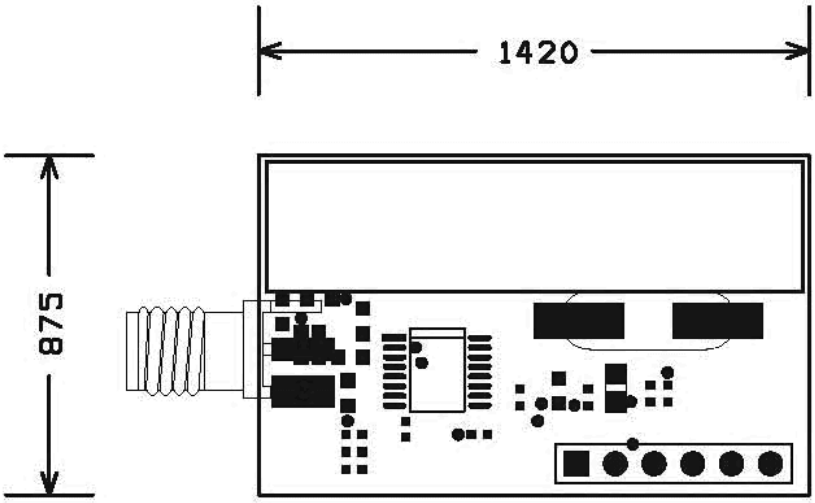


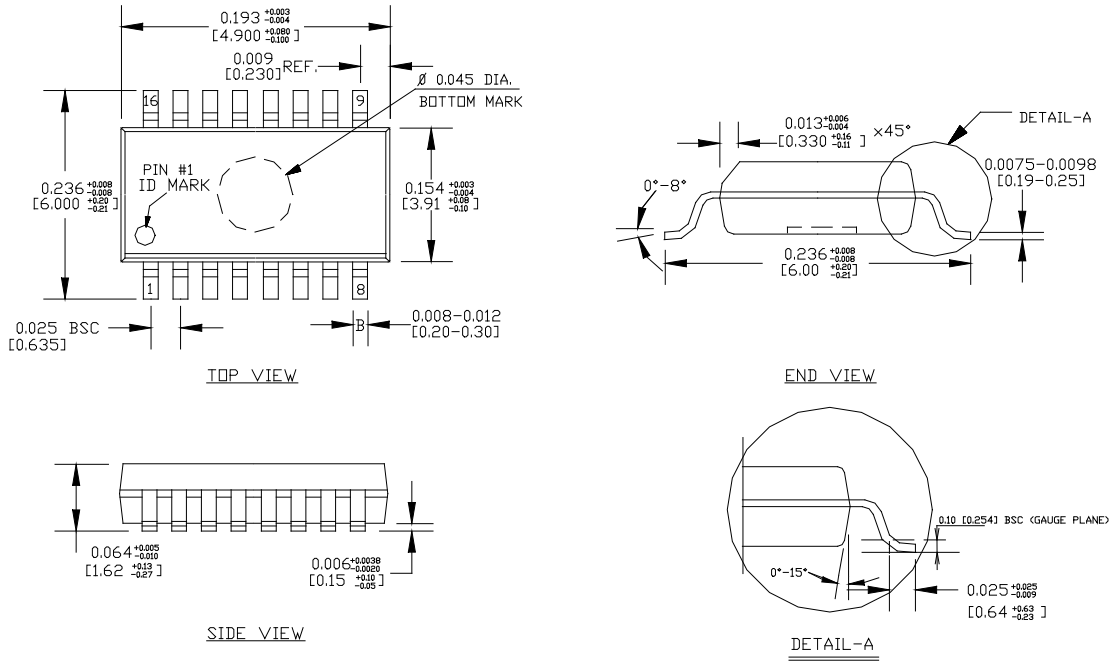
Figure 17. QR218HE1 Dimensions.

QR218HE1 Bill of Materials, 433.92 MHz

Item	Part Number	Manufacturer	Description	Qty.
ANT1			Helical PCB Antenna Pattern	1
ANT2			(np)50-ohm Ant 168mm 20 AWG, rigid wire	0
C9		Murata	1.5pF , 0402/0603	1
C4		Murata / Vishay	4.7µF, 0805	1
C3		Murata/Vishay	1.1pF, 0402/0603	
C6,C5		Murata / Vishay	0.1µF, 0402/0603	2
C8		Murata	5.6pF, 0402/0603	1
JP1,JP 2, JP3		Vishay	short, 0402, 0Ω resistor	2
JP4			(np) not placed	0
J2			(np) not placed	0
J3			CON6	1
L1		Coilcraft / Murata / ACT1	24nH 5%, 0402/0603	1
L2		Coilcraft / Murata / ACT1	39nH 5%, 0402/0603	1
L3		Coilcraft / Murata / ACT1	30nH 2%, 0402/0603	1
R1,R2, R4			(np) 0402, not placed	0
R3		Vishay	100kΩ , 0402	1
Y1	HCM49	www.hib.com.br	(np)13.51783MHz Crystal	0
Y1A	HC49/US	www.hib.com.br	13.51783MHz Crystal	1
U1	**MICRF218AYQS**	**Micrel, Inc.**	**3.3V, 315/433MHz Wide-IF Bandwidth ASK Receiver**	**1**

Table 11. QR218HE1 Bill of Materials, 433.92 MHz, Narrow Band.

Package Information and Recommended Land Pattern(1)



NOTE:
1. ALL DIMENSIONS ARE IN INCHES [MM].
2. LEAD COPLANARITY SHOULD BE 0.004" [0.10 mm] MAX.
3. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTER OF PACKAGE TO BE 0.004" [0.10 mm].
4. THE LEAD WIDTH, B TO BE DETERMINED AT .0075 [0.19 mm] FROM THE LEAD TIP.
5. BOTTOM MARK IS OPTIONAL, IT MAY NOT APPEAR ON THE ACTUAL UNITS.

QSOP16 Package Type (AQS16)

Note:

1. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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