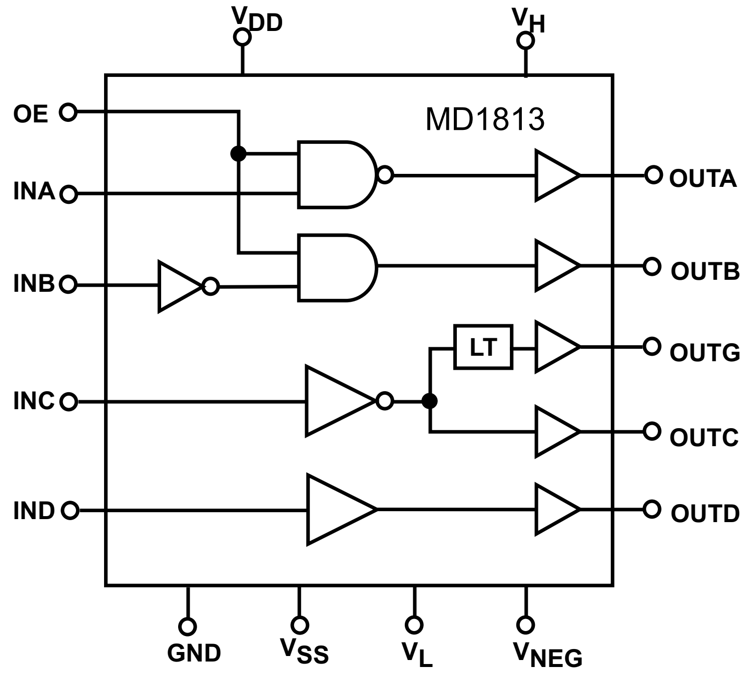
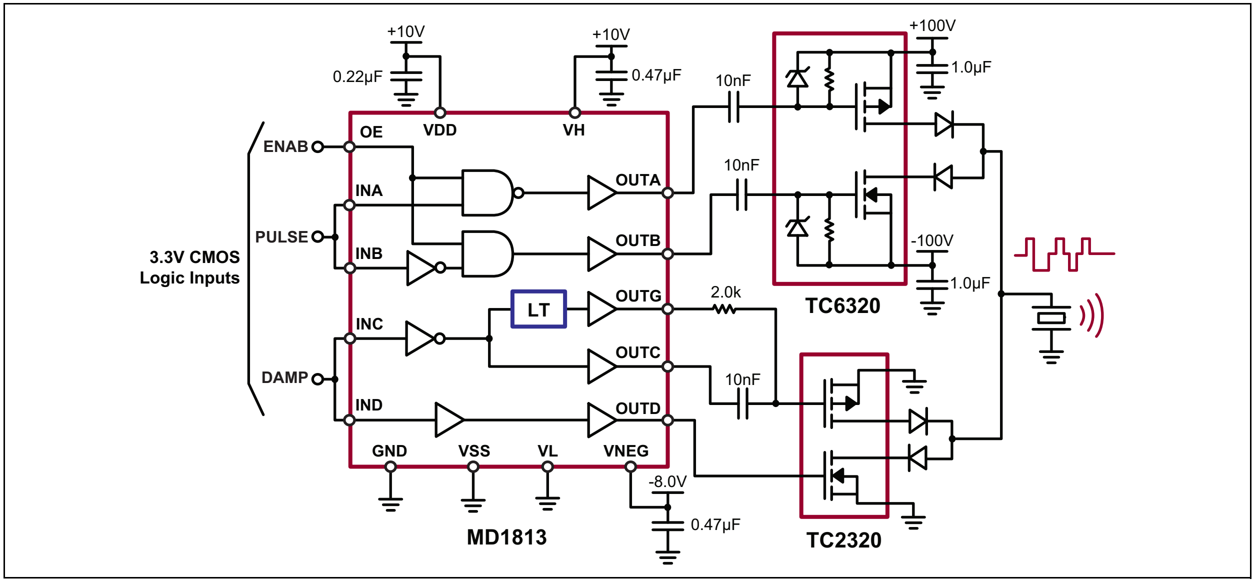
Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage, $V_{DD}-V_{SS}$	–0.5V to +13.5V
Output High Supply Voltage, V_H	V_L–0.5V to V_{DD} +0.5V
Output Low Supply Voltage, V_L	V_{SS}–0.5V to V_H+0.5V
Low-side Supply Voltage, V_{SS}	–7V to +0.5V
Supply Voltage, $V_{DD}-V_{NEG}$	–0.5V to +20V
Negative Supply Voltage, $V_{NEG}-V_{SS}$	V_{SS}–10V to V_{SS} +0.5V
Logic Input Levels	V_{SS}–0.5V to GND +7V
Maximum Junction Temperature, T_J	+125°C
Operating Ambient Temperature, T_A	–20°C to +85°C
Storage Temperature, T_S	–65°C to +150°C
Power Dissipation	2.2W
ESD Rating (**Note 1**)	ESD Sensitive

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Device is ESD sensitive. Handling precautions are recommended.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $V_H = V_{DD}$ = 12V, $V_L = V_{SS}$ = GND = 0V, V_{NEG} = –6V, V_{OE} = 3.3V and T_A = 25°C

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage		$V_{DD}-V_{SS}$	4.5	—	13	V	2.5V ≤ V_{DD} ≤ 13V
Supply Voltage		$V_{DD}-V_{NEG}$	—	—	18	V	
Low-side Supply Voltage		V_{SS}	–5.5	—	0	V	
Output High Supply Voltage		V_H	V_{SS} +2	—	V_{DD}	V	
Output Low Supply Voltage		V_L	V_{SS}	—	V_{DD}–2	V	
Negative Supply Voltage		V_{NEG}	–9	—	V_{SS}–2	V	May be connected to V_{SS} if OUTG is not used.
V_{DD} Quiescent Current		I_{DDQ}	—	1.5	—	mA	No input transitions, OE = 1
V_H Quiescent Current		I_{HQ}	—	—	10	μA	
V_{NEG} Quiescent Current		I_{NEGQ}	—	150	—	μA	
V_{DD} Average Current		I_{DD}	—	7	—	mA	One channel on at 5 MHz, no load
V_H Average Current		I_H	—	22	—	mA	
V_{NEG} Average Current		I_{NEG}	—	1.5	—	mA	
Input Logic Voltage High		V_{IH}	V_{OE}–0.3	—	5	V	For logic inputs INA, INB, INC and IND
Input logic Voltage Low		V_{IL}	0	—	0.3	V	
Input Logic Current High		I_{IH}	—	—	1	μA	
Input Logic Current Low		I_{IL}	—	—	1	μA	
OE Input Logic Voltage High		V_{IH}	1.7	—	5	V	For logic input OE
OE Input Logic Voltage Low		V_{IL}	0	—	0.3	V	
OE Input Resistance		R_{IN}	10	20	30	kΩ	
Logic Input Capacitance		C_{IN}	—	5	10	pF	
Output Sink Resistance	OUTA-D	R_{SINK}	—	—	12.5	Ω	I_{SINK} = 50 mA
	OUTG		—	—	200	Ω	I_{SINK} = 5 mA
Output Source Resistance	OUTA-D	R_{SOURCE}	—	—	12.5	Ω	I_{SOURCE} = 50 mA
	OUTG		—	—	200	Ω	I_{SOURCE} = 5 mA

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: $V_H = V_{DD} = 12V$, $V_L = V_{SS} = GND = 0V$, $V_{NEG} = –6V$, $V_{OE} = 3.3V$ and $T_A = 25°C$

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Peak Output Sink Current	I_{SINK}	—	2	—	A	
Peak Output Source Current	I_{SOURCE}	—	2	—	A	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $V_H = V_{DD} = 12V$, $V_L = V_{SS} = GND = 0V$, $V_{NEG} = –6V$, $V_{OE} = 3.3V$ and $T_A = 25°C$

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input or OE Rise and Fall Time	t_{irf}	—	—	10	ns	Logic input edge speed requirement
Propagation Delay INC to OUTG	t_{PCG}	—	40	—	ns	10 MΩ load to GND
Propagation Delay when Output is from Low to High for OUTA-D	t_{PLH}	—	7	—	ns	C_{LOAD} = 1000 pF, input signal rise/fall time of 2 ns (See **Timing Diagram**.)
Propagation Delay when Output is from High to Low for OUTA-D	t_{PHL}	—	7	—	ns	
Output Rise Time	t_r	—	6	—	ns	
Output Fall Time	t_f	—	6	—	ns	
Rise and Fall Time Matching	$\mid t_r – t_f \mid$	—	1	—	ns	For each channel
Propagation Low-to-high and High-to-low Matching	$\mid t_{PLH} – t_{PHL} \mid$	—	1	—	ns	
Propagation Delay Matching	Δt_{dm}	—	±2	—	ns	Device-to-device delay match
Output Enable Time	t_{POE}	—	9	—	ns	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Maximum Junction Temperature	T_J	—	—	+125	°C	
Operating Ambient Temperature	T_A	–20	—	+85	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
16-lead QFN	θ_{JA}	—	25	—	°C/W	**Note 1**

Note 1: 1 oz. 4-layer 3” x 4” PCB

Timing Diagram

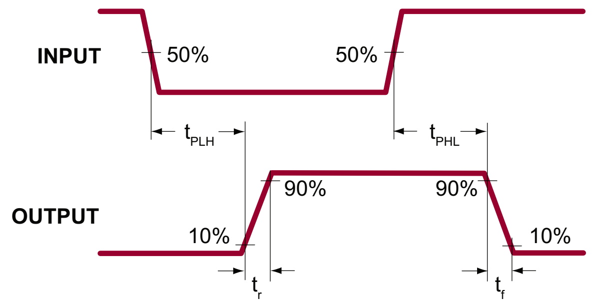


TABLE 1-1: TRUTH FUNCTION TABLE

Logic Inputs			Outputs		
OE	**INA**	**INB**	**OUTA**		**OUTB**
H	L	L	V_H		V_H
H	L	H	V_H		V_L
H	H	L	V_L		V_H
H	H	H	V_L		V_L
L	X	X	V_H		V_L
OE (1)	**INC**	**IND**	**OUTC**	**OUTG**	**OUTD** (2)
—	L	L	V_H	V_{SS}	V_L
—	L	H	V_H	V_{SS}	V_H
—	H	L	V_L	V_{NEG}	V_L
—	H	H	V_L	V_{NEG}	V_H

Note 1: No control to OUTG, OUTC or OUTD

2: OUTD is non-inverting output.

2.0 PIN DESCRIPTION

The details on the pins of MD1813 are listed on Table 2-1. See **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	INB	Logic input. Controls OUTB when OE is high.
2	VL	Supply voltage for N-channel output stage
3	GND	Device ground
4	VNEG	Supply voltage for the auxiliary gate drive. (**Note 1**)
5	INC	Logic input. Controls OUTC. Not controlled by OE.
6	IND	Logic input. Controls OUTD. Not controlled by OE.
7	VSS	Supply voltage for low-side analog, level shifter and gate drive circuit
8	OUTD	Output driver
9	OUTC	Output driver
10	OUTG	Not controlled by OE
11	VH	Supply voltage for P-channel output stage
12	OUTB	Output driver
13	OUTA	Output driver
14	VDD	Supply voltage for high-side analog, level shifter and gate drive circuit
15	INA	Logic input. Controls OUTA when OE is high.
16	OE	Output enable logic input (See Figure 3-1.)

Note 1: Thermal pad and pin 4, VNEG must be connected externally.

3.0 APPLICATION INFORMATION

For proper operation of the MD1813, low-inductance bypass capacitors should be used in the various supply pins. The GND pin should be connected to the logic ground. The INA, INB, INC, IND and OE pins should be connected to a logic source with a swing of GND to V_{CC}, where V_{CC} is 1.8V to 5V. Good trace practices should be followed corresponding to the desired operating speed. The internal circuitry of the MD1813 is capable of operating up to 100 MHz, with the primary speed limitation being the loading effects of the load capacitance. Because of this speed and the high transient currents due to the capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the V_{SS} and V_L pins should have low-inductance feed-through connections directly to a ground plane. If these voltages are not zero, they need bypass capacitors in a manner similar to the positive power supplies. The power connections V_{DD} should have a ceramic bypass capacitor to the ground plane with short leads and decoupling components to prevent resonance in the power leads.

Output drivers, OUTA and OUTC drive the gate of an external P-channel MOSFET, while output drivers OUTB and OUTD drive the gate of an external N-channel MOSFET, and they all swing from V_H to V_L. The auxiliary output drive, OUTG, swings from V_{SS} to V_{NEG}, and drives the external P-channel MOSFET as negative bias via a 2 kΩ series resistor.

The voltages of V_H and V_L decide the output signal levels. These two pins can draw fast transient currents of up to 2A, so they should be provided with an appropriate bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1 µF may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead going to the capacitor. Pay particular attention to minimizing trace lengths, current loop area, and using sufficient trace width to reduce inductance. Surface-mount components are highly recommended. Since the output impedance of this driver is very low, in some cases it may be desirable to add a small series resistor in series with the output signal to obtain better waveform transitions at the load terminals. This will reduce the output voltage slew rate at the terminals of a capacitive load.

The OE pin sets the threshold level of logic for inputs $(V_{OE} + V_{GND})/2$. When OE is low, OUTA is at V_H. OUTB is at V_L, regardless of the inputs INA and INB. This pin will not control OUTC, OUTD or OUTG.

Ensure that parasitic couplings are minimized from the output to the input signal terminals. The parasitic feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.8V, even small coupled voltages may cause problems. The use of a solid ground plane and good power and signal layout practices will prevent this problem. Make sure that a circulating ground return current from a capacitive load will not react with common inductance to cause noise voltages in the input logic circuitry. Best timing performance is obtained for OUTC when the voltage of $V_{SS} - V_{NEG} = V_H - V_L$. When input logic is high, output will swing to V_L, and when input logic is low, output will swing to V_H. All inputs must be kept low until the device is powered up.

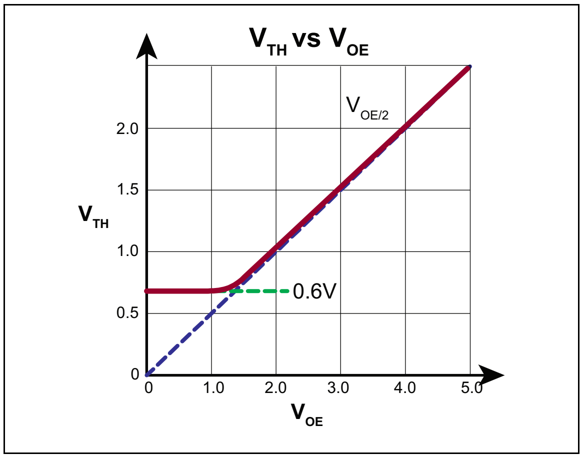


FIGURE 3-1: V_{TH}/V_{OE} Curve.

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

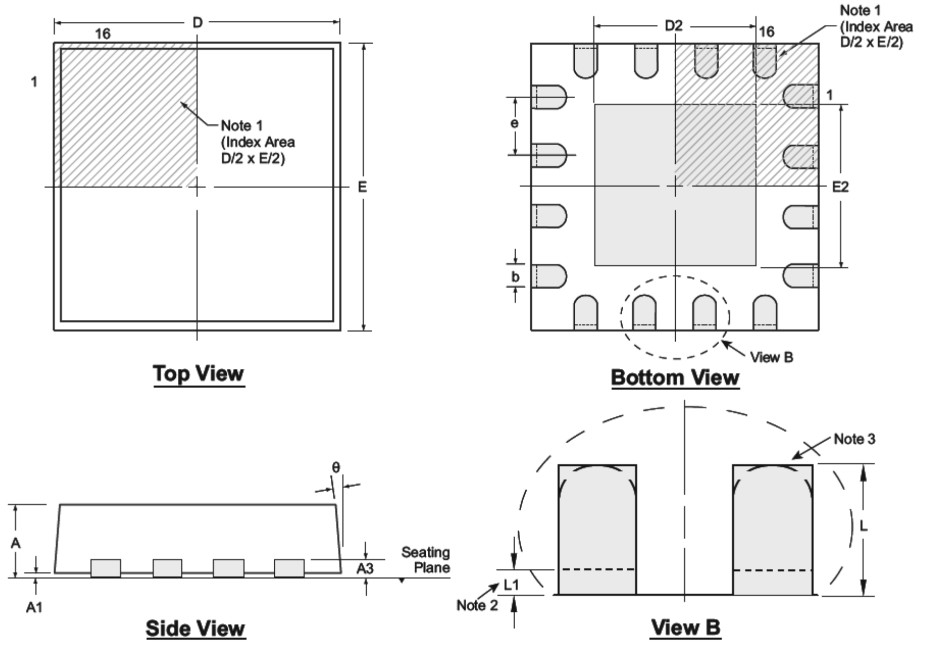
16-lead QFN	Example
XXXXXX XXXXXX e3YYWW NNN	MD 1813K6 e31714 895

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

16-Lead QFN Package Outline (K6)

4.00x4.00mm body, 1.00mm height (max), 0.65mm pitch



Top View

Bottom View

Side View

View B

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.25	3.85*	2.50	3.85*	2.50	0.65 BSC	0.30†	0.00	0°
	NOM	0.90	0.02		0.30	4.00	2.65	4.00	2.65		0.40†	-	-
	MAX	1.00	0.05		0.35	4.15*	2.80	4.15*	2.80		0.50†	0.15	14°

JEDEC Registration MO-220, Variation VGGC-2, Issue K, June 2006.

** This dimension is not specified in the JEDEC drawing.*

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (May 2017)

- Converted Supertex Doc# DSFP-MD1813 to Microchip DS20005747A
- Changed the package marking format
- Changed the quantity of the 16-lead QFN K6 package from 3000/Reel to 3300/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	**Package Options**		**Environmental**		**Media Type**

Device:	MD1813	=	High-Speed Quad-MOSFET Driver
Package:	K6	=	16-lead QFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	3300/Reel for a K6 Package

Example:

a) MD1813K6-G:	High-Speed Quad-MOSFET Driver, 16-lead QFN, 3300/Reel

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