NOTES:

1.0 DEVICE OVERVIEW

This document contains device specific information for the following device:

- MCP2150

The MCP2150 is a cost effective, low pin count (18-pin), easy to use device for implementing IrDA standard wireless connectivity. The MCP2150 provides support for the IrDA standard protocol “stack” plus bit encoding/decoding.

The serial interface baud rates are user selectable to one of four IrDA standard baud rates between 9600 baud and 115.2 kbaud (9600, 19200, 57600, 115200). The IR baud rates are user selectable to one of five IrDA standard baud rates between 9600 baud and 115.2 kbaud (9600, 19200, 37400, 57600, 115200). The serial interface baud rate will be specified by the BAUD1:BAUD0 pins, while the IR baud rate is specified by the Primary Device (during Discover phase). This means that the baud rates do not need to be the same. The MCP2150 operates in Data Terminal Equipment (DTE) applications and sits between a UART and an infrared optical transceiver.

The MCP2150 encodes an asynchronous serial data stream, converting each data bit to the corresponding infrared (IR) formatted pulse. IR pulses received are decoded and then handled by the protocol handler state machine. The protocol handler sends the appropriate data bytes to the Host Controller in UART formatted serial data.

The MCP2150 supports “point-to-point” applications. That is, one Primary device and one Secondary device. The MCP2150 operates as a Secondary device. It does not support “multi-point” applications.

Sending data using IR light requires some hardware and the use of specialized communication protocols. These protocol and hardware requirements are described, in detail, by the IrDA standard specifications. The encoding/decoding functionality of the MCP2150 is designed to be compatible with the physical layer component of the IrDA standard. This part of the standard is often referred to as “IrPHY”.

The complete IrDA standard specifications are available for download from the IrDA website (www.IrDA.org).

1.1 Applications

The MCP2150 Infrared Communications Controller supporting the IrDA standard provides embedded system designers the easiest way to implement IrDA standard wireless connectivity. Figure 1-1 shows a typical application block diagram. Table 1-2 shows the pin definitions.

TABLE 1-1: OVERVIEW OF FEATURES

Features	MCP2150
Serial Communications	UART, IR
Baud Rate Selection	Hardware
Low Power Mode	Yes
Resets (and Delays)	$\overline{\text{RESET}}$, POR (PWRT and OST)
Packages	18-pin DIP, SOIC, 20-pin SSOP

Infrared communication is a wireless two-way data connection, using infrared light generated by low-cost transceiver signaling technology. This provides reliable communication between two devices.

Infrared technology offers:

- Universal standard for connecting portable computing devices
- Easy, effortless implementation
- Economical alternative to other connectivity solutions
- Reliable, high-speed connection
- Safe to use in any environment (can even be used during air travel)
- Eliminates the hassle of cables
- Allows PCs and other electronic devices (such as PDAs, cell phones, etc.) to communicate with each other
- Enhances mobility by allowing users to easily connect

The MCP2150 allows the easy addition of IrDA standard wireless connectivity to any embedded application that uses serial data. Figure 1-1 shows typical implementation of the MCP2150 in an embedded system.

The IrDA protocols for printer support are not included in the IrCOMM 9-wire “cooked” service class.

FIGURE 1-1: SYSTEM BLOCK DIAGRAM

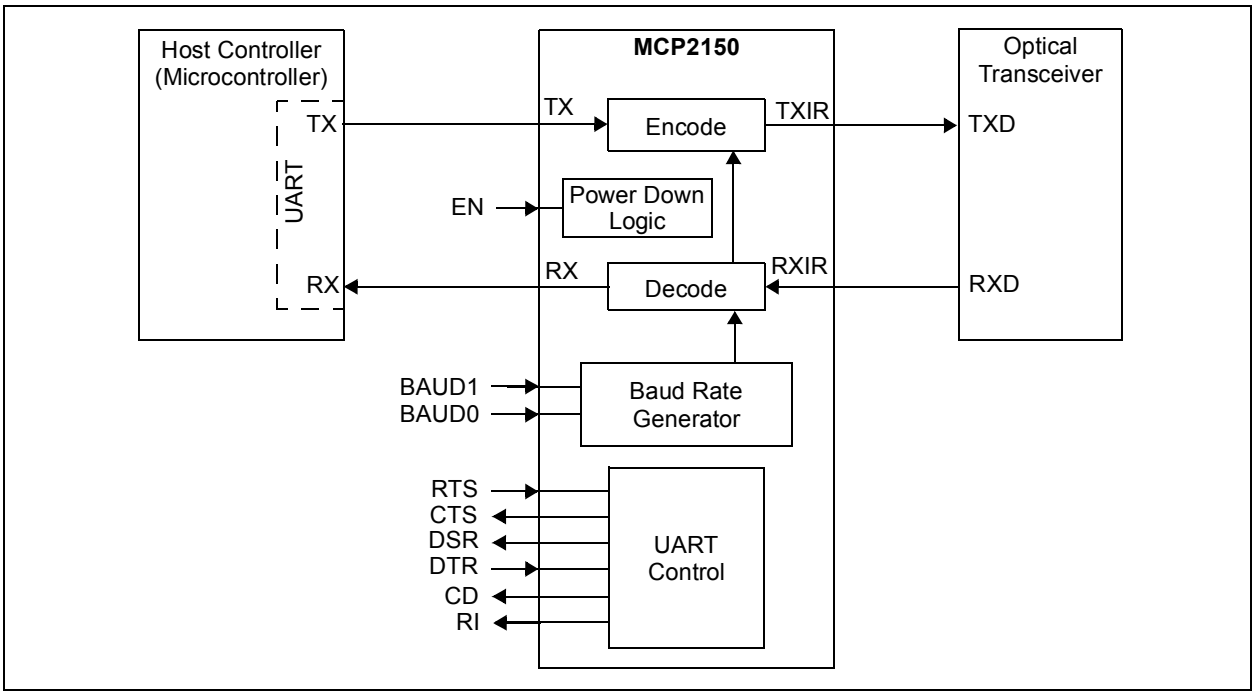


TABLE 1-2: PIN DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	SOIC	SSOP			
BAUD0	1	1	1	I	ST	BAUD1:BAUD0 specify the baud rate of the device.
TXIR	2	2	2	O	—	Asynchronous transmit to Infrared transceiver.
RXIR	3	3	3	I	ST	Asynchronous receive from Infrared transceiver.
$\overline{\text{RESET}}$	4	4	4	I	ST	Resets the device.
VSS	5	5	5, 6	—	P	Ground reference for logic and I/O pins.
EN	6	6	7	I	TTL	Device enable. 1 = Device is enabled. 0 = Device is disabled (low power). MCP2150 only monitors this pin when in the NDM state.
TX	7	7	8	I	TTL	Asynchronous receive; from Host Controller UART.
RX	8	8	9	O	—	Asynchronous transmit; to Host Controller UART.
RI	9	9	10	—	—	Ring Indicator. The value on this pin is driven high.
DSR	10	10	11	O	—	Data Set Ready. Indicates that the MCP2150 has completed reset. 1 = MCP2150 is initialized. 0 = MCP2150 is not initialized.
DTR	11	11	12	I	TTL	Data Terminal Ready. The value of this pin is ignored once the MCP2150 is initialized. It is recommended that this pin be connected so that the voltage level is either VSS or VCC. At device power up, this signal is used with the RTS signal to enter device ID programming. 1 = Enter Device ID programming mode (if RTS is cleared). 0 = Do not enter Device ID programming mode.
CTS	12	12	13	O	—	Clear to Send. Indicates that the MCP2150 is ready to receive data from the Host Controller. 1 = Host Controller should not send data. 0 = Host Controller may send data.
RTS	13	13	14	I	TTL	Request to Send. Indicates that a Host Controller is ready to receive data from the MCP2150. The MCP2150 prepares to send data, if available. 1 = Host Controller not ready to receive data. 0 = Host Controller ready to receive data. At device power up, this signal is used with the DTR signal to enter device ID programming. 1 = Do not enter Device ID programming mode. 0 = Enter Device ID programming mode (if DTR is set).
VDD	14	14	15, 16	—	P	Positive supply for logic and I/O pins.
OSC2	15	15	17	O	—	Oscillator crystal output.
OSC1/CLKIN	16	16	18	I	CMOS	Oscillator crystal input/external clock source input.
CD	17	17	19	O	—	Carrier Detect. Indicates that the MCP2150 has established a valid link with a Primary Device. 1 = An IR link has not been established (No IR Link). 0 = An IR link has been established (IR Link).
BAUD1	18	18	20	I	ST	BAUD1:BAUD0 specify the baud rate of the device.

Legend: TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels
I = Input; O = Output
P = Power; CMOS = CMOS compatible input

1.1.1 SIGNAL DIRECTIONS

Table 1-3 shows the direction of the MCP2150 signals. The MCP2150 is designed for use in Data Terminal Equipment (DTE) applications.

TABLE 1-3: MCP2150 SIGNAL DIRECTION

DB-9 Pin No.	Signal	Direction	Comment
1	CD	MCP2150 → HC	Carrier Detect
2	RX	MCP2150 → HC	Received Data
3	TX	HC → MCP2150	Transmit Data
4	DTR (1)	—	Data Terminal Ready
5	GND	—	Ground
6	DSR	MCP2150 → HC	Data Set Ready
7	RTS	HC → MCP2150	Request to Send
8	CTS	MCP2150 → HC	Clear to Send
9	RI (1)	—	Ring Indicator

Legend: HC = Host Controller

Note 1: This signal is not implemented in the MCP2150.

2.0 DEVICE OPERATION

The MCP2150 is a cost effective, low pin count (18-pin), easy to use device for implementing IrDA standard wireless connectivity. The MCP2150 provides support for the IrDA standard protocol “stack” plus bit encoding/decoding. The Serial interface and IR baud rates are independantly selectable.

2.1 Power Up

Any time the device is powered up (parameter D003), the Power Up Timer delay (parameter 33) occurs, followed by an Oscillator Start-up Timer (OST) delay (parameter 32). Once these delays complete, communication with the device may be initiated. This communication is from both the infrared transceiver’s side as well as the controller’s UART interface.

2.2 Device Reset

The MCP2150 is forced into the reset state when the $\overline{\text{RESET}}$ pin is in the low state. Once the $\overline{\text{RESET}}$ pin is brought to a high state, the Device Reset sequence occurs. Once the sequence completes, functional operation begins.

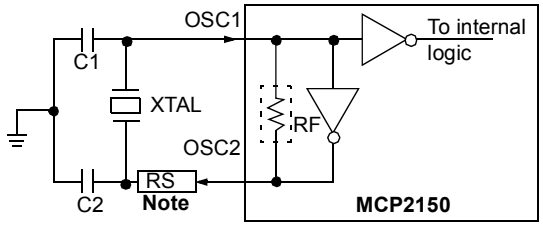
2.3 Clock Source

The MCP2150 requires a clock source to operate. The frequency of this clock is 11.0592 MHz (electrical specification parameter 1A). This clock can be supplied by either a crystal/resonator or as an external clock input.

2.3.1 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

A crystal or ceramic resonator can be connected to the OSC1 and OSC2 pins to establish oscillation (Figure 2-1). The MCP2150 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency outside of the crystal manufacturers specifications.

FIGURE 2-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR)



See Table 2-1 and Table 2-2 for recommended values of C1 and C2.

Note: A series resistor may be required for AT strip cut crystals.

TABLE 2-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Freq	OSC1 (C1)	OSC2 (C2)
11.0592 MHz	10 - 22 pF	10 - 22 pF
Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.		

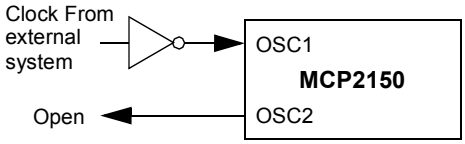
TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Freq	OSC1 (C1)	OSC2 (C2)
11.0592 MHz	15 - 30 pF	15 - 30 pF
Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. RS may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.		

2.3.2 EXTERNAL CLOCK IN

For applications where a clock is already available elsewhere, users may directly drive the MCP2150 provided that this external clock source meets the AC/DC timing requirements listed in Section 4.3. Figure 2-2 shows how an external clock circuit should be configured.

FIGURE 2-2: EXTERNAL CLOCK INPUT OPERATION



2.4 Bit Clock

The device crystal is used to derive the communication bit clock (BITCLK). There are 16 BITCLKs for each bit time. The BITCLKs are used for the generation of the start bit and the eight data bits. The stop bit uses the BITCLK when the data is transmitted (not for reception).

This clock is a fixed frequency and has minimal variation in frequency (specified by crystal manufacturer).

2.5 UART Interface

The UART interface communicates with the "controller". This interface is a half duplex interface, meaning that the system is either transmitting or receiving, but not both simultaneously.

2.5.1 BAUD RATE

The baud rate for the MCP2150 serial port (the TX and RX pins) is configured by the state of the BAUD1 and BAUD0 pins. These two device pins are used to select the baud rate at which the MCP2150 will transmit and receive serial data (not IR data). Table 2-3 shows the baud rate configurations.

TABLE 2-3: SERIAL BAUD RATE SELECTION VS. FREQUENCY

BAUD1:BAUD0	Baud Rate @ 11.0592 MHz	Bit Rate
00	9600	FOSC / 1152
01	19200	FOSC / 576
10	57600	FOSC / 192
11	115200	FOSC / 96

2.5.2 TRANSMITTING

When the controller sends serial data to the MCP2150, the controller's baud rate is required to match the baud rate of the MCP2150's serial port.

2.5.3 RECEIVING

When the controller receives serial data from the MCP2150, the controller's baud rate is required to match the baud rate of the MCP2150's serial port.

2.6 Modulation

The data that the MCP2150 UART received (on the TX pin) that needs to be transmitted (on the TXIR pin) will need to be modulated. This modulated signal drives the IR transceiver module. Figure 2-3 shows the encoding of the modulated signal.

Note:	The signal on the TXIR pin does not actually line up in time with the bit value that was transmitted on the TX pin, as shown in Figure 2-3. The TX bit value is shown to represent the value to be transmitted on the TXIR pin.

Each bit time is comprised of 16-bit clocks. If the value to be transmitted (as determined by the TX pin) is a logic low, then the TXIR pin will output a low level for 7-bit clock cycles, a logic high level for 3-bit clock cycles or a minimum of 1.6 µsec. (see parameter IR121). The remaining 6-bit clock cycles will be low. If the value to transmit is a logic high, then the TXIR pin will output a low level for the entire 16-bit clock cycles.

2.7 Demodulation

The modulated signal (data) from the IR transceiver module (on RXIR pin) needs to be demodulated to form the received data (on RX pin). Once demodulation of the data byte occurs, the data that is received is transmitted by the MCP2150 UART (on the RX pin). Figure 2-4 shows the decoding of the modulated signal.

Note:	The signal on the RX pin does not actually line up in time with the bit value that was received on the RXIR pin, as shown in Figure 2-4. The RXIR bit value is shown to represent the value to be transmitted on the RX pin.

Each bit time is comprised of 16-bit clocks. If the value to be received is a logic low, then the RXIR pin will be a low level for the first 3-bit clock cycles or a minimum of 1.6 µs. The remaining 13-bit clock cycles (or difference up to the 16-bit clock time) will be high. If the value to be received is a logic high, then the RXIR pin will be a high level for the entire 16-bit clock cycles. The level on the RX pin will be in the appropriate state for the entire 16 clock cycles.

FIGURE 2-3: ENCODING

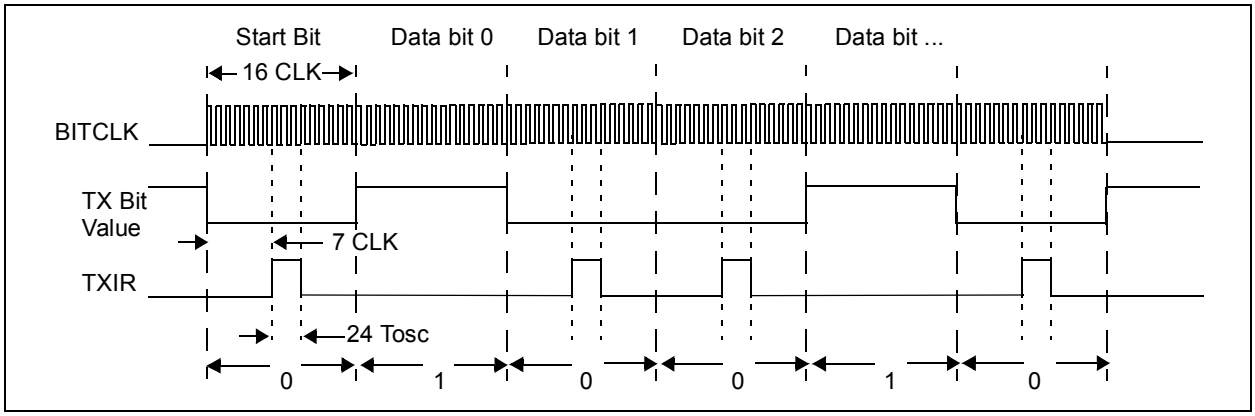
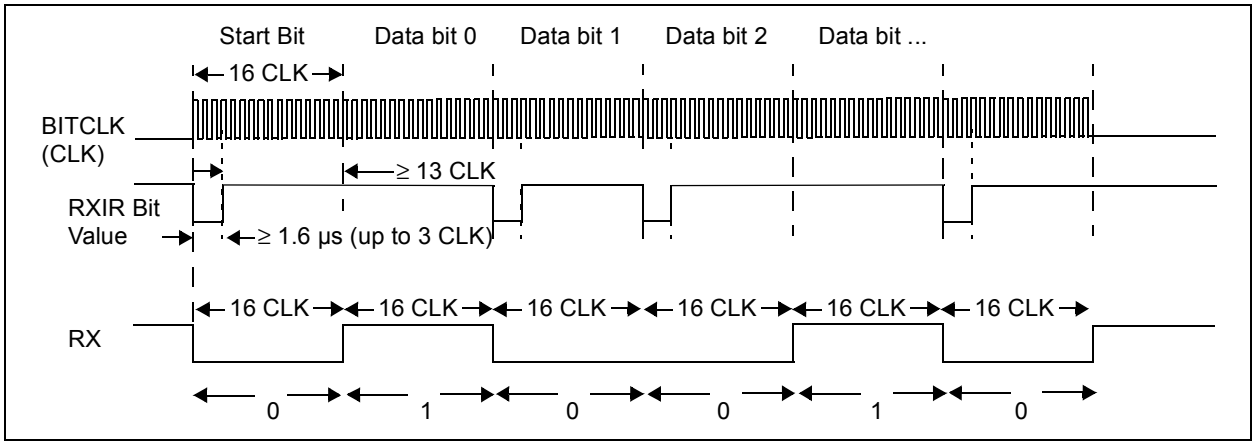


FIGURE 2-4: DECODING



2.8 Minimizing Power

The device can be placed in a low power mode by disabling the device (holding the EN pin at the low state). The internal state machine is monitoring this pin for a low level and, once this is detected, the device is disabled and enters into a low power state.

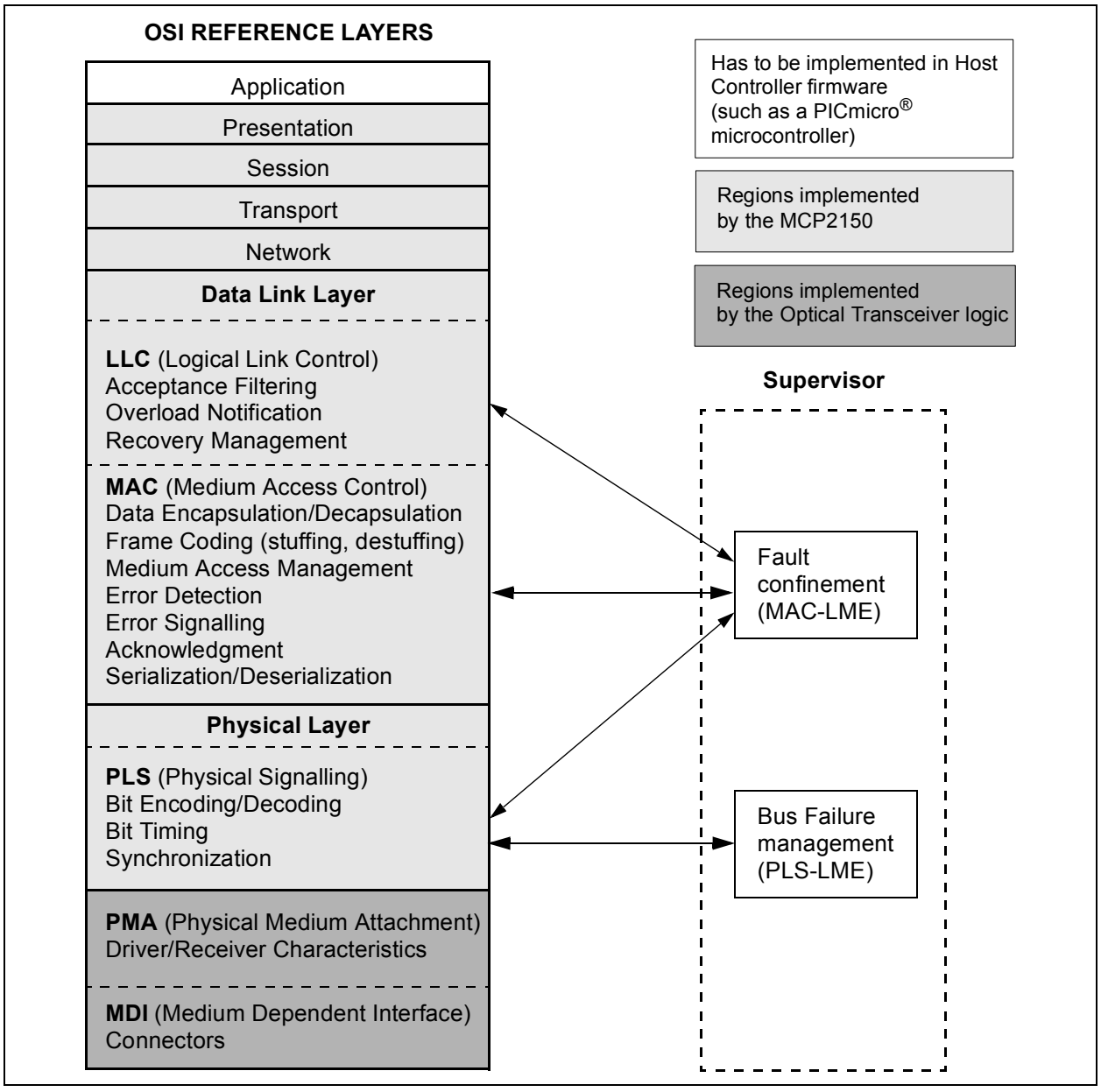
2.8.1 RETURNING TO DEVICE OPERATION

When disabled, the device is in a low power state. When the EN pin is brought to a high level, the device will return to the operating mode. The device requires a delay of 1024 TOSC before data may be transmitted or received.

2.9 Network Layering Reference Model

Figure 2-5 shows the ISO Network Layering Reference Model. The shaded areas are implemented by the MCP2150, the cross-hatched area is implemented by an infrared transceiver. The unshaded areas should be implemented by the Host Controller.

FIGURE 2-5: ISO REFERENCE LAYER MODEL



The IrDA standard specifies the following protocols:

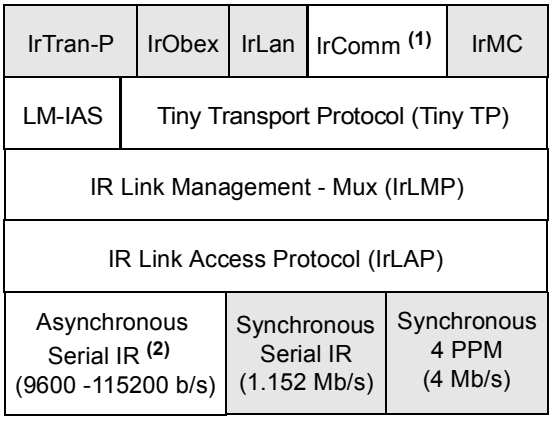
- Physical Signaling Layer (PHY)
- Link Access Protocol (IrLAP)
- Link Management Protocol/Information Access Service (IrLMP/IAS)

The IrDA data lists optional protocols. They are:

- Tiny TP
- IrTran-P
- IrOBEX
- IrLAN
- IrCOMM
- IrMC
- IrDA Lite

Figure 2-6 shows the IrDA data protocol stack and which components are implemented by the MCP2150.

FIGURE 2-6: IRDA DATA - PROTOCOL STACKS



Note 1: The MCP2155 implements the 9-wire "cooked" service class serial replicator.
2: An optical transceiver is required.

2.9.1 IrDA DATA PROTOCOLS SUPPORTED BY MCP2150

The MCP2150 supports these required IrDA standard protocols:

- Physical Signaling Layer (PHY)
- Link Access Protocol (IrLAP)
- Link Management Protocol/Information Access Service (IrLMP/IAS)

The MCP2150 also supports some of the optional protocols for IrDA data. The optional protocols that the MCP2150 implements are:

- Tiny TP
- IrCOMM

2.9.1.1 Physical Signal Layer (PHY)

The MCP2150 provides the following Physical Signal Layer specification support:

- Bidirectional communication
- Data Packets are protected by a CRC
  - 16-bit CRC for speeds up to 115.2 kbaud
- Data Communication Rate
  - 9600 baud minimum data rate

The following Physical Layer Specification is dependant on the optical transceiver logic used in the application. The specification states:

- Communication Range, which sets the end user expectation for discovery, recognition and performance.
  - Continuous operation from contact to at least 1 meter (typically 2 meters can be reached)
  - A low power specification reduces the objective for operation from contact to at least 20 cm (low power and low power) or 30 cm (low power and standard power).

2.9.1.2 IrLAP

The MCP2150 supports the IrLAP protocol. The IrLAP protocol provides:

- Management of communication processes on the link between devices.
- A device-to-device connection for the reliable, ordered transfer of data.
- Device discover procedures.
- Hidden node handling.

Figure 2-7 identifies the key parts and hierarchy of the IrDA protocols. The bottom layer is the Physical layer, IrPHY. This is the part that converts the serial data to and from pulses of IR light. IR transceivers can't transmit and receive at the same time. The receiver has to wait for the transmitter to finish sending. This is sometimes referred to as a "Half-Duplex" connection. The IR Link Access Protocol (IrLAP) provides the structure for packets (or "frames") of data to emulate data that would normally be free to stream back and forth.

FIGURE 2-7: IRDA STANDARD PROTOCOL LAYERS

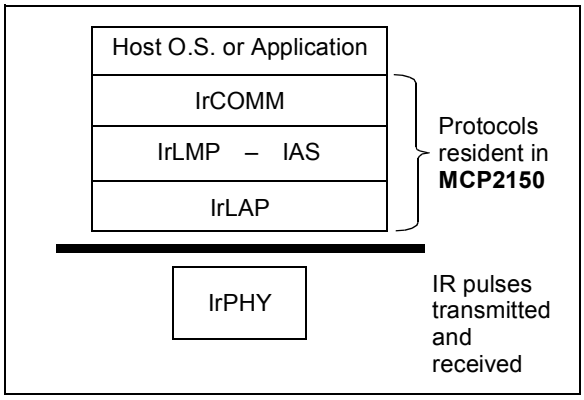


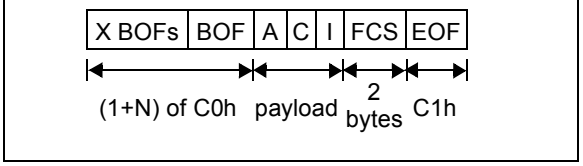
Figure 2-8 shows how the IrLAP frame is organized. The frame is proceeded by some number of Beginning of Frame characters (BOFs). The value of the BOF is generally 0xC0, but 0xFF may be used if the last BOF character is a 0xC0. The purpose of multiple BOFs is to give the other station some warning that a frame is coming.

The IrLAP frame begins with an address byte ("A" field), then a control byte ("C" field). The control byte is used to differentiate between different types of frames and is also used to count frames. Frames can carry status, data or commands. The IrLAP protocol has a command syntax of it's own. These commands are part of the control byte. Lastly, IrLAP frames carry data. This data is the information (or "I") field. The integrity of the frame is ensured with a 16-bit CRC, referred to as the Frame Check Sequence (FCS). The 16-bit CRC value is transmitted LSB first. The end of the frame is marked with an EOF character, which is always a 0xC1. The frame structure described here is used for all versions of IrDA protocols used for serial wire replacement for speeds up to 115.2 kbaud.

Note 1: Another IrDA standard that is entering general usage is IR Object Exchange (IrOBEX). This standard is not used for serial connection emulation.

2: IrDA communication standards faster than 115.2 kbaud use a different CRC method and physical layer.

FIGURE 2-8: IRLAP FRAME



In addition to defining the frame structure, IrLAP provides the "housekeeping" functions of opening, closing and maintaining connections. The critical parameters that determine the performance of the link are part of this function. These parameters control how many BOFs are used, identify the speed of the link, how fast either party may change from receiving to transmitting, etc. IrLAP has the responsibility of negotiating these parameters to the highest common set so that both sides can communicate as quickly, and as reliably, as possible.

2.9.1.3 IrLMP

The MCP2150 implements the IrLMP protocol. The IrLMP protocol provides:

- Multiplexing of the IrLAP layer. This allows multiple channels above an IrLAP connection.
- Protocol and service discovery. This is via the Information Access Service (IAS).

When two devices that contain the IrDA standard feature are connected, there is generally one device that has something to do and the other device that has the resource to do it. For example, a laptop may have a job to print and an IrDA standard compatible printer has the resources to print it. In IrDA standard terminology, the laptop is a Primary device and the printer is the Secondary device. When these two devices connect, the Primary device must determine the capablities of the Secondary device to determine if the Secondary device is capable of doing the job. This determination is made by the Primary device asking the Secondary device a series of questions. Depending on the answers to these questions, the Primary device may or may not elect to connect to the Secondary device.

The queries from the Primary device are carried to the Secondary device using IrLMP. The responses to these queries can be found in the Information Access Service (IAS) of the Secondary device. The IAS is a list of the resources of the Secondary device. The Primary device compares the IAS responses with its requirements and then makes the decision if a connection should be made.

The MCP2150 identifies itself to the Primary device as a modem.

Note:	The MCP2150 identifies itself as a modem to ensure that it is identified as a serial device with a limited amount of memory.

The MCP2150 is not a modem, and the non-data circuits are not handled in a modem fashion.

2.9.1.4 Link Management - Information Access Service (LM-IAS)

The MCP2150 implements the LM-IAS. Each LM-IAS entity maintains an information database to provide:

- Information on services for other devices that contain the IrDA standard feature (Discovery).
- Information on services for the device itself.
- Remote accessing of another device's information base.

This is required so that clients on a remote device can find configuration information needed to access a service.

2.9.1.5 Tiny TP

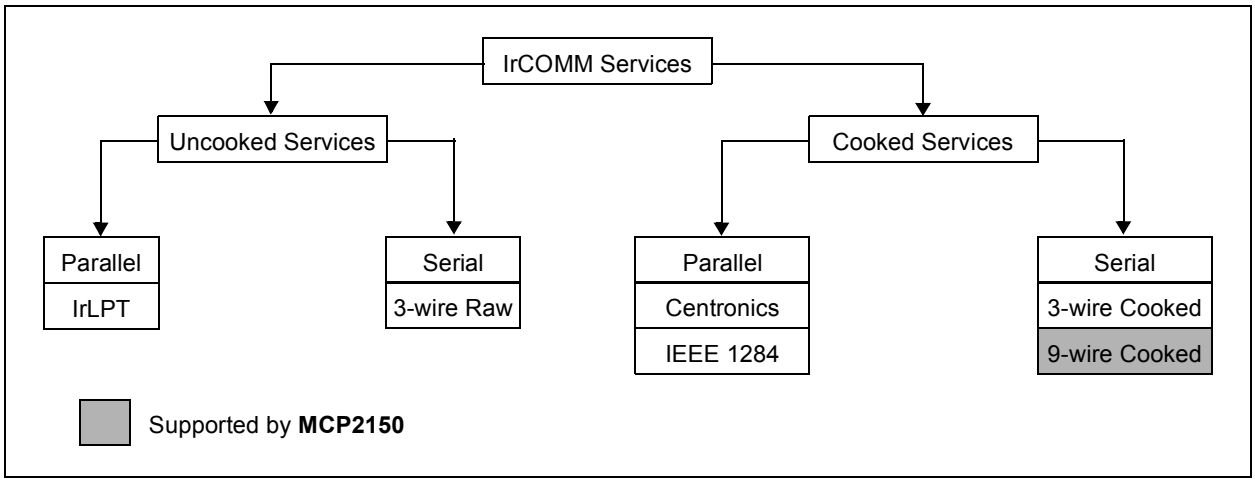
Tiny TP provides the flow control on IrLMP connections. An optional service of Segmentation and Reassembly can be handled.

2.9.1.6 IrCOMM

IrCOMM provides the method to support serial and parallel port emulation. This is useful for legacy COM applications, such as printers and modem devices.

The IrCOMM standard is just a syntax that allows the Primary device to consider the Secondary device as a serial device. IrCOMM allows for emulation of serial or parallel (printer) connections of various capabilities. The MCP2150 supports the 9-wire "cooked" service class of IrCOMM. Other service classes supported by IrCOMM are shown in Figure 2-9.

FIGURE 2-9: IRCOMM SERVICE CLASSES



2.9.2 OTHER OPTIONAL IrDA DATA PROTOCOLS

Other IrDA data protocols have been developed to specific application requirements. These optional protocols are not supported by the MCP2150. These IrDA data protocols are briefly described in the following sub-sections. For additional information, please refer to the IrDA website **(www.IrDA.org)**.

2.9.2.1 IrTran-P

IrTran-P provides the protocol to exchange images with digital image capture devices/cameras.

2.9.2.2 IrOBEX

IrOBEX provides OBject EXchange services. This is similar to HTTP.

2.9.2.3 IrLAN

IrLAN describes a protocol to support IR wireless access to a Local Area Network (LAN).

2.9.2.4 IrMC

IrMC describes how mobile telephony and communication devices can exchange information. This information includes phonebook, calender and message data.

Also how call control and real-time voice are handled (RTCON).

2.9.2.5 IrDA Lite

IrDA Lite describes how to reduce the application code requirements, while maintaining compatibility with the full implementation.

2.9.3 HOW DEVICES CONNECT

When two devices implementing the IrDA standard feature establish a connection using the IrCOMM protocol, the process is analogous to connecting two devices with serial ports using a cable. This is referred to as a "point-to-point" connection. This connection is limited to half-duplex operation because the IR transceiver cannot transmit and receive at the same time. The purpose of the IrDA protocol is to allow this half-duplex link to emulate, as much as possible, a full-duplex connection. In general, this is done by dividing the data into “packets”, or groups of data. These packets can then be sent back and forth, when needed, without risk of collision. The rules of how and when these packets are sent constitute the IrDA protocols. The MCP2150 supports elements of this IrDA protocol to communicate with other IrDA standard compatible devices.

When a wired connection is used, the assumption is made that both sides have the same communications parameters and features. A wired connection has no need to identify the other connector because it is assumed that the connectors are properly connected. In the IrDA standard, a connection process has been defined to identify other IrDA compatible devices and establish a communication link. There are three steps that these two devices go through to make this connection. They are:

- Normal Disconnect Mode (NDM)
- Discovery Mode
- Normal Connect Mode (NCM)

Figure 2-10 shows the connection sequence.

2.9.3.1 Normal Disconnect Mode (NDM)

When two IrDA standard compatible devices come into range they must first recognize each other. The basis of this process is that one device has some task to accomplish and the other device has a resource needed to accomplish this task. One device is referred to as a Primary device and the other is referred to as a Secondary device. This distinction between Primary device and Secondary device is important. It is the responsibility of the Primary device to provide the mechanism to recognize other devices. So the Primary device must first poll for nearby IrDA standard compatible devices. During this polling, the defaut baud rate of 9600 baud is used by both devices.

For example, if you want to print from an IrDA equipped laptop to an IrDA printer, utilizing the IrDA standard feature, you would first bring your laptop in range of the printer. In this case, the laptop is the one that has something to do and the printer has the resource to do it. The laptop is called the Primary device and the printer is the Secondary device. Some data-capable cellphones have IrDA standard infrared ports. If you used such a cellphone with a Personal Digital Assistant (PDA), the PDA that supports the IrDA standard feature would be the Primary device and the cellphone would be the Secondary device.

When a Primary device polls for another device, a nearby Secondary device may respond. When a Secondary device responds, the two devices are defined to be in the Normal Disconnect Mode (NDM) state. NDM is established by the Primary device broadcasting a packet and waiting for a response. These broadcast packets are numbered. Usually 6 or 8 packets are sent. The first packet is number 0, the last packet is usually number 5 or 7. Once all the packets are sent, the Primary device sends an ID packet, which is not numbered.

The Secondary device waits for these packets and then responds to one of the packets. The packet it responds to determines the “time slot” to be used by the Secondary device. For example, if the Secondary device responds after packet number 2, then the Secondary device will use time slot 2. If the Secondary device responds after packet number 0, then the Secondary device will use time slot 0. This mechanism allows the Primary device to recognize as many nearby devices as there are time slots. The Primary device will continue to generate time slots and the Secondary device should continue to respond, even if there’s nothing to do.

Note 1: The MCP2150 can only be used to implement a Secondary device.

2: The MCP2150 supports a system with only one Secondary device having exclusive use of the IrDA standard infrared link (known as "point-to-point" communication).

3: The MCP2150 always responds to packet number 2. This means that the MCP2150 will always use time slot 2.

4: If another Secondary device is nearby, the Primary device may fail to recognize the MCP2150, or the Primary device may not recognize either of the devices.

During NDM, the MCP2150 handles all of the responses to the Primary device (Figure 2-10) without any communication with the Host Controller. The Host Controller is inhibited by the CTS signal of the MCP2150 from sending data to the MCP2150.

2.9.3.2 Discovery Mode

Discovery mode allows the Primary device to determine the capabilities of the MCP2150 (Secondary device). Discovery mode is entered once the MCP2150 (Secondary device) has sent an XID response to the Primary device and the Primary device has completed sending the XIDs and then sends a Broadcast ID. If this sequence is not completed, then a Primary and Secondary device can stay in NDM indefinitely.

When the Primary device has something to do, it initiates Discovery. Discovery has two parts. They are:

- Link initialization
- Resource determination

The first step is for the Primary and Secondary devices to determine, and then adjust to, each other's hardware capabilities. These capabilities are parameters like:

- Data rate
- Turn around time
- Number of packets without a response
- How long to wait before disconnecting

Both the Primary and Secondary device begin communications at 9600 baud, which is the default baud rate. The Primary device sends its parameters, then the Secondary device responds with its parameters. For example, if the Primary supports all data rates up to 115.2 kbaud and the Secondary device only supports 19.2 kbaud, the link will be established at 19.2 kbaud.

Note:	The MCP2150 is limited to a data rate of 115.2 kbaud.

Once the hardware parameters are established, the Primary device must determine if the Secondary device has the resources it requires. If the Primary device has a job to print, then it must know if it's talking to a printer, not a modem or other device. This determination is made using the Information Access Service (IAS). The job of the Secondary device is to respond to IAS queries made by the Primary device. The Primary device must ask a series of questions like:

- What is the name of your service?
- What is the address of this service?
- What are the capabilities of this device?

When all the Primary device's questions are answered, the Primary device can access the service provided by the Secondary device.

During Discovery mode, the MCP2150 handles all responses to the Primary device (see Figure 2-10) without any communication with the Host Controller. The Host Controller is inhibited by the CTS signal of the MCP2150 from sending data to the MCP2150.

2.9.3.3 Normal Connect Mode (NCM)

Once discovery has been completed, the Primary device and MCP2150 (Secondary device) can freely exchange data.

The MCP2150 can receive IR data or serial data, but not both simultaneously. The MCP2150 uses a hardware handshake to stop the local serial port from sending data while the MCP2150 is receiving IR data.

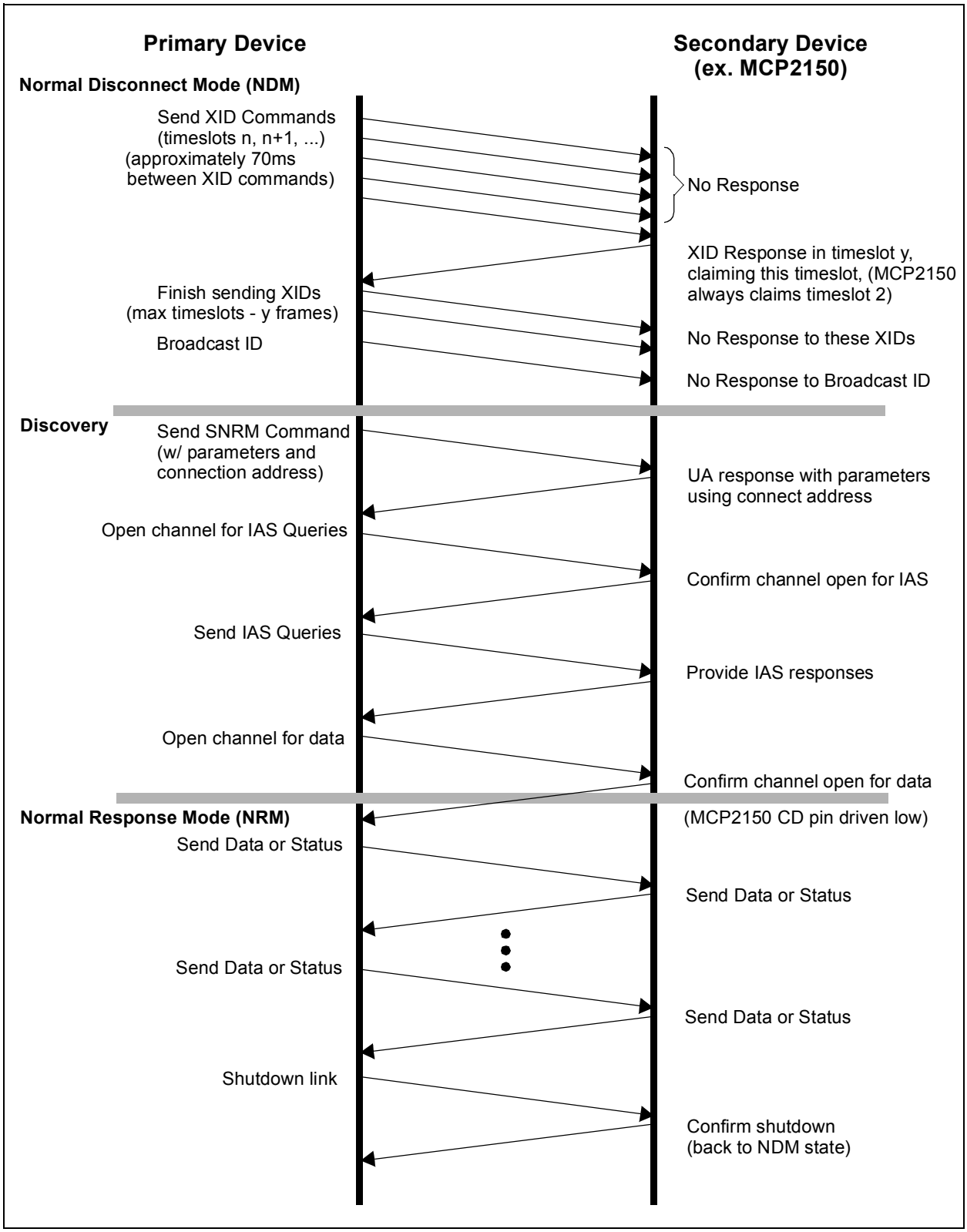
Note:	Data loss will result if this hardware handshake is not observed.

Both the Primary device and the MCP2150 (Secondary device) check to make sure that data packets are received by the other without errors. Even when data is required to be sent, the Primary and Secondary devices will still exchange packets to ensure that the connection hasn't, unexpectedly, been dropped. When the Primary device has finished, it then transmits the close link command to the MCP2150 (Secondary device). The MCP2150 will confirm the close link command and both the Primary device and the MCP2150 (Secondary device) will revert to the NDM state.

Note:	If the NCM mode is unexpectedly terminated for any reason (including the Primary device not issuing a close link command), the MCP2150 will revert to the NDM state 10 seconds after the last frame has been received.

It is the responsability of the Host Controller program to understand the meaning of the data received and how the program should respond to it. It's just as if the data were being received by the Host Controller from a UART.

FIGURE 2-10: CONNECTION SEQUENCE



2.10 Operation

The MCP2150 emulates a null modem connection. The application on the DTE device sees a virtual serial port. This serial port emulation is provided by the IrDA standard protocols. The link between the DTE device and the embedded application is made using the MCP2150. The connection between the MCP2150 and the embedded application is wired as if there were a null modem connection.

The Carrier Detect (CD) signal of the MCP2150 is used to indicate that a valid IrDA standard infrared link has been established between the MCP2150 and the Primary device. The CD signal should be monitored closely to make sure that any communication tasks can be completed. The MCP2150 DSR signal indicates that the device has powered-up, successfully initialized and is ready for service. This signal is intended to be connected to the DSR input of the Host Controller. If the Host Controller was directly connected to an IrDA standard Primary device using a serial cable (the MCP2150 is not present), the Host Controller would be connected to the Primary device's DTR output signal.

The MCP2150 generates the CTS signal locally because of buffer limitations.

Note 1: The MCP2150 generates non-data signals locally.

2: Only transceiver's TXD and RXD signals are carried back and forth to the Primary device. The MCP2150 emulates a 3-wire serial connection (TXD, RXD and GND).

2.10.1 HARDWARE HANDSHAKING

The MCP2150 uses a 64-byte buffer for incoming data from the IR Host. Another 64-byte buffer is provided to buffer data from the UART serial port. When an IR packet begins the IrComm, the MCP2150 handles IR data exclusively (the UART serial port buffer is not available). A hardware handshaking pin (CTS) is provided to inhibit the Host Controller from sending serial data while IR Data is being sent or received.

Note: When the CTS output from the IrComm is high, no data should be sent from the Host Controller. The UART FIFO will store up to 2 bytes. Any additional data bytes will be lost.

2.10.2 BUFFERS AND THROUGHPUT

The maximum IR data rate of the MCP2150 is 115.2 kbaud. The actual throughput will be less, due to several factors. The most significant factors are under the control of the developer. One factor beyond the control of the designer is the overhead associated with the IrDA standard. The MCP2150 uses a fixed data block size of 64 bytes. To carry 64 bytes of data, the MCP2150 must send 72 bytes (64+8). The additional 8 bytes are used by the protocol. When the Primary device receives the frame, it must wait for a minimum latency period before sending a packet of its own. This turnaround time is set by IrLAP when the parameters of the link are negotiated. A common turnaround time is 1 ms, although longer and shorter times may be encountered. 1 ms represents approximately 12 byte times at a data rate of 115.2 kbaud. The minimum size frame the Primary device can respond with is 6 bytes. The MCP2150 will add the 12 byte-time latency on its own, again assuming a 1 ms latency. This means that the maximum throughput will be 64 data bytes out of a total of 64 + 38 byte times. Thus, the maximum theoretical throughput will be limited to about 64/(64+38)=63% of the IR data rate. Actual maximum throughput will be dependent on both the MCP2150 and the characteristics of the Primary device.

The most significant factor in data throughput is how well the data frames are filled. If only 1 byte is sent at a time, then the maximum throughput is 1/(1+38)=2.5% of the IR data rate. The best way to maximize throughput is to align the amounts of data with the packet size of the MCP2150. Throughput examples are shown in Table 2-4.

Note: IrDA throughput is based on many factors associated with characteristics of the Primary and Secondary devices. These characteristics may cause your application throughput to be less than the theoretical example shown in Table 2-4.

TABLE 2-4: THEORETICAL IrDA STANDARD THROUGHPUT EXAMPLES @ 115.2 KBAUD

MCP2150 Data Packet Size (Bytes)	Overhead (Bytes)	Primary Device Minimum Response (Bytes)	Primary Device Turn-around Time(1) (Bytes)	MCP2150 Turn-around Time(1) (Bytes)	Total Bytes Transmitted	Throughput % (Data/Total)
64	8	6	12	12	102	62.7%
1	8	6	12	12	39	2.6%

Note 1: Number of bytes calculated based on a common turnaround time of 1 ms.

2.11 Turnaround Latency

An IR link can be compared to a one-wire data connection. The IR transceiver can transmit or receive, but not both at the same time. A delay of one bit time is recommended between the time a byte is received and another byte is transmitted.

2.12 IR Port Baud Rate

The baud rate for the MCP2150 IR port (the TXIR and RXIR pins) is, initially, at the default rate of 9600 baud. The Primary device determines the maximum baud rate that the MCP2150 will operate at. This information is used during NDM, with the Primary device setting the baud rate of the IR link. The maximum IR baud rate is not required to be the same as the MCP2150's serial port (UART) baud rate (as determined by the BAUD1:BAUD0 pins).

2.13 Programmable Device ID

The MCP2150 has a flexible feature that allows the MCP2150 Device ID to be changed by the Host Controller. The default ID is "Generic IrDA" and is stored in non-volatile, electrically erasable programmable memory (EEPROM). The maximum ID String length is 19 bytes. The format of the ID EEPROM is shown in Figure 2-11.

The ID String must only contain the ASCII characters from 20h to 7Ah (inclusive).

The MCP2150 enters into ID String programming when it exits the reset state and detects that the DTR pin is high and the RTS pin is low.

A Host Controller connected to the MCP2150 would, typically, perform the following steps to place the MCP2150 into ID String programming mode:

1. Force the MCP2150 into reset (RESET pin forced low).
2. Force the DTR pin high and the RTS pin low.
3. Release the MCP2150 from reset (RESET pin forced high).
4. Wait for device to complete initialization.

TABLE 2-5: DTR/RTS STATE & DEVICE MODE

DTR	RTS	After Device Reset *
0	X	Enter Normal Mode
1	0	Enter Programmable Device ID
1	1	Enter Normal Mode

* Until device initialization is complete.

Once the MCP2150 is ready to receive data, the CTS pin will be forced low. Data may now be transferred, following the format in Figure 2-11. The CTS pin determines the flow control and the Host Controller must monitor this signal to ensure that the data byte may be sent.

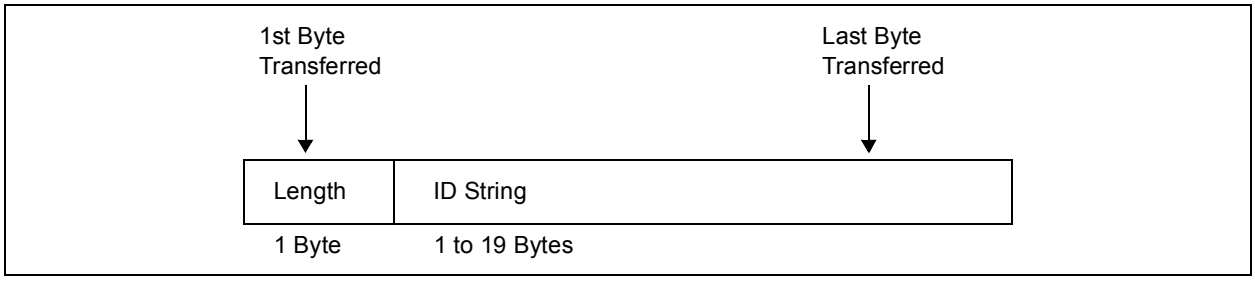
Once the Host Controller has sent its last byte, the DTR pin must be set low. This ensures that, if another reset occurs, the MCP2150 will not reenter ID String programming mode. The MCP2150 uses the String Length (1st byte transmitted) to determine when the ID String programming mode has completed. This returns the MCP2150 to normal operation.

Note 1: If a non-valid ID String (containing an ASCII character not in the valid range) is programmed, the MCP2150 will not create a link with a Primary device.

2: The communication program supplied with Microsoft's Windows® operating system (called HyperTerminal) may leave the DTR signal high and the RTS signals low when the program disconnects, or is closed. Care should be taken to ensure that this does not accidently cause the MCP2150 to enter Device ID String Programming.

Example 2-1 shows the firmware code for a PIC16CXXX acting as the Host Controller to modify the MCP2150 Device ID String.

FIGURE 2-11: ID STRING FORMAT



EXAMPLE 2-1: PIC16FXX Code to Program the Device ID

```
;#define     dtr    PORTx, Pinx    ; Must specify which Port and Which Pin
;#define     cts    PORTx, Pinx    ; Must specify which Port and Which Pin
;#define     rts    PORTx, Pinx    ; Must specify which Port and Which Pin
;#define     clr    PORTx, Pinx    ; Must specify which Port and Which Pin
;
;*****************************************************************
; String Table
; This table stores a string, breg is the offset.  The string
; is terminated by a null character.
;*****************************************************************
string1 clrf   PCLATH           ; this routine is on page 0
        movf   breg, W          ; get the offset
        addwf  PCL, F           ; add the offset to PC
        DT     D'15'            ; the first byte is the byte count
        DT     "My IR ID String"
;
UpdateID
        call   deviceInit       ; Initialize the PIC16Fxxx
        bcf    clr              ; place the MCP2150 in reset
        bsf    dtr              ; Force the DTR pin high for program mode
        bcf    rts              ; Force the RTS pin low for program mode
        call   delay1mS         ; delay for 1 ms.
        bsf    clr              ; allow the MCP2150 to come out of reset
;
        clrf   LoopCnt          ; LoopCnt = 0
ctsLP1  call   delay1mS         ; delay for 1 ms.
        btfss  cts              ; if cts=0 then we're ready to program
        goto   ctsLow           ; MCP2150 is ready to receive data
        decfsz LoopCnt, F       ;
        goto   ctsLP1           ; NO, wait for MCP2150 to be ready
        goto   StuckReset       ; The MCP2150 did not exit reset, do your recovery
                                ;   in this routine.
```

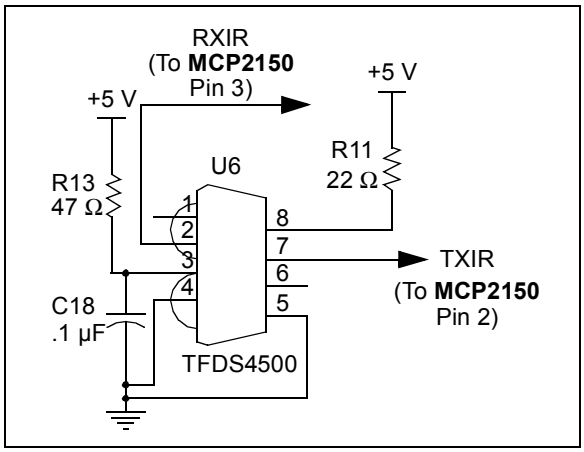

EXAMPLE 2-1: PIC16FXX Code to Program the Device ID (Continued)

```
ctsLow  clrf    breg            ; clear the offset
        call    string1         ; get the byte count
                                ;   (ID length byte + # bytes in string)
        movwf   creg            ; use creg as the loop counter
        incf    creg, f         ; add 1 to the loop count since
                                ;    we're jumping into the middle
        movwf   areg            ; save the count in areg to send it
        goto    sndwt           ; start sending the count + ID string
;
sndlp   call    string1         ; get the byte
        movwf   areg            ; save the byte
sndwt   btfsc   cts             ; check the cts input
        goto    sndwt           ; wait if cts=1
        call    txser           ; send the byte using the Transmit Routine
        incf    breg,f          ; increment the table pointer
        decfsz  creg, f         ; more bytes to send?
        goto    sndlp           ; YES, send more bytes
;
        bcf     clr             ; NO, place the MCP2150 in reset
        bcf     dtr             ; Force the DTR pin low for normal mode
        bsf     rts             ; Force the RTS pin high for normal mode
        call    delay1mS        ; delay for 1 ms.
        bsf     clr             ; allow the MCP2150 to come out of reset
;
ctsLP2  btfss   cts             ; if cts=1 then MCP2150 is in Normal mode
        goto    ctsLP2          ; NO, wait for MCP2150 to be ready
        goto    NormalOperation ; The MCP2150 in now programmed with new ID,
                                ; and is ready to establish an IR link
```

2.14 Optical Transceiver

The MCP2150 requires an infrared transceiver. The transceiver can be an integrated solution. Table 2-6 shows a list of common manufacturers of integrated optical transceivers. A typical optical transceiver circuit, using a Vishay/Temic TFDS4500, is shown in Figure 2-12.

FIGURE 2-12: TYPICAL OPTICAL TRANSCEIVER CIRCUIT



The optical transceiver logic can be implemented with discrete components for cost savings. Care must be taken in the design and layout of the photo detect circuit, due to the small signals that are being detected and their sensitivity to noise. A discrete implementation of the optical transceiver logic is implemented on the MCP2120 and MCP2150 Developer's Kit boards.

Note:	The discrete optical transceiver implementation on the MCP2120 and MCP2150 Developer's Kit boards may not meet the IrDA specifications for the physical layer (IrPHY). Any discrete solution will require appropriate validation for the user's application.

2.15 References

The IrDA Standards download page can be found at:

http://www.irda.org/standards/specifications

Some common manufacturers of Optical Transceivers are shown in Table 2-6.

TABLE 2-6: COMMON OPTICAL TRANSCEIVER MANUFACTURERS

Company	Company Web Site Address
Infineon	www.infineon.com
Agilent	www.agilent.com
Vishay/Temic	www.vishay.com
Rohm	www.rohm.com

3.0 DEVELOPMENT TOOLS

The MCP2150 is supported by the MCP2120/ MCP2150 Developer's Kit (order number DM163008). This kit allows the user to evaluate the operation of the MCP2150.

Each kit comes with two MCP2120 Developer's Boards and one MCP2150 Developer's Board to demonstrate transmission/reception of infrared data streams. Figure 3-1 shows a block diagram of the MCP2150 Developer's Board.

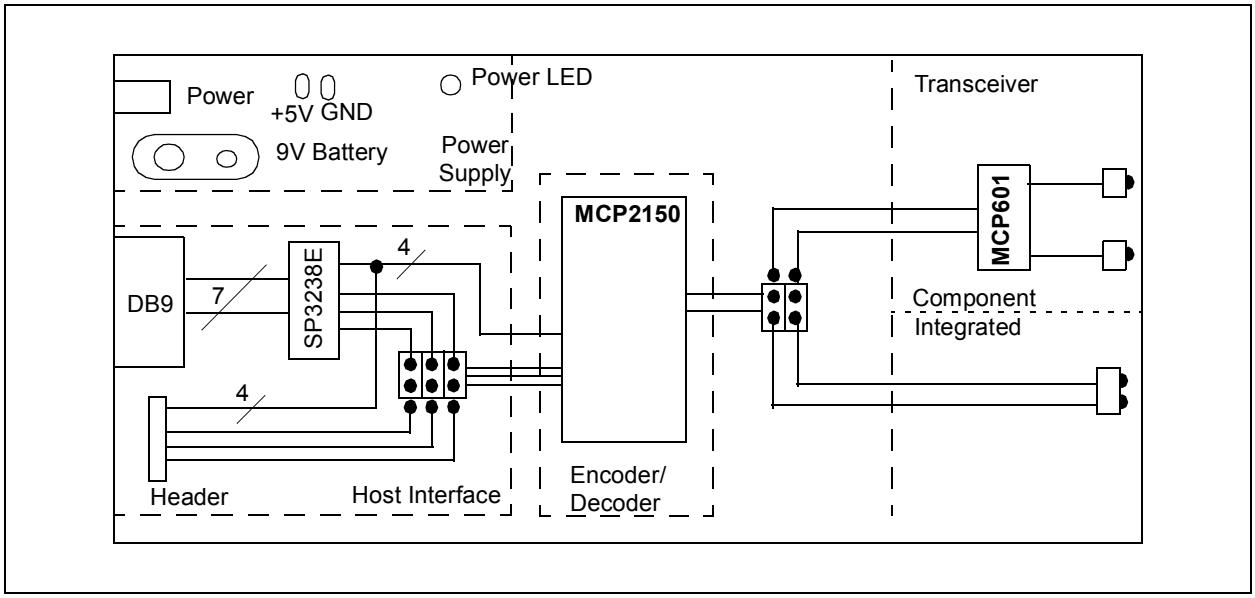
As can be seen, the user has jumper options for both the interface to the Host Controller (UART or Header) and the transceiver solution (Integrated or discrete component).

The UART interface allows a direct connection to a PC (use a terminal emulation program), or a header, to allow easy connection to host prototypes (or one of the Microchip PICDEM™ boards).

The transceiver logic is jumpered to allow the selection of either a single chip transceiver solution, or a low cost discrete solution. This low cost discrete solution allows a lower system cost to be achieved. With the lower cost come some trade-offs of the IrDA standard physical layer specifications. These trade-offs need to be evaluated to ensure the characteristics of the component solution meet the requirements of the system.

This kit comes with two identical MCP2120 Developer's Boards and a single MCP2150 Developer's Board. This allows a complete system (Transmitter and Receiver) to be implemented with either system requirement (simple encoder/decoder or IrDA standard protocol stack plus encoder/decoder).

FIGURE 3-1: MCP2150 DEVELOPER'S KIT BLOCK DIAGRAM



NOTES:

4.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Ambient Temperature under bias ..... –40°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ..... -0.3 V to +6.5 V

Voltage on $\overline{RESET}$ with respect to V_{SS} ..... -0.3 V to +14 V

Voltage on all other pins with respect to V_{SS} ..... –0.3 V to (V_{DD} + 0.3 V)

Total Power Dissipation (1) ..... 800 mW

Max. Current out of V_{SS} pin ..... 300 mA

Max. Current into V_{DD} pin ..... 250 mA

Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output Clamp Current, I_{OK} (V_0 < 0 or V_0 > V_{DD}) ..... ±20 mA

Max. Output Current sunk by any Output pin ..... 25 mA

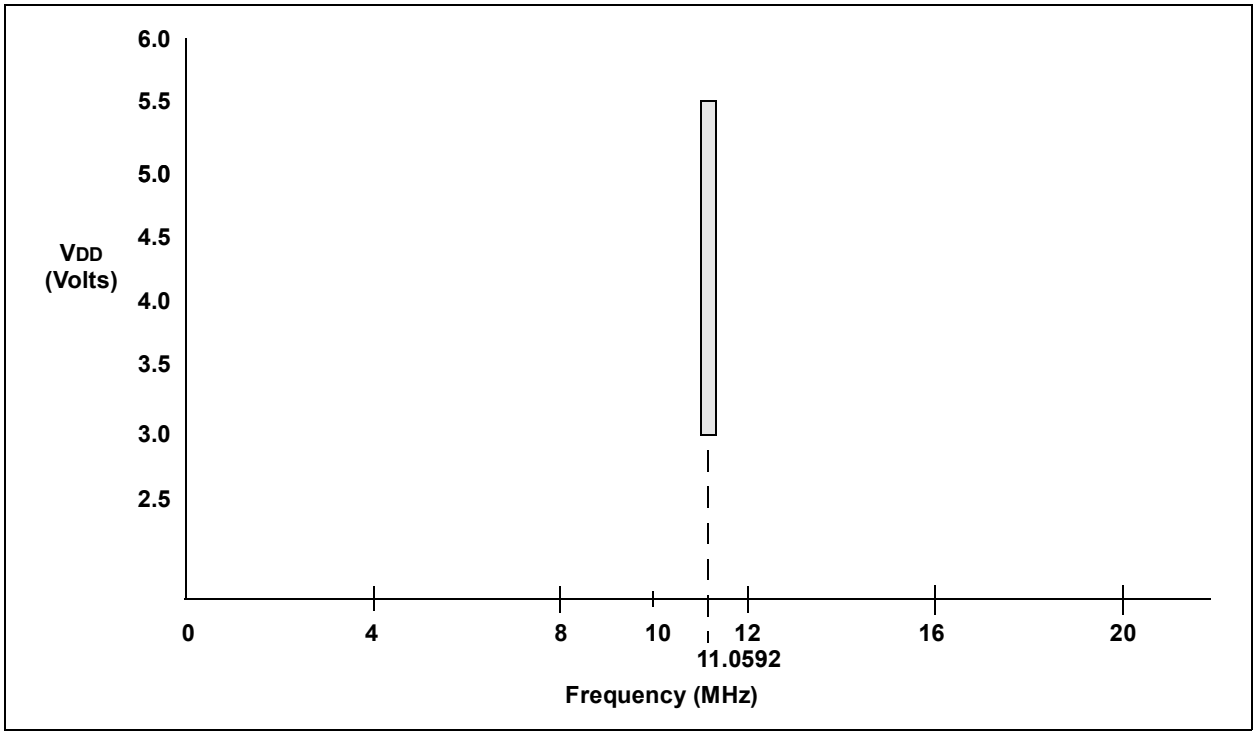
Max. Output Current sourced by any Output pin ..... 25 mA

Note 1: Power Dissipation is calculated as follows:

$$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$$

†NOTICE: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 4-1: VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



4.1 DC Characteristics

DC Specifications			Electrical Characteristics: Standard Operating Conditions (unless otherwise specified) Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial)				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D001	VDD	Supply Voltage	3.0	—	5.5	V	See Figure 4-1
D002	VDR	RAM Data Retention Voltage (2)	2.0	—	—	V	Device Oscillator/Clock stopped
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	VSS	—	V	
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05	—	—	V/ms	
D010	IDD	Supply Current (3)	— —	— 4.0	2.2 7.0	mA mA	FOSC = 11.0592 MHz, VDD = 3.0 V FOSC = 11.0592 MHz, VDD = 5.5 V
D020	IPD	Device Disabled Current (3, 4)	— —	— —	2.2 9	µA µA	VDD = 3.0 V VDD = 5.5 V

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Pin loading, pin rate and temperature have an impact on the current consumption.

a) The test conditions for all IDD measurements are made when device is enabled (EN pin is high): OSC1 = external square wave, from rail-to-rail; all input pins pulled to VSS, RXIR = VDD, $\overline{\text{RESET}}$ = VDD;

b) When device is disabled (EN pin is low), the conditions for current measurements are the same.

4: When the device is disabled (EN pin is low), current is measured with all input pins tied to VDD or VSS and the output pins driving a high or low level into infinite impedance.

4.1 DC Characteristics (Continued)

DC Specifications			Electrical Characteristics: Standard Operating Conditions (unless otherwise specified) Operating temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 4.1.				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
		Input Low Voltage					
	VIL	Input pins					
D030		with TTL buffer (TX, RI, DTR, RTS, and EN)	VSS	—	0.8 V	V	4.5 V ≤ VDD ≤ 5.5 V
D030A			VSS	—	0.15 VDD	V	otherwise
D031		with Schmitt Trigger buffer (BAUD1, BAUD0, and RXIR)	VSS	—	0.2 VDD	V	
D032		$\overline{\text{RESET}}$	VSS	—	0.2 VDD	V	
D033		OSC1	VSS	—	0.3 VDD	V	
		Input High Voltage					
	VIH	Input pins		—			
D040		with TTL buffer (TX, RI, DTR, RTS, and EN)	2.0	—	VDD	V	4.5 V ≤ VDD ≤ 5.5 V
D040A			0.25 VDD + 0.8	—	VDD	V	otherwise
D041		with Schmitt Trigger buffer (BAUD1, BAUD0, and RXIR)	0.8 VDD	—	VDD	V	
D042		$\overline{\text{RESET}}$	0.8 VDD	—	VDD	V	
D043		OSC1	0.7 VDD	—	VDD	V	
		Input Leakage Current (Notes 1, 2)					
D060	IIL	Input pins	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D061		$\overline{\text{RESET}}$	—	—	±5	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	µA	VSS ≤ VPIN ≤ VDD

Note 1: The leakage current on the $\overline{\text{RESET}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

2: Negative current is defined as coming out of the pin.

4.1 DC Characteristics (Continued)

DC Specifications			Electrical Characteristics: Standard Operating Conditions (unless otherwise specified) Operating temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 4.1				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
		Output Low Voltage					
D080	VOL	TXIR, RX, DSR, CTS, and CD pins	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5 V
D083		OSC2	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5 V
		Output High Voltage					
D090	VOH	TXIR, RX, DSR, CTS, and CD pins **(Note 1)**	VDD - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5 V
D092		OSC2	VDD - 0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5 V
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15	pF	when external clock is used to drive OSC1.
D101	CIO	All Input or Output pins	—	—	50	pF	

Note 1: Negative current is defined as coming out of the pin.

4.2 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

4.2.1 TIMING CONDITIONS

The temperature and voltages specified in Table 4-2 apply to all timing specifications unless otherwise noted. Figure 4-2 specifies the load conditions for the timing specifications.

TABLE 4-1: SYMBOLOGY

1. TppS2ppS		2. TppS	
T			
F	Frequency	T	Time
E	Error		

Lowercase letters (pp) and their meanings:

pp			
io	Input or Output pin	osc	Oscillator
rx	Receive	tx	Transmit
bitclk	RX/TX BITCLK	RST	Reset
drt	Device Reset Timer		

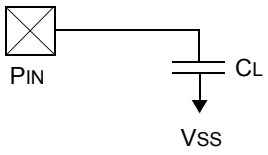
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (high-impedance)	V	Valid
L	Low	Z	High-impedance

TABLE 4-2: AC TEMPERATURE AND VOLTAGE SPECIFICATIONS

AC Specifications	**Electrical Characteristics:** **Standard Operating Conditions (unless otherwise stated):** Operating temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating voltage VDD range as described in DC spec Section 4.1.

FIGURE 4-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



CL = 50 pF for all pins except OSC2
15 pF for OSC2 when external clock is used to drive OSC1

4.3 Timing Diagrams and Specifications

FIGURE 4-3: EXTERNAL CLOCK TIMING

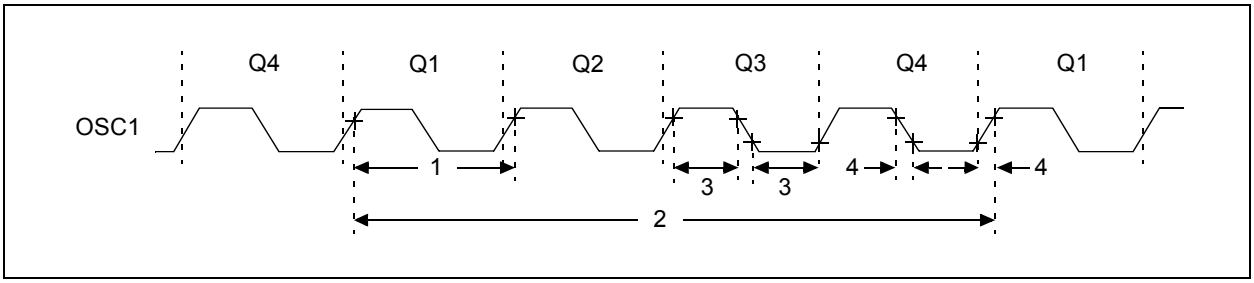


TABLE 4-3: EXTERNAL CLOCK TIMING REQUIREMENTS

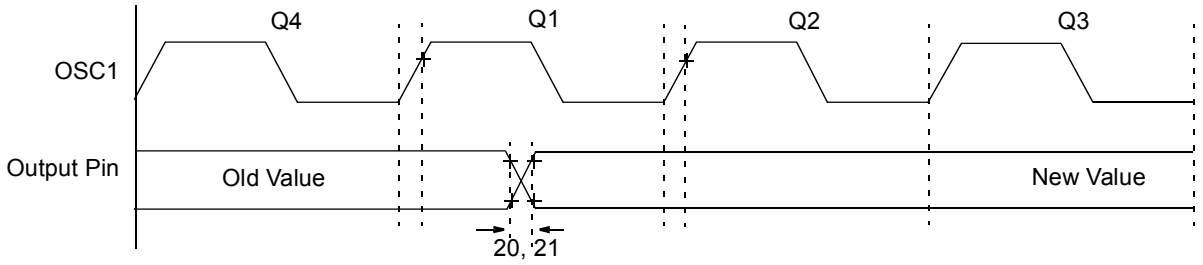
AC Specifcations			Electrical Characteristics: Standard Operating Conditions (unless otherwise specified): Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 4.1				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
1	TOSC	External CLKIN Period (2, 3) Oscillator Period (2)	90.422 90.422 90.422	— — —	90.422 — 90.422	ns ns ns	Device Operation Disable Clock for low power
1A	FOSC	External CLKIN Frequency (2, 3) Oscillator Frequency (2)	11.0592 11.0592	— —	11.0592 11.0592	MHz MHz	
1B	FERR	Error in Frequency	—	—	± 0.01	%	
1C	ECLK	External Clock Error	—	—	± 0.01	%	
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	15	ns	

Note 1: Data in the Typical ("Typ") column is at 5 V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on oscillator characterization data under standard operating conditions. Exceeding these specified limits may result in unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: A duty cycle of no more than 60% (High time/Low time or Low time/High time) is recommended for external clock inputs.

FIGURE 4-4: OUTPUT WAVEFORM



Note: Refer to Figure 4-2 for load conditions.

TABLE 4-4: OUTPUT TIMING REQUIREMENTS

AC Specifications			**Electrical Characteristics:** **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 4.1				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
20	ToR	RX and TXIR pin rise time (2)	—	10	25	ns	
21	ToF	RX and TXIR pin fall time (2)	—	10	25	ns	

Note 1: Data in the Typical (“Typ”) column is at 5 V, 25°C unless otherwise stated.

2: See Figure 4-2 for loading conditions.

FIGURE 4-5: $\overline{\text{RESET}}$ AND DEVICE RESET TIMING

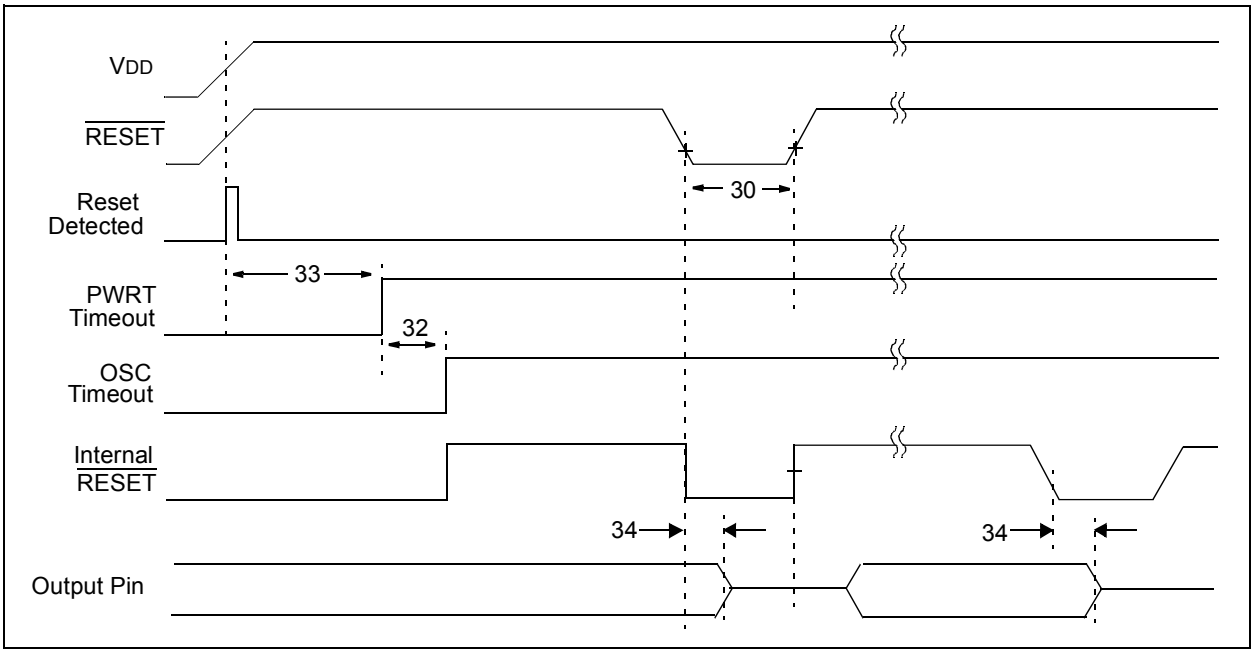
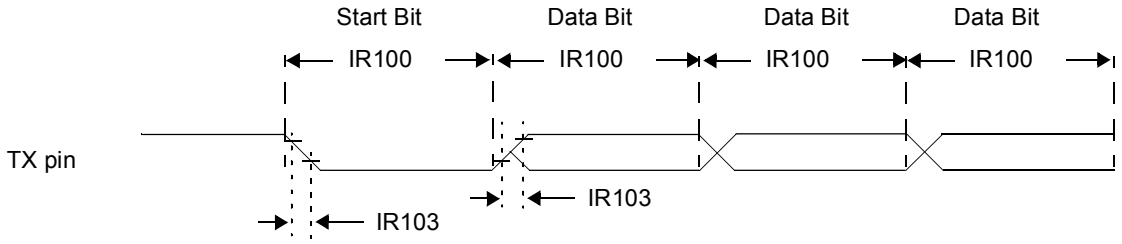


TABLE 4-5: $\overline{\text{RESET}}$ AND DEVICE RESET REQUIREMENTS

AC Specifications			Electrical Characteristics: Standard Operating Conditions (unless otherwise specified): Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 4.1				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TRSTL	$\overline{\text{RESET}}$ Pulse Width (low)	2000	—	—	ns	VDD = 5.0 V
32	TOST	Oscillator Start-up Timer Period	1024	—	1024	TOSC	
33	TPWRT	Power up Timer Period	28	72	132	ms	VDD = 5.0 V
34	TIOZ	Output High-impedance from $\overline{\text{RESET}}$ Low or device Reset	—	—	2	µs	

Note 1: Data in the Typical ("Typ") column is at 5 V, 25°C unless otherwise stated.

FIGURE 4-6: UART ASYNCHRONOUS TRANSMISSION WAVEFORM



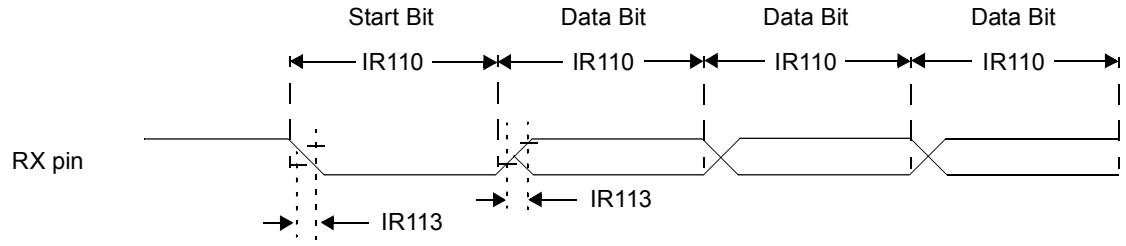
Note: Refer to Figure 4-2 for load conditions.

TABLE 4-6: UART ASYNCHRONOUS TRANSMISSION REQUIREMENTS

AC Specifications			**Electrical Characteristics:** **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 4.1				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
IR100	TTXBIT	Transmit Baud rate	1152	—	1152	TOSC	BAUD2:BAUD0 = 00
			576	—	576	TOSC	BAUD2:BAUD0 = 01
			192	—	192	TOSC	BAUD2:BAUD0 = 10
			96	—	96	TOSC	BAUD2:BAUD0 = 11
IR101	ETXBIT	Transmit (TX pin) Baud rate Error (into MCP2150)	—	—	±2	%	
IR102	ETXIRBIT	Transmit (TXIR pin) Baud rate Error (out of MCP2150) (1)	—	—	±1	%	
IR103	TTXRF	TX pin rise time and fall time	—	—	25	ns	

Note 1: This error is not additive to IR101 parameter.

FIGURE 4-7: UART ASYNCHRONOUS RECEIVE TIMING



Note: Refer to Figure 4-2 for load conditions.

TABLE 4-7: UART ASYNCHRONOUS RECEIVE REQUIREMENTS

AC Specifications			**Electrical Characterisitcs:** **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 4.1				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
IR110	TRXBIT	Receive Baud Rate	1152	—	1152	TOSC	BAUD2:BAUD0 = 00
			576	—	576	TOSC	BAUD2:BAUD0 = 01
			192	—	192	TOSC	BAUD2:BAUD0 = 10
			96	—	96	TOSC	BAUD2:BAUD0 = 11
IR111	ERXBIT	Receive (RXIR pin) Baud rate Error (into MCP2150)	—	—	±1	%	
IR112	ERXBIT	Receive (RX pin) Baud rate Error (out of MCP2150) (1)	—	—	±1	%	
IR113	TTXRF	RX pin rise time and fall time	—	—	25	ns	

Note 1: This error is not additive to the IR111 parameter.

FIGURE 4-8: TXIR WAVEFORMS

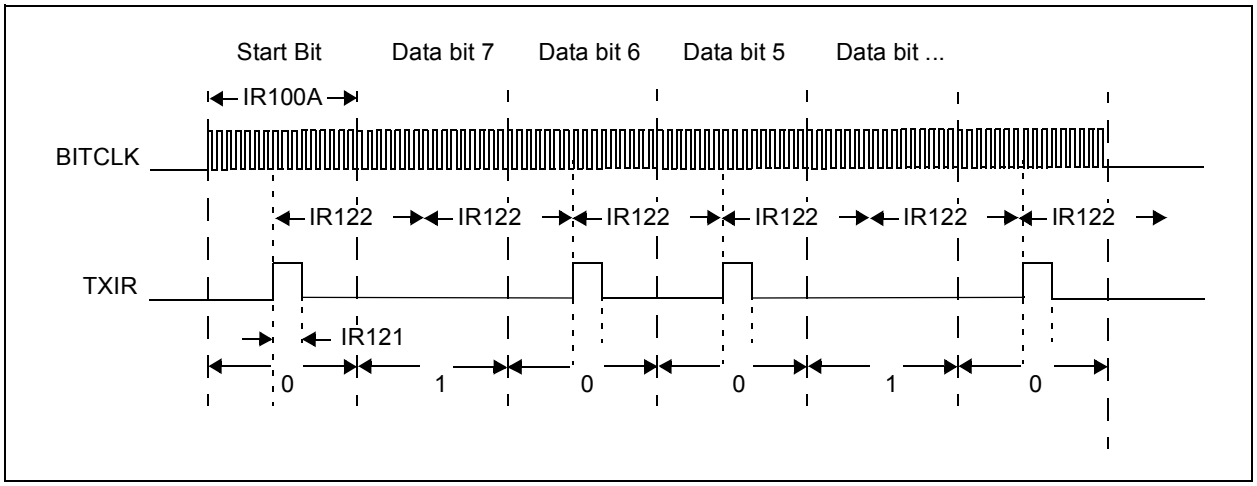


TABLE 4-8: TXIR REQUIREMENTS

AC Specifications			**Electrical Characteristics:** **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 4.1				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
IR100A	TTXIRBIT	Transmit Baud Rate	1152	—	1152	TOSC	BAUD = 9600
			576	—	576	TOSC	BAUD = 19200
			288	—	288	TOSC	BAUD = 38400
			192	—	192	TOSC	BAUD = 57600
			96	—	96	TOSC	BAUD = 115200
IR121	TTXIRPW	TXIR pulse width	24	—	24	TOSC	
IR122	TTXIRP	TXIR bit period (1)	—	16	—	TBITCLK	

Note 1: TBITCLK = TTXBIT/16.

FIGURE 4-9: RXIR WAVEFORMS

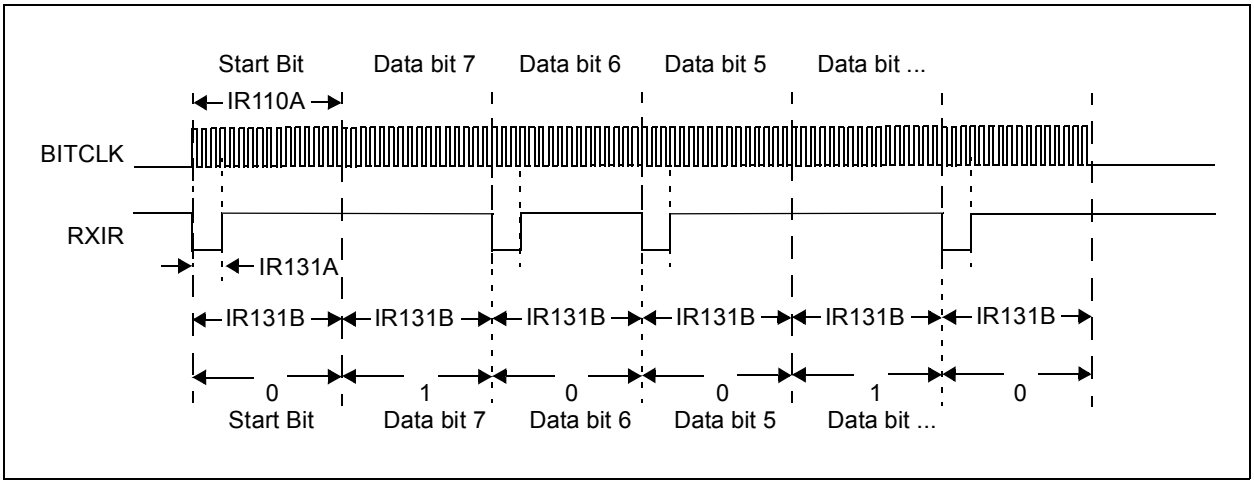


TABLE 4-9: RXIR REQUIREMENTS

AC Specifications			**Electrical Characteristics:** **Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 4.1				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
IR110A	TRXIRBIT	Receive Baud Rate	1152	—	1152	TOSC	BAUD = 9600
			576	—	576	TOSC	BAUD = 19200
			288	—	288	TOSC	BAUD = 38400
			192	—	192	TOSC	BAUD = 57600
			96	—	96	TOSC	BAUD = 115200
IR131A	TRXIRPW	RXIR pulse width	2	—	24	TOSC	
IR132	TRXIRP	RXIR bit period (1)	—	16	—	TBITCLK	

Note 1: TBITCLK = TRXBIT/16.

NOTES:

5.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

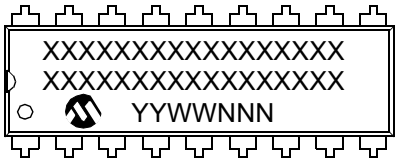
Not available at this time.

NOTES:

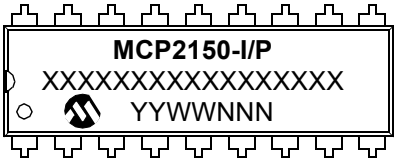
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

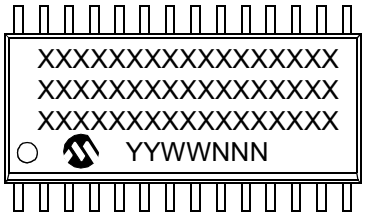
18-Lead PDIP (300 mil)



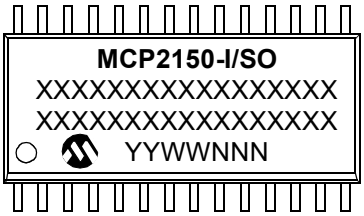
Example:



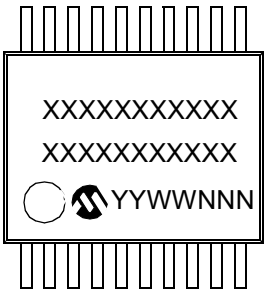
18-Lead SOIC (300 mil)



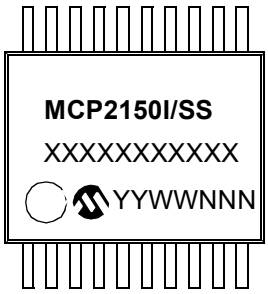
Example:



20-Lead SSOP (209 mil, 5.30 mm)



Example:

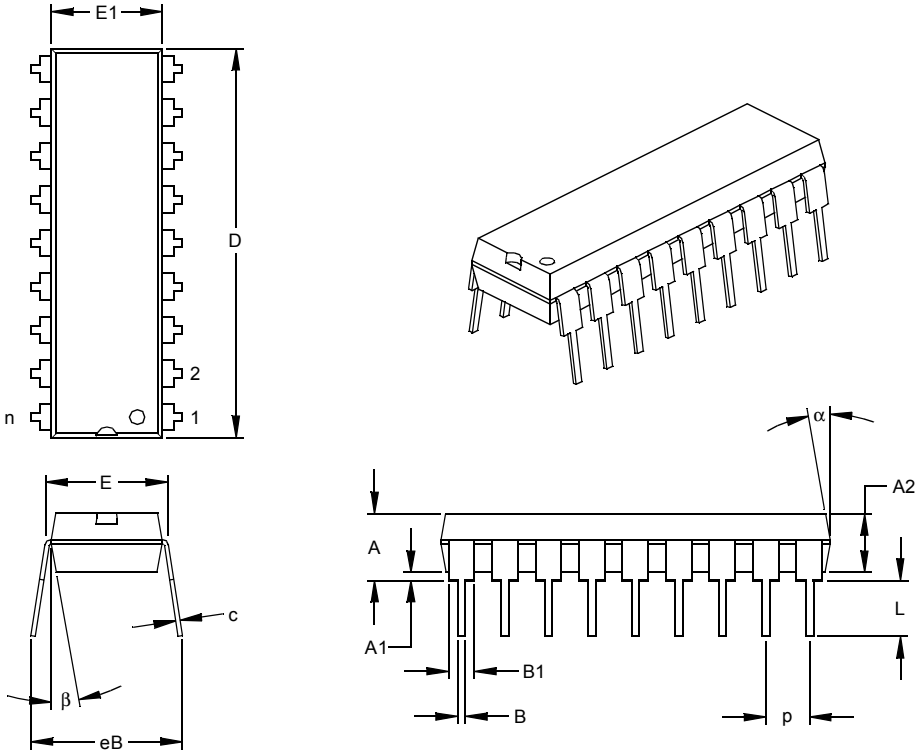


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard device marking consists of Microchip part number, year code, week code and traceability code.

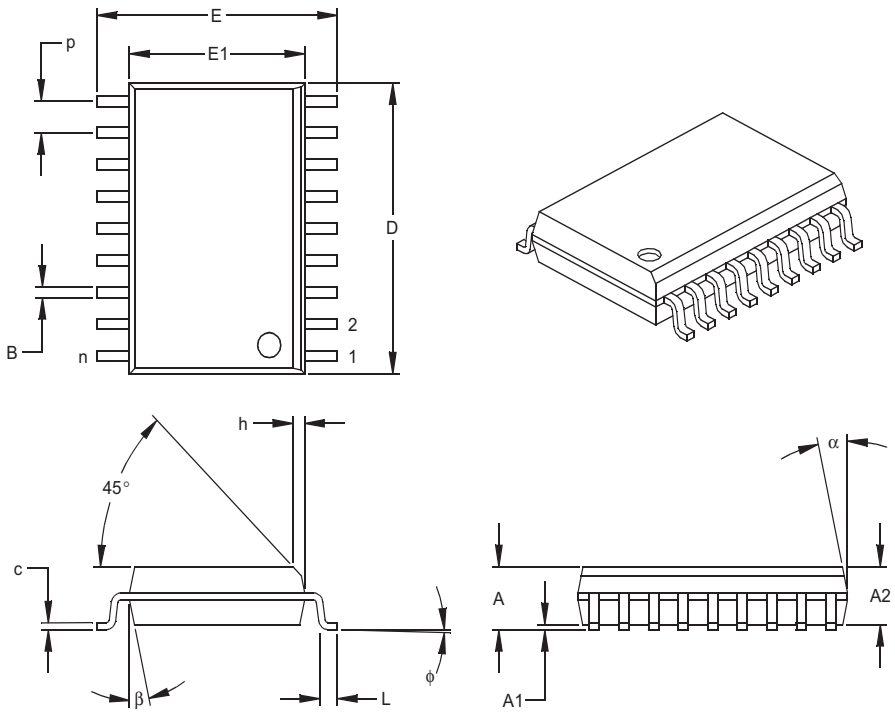
18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-007

18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

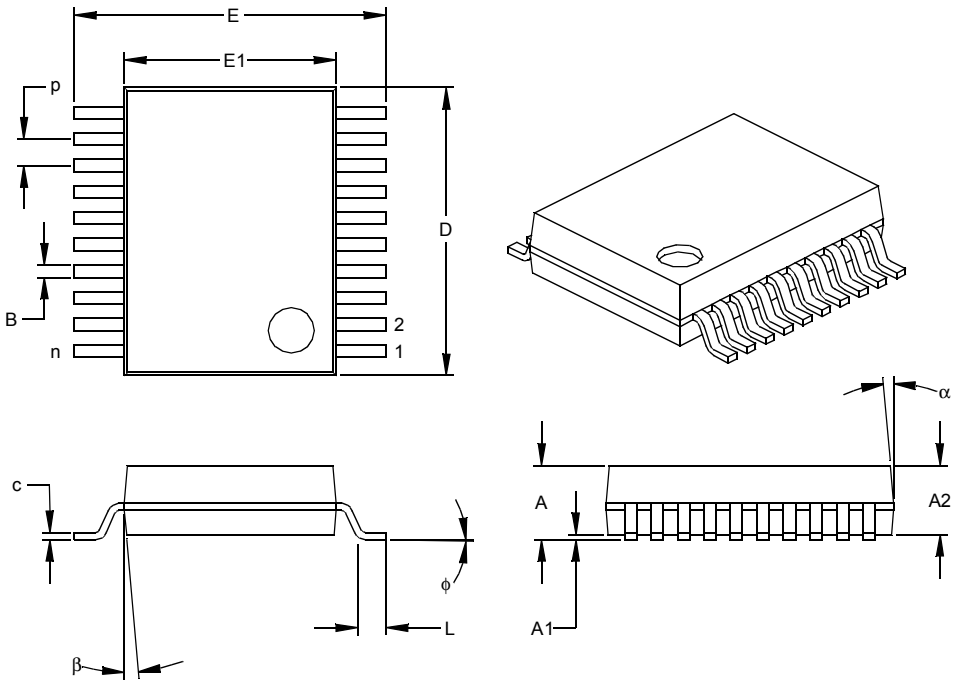


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-051

20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	c	.004	.007	.010	0.10	0.18	0.25
Foot Angle	φ	0	4	8	0.00	101.60	203.20
Lead Width	B	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-150
Drawing No. C04-072

APPENDIX A: REVISION HISTORY

Revision A

- This is a new data sheet

Revision B

- Updated feature list
- Enhanced pin descriptions. Refer to Table 1-2
- Added description for programmable device ID
- Standardize use of terms for Host Controller and Primary Device

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device	MCP2150: Infrared Communications Controller MCP2150T: Infrared Communications Controller (Tape and Reel)	
Temperature Range	I =	-40°C to +85°C
Package	P =	Plastic DIP (300 mil, Body), 18-lead
	SO =	Plastic SOIC (300 mil, Body), 18-lead
	SS =	Plastic SSOP (209 mil, Body), 20-lead

Examples:

a) MCP2150-I/P = Industrial Temp., PDIP packaging

b) MCP2150-I/SO = Industrial Temp., SOIC package

c) MCP2150T-I/SS = Tape and Reel, Industrial Temp., SSOP package

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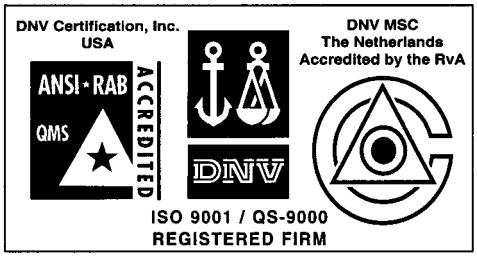

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