## ■ FEATURES

- **Clock**
  - Built-in PLL clock frequency multiplication circuit
  - Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 6 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 24 MHz).
  - Operation by sub-clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed. (devices without S-suffix only)
  - Minimum execution time of instruction : 42 ns (when operating with 4-MHz oscillation clock, and 6-time multiplied PLL clock).
- **16 Mbyte CPU memory space**
  - 24-bit internal addressing
- **Instruction system best suited to controller**
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - Enhanced multiply-divide instructions and RETI instructions
  - Enhanced high-precision computing with 32-bit accumulator
- **Instruction system compatible with high-level language (C language) and multitask**
  - Employing system stack pointer
  - Enhanced various pointer indirect instructions
  - Barrel shift instructions
- **Increased processing speed**
  - 4-byte instruction queue
- **Powerful interrupt function**
  - Powerful 8-level, 34-condition interrupt feature
  - Up to 16 external interrupts are supported
- **Automatic data transfer function independent of CPU**
  - Extended intelligent I/O service function ($EI^2OS$) : up to 16 channels
  - DMA : up to 16 channels
- **Low power consumption (standby) mode**
  - Sleep mode (a mode that halts CPU operating clock)
  - Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and clock timer only)
  - Watch mode (a mode that operates sub clock and clock timer only)
  - Stop mode (a mode that stops oscillation clock and sub clock)
  - CPU blocking operation mode
- **Process**
  - CMOS technology
- **I/O port**
  - General-purpose input/output port (CMOS output)
    - 80 ports (devices without S-suffix)
    - 82 ports (devices with S-suffix)

*(Continued)*

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- **Timer**
  - Time-base timer, clock timer, watchdog timer : 1 channel
  - 8/16-bit PPG timer : 8-bit X 16 channels, or 16-bit X 8 channels
  - 16-bit reload timer : 4 channels
  - 16- bit input/output timer
    - 16-bit free run timer : 2 channel (FRT0 : ICU 0/1/2/3, OCU 0/1/2/3, FRT1 : ICU 4/5/6/7, OCU 4/5/6/7)
    - 16- bit input capture: (ICU) : 8 channels
    - 16-bit output compare : (OCU) : 8 channels
- **UART (LIN/SCI) : 4 channels**
  - Equipped with full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transmission is available
- **$I^2C$ interface* : 2 channels**
  - Up to 400 kbit/s transfer rate
- **DTP/External interrupt : 16 channels, CAN wakeup : 2 channels**
  - Module for activation of extended intelligent I/O service (EI$^2$OS), DMA, and generation of external interrupt.
- **Delay interrupt generator module**
  - Generates interrupt request for task switching.
- **8/10-bit A/D converter : 24 channels**
  - Resolution is selectable between 8-bit and 10-bit.
  - Activation by external trigger input is allowed.
  - Conversion time : 3 μs (at 24-MHz machine clock, including sampling time)
- **Program patch function**
  - Address matching detection for 6 address pointers.
- **Internal voltage regulator**
  - Supports 3 V MCU core, offering low EMI and low power consumption figures
- **Programmable input levels**
  - Automotive/CMOS-Schmitt (initial level is Automotive in Single chip mode)
  - TTL level (initial level for External bus mode)
- **ROM security function**
  - Protects the content of ROM (MASK ROM device only)
- **Flash security function**
  - Protects the content of Flash (Flash device only)
- **External bus interface**
- **Clock monitor function**

* : $I^2C$ license :
Purchase of Fujitsu $I^2C$ components conveys a license under the Philips $I^2C$ Patent Rights to use, these components in an $I^2C$ system provided that the system conforms to the $I^2C$ standard Specification as defined by Philips.

## ■ PRODUCT LINEUP

| Part Number / Parameter | MB90F867A (S) , MB90867A (S) | MB90V340(S) |
|---|---|---|
| CPU | F²MC-16LX CPU | |
| System clock | On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops)<br>Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6) | |
| ROM | Boot-block,Flash memory<br>128 Kbytes | External |
| RAM | 6 Kbytes | 30 Kbytes |
| Emulator-specific power supply*1 | — | Yes |
| Technology | 0.35 µm CMOS with on-chip voltage regulator for internal power supply + Flash memory with<br>On-chip charge pump for programming voltage | 0.35 µm CMOS with on-chip voltage regulator for internal power supply |
| Operating voltage range | 3.5 V to 5.5 V : at normal operating (not using A/D converter)<br>4.0 V to 5.5 V : at using A/D converter/Flash programming<br>4.5 V to 5.5 V : at using external bus | 5 V ± 10% |
| Temperature range | −40 °C to +105 °C | — |
| Package | QFP-100, LQFP-100 | PGA-299 |
| UART | 4 channels | 5 channels |
| | Wide range of baud rate settings using a dedicated reload timer<br>Special synchronous options for adapting to different synchronous serial protocols<br>LIN functionality working either as master or slave LIN device | |
| I²C (400 Kbit/s) | 2 channel | |
| A/D Converter | 24 input channels | |
| | 10-bit or 8-bit resolution<br>Conversion time : Min 3 µs include sample time (per one channel) | |
| 16-bit Reload Timer (4 channels) | Operation clock frequency : fsys/2¹, fsys/2³, fsys/2⁵ (fsys = Machine clock frequency)<br>Supports External Event Count function | |
| 16-bit I/O Timer (2 channels) | Signals an interrupt when overflowing<br>Supports Timer Clear when a match with Output Compare (Channel 0, 4)<br>Operation clock freq. : fsys, fsys/2¹, fsys/2², fsys/2³, fsys/2⁴, fsys/2⁵, fsys/2⁶, fsys/2⁷<br>(fsys = Machine clock freq.)<br>I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3<br>I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7 | |
| 16-bit Output Compare (8 channels (16-bit) / 16 channels (8-bit) ) | Signals an interrupt when 16-bit I/O Timer match output compare registers.<br>A pair of compare registers can be used to generate an output signal. | |
| 16-bit Input Capture (8 channels) | Rising edge, falling edge or rising & falling edge sensitive<br>Signals an interrupt upon external event | |

*(Continued)*

*(Continued)*

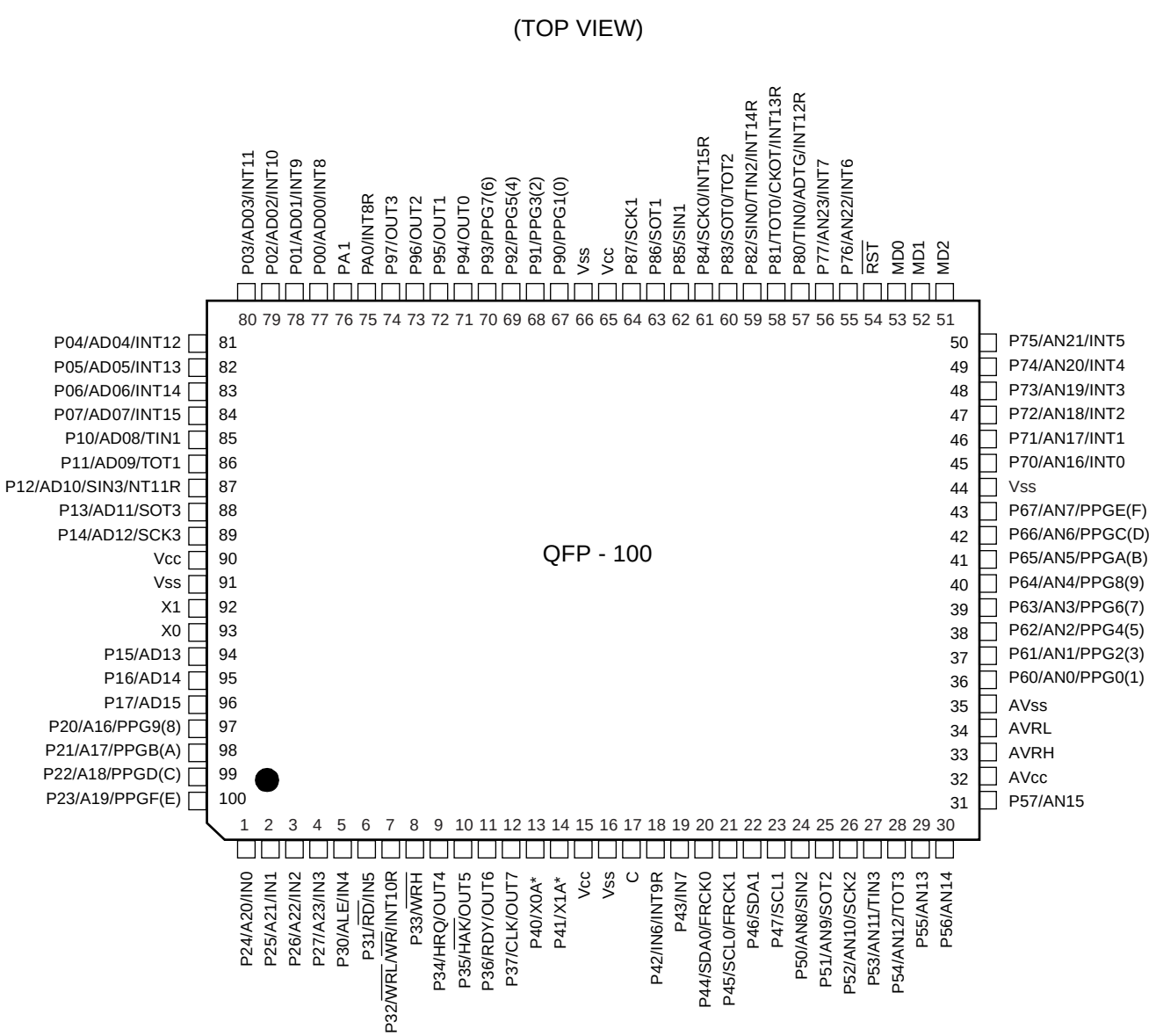
| Part Number / Parameter | MB90F867A (S) , MB90867A (S) | MB90V340(S) |
|---|---|---|
| 8/16-bit Programmable Pulse Generator (8 channels) | Supports 8-bit and 16-bit operation modes<br>Sixteen 8-bit reload counters<br>Sixteen 8-bit reload registers for L pulse width<br>Sixteen 8-bit reload registers for H pulse width<br>A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter<br>Operation clock freq. : fsys, fsys/$2^1$, fsys/$2^2$, fsys/$2^3$, fsys/$2^4$ or 128 µs@fosc = 4 MHz<br>(fsys = Machine clock frequency, fosc = Oscillation clock frequency) | |
| CAN Interface | — | 3 channels |
| External Interrupt (16 channels) | Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, expanded inteligent I/O services (EI$^2$OS) and DMA | |
| D/A converter | — | 2 channels |
| Up to100 kHz Subclock for low power operation | devices with 'S'-suffix : without subclock<br>devices without 'S'-suffix : with subclock | |
| I/O Ports | Virtually all external pins can be used as general purpose I/O port<br>All push-pull outputs<br>Bit-wise settable as input/output or peripheral signal<br>Settable in pin-wise of 8 as CMOS schmitt trigger/ automotive inputs (default)<br>TTL input level settable for external bus (32-pin only for external bus) | |
| Flash Memory | Supports automatic programming, Embedded Algorithm™*2<br>Write/Erase/Erase-Suspend/Resume commands<br>A flag indicating completion of the algorithm<br>Number of erase cycles : 10,000 times<br>Data retention time : 20 years<br>Boot block configuration<br>Erase can be performed on each block<br>Block protection with external programming voltage<br>Flash Security Feature for protecting the content of the Flash | — |

*1 : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

*2 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

## ■ PIN ASSIGNMENTS

- MB90F867A (S) , MB90867A (S)




(FPT-100P-M06)

* : MB90F867A, MB90867A : X0A, X1A
MB90F867AS, MB90867AS : P40, P41

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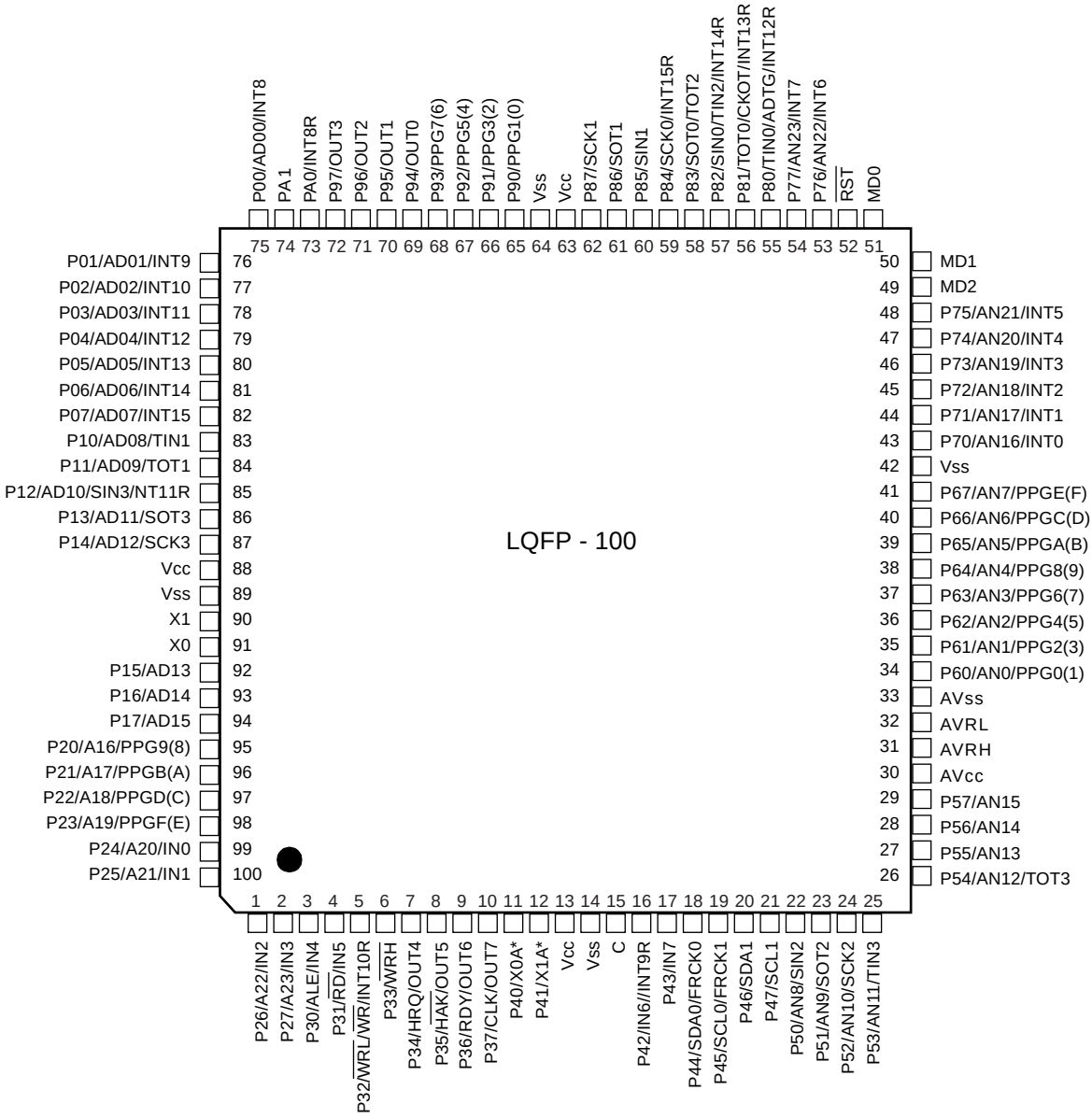
(TOP VIEW)




(FPT-100P-M05)

* : MB90F867A, MB90867A : X0A, X1A
MB90F867AS, MB90867AS : P40, P41

## ■ PIN DESCRIPTION

| Pin No. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP100*2 | QFP100*1 | | | |
| 90 | 92 | X1 | A | Oscillation output |
| 91 | 93 | X0 | | Oscillation input |
| 52 | 54 | $\overline{\text{RST}}$ | E | Reset input |
| 75 to 82 | 77 to 84 | P00 to P07 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD00 to AD07 | | I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled. |
| | | INT8 to INT15 | | External interrupt request input pins for INT8 to INT15. |
| 83 | 85 | P10 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD08 | | I/O pin for bit 8 of the external address/data bus. This function is enabled when the external bus is enabled. |
| | | TIN1 | | Event input pin for the reload timer 1 |
| 84 | 86 | P11 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD09 | | I/O pin for bit 9 of the external address/data bus. This function is enabled when the external bus is enabled. |
| | | TOT1 | | Output pin for the reload timer 1 |
| 85 | 87 | P12 | N | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD10 | | I/O pin for bit 10 of the external address/data bus. This function is enabled when the external bus is enabled. |
| | | SIN3 | | Serial data input pin for UART3 |
| | | INT11R | | Sub external interrupt request input pin for INT11 |
| 86 | 88 | P13 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD11 | | I/O pin for bit 11 of the external address/data bus. This function is enabled when the external bus is enabled. |
| | | SOT3 | | Serial data output pin for UART3 |
| 87 | 89 | P14 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD12 | | I/O pin for bit 12 of the external address/data bus. This function is enabled when the external bus is enabled. |
| | | SCK3 | | Clock I/O pin for UART3 |

*(Continued)*

| Pin No. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP100*2 | QFP100*1 | | | |
| 92 | 94 | P15 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD13 | | I/O pin for bit 13 of the external address/data bus.<br>This function is enabled when the external bus is enabled. |
| | | SIN4 | | Serial data input pin for UART4 (MB90V340 only) |
| 93 | 95 | P16 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD14 | | I/O pin for bit 14 of the external address/data bus.<br>This function is enabled when the external bus is enabled. |
| | | SOT4 | | Serial data output pin for UART4 (MB90V340 only) |
| 94 | 96 | P17 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD15 | | I/O pin for bit 15 of the external address/data bus. This function is enabled when the external bus is enabled. |
| | | SCK4 | | Clock I/O pin for UART4 (MB90V340 only) |
| 95 to 98 | 97 to 100 | P20 to P23 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1. |
| | | A16 to A19 | | Output pins for A16 to A19 of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19). |
| | | PPG9,PPGB, PPGD,PPGF | | Output pins for PPGs |
| 99 to 2 | 1 to 4 | P24 to P27 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1. |
| | | A20 to A23 | | Output pins for A20 to A23 of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23). |
| | | IN0 to IN3 | | Data sample input pins for input captures ICU0 to ICU3 |
| 3 | 5 | P30 | G | General purpose I/O.The register can be set to select whether to use a pull-up resistor.This function is enabled in single-chip mode. |
| | | ALE | | Address latch enable output pin. This function is enabled when the external bus is enabled. |
| | | IN4 | | Data sample input pin for input capture ICU4 |

*(Continued)*

| Pin No. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP100*2 | QFP100*1 | | | |
| 4 | 6 | P31 | G | General purpose I/O.The register can be set to select whether to use a pull-up resistor.This function is enabled in single-chip mode. |
| | | $\overline{RD}$ | | Read strobe output pin for the data bus. This function is enabled when the external bus is enabled. |
| | | IN5 | | Data sample input pin for input capture ICU5 |
| 5 | 7 | P32 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the $\overline{WR}$/$\overline{WRL}$ pin output disabled. |
| | | $\overline{WRL}$ / $\overline{WR}$ | | Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{WR}$/$\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access while $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access. |
| | | RX2 | | RX input pin for CAN2 Interface (MB90V340 only) |
| | | INT10R | | Sub external interrupt request input pin for INT10 |
| 6 | 8 | P33 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor.This function is enabled either in single-chip mode or with the $\overline{WRH}$ pin output disabled. |
| | | $\overline{WRH}$ | | Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled. |
| | | TX2 | | TX Output pin for CAN2 (MB90V340 only) |
| 7 | 9 | P34 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled. |
| | | HRQ | | Hold request input pin. This function is enabled when both the external bus and the hold function are enabled. |
| | | OUT4 | | Waveform output pin for output compare OCU4 |
| 8 | 10 | P35 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled. |
| | | $\overline{HAK}$ | | Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled. |
| | | OUT5 | | Waveform output pin for output compare OCU5 |
| 9 | 11 | P36 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the external ready function disabled. |
| | | RDY | | Ready input pin. This function is enabled when both the external bus and the external ready function are enabled. |
| | | OUT6 | | Waveform output pin for output compare OCU6 |

*(Continued)*

| Pin No. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP100*2 | QFP100*1 | | | |
| 10 | 12 | P37 | G | General purpose I/O. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the CLK output disabled. |
| | | CLK | | CLK output pin. This function is enabled when both the external bus and CLK output are enabled. |
| | | OUT7 | | Waveform output pin for output compare OCU7 |
| 11 to 12 | 13 to 14 | P40 , P41 | F | General purpose I/O (devices with S-suffix) |
| | | X0A , X1A | B | Oscillator input pins for sub-clock (devices without S-suffix) |
| 16 | 18 | P42 | F | General purpose I/O |
| | | IN6 | | Data sample input pin for input capture ICU6 |
| | | RX1 | | RX input pin for CAN1 (MB90V340 (S) only) |
| | | INT9R | | Sub external interrupt request input pin for INT10 |
| 17 | 19 | P43 | F | General purpose I/O |
| | | IN7 | | Data sample input pin for input capture ICU7 |
| | | TX1 | | TX Output pin for CAN1 (MB90V340 (S) only) |
| 18 | 20 | P44 | H | General purpose I/O |
| | | SDA0 | | Serial data I/O pin for $I^2C$ 0 |
| | | FRCK0 | | Input for the 16-bit I/O Timer 0 |
| 19 | 21 | P45 | H | General purpose I/O |
| | | SCL0 | | Serial clock I/O pin for $I^2C$ 0 |
| | | FRCK1 | | Input for the 16-bit I/O Timer 1 |
| 20 | 22 | P46 | H | General purpose I/O |
| | | SDA1 | | Serial data I/O pin for $I^2C$ 1 |
| 21 | 23 | P47 | H | General purpose I/O |
| | | SCL1 | | Serial clock I/O pin for $I^2C$ 1 |
| 22 | 24 | P50 | O | General purpose I/O |
| | | AN8 | | Analog input pin for the A/D converter |
| | | SIN2 | | Serial data input pin for UART2 |
| 23 | 25 | P51 | I | General purpose I/O |
| | | AN9 | | Analog input pin for the A/D converter |
| | | SOT2 | | Serial data output pin for UART2 |
| 24 | 26 | P52 | I | General purpose I/O |
| | | AN10 | | Analog input pin for the A/D converter |
| | | SCK2 | | Clock I/O pin for UART2 |
| 25 | 27 | P53 | I | General purpose I/O |
| | | AN11 | | Analog input pin for the A/D converter |
| | | TIN3 | | Event input pin for the reload timer 3 |

*(Continued)*

| Pin No. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP100*2 | QFP100*1 | | | |
| 26 | 28 | P54 | I | General purpose I/O |
| | | AN12 | | Analog input pin for the A/D converter |
| | | TOT3 | | Output pin for the reload timer 3 |
| 27 | 29 | P55 | I | General purpose I/O |
| | | AN13 | | Analog input pin for the A/D converter |
| 28, 29 | 30, 31 | P56 to P57 | J | General purpose I/O |
| | | AN14 to AN15 | | Analog input pin for the A/D converter |
| | | DA00 to DA01 | | D/A converter analog output pins (MB90V340 only) |
| 34 to 41 | 36 to 43 | P60 to P67 | I | General purpose I/O |
| | | AN0 to AN7 | | Analog input pins for the A/D converter |
| | | PPG0, 2, 4, 6, 8, A, C, E | | Output pins for PPGs |
| 43 to 48, 53, 54 | 45 to 50, 55, 56 | P70 to P77 | I | General purpose I/O |
| | | AN16 to AN23 | | Analog input pins for the A/D converter (devices with C-suffix) |
| | | INT0 to INT7 | | External interrupt request input pins for INT0 to INT7 |
| 55 | 57 | P80 | F | General purpose I/O |
| | | TIN0 | | Event input pin for the reload timers 0 |
| | | ADTG | | Trigger input pin for the A/D converter |
| | | INT12R | | Sub external interrupt request input pin for INT12 |
| 56 | 58 | P81 | F | General purpose I/O |
| | | TOT0 | | Output pin for the reload timer 0 |
| | | CKOT | | Output pin for the clock monitor |
| | | INT13R | | Sub external interrupt request input pin for INT13 |
| 57 | 59 | P82 | M | General purpose I/O |
| | | SIN0 | | Serial data input pin for UART0 |
| | | TIN2 | | Event input pin for the reload timers 2 |
| | | INT14R | | Sub external interrupt request input pin for INT14 |
| 58 | 60 | P83 | F | General purpose I/O |
| | | SOT0 | | Serial data output pin for UART0 |
| | | TOT2 | | Output pin for the reload timer 2 |
| 59 | 61 | P84 | F | General purpose I/O |
| | | SCK0 | | Clock I/O pin for UART0 |
| | | INT15R | | Sub external interrupt request input pin for INT15 |
| 60 | 62 | P85 | M | General purpose I/O |
| | | SIN1 | | Serial data input pin for UART1 |
| 61 | 63 | P86 | F | General purpose I/O |
| | | SOT1 | | Serial data output pin for UART1 |

*(Continued)*

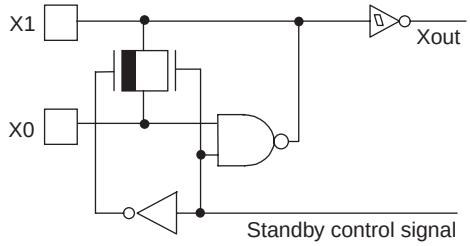
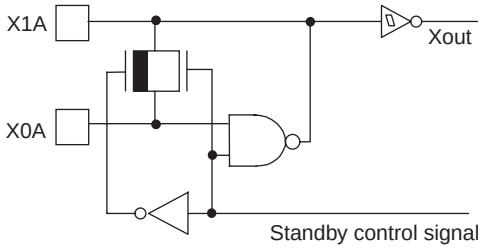
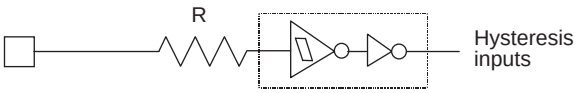
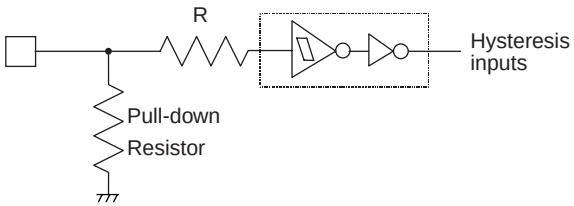
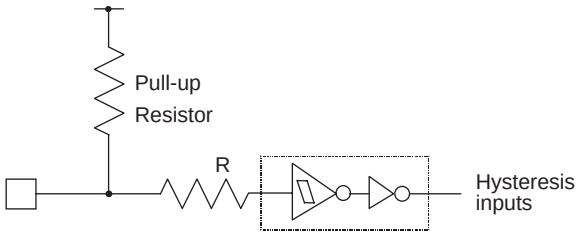
*(Continued)*

| Pin No. | | Pin name | Circuit type | Function |
|---|---|---|---|---|
| LQFP100*2 | QFP100*1 | | | |
| 62 | 64 | P87 | F | General purpose I/O |
| | | SCK1 | | Clock I/O pin for UART1 |
| 65 to 68 | 67 to 70 | P90 to P93 | F | General purpose I/O |
| | | PPG1, 3, 5, 7 | | Output pins for PPGs |
| 69 to 72 | 71 to 74 | P94 to P97 | F | General purpose I/O |
| | | OUT0 to OUT3 | | Waveform output pins for output compares OCU0 to OCU3. This function is enabled when the OCU enables waveform output. |
| 73 | 75 | PA0 | F | General purpose I/O |
| | | RX0 | | RX input pin for CAN0 (MB90V340 (s) only) |
| | | INT8R | | Sub external interrupt request input pin for INT8 |
| 74 | 76 | PA1 | F | General purpose I/O |
| | | TX0 | | TX Output pin for CAN0 (MB90V340 (s) only) |
| 30 | 32 | $AV_{CC}$ | K | Vcc power input pin for analog circuits |
| 31 | 33 | AVRH | L | Reference voltage input for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to $AV_{CC}$. |
| 32 | 34 | AVRL | K | Lower reference voltage input for the A/D Converter |
| 33 | 35 | $AV_{SS}$ | K | Vss power input pin for analog circuits |
| 50, 51 | 52, 53 | MD1, MD0 | C | Input pins for specifying the operating mode. The pins must be directly connected to Vcc or Vss |
| 49 | 51 | MD2 | D | Input pin for specifying the operating mode. The pins must be directly connected to Vcc or Vss. |
| 13<br>63<br>88 | 15<br>65<br>90 | $V_{CC}$ | — | Power (3.5 V to 5.5 V) input pins |
| 14<br>42<br>64<br>89 | 16<br>44<br>66<br>91 | $V_{SS}$ | — | Power (0V) input pins |
| 15 | 17 | C | K | This is the power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 µF ceramic capacitor. |

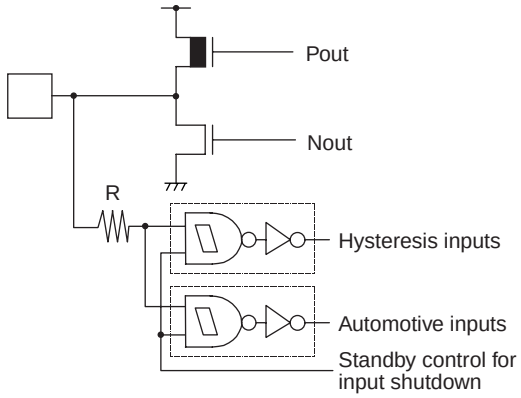
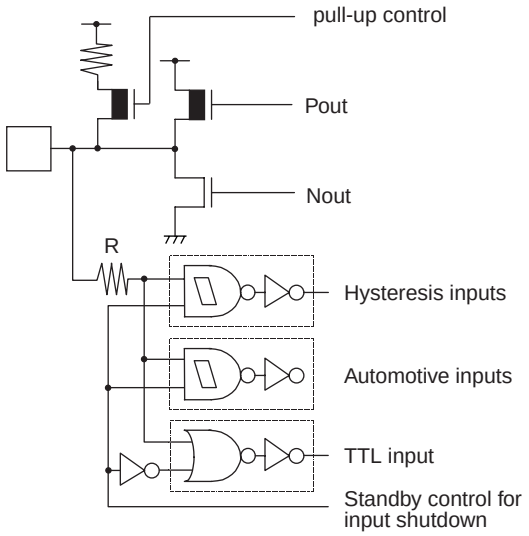
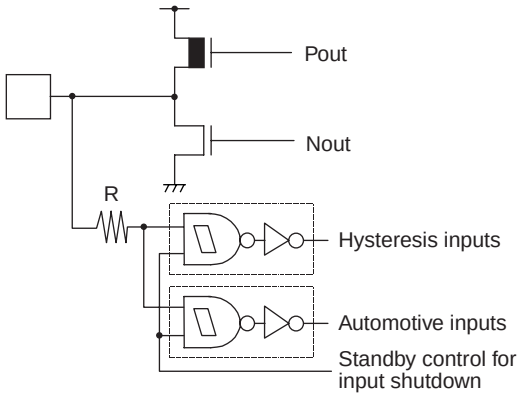
*1 : FPT-100P-M06

*2 : FPT-100P-M05

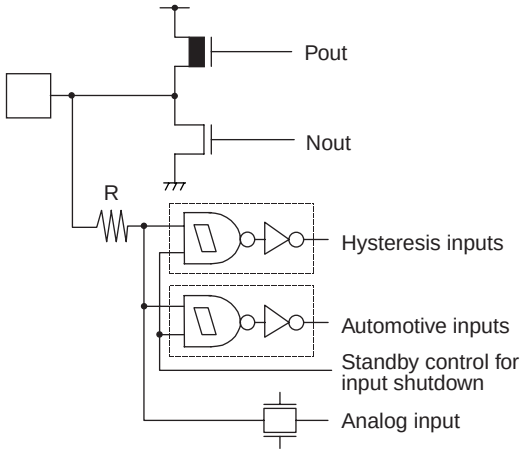
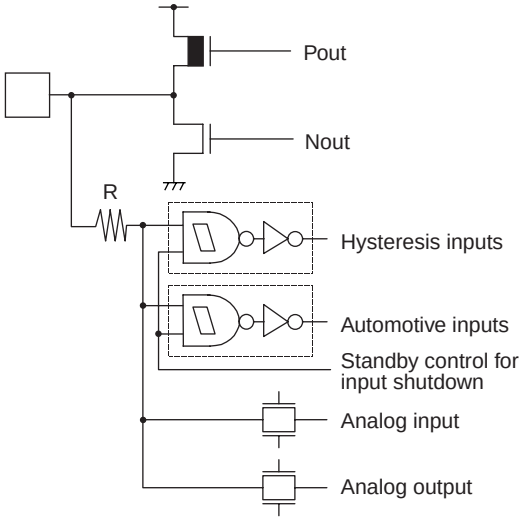
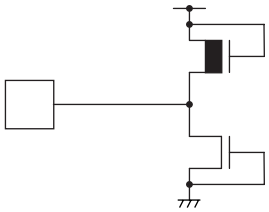
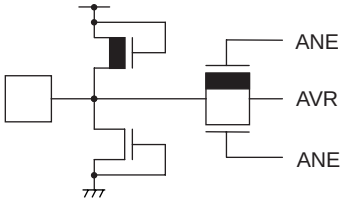
## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | Oscillation circuit<br>• High-speed oscillation feedback resistor = approx. 1 MΩ |
| B |  | Oscillation circuit<br>• Low-speed oscillation feedback resistor = approx. 10 MΩ |
| C |  | Mask ROM and EVA device:<br>• CMOS Hysteresis input pin<br><br>Flash device:<br>• CMOS input pin |
| D |  | Mask ROM and EVA device:<br>• CMOS Hysteresis input pin<br>• Pull-down resistor valule: approx. 50 kΩ<br><br>Flash device:<br>• CMOS input pin<br>• No Pull-down |
| E |  | CMOS Hysteresis input pin<br>• Pull-up resistor valule: approx. 50 kΩ |

*(Continued)*

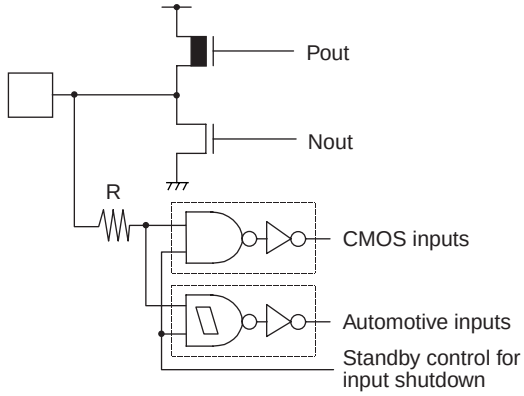
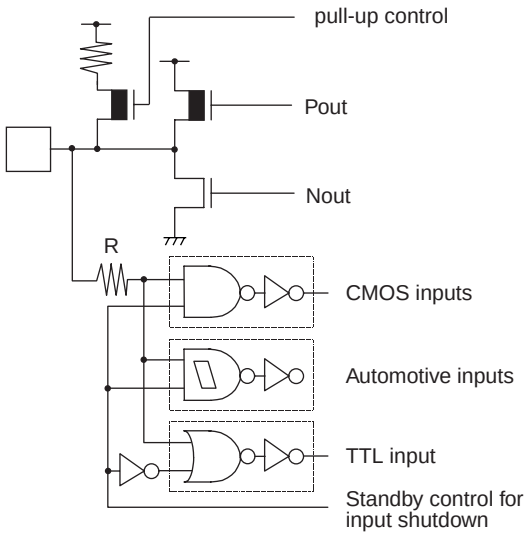
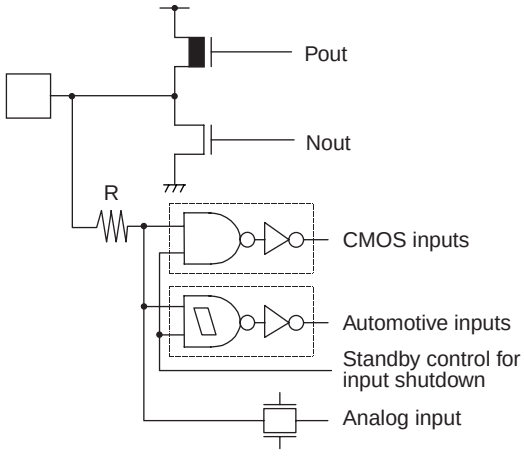
| Type | Circuit | Remarks |
|---|---|---|
| F |  | • CMOS level output($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS hysteresis inputs (With the stand-by-time input shutdown function)<br>• Automotive input (With the standby-time input shutdown function) |
| G |  | • CMOS level output($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS hysteresis inputs (With the stand-by-time input shutdown function)<br>• Automotive input (With the standby-time input shutdown function)<br>• TTL input (With the standby-time input shutdown function)<br>• Programmalble pullup resistor: 50 kΩ approx. |
| H |  | • CMOS level output($I_{OL}$ = 3 mA, $I_{OH}$ = –3 mA)<br>• CMOS hysteresis inputs (With the stand-by-time input shutdown function)<br>• Automotive input (With the standby-time input shutdown function) |

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| I |  | • CMOS level output($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS hysteresis inputs (With the standby-time input shutdown function)<br>• Automotive input (With the standby-time input shutdown function)<br>• A/D analog input |
| J |  | • CMOS level output($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• D/A analg output<br>• CMOS hysteresis inputs (With the standby-time input shutdown function)<br>• Automotive input (With the standby-time input shutdown function)<br>• A/D analog input |
| K |  | • Power supply input protection circuit |
| L |  | • A/D converter reference voltage power supply input pin, with the protection circuit<br>• Flash devices do not have a protection circuit against $V_{CC}$ for pin AVRH |

*(Continued)*

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| M |  | • CMOS level output($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS inputs (With the standby-time input shutdown function)<br>• Automotive input (With the standby-time input shutdown function) |
| N |  | • CMOS level output($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS inputs (With the standby-time input shutdown function)<br>• Automotive input (With the standby-time input shutdown function)<br>• TTL input (With the standby-time input shutdown function)<br>Programmable pullup registor:50 kΩ approx. |
| O |  | • CMOS level output($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>• CMOS inputs (With the standby-time input shutdown function)<br>• Automotive input (With the standby-time input shutdown function)<br>• A/D analog input |

## ■ HANDLING DEVICES

**Special care is required for the following when handling the device :**

- Preventing latch-up
- Treatment of unused pins
- Using external clock
- Precautions for when not using a sub clock signal
- Notes on during operation of PLL clock mode
- Power supply pins ($V_{CC}$/$V_{SS}$)
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter
- Notes on Energization
- Stabilization of power supply voltage
- Initialization
- Port0 to port3 output during Power-on**(External-bus mode)**
- Flash security Function

### 1. Preventing latch-up

**CMOS IC chips may suffer latch-up under the following conditions** :

- A voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between $V_{CC}$ and $V_{SS}$.
- The $AV_{CC}$ power supply is applied before the $V_{CC}$ voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage ($AV_{CC}$, AVRH) exceed the digital power-supply voltage.

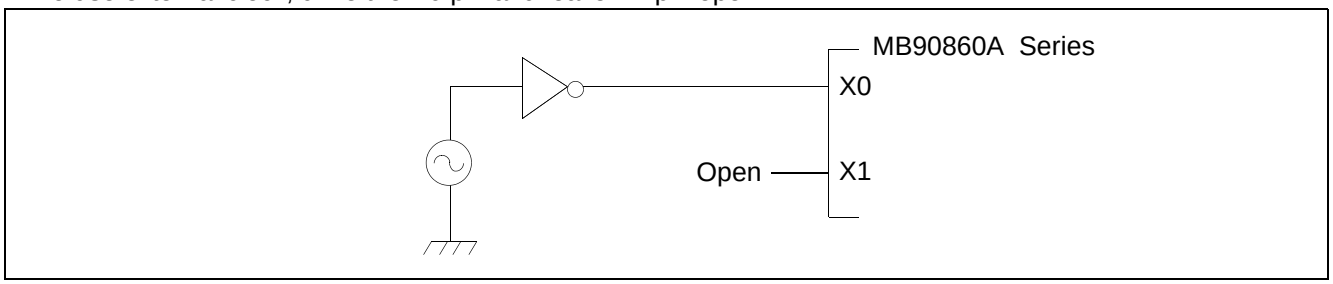
### 2. Treatment of unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ .

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

### 3. Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.




### 4. Precautions for when not using a sub clock signal

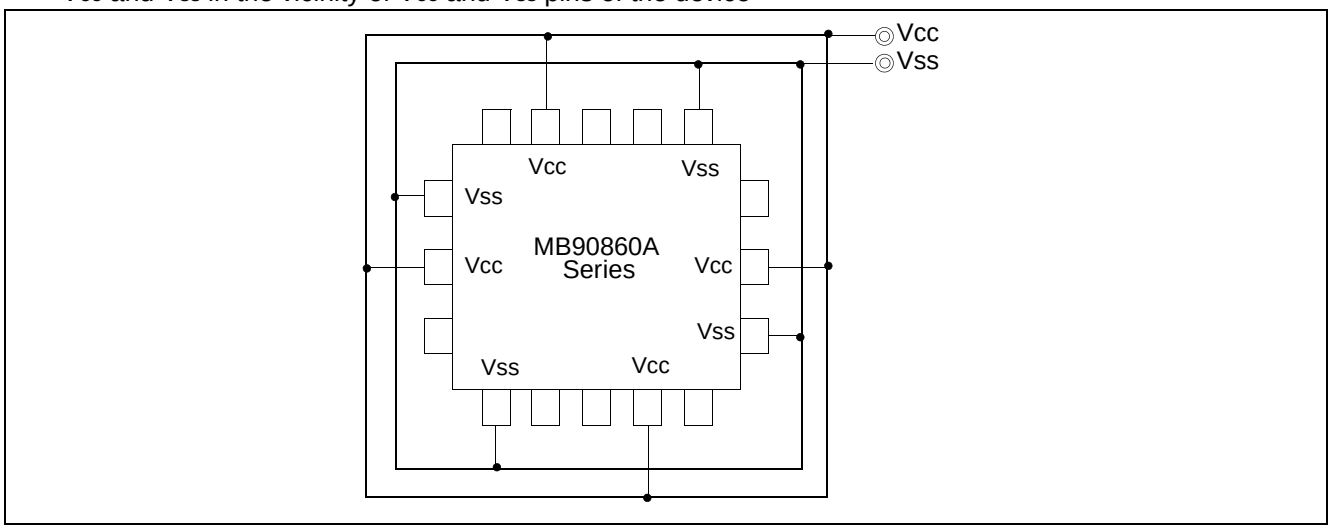
If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

## 5. Notes on during operation of PLL clock mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

## 6. Power supply pins ($V_{CC}$/$V_{SS}$)

- If there are multiple $V_{CC}$ and $V_{SS}$ pins, from the point of view of device design, pins to be of the same potential are connected the inside of the device to prevent such malfunctioning as latch up.
  To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the $V_{CC}$ and $V_{SS}$ pins to the power supply and ground externally.
- Connect $V_{CC}$ and $V_{SS}$ to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1 µF as a bypass capacitor between $V_{CC}$ and $V_{SS}$ in the vicinity of $V_{CC}$ and $V_{SS}$ pins of the device




## 7. Pull-up/down resistors

The MB90860A Series does not support internal pull-up/down resistors (Port 0 to Port 3: built-in pull-up resistors). Use external components where needed.

## 8. Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.

## 9. Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply ($AV_{CC}$, AVRH, AVRL) and analog inputs (AN0 to AN23) after turning-on the digital power supply ($V_{CC}$) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage not exceed AVRH or $AV_{CC}$ (turning on/off the analog and digital power supplies simultaneously is acceptable) .

## 10. Connection of Unused Pins of A/D Converter if A/D Converter is used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS}$ = AVRH = AVRL = $V_{SS}$.

## 11. Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V)

## 12. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified $V_{CC}$ supply voltage operating range. Therefore, the $V_{CC}$ supply voltage should be stabilized.

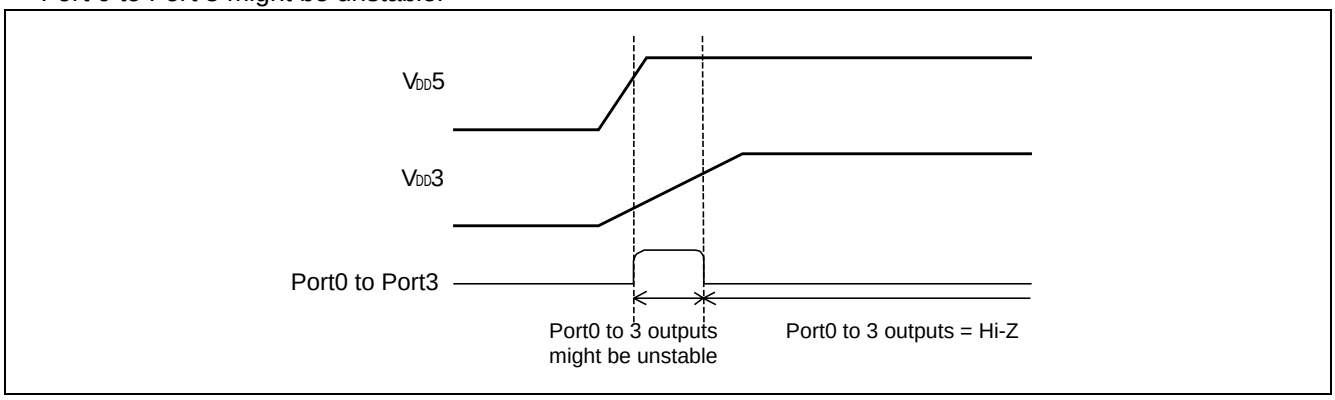
For reference, the supply voltage should be controlled so that $V_{CC}$ ripple variations (peak-to-peak value) at commercial frequencies (50 Hz to 60 Hz) fall below 10% of the standard $V_{CC}$ supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

## 13. Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

## 14. Port 0 to port 3 output during Power-on (External-bus mode)

As shown below, when power is turned on in External-Bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable.



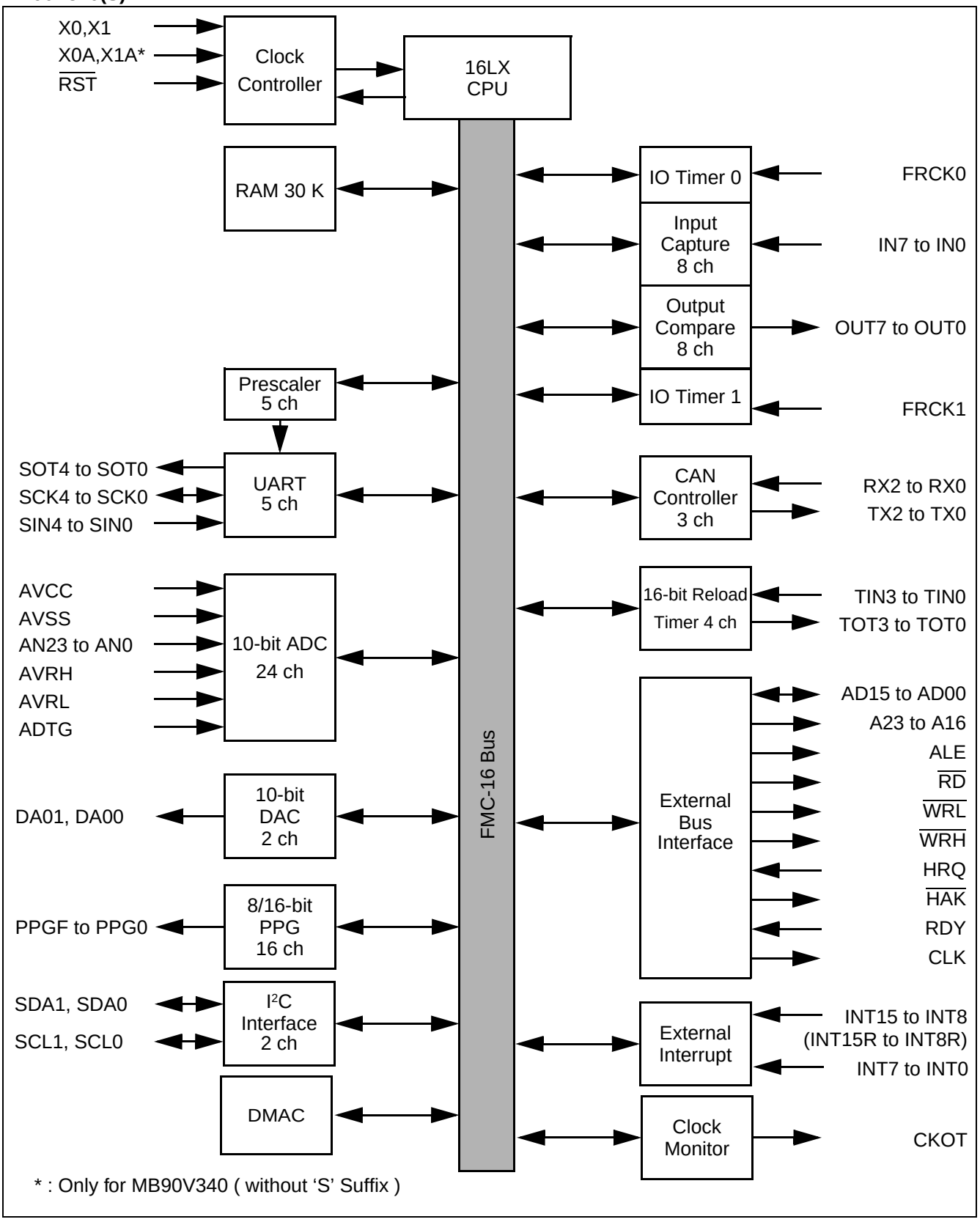

## 15. Flash security Function

The security byte is located in the area of the flash memory.
If protection code $01_H$ is written in the security byte, the flash memory is in the protected state by security.
Therefore please do not write $01_H$ in this address if you do not use the security function.
Please refer to following table for the address of the security byte.

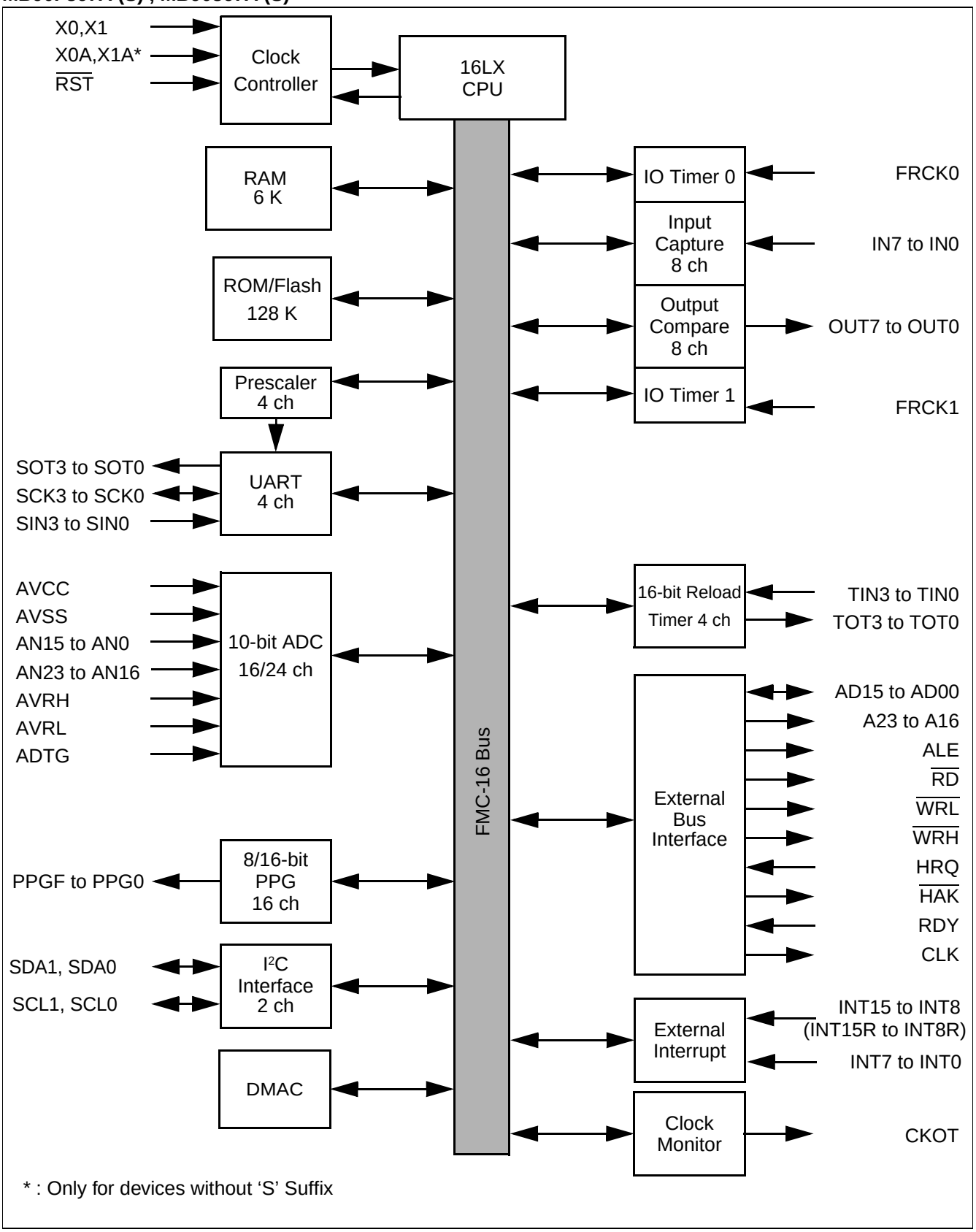
| | Flash memory size | Address for security byte |
|---|---|---|
| MB90F867A (S) | Embedded 1 Mbit Flash Memory | $FE0001_H$ |

## ■ BLOCK DIAGRAMS

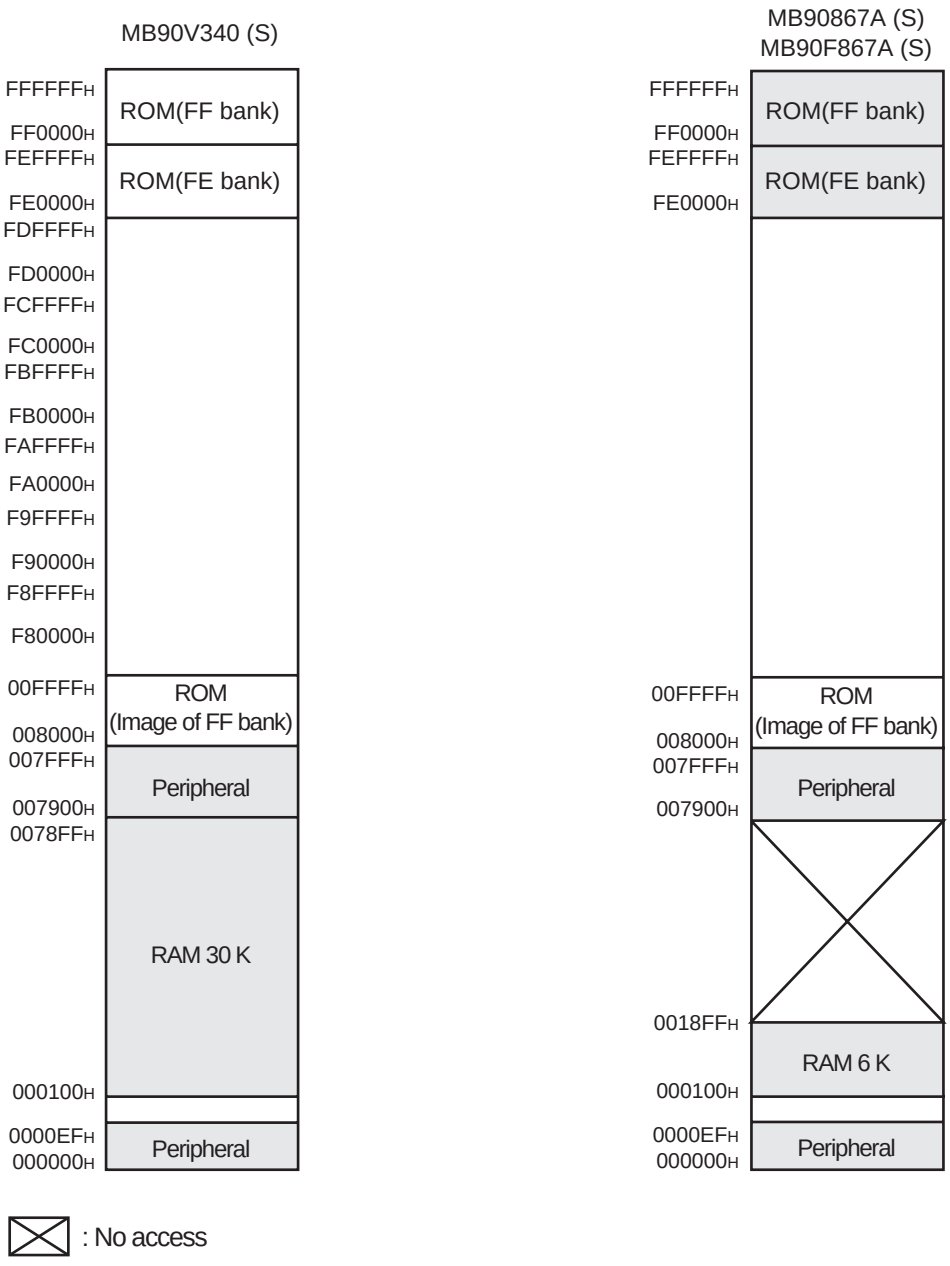
**MB90V340(S)**



**MB90F867A (S) , MB90867A (S)**



## ■ MEMORY MAP




Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration.
For example, an attempt to access 00C000H accesses the value at FFC000H in ROM.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
The image between FF8000H and FFFFFFH is visible in bank 00, while the image between FF0000H and FF7FFFH is visible only in bank FF.

## ■ I/O MAP

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 00H | Port 0 Data Register | PDR0 | R/W | Port 0 | XXXXXXXX |
| 01H | Port 1 Data Register | PDR1 | R/W | Port 1 | XXXXXXXX |
| 02H | Port 2 Data Register | PDR2 | R/W | Port 2 | XXXXXXXX |
| 03H | Port 3 Data Register | PDR3 | R/W | Port 3 | XXXXXXXX |
| 04H | Port 4 Data Register | PDR4 | R/W | Port 4 | XXXXXXXX |
| 05H | Port 5 Data Register | PDR5 | R/W | Port 5 | XXXXXXXX |
| 06H | Port 6 Data Register | PDR6 | R/W | Port 6 | XXXXXXXX |
| 07H | Port 7 Data Register | PDR7 | R/W | Port 7 | XXXXXXXX |
| 08H | Port 8 Data Register | PDR8 | R/W | Port 8 | XXXXXXXX |
| 09H | Port 9 Data Register | PDR9 | R/W | Port 9 | XXXXXXXX |
| 0AH | Port A Data Register | PDRA | R/W | Port A | XXXXXXXX |
| 0BH | Port 5 Analog Input Enable Register | ADER5 | R/W | Port 5, A/D | 11111111 |
| 0CH | Port 6 Analog Input Enable Register | ADER6 | R/W | Port 6, A/D | 11111111 |
| 0DH | Port 7 Analog Input Enable Register | ADER7 | R/W | Port 7, A/D | 11111111 |
| 0EH | Input Level Select Register 0 | ILSR0 | R/W | Ports | 00000000 |
| 0FH | Input Level Select Register 1 | ILSR1 | R/W | Ports | 00000000 |
| 10H | Port 0 Direction Register | DDR0 | R/W | Port 0 | 00000000 |
| 11H | Port 1 Direction Register | DDR1 | R/W | Port 1 | 00000000 |
| 12H | Port 2 Direction Register | DDR2 | R/W | Port 2 | 00000000 |
| 13H | Port 3 Direction Register | DDR3 | R/W | Port 3 | 00000000 |
| 14H | Port 4 Direction Register | DDR4 | R/W | Port 4 | 00000000 |
| 15H | Port 5 Direction Register | DDR5 | R/W | Port 5 | 00000000 |
| 16H | Port 6 Direction Register | DDR6 | R/W | Port 6 | 00000000 |
| 17H | Port 7 Direction Register | DDR7 | R/W | Port 7 | 00000000 |
| 18H | Port 8 Direction Register | DDR8 | R/W | Port 8 | 00000000 |
| 19H | Port 9 Direction Register | DDR9 | R/W | Port 9 | 00000000 |
| 1AH | Port A Direction Register | DDRA | R/W | Port A | 00000100 |
| 1BH | Reserved | | | | |
| 1CH | Port 0 Pullup Control Register | PUCR0 | R/W | Port 0 | 00000000 |
| 1DH | Port 1 Pullup Control Register | PUCR1 | R/W | Port 1 | 00000000 |
| 1EH | Port 2 Pullup Control Register | PUCR2 | R/W | Port 2 | 00000000 |
| 1FH | Port 3 Pullup Control Register | PUCR3 | R/W | Port 3 | 00000000 |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 20H | Serial Mode Register 0 | SMR0 | W, R/W | UART0 | 00000000 |
| 21H | Serial Control Register 0 | SCR0 | W, R/W | | 00000000 |
| 22H | Reception/Transmission Data Register 0 | RDR0/ TDR0 | R/W | | 00000000 |
| 23H | Serial Status Register 0 | SSR0 | R, R/W | | 00001000 |
| 24H | Extended Communication Control Reg. 0 | ECCR0 | R, W, R/W | | 000000XX |
| 25H | Extended Status/Control Register 0 | ESCR0 | R/W | | 00000100 |
| 26H | Baud Rate Generator Register 00 | BGR00 | R/W | | 00000000 |
| 27H | Baud Rate Generator Register 01 | BGR01 | R/W | | 00000000 |
| 28H | Serial Mode Register 1 | SMR1 | W, R/W | UART1 | 00000000 |
| 29H | Serial Control Register 1 | SCR1 | W, R/W | | 00000000 |
| 2AH | Reception/Transmission Data Register 1 | RDR1/ TDR1 | R/W | | 00000000 |
| 2BH | Serial Status Register 1 | SSR1 | R, R/W | | 00001000 |
| 2CH | Extended Communication Control Reg. 1 | ECCR1 | R, W, R/W | | 000000XX |
| 2DH | Extended Status Control Register 1 | ESCR1 | R/W | | 00000100 |
| 2EH | Baud Rate Generator Register 10 | BGR10 | R/W | | 00000000 |
| 2FH | Baud Rate Generator Register 11 | BGR11 | R/W | | 00000000 |
| 30H | PPG 0 Operation Mode Control Register | PPGC0 | W, R/W | 16-bit PPG 0/1 | 0X000XX1 |
| 31H | PPG 1 Operation Mode Control Register | PPGC1 | W, R/W | | 0X000001 |
| 32H | PPG 01 Clock Select Register | PPG01 | R/W | | 000000X0 |
| 33H | Reserved | | | | |
| 34H | PPG 2 Operation Mode Control Register | PPGC2 | W, R/W | 16-bit PPG 2/3 | 0X000XX1 |
| 35H | PPG 3 Operation Mode Control Register | PPGC3 | W, R/W | | 0X000001 |
| 36H | PPG 23 Clock Select Register | PPG23 | R/W | | 000000X0 |
| 37H | Reserved | | | | |
| 38H | PPG 4 Operation Mode Control Register | PPGC4 | W, R/W | 16-bit PPG 4/5 | 0X000XX1 |
| 39H | PPG 5 Operation Mode Control Register | PPGC5 | W, R/W | | 0X000001 |
| 3AH | PPG 4 and PPG 5 Clock Select Register | PPG45 | R/W | | 000000X0 |
| 3BH | Program Address Detection Control Status Register 1 | PACSR1 | R/W | Address Match Detection 1 | 00000000 |
| 3CH | PPG 6 Operation Mode Control Register | PPGC6 | W, R/W | 16-bit PPG 6/7 | 0X000XX1 |
| 3DH | PPG 7 Operation Mode Control Register | PPGC7 | W, R/W | | 0X000001 |
| 3EH | PPG 67 Clock Select Register | PPG67 | R/W | | 000000X0 |
| 3FH | Reserved | | | | |

*(Continued)*

| Address | Register | Abbrevi-ation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 40H | PPG 8 Operation Mode Control Register | PPGC8 | W, R/W | 16-bit PPG 8/9 | 0X000XX1 |
| 41H | PPG 9 Operation Mode Control Register | PPGC9 | W, R/W | | 0X000001 |
| 42H | PPG 89 Clock Select Register | PPG89 | R/W | | 000000X0 |
| 43H | Reserved | | | | |
| 44H | PPG A Operation Mode Control Register | PPGCA | W, R/W | 16-bit PPG A/B | 0X000XX1 |
| 45H | PPG B Operation Mode Control Register | PPGCB | W, R/W | | 0X000001 |
| 46H | PPG AB Clock Select Register | PPGAB | R/W | | 000000X0 |
| 47H | Reserved | | | | |
| 48H | PPG C Operation Mode Control Register | PPGCC | W, R/W | 16-bit PPG C/D | 0X000XX1 |
| 49H | PPG D Operation Mode Control Register | PPGCD | W, R/W | | 0X000001 |
| 4AH | PPG CD Clock Select Register | PPGCD | R/W | | 000000X0 |
| 4BH | Reserved | | | | |
| 4CH | PPG E Operation Mode Control Register | PPGCE | W, R/W | 16-bit PPG E/F | 0X000XX1 |
| 4DH | PPG F Operation Mode Control Register | PPGCF | W, R/W | | 0X000001 |
| 4EH | PPG EF Clock Select Register | PPGEF | R/W | | 000000X0 |
| 4FH | Reserved | | | | |
| 50H | Input Capture Control Status Register 0/1 | ICS01 | R/W | Input Capture 0/1 | 00000000 |
| 51H | Input Capture Edge Register 0/1 | ICE01 | R/W, R | | XXX0X0XX |
| 52H | Input Capture Control Status Register 2/3 | ICS23 | R/W | Input Capture 2/3 | 00000000 |
| 53H | Input Capture Edge Register 2/3 | ICE23 | R | | XXXXXXXX |
| 54H | Input Capture Control Status Register 4/5 | ICS45 | R/W | Input Capture 4/5 | 00000000 |
| 55H | Input Capture Edge Register 4/5 | ICE45 | R | | XXXXXXXX |
| 56H | Input Capture Control Status Register 6/7 | ICS67 | R/W | Input Capture 6/7 | 00000000 |
| 57H | Input Capture Edge Register 6/7 | ICE67 | R/W, R | | XXX000XX |
| 58H | Output Compare Control Status Register 0 | OCS0 | R/W | Output Compare 0/1 | 0000XX00 |
| 59H | Output Compare Control Status Register 1 | OCS1 | R/W | | 0XX00000 |
| 5AH | Output Compare Control Status Register 2 | OCS2 | R/W | Output Compare 2/3 | 0000XX00 |
| 5BH | Output Compare Control Status Register 3 | OCS3 | R/W | | 0XX00000 |
| 5CH | Output Compare Control Status Register 4 | OCS4 | R/W | Output Compare 4/5 | 0000XX00 |
| 5DH | Output Compare Control Status Register 5 | OCS5 | R/W | | 0XX00000 |
| 5EH | Output Compare Control Status Register 6 | OCS6 | R/W | Output Compare 6/7 | 0000XX00 |
| 5FH | Output Compare Control Status Register 7 | OCS7 | R/W | | 0XX00000 |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 60H | Timer Control Status Register 0 | TMCSR0 | R/W | 16-bit Reload Timer 0 | 00000000 |
| 61H | Timer Control Status Register 0 | TMCSR0 | R/W | | XXXX0000 |
| 62H | Timer Control Status Register 1 | TMCSR1 | R/W | 16-bit Reload Timer 1 | 00000000 |
| 63H | Timer Control Status Register 1 | TMCSR1 | R/W | | XXXX0000 |
| 64H | Timer Control Status Register 2 | TMCSR2 | R/W | 16-bit Reload Timer 2 | 00000000 |
| 65H | Timer Control Status Register 2 | TMCSR2 | R/W | | XXXX0000 |
| 66H | Timer Control Status Register 3 | TMCSR3 | R/W | 16-bit Reload Timer 3 | 00000000 |
| 67H | Timer Control Status Register 3 | TMCSR3 | R/W | | XXXX0000 |
| 68H | A/D Control Status Register 0 | ADCS0 | R/W | A/D Converter | 000XXXX0 |
| 69H | A/D Control Status Register 1 | ADCS1 | R/W | | 0000000X |
| 6AH | A/D Data Register 0 | ADCR0 | R | | 00000000 |
| 6BH | A/D Data Register 1 | ADCR1 | R | | XXXXXX00 |
| 6CH | ADC Setting Register 0 | ADSR0 | R/W | | 00000000 |
| 6DH | ADC Setting Register 1 | ADSR1 | R/W | | 00000000 |
| 6EH | Reserved | | | | |
| 6FH | ROM Mirroring Register | ROMM | W | ROM Mirror | XXXXXXX1 |
| 70H to 8FH | Reserved | | | | |
| 90H to 9AH | Reserved | | | | |
| 9BH | DMA Descriptor Channel Specification Register | DCSR | R/W | DMA | 00000000 |
| 9CH | DMA Status Register L | DSRL | R/W | | 00000000 |
| 9DH | DMA Status Register H | DSRH | R/W | | 00000000 |
| 9EH | Program Address Detection Control Status Register 0 | PACSR0 | R/W | Address Match Detection 0 | 00000000 |
| 9FH | Delayed Interrupt/Release | DIRR | R/W | Delayed Interrupt | XXXXXXX0 |
| A0H | Low-power Mode Control Register | LPMCR | W, R/W | Low Power Controller | 00011000 |
| A1H | Clock Selection Register | CKSCR | R, R/W | Low Power Controller | 11111100 |
| A2H, A3H | Reserved | | | | |
| A4H | DMA Stop Status Register | DSSR | R/W | DMA | 00000000 |
| A5H | Automatic Ready Function Select Reg. | ARSR | W | External Memory Access | 0011XX00 |
| A6H | External Address Output Control Reg. | HACR | W | | 00000000 |
| A7H | Bus Control Signal Selection Register | ECSR | W | | 0000000X |
| A8H | Watchdog Control Register | WDTC | R, W | Watchdog Timer | XXXXX111 |
| A9H | Timebase Timer Control Register | TBTC | W, R/W | Time Base Timer | 1XX00100 |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| AA$_H$ | Watch Timer Control Register | WTC | R, R/W | Watch Timer | 1X001000 |
| AB$_H$ | Reserved | | | | |
| AC$_H$ | DMA Enable Register L | DERL | R/W | DMA | 00000000 |
| AD$_H$ | DMA Enable Register H | DERH | R/W | | 00000000 |
| AE$_H$ | Flash Control Status Register (FlashDevices only. Otherwise reserved) | FMCS | R, R/W | Flash Memory | 000X0000 |
| AF$_H$ | Reserved | | | | |
| B0$_H$ | Interrupt Control Register 00 | ICR00 | W, R/W | Interrupt Controller | 00000111 |
| B1$_H$ | Interrupt Control Register 01 | ICR01 | W, R/W | | 00000111 |
| B2$_H$ | Interrupt Control Register 02 | ICR02 | W, R/W | | 00000111 |
| B3$_H$ | Interrupt Control Register 03 | ICR03 | W, R/W | | 00000111 |
| B4$_H$ | Interrupt Control Register 04 | ICR04 | W, R/W | | 00000111 |
| B5$_H$ | Interrupt Control Register 05 | ICR05 | W, R/W | | 00000111 |
| B6$_H$ | Interrupt Control Register 06 | ICR06 | W, R/W | | 00000111 |
| B7$_H$ | Interrupt Control Register 07 | ICR07 | W, R/W | | 00000111 |
| B8$_H$ | Interrupt Control Register 08 | ICR08 | W, R/W | | 00000111 |
| B9$_H$ | Interrupt Control Register 09 | ICR09 | W, R/W | | 00000111 |
| BA$_H$ | Interrupt Control Register 10 | ICR10 | W, R/W | | 00000111 |
| BB$_H$ | Interrupt Control Register 11 | ICR11 | W, R/W | | 00000111 |
| BC$_H$ | Interrupt Control Register 12 | ICR12 | W, R/W | | 00000111 |
| BD$_H$ | Interrupt Control Register 13 | ICR13 | W, R/W | | 00000111 |
| BE$_H$ | Interrupt Control Register 14 | ICR14 | W, R/W | | 00000111 |
| BF$_H$ | Interrupt Control Register 15 | ICR15 | W, R/W | | 00000111 |
| C0$_H$ | D/A Converter Data 0 | DAT0 | R/W | D/A Converter | XXXXXXXX |
| C1$_H$ | D/A Converter Data 1 | DAT1 | R/W | | XXXXXXXX |
| C2$_H$ | D/A Control 0 | DACR0 | R/W | | XXXXXXX0 |
| C3$_H$ | D/A Control 1 | DACR1 | R/W | | XXXXXXX0 |
| C4$_H$, C5$_H$ | Reserved | | | | |
| C6$_H$ | External Interrupt Request Enable Register 0 | ENIR0 | R/W | External Interrupt 0 | 00000000 |
| C7$_H$ | External Interrupt Request Register 0 | EIRR0 | R/W | | XXXXXXXX |
| C8$_H$ | External Interrupt Level Register 0 | ELVR0 | R/W | | 00000000 |
| C9$_H$ | External Interrupt Level Register 0 | ELVR0 | R/W | | 00000000 |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| CA$_H$ | External Interrupt Request Enable Register 1 | ENIR1 | R/W | External Interrupt 1 | 00000000 |
| CB$_H$ | External Interrupt Request Register 1 | EIRR1 | R/W | | XXXXXXXX |
| CC$_H$ | External Interrupt Level Register 1 | ELVR1 | R/W | | 00000000 |
| CD$_H$ | External Interrupt Level Register 1 | ELVR1 | R/W | | 00000000 |
| CE$_H$ | External Interrupt Source Select Register | EISSR | R/W | | 00000000 |
| CF$_H$ | PLL/Subclock Control Register | PSCCR | W | PLL | XXXX0000 |
| D0$_H$ | DMA Buffer Address Pointer L | BAPL | R/W | DMA | XXXXXXXX |
| D1$_H$ | DMA Buffer Address Pointer M | BAPM | R/W | | XXXXXXXX |
| D2$_H$ | DMA Buffer Address Pointer H | BAPH | R/W | | XXXXXXXX |
| D3$_H$ | DMA Control Register | DMACS | R/W | | XXXXXXXX |
| D4$_H$ | I/O Register Address Pointer L | IOAL | R/W | | XXXXXXXX |
| D5$_H$ | I/O Register Address Pointer H | IOAH | R/W | | XXXXXXXX |
| D6$_H$ | Data Counter L | DCTL | R/W | | XXXXXXXX |
| D7$_H$ | Data Counter H | DCTH | R/W | | XXXXXXXX |
| D8$_H$ | Serial Mode Register 2 | SMR2 | W, R/W | UART2 | 00000000 |
| D9$_H$ | Serial Control Register 2 | SCR2 | W, R/W | | 00000000 |
| DA$_H$ | Reception/Transmission Data Register 2 | RDR2/ TDR2 | R/W | | 00000000 |
| DB$_H$ | Serial Status Register 2 | SSR2 | R, R/W | | 00001000 |
| DC$_H$ | Extended Communication Control Register 2 | ECCR2 | R, W, R/W | | 000000XX |
| DD$_H$ | Extended Status/Control Register 2 | ESCR2 | R/W | | 00000100 |
| DE$_H$ | Baud Rate Reload Register 20 | BGR20 | R/W | | 00000000 |
| DF$_H$ | Baud Rate Reload Register 21 | BGR21 | R/W | | 00000000 |
| E0$_H$ to EF$_H$ | Reserved | | | | |
| F0$_H$ to FF$_H$ | External | | | | |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 7900H | Reload Register L0 | PRLL0 | R/W | 16-bit PPG 0/1 | XXXXXXXX |
| 7901H | Reload Register H0 | PRLH0 | R/W | | XXXXXXXX |
| 7902H | Reload Register L1 | PRLL1 | R/W | | XXXXXXXX |
| 7903H | Reload Register H1 | PRLH1 | R/W | | XXXXXXXX |
| 7904H | Reload Register L2 | PRLL2 | R/W | 16-bit PPG 2/3 | XXXXXXXX |
| 7905H | Reload Register H2 | PRLH2 | R/W | | XXXXXXXX |
| 7906H | Reload Register L3 | PRLL3 | R/W | | XXXXXXXX |
| 7907H | Reload Register H3 | PRLH3 | R/W | | XXXXXXXX |
| 7908H | Reload Register L4 | PRLL4 | R/W | 16-bit PPG 4/5 | XXXXXXXX |
| 7909H | Reload Register H4 | PRLH4 | R/W | | XXXXXXXX |
| 790AH | Reload Register L5 | PRLL5 | R/W | | XXXXXXXX |
| 790BH | Reload Register H5 | PRLH5 | R/W | | XXXXXXXX |
| 790CH | Reload Register L6 | PRLL6 | R/W | 16-bit PPG 6/7 | XXXXXXXX |
| 790DH | Reload Register H6 | PRLH6 | R/W | | XXXXXXXX |
| 790EH | Reload Register L7 | PRLL7 | R/W | | XXXXXXXX |
| 790FH | Reload Register H7 | PRLH7 | R/W | | XXXXXXXX |
| 7910H | Reload Register L8 | PRLL8 | R/W | 16-bit PPG 8/9 | XXXXXXXX |
| 7911H | Reload Register H8 | PRLH8 | R/W | | XXXXXXXX |
| 7912H | Reload Register L9 | PRLL9 | R/W | | XXXXXXXX |
| 7913H | Reload Register H9 | PRLH9 | R/W | | XXXXXXXX |
| 7914H | Reload Register LA | PRLLA | R/W | 16-bit PPG A/B | XXXXXXXX |
| 7915H | Reload Register HA | PRLHA | R/W | | XXXXXXXX |
| 7916H | Reload Register LB | PRLLB | R/W | | XXXXXXXX |
| 7917H | Reload Register HB | PRLHB | R/W | | XXXXXXXX |
| 7918H | Reload Register LC | PRLLC | R/W | 16-bit PPG C/D | XXXXXXXX |
| 7919H | Reload Register HC | PRLHC | R/W | | XXXXXXXX |
| 791AH | Reload Register LD | PRLLD | R/W | | XXXXXXXX |
| 791BH | Reload Register HD | PRLHD | R/W | | XXXXXXXX |
| 791CH | Reload Register LE | PRLLE | R/W | 16-bit PPG E/F | XXXXXXXX |
| 791DH | Reload Register HE | PRLHE | R/W | | XXXXXXXX |
| 791EH | Reload Register LF | PRLLF | R/W | | XXXXXXXX |
| 791FH | Reload Register HF | PRLHF | R/W | | XXXXXXXX |
| 7920H | Input Capture Data Register 0 | IPCP0 | R | Input Capture 0/1 | XXXXXXXX |
| 7921H | Input Capture Data Register 0 | IPCP0 | R | | XXXXXXXX |
| 7922H | Input Capture Data Register 1 | IPCP1 | R | | XXXXXXXX |
| 7923H | Input Capture Data Register 1 | IPCP1 | R | | XXXXXXXX |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 7924H | Input Capture Data Register 2 | IPCP2 | R | Input Capture 2/3 | XXXXXXXX |
| 7925H | Input Capture Data Register 2 | IPCP2 | R | | XXXXXXXX |
| 7926H | Input Capture Data Register 3 | IPCP3 | R | | XXXXXXXX |
| 7927H | Input Capture Data Register 3 | IPCP3 | R | | XXXXXXXX |
| 7928H | Input Capture Data Register 4 | IPCP4 | R | Input Capture 4/5 | XXXXXXXX |
| 7929H | Input Capture Data Register 4 | IPCP4 | R | | XXXXXXXX |
| 792AH | Input Capture Data Register 5 | IPCP5 | R | | XXXXXXXX |
| 792BH | Input Capture Data Register 5 | IPCP5 | R | | XXXXXXXX |
| 792CH | Input Capture Data Register 6 | IPCP6 | R | Input Capture 6/7 | XXXXXXXX |
| 792DH | Input Capture Data Register 6 | IPCP6 | R | | XXXXXXXX |
| 792EH | Input Capture Data Register 7 | IPCP7 | R | | XXXXXXXX |
| 792FH | Input Capture Data Register 7 | IPCP7 | R | | XXXXXXXX |
| 7930H | Output Compare Register 0 | OCCP0 | R/W | Output Compare 0/1 | XXXXXXXX |
| 7931H | Output Compare Register 0 | OCCP0 | R/W | | XXXXXXXX |
| 7932H | Output Compare Register 1 | OCCP1 | R/W | | XXXXXXXX |
| 7933H | Output Compare Register 1 | OCCP1 | R/W | | XXXXXXXX |
| 7934H | Output Compare Register 2 | OCCP2 | R/W | Output Compare 2/3 | XXXXXXXX |
| 7935H | Output Compare Register 2 | OCCP2 | R/W | | XXXXXXXX |
| 7936H | Output Compare Register 3 | OCCP3 | R/W | | XXXXXXXX |
| 7937H | Output Compare Register 3 | OCCP3 | R/W | | XXXXXXXX |
| 7938H | Output Compare Register 4 | OCCP4 | R/W | Output Compare 4/5 | XXXXXXXX |
| 7939H | Output Compare Register 4 | OCCP4 | R/W | | XXXXXXXX |
| 793AH | Output Compare Register 5 | OCCP5 | R/W | | XXXXXXXX |
| 793BH | Output Compare Register 5 | OCCP5 | R/W | | XXXXXXXX |
| 793CH | Output Compare Register 6 | OCCP6 | R/W | Output Compare 6/7 | XXXXXXXX |
| 793DH | Output Compare Register 6 | OCCP6 | R/W | | XXXXXXXX |
| 793EH | Output Compare Register 7 | OCCP7 | R/W | | XXXXXXXX |
| 793FH | Output Compare Register 7 | OCCP7 | R/W | | XXXXXXXX |
| 7940H | Data Register 0 | TCDT0 | R/W | I/O Timer 0 | 00000000 |
| 7941H | Data Register 0 | TCDT0 | R/W | | 00000000 |
| 7942H | Control Status Register 0 | TCCSL0 | R/W | | 00000000 |
| 7943H | Control Status Register 0 | TCCSH0 | R/W | | 0XXXXXXX |
| 7944H | Data Register 1 | TCDT1 | R/W | I/O Timer 1 | 00000000 |
| 7945H | Data Register 1 | TCDT1 | R/W | | 00000000 |
| 7946H | Control Status Register 1 | TCCSL1 | R/W | | 00000000 |
| 7947H | Control Status Register 1 | TCCSH1 | R/W | | 0XXXXXXX |

*(Continued)*

| Address | Register | Abbrevia-tion | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 7948H | Timer Register 0/Reload Register 0 | TMR0/ TMRLR0 | R/W | 16-bit Reload Timer 0 | XXXXXXXX |
| 7949H | | | R/W | | XXXXXXXX |
| 794AH | Timer Register 1/Reload Register 1 | TMR1/ TMRLR1 | R/W | 16-bit Reload Timer 1 | XXXXXXXX |
| 794BH | | | R/W | | XXXXXXXX |
| 794CH | Timer Register 2/Reload Register 2 | TMR2/ TMRLR2 | R/W | 16-bit Reload Timer 2 | XXXXXXXX |
| 794DH | | | R/W | | XXXXXXXX |
| 794EH | Timer Register 3/Reload Register 3 | TMR3/ TMRLR3 | R/W | 16-bit Reload Timer 3 | XXXXXXXX |
| 794FH | | | R/W | | XXXXXXXX |
| 7950H | Serial Mode Register 3 | SMR3 | W, R/W | UART3 | 00000000 |
| 7951H | Serial Control Register 3 | SCR3 | W, R/W | | 00000000 |
| 7952H | Reception/Transmission Data Register 3 | RDR3/ TDR3 | R/W | | 00000000 |
| 7953H | Serial Status Register 3 | SSR3 | R, R/W | | 00001000 |
| 7954H | Extended Communication Control Reg. 3 | ECCR3 | R, W, R/W | | 000000XX |
| 7955H | Extended Status/Control Register 3 | ESCR3 | R/W | | 00000100 |
| 7956H | Baud Rate Reload Register 30 | BGR30 | R/W | | 00000000 |
| 7957H | Baud Rate Reload Register 31 | BGR31 | R/W | | 00000000 |
| 7958H | Serial Mode Register 4 | SMR4 | W, R/W | UART4 | 00000000 |
| 7959H | Serial Control Register 4 | SCR4 | W, R/W | | 00000000 |
| 795AH | Reception/Transmission Data Register 4 | RDR4/ TDR4 | R/W | | 00000000 |
| 795BH | Serial Status Register 4 | SSR4 | R, R/W | | 00001000 |
| 795CH | Extended Communication Control Reg. 4 | ECCR4 | R, W, R/W | | 000000XX |
| 795DH | Extended Status/Control Register 4 | ESCR4 | R/W | | 00000100 |
| 795EH | Baud Rate Reload Register 40 | BGR40 | R/W | | 00000000 |
| 795FH | Baud Rate Reload Register 41 | BGR41 | R/W | | 00000000 |
| 7960H to 796BH | Reserved | | | | |
| 796CH | Clock Output Enable Register | CLKR | R/W | Clock Monitor | XXXX0000 |
| 796DH to 796FH | Reserved | | | | |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 7970H | I²C Bus Status Register 0 | IBSR0 | R | I²C Interface 0 | 00000000 |
| 7971H | I²C Bus Control Register 0 | IBCR0 | W, R/W | | 00000000 |
| 7972H | I²C 10-bit Slave Address Register 0 | ITBAL0 | R/W | | 00000000 |
| 7973H | | ITBAH0 | R/W | | 00000000 |
| 7974H | I²C 10-bit Slave Address Mask Register 0 | ITMKL0 | R/W | | 11111111 |
| 7975H | | ITMKH0 | R/W | | 00111111 |
| 7976H | I²C 7-bit Slave Address Register 0 | ISBA0 | R/W | | 00000000 |
| 7977H | I²C 7-bit Slave Address Mask Register 0 | ISMK0 | R/W | | 01111111 |
| 7978H | I²C Data Register 0 | IDAR0 | R/W | | 00000000 |
| 7979H, 797AH | Reserved | | | | |
| 797BH | I²C Clock Control Register 0 | ICCR0 | R/W | I²C Interface 0 | 00011111 |
| 797CH to 797FH | Reserved | | | | |
| 7980H | I²C Bus Status Register 1 | IBSR1 | R | I²C Interface 1 | 00000000 |
| 7981H | I²C Bus Control Register 1 | IBCR1 | W, R/W | | 00000000 |
| 7982H | I²C 10-bit Slave Address Register 1 | ITBAL1 | R/W | | 00000000 |
| 7983H | | ITBAH1 | R/W | | 00000000 |
| 7984H | I²C 10-bit Slave Address Mask Register 1 | ITMKL1 | R/W | | 11111111 |
| 7985H | | ITMKH1 | R/W | | 00111111 |
| 7986H | I²C 7-bit Slave Address Register 1 | ISBA1 | R/W | | 00000000 |
| 7987H | I²C 7-bit Slave Address Mask Register 1 | ISMK1 | R/W | | 01111111 |
| 7988H | I²C Data Register 1 | IDAR1 | R/W | | 00000000 |
| 7989H, 798AH | Reserved | | | | |
| 798BH | I²C Clock Control Register 1 | ICCR1 | R/W | I²C Interface 1 | 00011111 |
| 798CH to 79C1H | Reserved | | | | |
| 79C2H | Clock Modulator Control Register | CMCR | R, R/W | Clock Modulator | 0001X000 |
| 79C3H to 79DFH | Reserved | | | | |

*(Continued)*

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| 79E0H | Program Address Detection Register 0 | PADR0 | R/W | Address Match Detection 0 | XXXXXXXX |
| 79E1H | Program Address Detection Register 0 | PADR0 | R/W | | XXXXXXXX |
| 79E2H | Program Address Detection Register 0 | PADR0 | R/W | | XXXXXXXX |
| 79E3H | Program Address Detection Register 1 | PADR1 | R/W | | XXXXXXXX |
| 79E4H | Program Address Detection Register 1 | PADR1 | R/W | | XXXXXXXX |
| 79E5H | Program Address Detection Register 1 | PADR1 | R/W | | XXXXXXXX |
| 79E6H | Program Address Detection Register 2 | PADR2 | R/W | | XXXXXXXX |
| 79E7H | Program Address Detection Register 2 | PADR2 | R/W | | XXXXXXXX |
| 79E8H | Program Address Detection Register 2 | PADR2 | R/W | | XXXXXXXX |
| 79E9H to 79EFH | Reserved | | | | |
| 79F0H | Program Address Detection Register 3 | PADR3 | R/W | Address Match Detection 1 | XXXXXXXX |
| 79F1H | Program Address Detection Register 3 | PADR3 | R/W | | XXXXXXXX |
| 79F2H | Program Address Detection Register 3 | PADR3 | R/W | | XXXXXXXX |
| 79F3H | Program Address Detection Register 4 | PADR4 | R/W | | XXXXXXXX |
| 79F4H | Program Address Detection Register 4 | PADR4 | R/W | | XXXXXXXX |
| 79F5H | Program Address Detection Register 4 | PADR4 | R/W | | XXXXXXXX |
| 79F6H | Program Address Detection Register 5 | PADR5 | R/W | | XXXXXXXX |
| 79F7H | Program Address Detection Register 5 | PADR5 | R/W | | XXXXXXXX |
| 79F8H | Program Address Detection Register 5 | PADR5 | R/W | | XXXXXXXX |
| 79F9H to 7FFFH | Reserved | | | | |

Notes : • Initial value of “X” represents unknown value.
• Addresses in the range 0000H to 00BFH, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results reading “X” and any write access should not be performed.

## ■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

| Interrupt cause | EI²OS clear | DMA ch number | Interrupt vector | | Interrupt control register | |
|---|---|---|---|---|---|---|
| | | | Number | Address | Number | Address |
| Reset | N | — | #08 | FFFFDC$_H$ | — | — |
| INT9 instruction | N | — | #09 | FFFFD8$_H$ | — | — |
| Exception | N | — | #10 | FFFFD4$_H$ | — | — |
| (Reserved) | N | — | #11 | FFFFD0$_H$ | ICR00 | 0000B0$_H$ |
| (Reserved) | N | — | #12 | FFFFCC$_H$ | | |
| Input Capture 6 | Y1 | — | #13 | FFFFC8$_H$ | ICR01 | 0000B1$_H$ |
| Input Capture 7 | Y1 | — | #14 | FFFFC4$_H$ | | |
| I²C0 | N | — | #15 | FFFFC0$_H$ | ICR02 | 0000B2$_H$ |
| (Reserved) | N | — | #16 | FFFFBC$_H$ | | |
| 16-bit Reload Timer 0 | Y1 | 0 | #17 | FFFFB8$_H$ | ICR03 | 0000B3$_H$ |
| 16-bit Reload Timer 1 | Y1 | 1 | #18 | FFFFB4$_H$ | | |
| 16-bit Reload Timer 2 | Y1 | 2 | #19 | FFFFB0$_H$ | ICR04 | 0000B4$_H$ |
| 16-bit Reload Timer 3 | Y1 | — | #20 | FFFFAC$_H$ | | |
| PPG 0/1/4/5 | N | — | #21 | FFFFA8$_H$ | ICR05 | 0000B5$_H$ |
| PPG 2/3/6/7 | N | — | #22 | FFFFA4$_H$ | | |
| PPG 8/9/C/D | N | — | #23 | FFFFA0$_H$ | ICR06 | 0000B6$_H$ |
| PPG A/B/E/F | N | — | #24 | FFFF9C$_H$ | | |
| Time Base Timer | N | — | #25 | FFFF98$_H$ | ICR07 | 0000B7$_H$ |
| External Interrupt 0 to 3, 8 to 11 | Y1 | 3 | #26 | FFFF94$_H$ | | |
| Watch Timer | N | — | #27 | FFFF90$_H$ | ICR08 | 0000B8$_H$ |
| External Interrupt 4 to 7, 12 to 15 | Y1 | 4 | #28 | FFFF8C$_H$ | | |
| A/D Converter | Y1 | 5 | #29 | FFFF88$_H$ | ICR09 | 0000B9$_H$ |
| I/O Timer 0 / I/O Timer 1 | N | — | #30 | FFFF84$_H$ | | |
| Input Capture 4/5 / I²C1 | Y1 | 6 | #31 | FFFF80$_H$ | ICR10 | 0000BA$_H$ |
| Output Compare 0/1/4/5 | Y1 | 7 | #32 | FFFF7C$_H$ | | |
| Input Capture 0 to 3 | Y1 | 8 | #33 | FFFF78$_H$ | ICR11 | 0000BB$_H$ |
| Output Compare 2/3/6/7 | Y1 | 9 | #34 | FFFF74$_H$ | | |
| UART 0 RX | Y2 | 10 | #35 | FFFF70$_H$ | ICR12 | 0000BC$_H$ |
| UART 0 TX | Y1 | 11 | #36 | FFFF6C$_H$ | | |
| UART 1 RX / UART 3 RX | Y2 | 12 | #37 | FFFF68$_H$ | ICR13 | 0000BD$_H$ |
| UART 1 TX / UART 3 TX | Y1 | 13 | #38 | FFFF64$_H$ | | |

*(Continued)*

*(Continued)*

| Interrupt cause | EI²OS clear | DMA ch number | Interrupt vector | | Interrupt control register | |
|---|---|---|---|---|---|---|
| | | | Number | Address | Number | Address |
| UART 2 RX / UART 4 RX | Y2 | 14 | #39 | FFFF60H | ICR14 | 0000BEH |
| UART 2 TX / UART 4 TX | Y1 | 15 | #40 | FFFF5CH | | |
| Flash Memory | N | — | #41 | FFFF58H | ICR15 | 0000BFH |
| Delayed interrupt | N | — | #42 | FFFF54H | | |

Y1 : Usable

Y2 : Usable, with EI²OS stop function

N : Unusable

Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
- When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

($V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $V_{CC}$ = $AV_{CC}$ *1 |
| | AVRH, AVRL | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC}$ ≥ AVRH, $AV_{CC}$ ≥ AVRL, AVRH ≥ AVRL |
| Input voltage | $V_I$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *2 |
| Output voltage | $V_O$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *2 |
| Maximum Clamp Current | $I_{CLAMP}$ | –4.0 | +4.0 | mA | *4 |
| Total Maximum Clamp Current | $\Sigma\lvert I_{CLAMP}\rvert$ | — | 40 | mA | *4 |
| “L” level maximum output current | $I_{OL}$ | — | 15 | mA | *3 |
| “L” level average output current | $I_{OLAV}$ | — | 4 | mA | *3 |
| “L” level maximum overall output current | $\Sigma I_{OL}$ | — | 100 | mA | *3 |
| “L” level average overall output current | $\Sigma I_{OLAV}$ | — | 50 | mA | *3 |
| “H” level maximum output current | $I_{OH}$ | — | –15 | mA | *3 |
| “H” level average output current | $I_{OHAV}$ | — | –4 | mA | *3 |
| “H” level maximum overall output current | $\Sigma I_{OH}$ | — | –100 | mA | *3 |
| “H” level average overall output current | $\Sigma I_{OHAV}$ | — | –50 | mA | *3 |
| Power consumption | $P_D$ | — | 340 | mW | MB90F867A |
| Operating temperature | $T_A$ | –40 | +105 | °C | |
| Storage temperature | $T_{STG}$ | –55 | +150 | °C | |

*(Continued)*

*(Continued)*

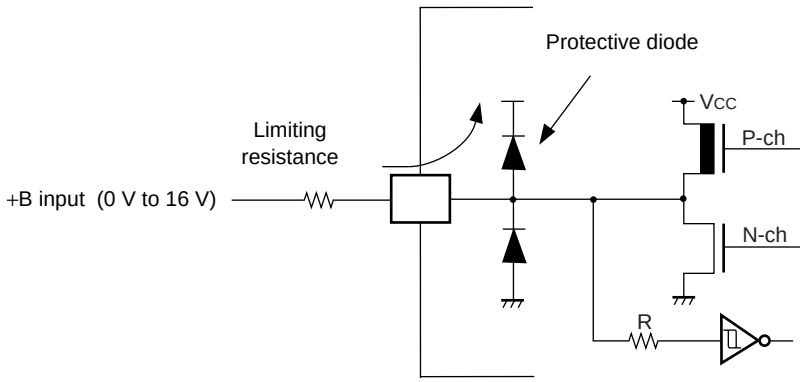
*1: Set $AV_{CC}$ and $V_{CC}$ to the same voltage. Make sure that $AV_{CC}$ does not exceed $V_{CC}$ and that the voltage at the analog inputs does not exceed $AV_{CC}$ when the power is switched on.

*2: $V_I$ and $V_O$ should not exceed $V_{CC}$ + 0.3 V. $V_I$ should not exceed the specified ratings. However if the maximun current to/from an input is limited by some means with external components, the $I_{CLAMP}$ rating supercedes the $V_I$ rating.

*3: Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1

*4:
- Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67 P70 to P77, P80 to P87, P90 to P97, PA0 to PA1
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

• Input/output equivalent circuits

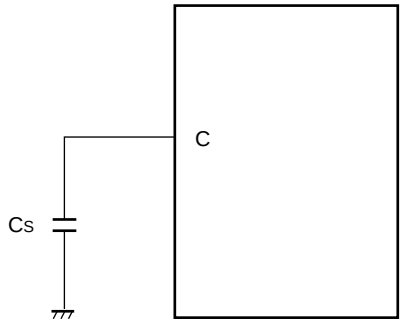



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Conditions

($V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$, $AV_{CC}$ | 4.0 | 5.0 | 5.5 | V | Under normal operation |
| | | 3.5 | 5.0 | 5.5 | V | Under normal operation, when not using the A/D converter and not Flash programming. |
| | | 4.5 | 5.0 | 5.5 | V | When External bus is used. |
| | | 3.0 | — | 5.5 | V | Maintains RAM data in stop mode |
| Smooth capacitor | $C_S$ | 0.1 | — | 1.0 | µF | Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the $V_{CC}$ should be greater than this capacitor. |
| Operating temperature | $T_A$ | –40 | — | +105 | °C | |




**C Pin Connection Diagram**

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

### 3. DC Characteristics

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input H voltage (At $V_{CC}$ = 5 V ± 10%) | $V_{IHS}$ | — | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Port inputs if CMOS hysteresis input levels are selected (except UART SIN input pins and I²C input pins) |
| | $V_{IHA}$ | — | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | Port inputs if AUTOMOTIVE input levels are selected |
| | $V_{IHT}$ | — | — | 2.0 | — | $V_{CC}$ + 0.3 | V | Port inputs if TTL input levels are selected |
| | $V_{IHS}$ | — | — | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | UART SIN inputs if CMOS input levels are selected |
| | $V_{IHI}$ | — | — | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | I²C Port inputs if CMOS hysteresis input levels are selected |
| | $V_{IHR}$ | — | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | $\overline{RST}$ input pin (CMOS hysteresis) |
| | $V_{IHM}$ | — | — | $V_{CC}$ – 0.3 | — | $V_{CC}$ + 0.3 | V | MD input pin |
| Input L voltage (At $V_{CC}$ = 5 V ± 10%) | $V_{ILS}$ | — | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | Port inputs if CMOS hysteresis input levels are selected (except UART SIN input pins and I²C input pins) |
| | $V_{ILA}$ | — | — | $V_{SS}$ – 0.3 | — | 0.5 $V_{CC}$ | V | Port inputs if AUTOMOTIVE input levels are selected |
| | $V_{ILT}$ | — | — | $V_{SS}$ – 0.3 | — | 0.8 | V | Port inputs if TTL input levels are selected |
| | $V_{ILS}$ | — | — | $V_{SS}$ – 0.3 | — | 0.3 $V_{CC}$ | V | UART SIN inputs if CMOS input levels are selected |
| | $V_{ILI}$ | — | — | $V_{SS}$ – 0.3 | — | 0.3 $V_{CC}$ | V | I²C Port inputs if CMOS hysteresis input levels are selected |
| | $V_{ILR}$ | — | — | $V_{SS}$ – 0.3 | — | 0.2 $V_{CC}$ | V | $\overline{RST}$ input pin (CMOS hysteresis) |
| | $V_{ILM}$ | — | — | $V_{SS}$ – 0.3 | — | $V_{SS}$ + 0.3 | V | MD input pin |
| Output H voltage | $V_{OH}$ | Normal outputs | $V_{CC}$ = 4.5 V, $I_{OH}$ = –4.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| Output H voltage | $V_{OHI}$ | I²C current outputs | $V_{CC}$ = 4.5 V, $I_{OH}$ = –3.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| Output L voltage | $V_{OL}$ | Normal outputs | $V_{CC}$ = 4.5 V, $I_{OL}$ = 4.0 mA | — | — | 0.4 | V | |
| Output L voltage | $V_{OLI}$ | I²C current outputs | $V_{CC}$ = 4.5 V, $I_{OL}$ = 3.0 mA | — | — | 0.4 | V | |

*(Continued)*

*(Continued)*

($T_A$ = –40 °C to +105, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Input leak current | $I_{IL}$ | — | $V_{CC}$ = 5.5 V, $V_{SS}$ < $V_I$ < $V_{CC}$ | –1 | — | 1 | µA | |
| Pull-up resistance | $R_{UP}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{RST}$ | — | 25 | 50 | 100 | kΩ | |
| Pull-down resistance | $R_{DOWN}$ | MD2 | — | 25 | 50 | 100 | kΩ | Except Flash devices |
| Power supply current* | $I_{CC}$ | $V_{CC}$ | $V_{CC}$ = 5.0 V, Internal frequency : 24 MHz, At normal operation. | — | 55 | 70 | mA | MB90F867A |
| | | | $V_{CC}$ = 5.0 V, Internal frequency : 24 MHz, At writing FLASH memory. | — | 70 | 85 | mA | MB90F867A |
| | | | $V_{CC}$ = 5.0 V, Internal frequency : 24 MHz, At erasing FLASH memory. | — | 75 | 90 | mA | MB90F867A |
| | $I_{CCS}$ | | $V_{CC}$ = 5.0 V, Internal frequency : 24 MHz, At Sleep mode. | — | 25 | 35 | mA | MB90F867A |
| | $I_{CTS}$ | | $V_{CC}$ = 5.0 V, Internal frequency : 2 MHz, At Main Timer mode | — | 0.3 | 0.8 | mA | MB90F867A |
| | $I_{CTSPLL6}$ | | $V_{CC}$ = 5.0 V, Internal frequency : 24 MHz, At PLL Timer mode, external frequency = 4 MHz | — | 4 | 7 | mA | MB90F867A |
| | $I_{CCL}$ | | $V_{CC}$ = 5.0V Internal frequency: 8 kHz, At sub operation $T_A$ = +25°C | — | 170 | 360 | µA | MB90F867A |
| | $I_{CCLS}$ | | $V_{CC}$ = 5.0V Internal frequency: 8 kHz, At sub sleep $T_A$ = +25°C | — | 20 | 50 | µA | MB90F867A |
| | $I_{CCT}$ | | $V_{CC}$ = 5.0V Internal frequency: 8 kHz, At watch mode $T_A$ = +25°C | — | 10 | 35 | µA | MB90F867A |
| | $I_{CCH}$ | | $V_{CC}$ = 5.0 V, At Stop mode, $T_A$ = +25°C | — | 7 | 25 | µA | MB90F867A |
| Input capacity | $C_{IN}$ | Other than C, $AV_{CC}$, $AV_{SS}$, AVRH, AVRL, $V_{CC}$, $V_{SS}$, | — | — | 5 | 15 | pF | |

* : Current values are tentative. They are subject to change without notice according to improvements in the characteristics. The power supply current is measured with an external clock.

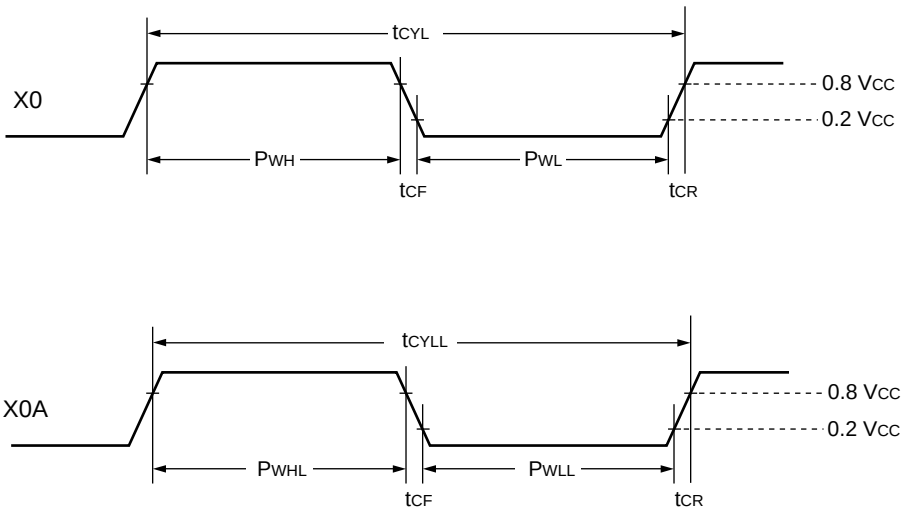
## 4. AC Characteristics

### (1) Clock Timing

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0 V)

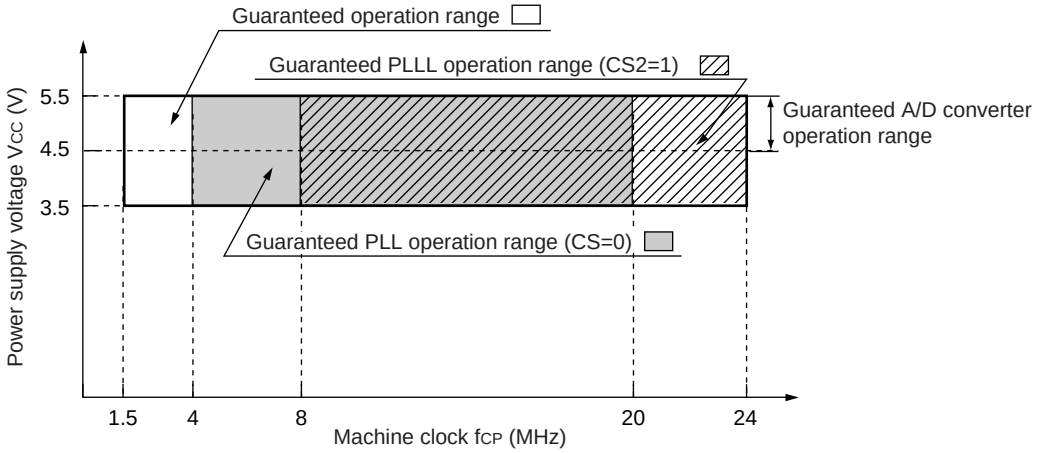
| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $f_C$ | X0, X1 | 3 | — | 16 | MHz | When using an oscillation circuit |
| | | X0 | 3 | — | 24 | MHz | When using an external clock* |
| | $f_{CL}$ | X0A, X1A | — | 32.768 | 100 | kHz | |
| Clock cycle time | $t_{CYL}$ | X0, X1 | 62.5 | — | 333 | ns | When using an oscillation circuit |
| | | X0 | 41.67 | — | 333 | ns | When using an external clock |
| | $t_{CYLL}$ | X0A, X1A | 10 | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0 | 10 | — | — | ns | Duty ratio is about 30% to 70%. |
| | $P_{WHL}$, $P_{WLL}$ | X0A | 5 | 15.2 | — | µs | |
| Input clock rise and fall time | $t_{CR}$, $t_{CF}$ | X0 | — | — | 5 | ns | When using external clock |
| Internal operating clock frequency (machine clock) | $f_{CP}$ | — | 1.5 | — | 24 | MHz | When using main clock |
| | $f_{CPL}$ | — | | 8.192 | 50 | kHz | When using sub clock |
| Internal operating clock cycle time (machine clock) | $t_{CP}$ | — | 41.67 | — | 666 | ns | When using main clock |
| | $t_{CPL}$ | — | 20 | 122.1 | — | µs | When using sub clock |

* : Whem selecting the PLL clock, the range of clock frequency is limitted. Use this product within range as mentioned in “Relation among external clock frequency and machine clock frequency”.



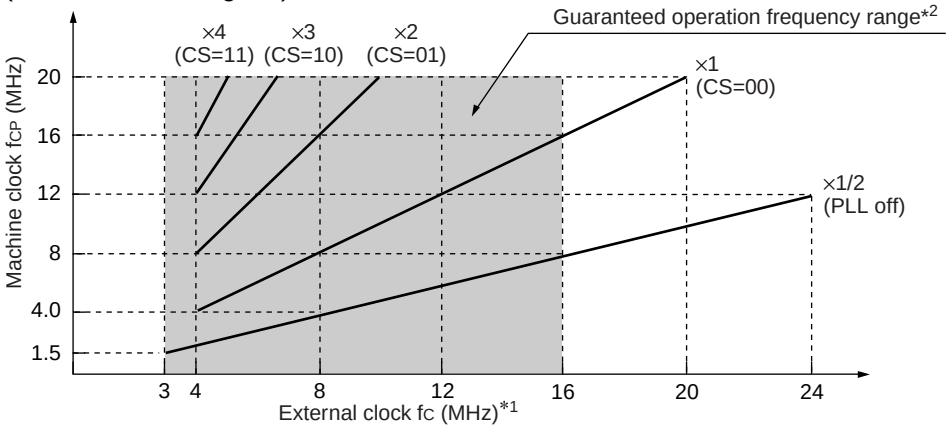

**Clock Timing**

• Guaranteed PLL operation range

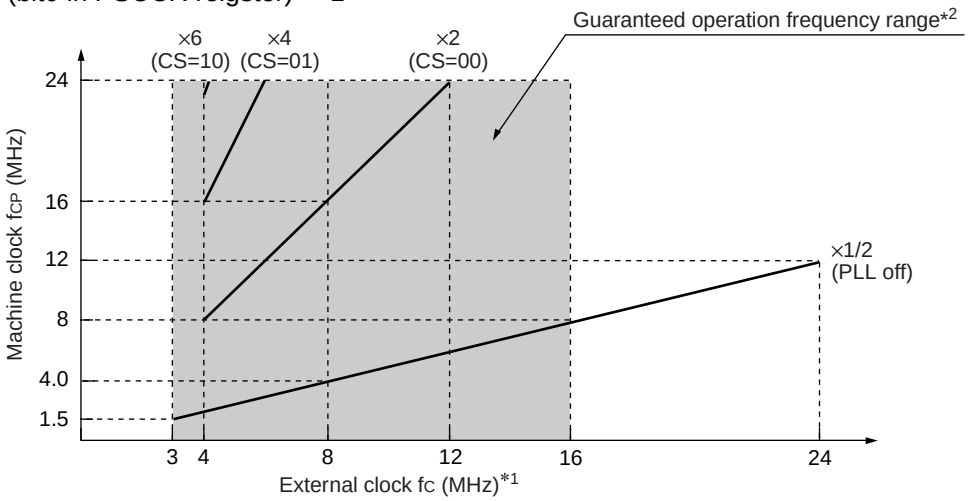



**Guaranteed operation range of MB90860A Series**

CS2 (bit0 in PSCCR reigster) = 0




CS2 (bit0 in PSCCR reigster) = 1




*1 : PLL × 1 guaranteed operation range is from 4.0 MHz to 20 MHz.
*2 : When using a crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz.

**External clock frequency and Machine clock frequency**

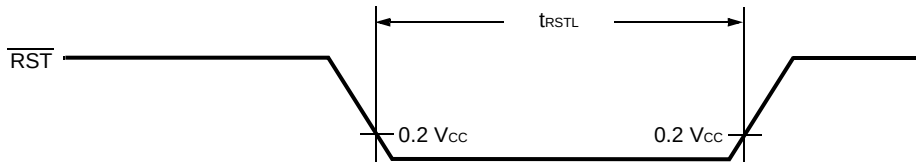
### (2) Reset Standby Input

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

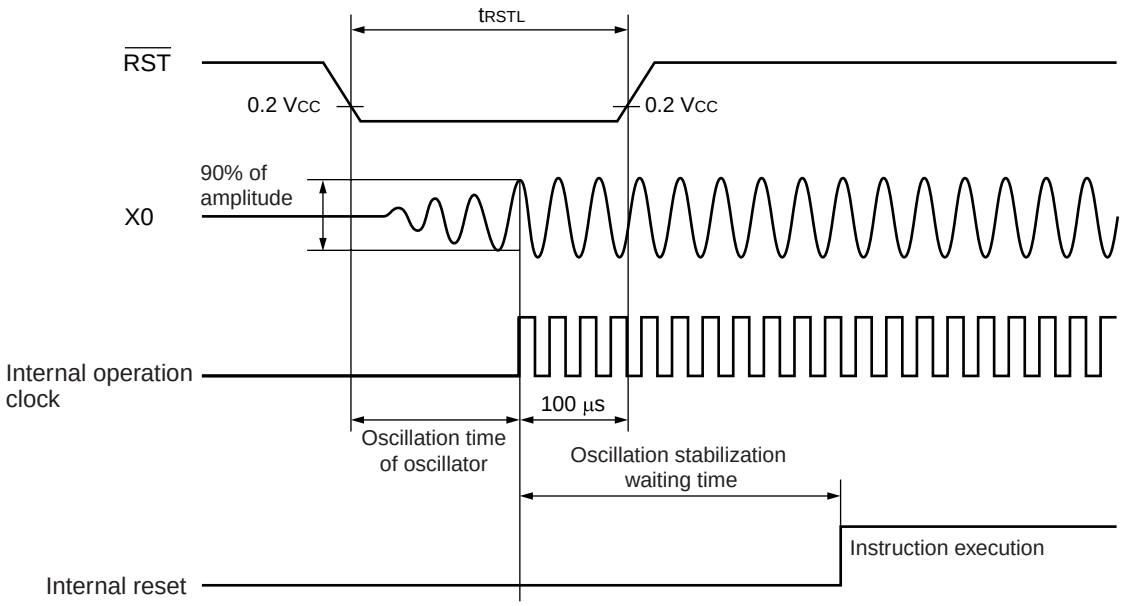
| Parameter | Symbol | Pin | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | 500 | — | ns | Under normal operation |
| | | | Oscillation time of oscillator* + 100 µs | — | ns | In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode |
| | | | 100 | — | µs | In Time Timer mode |

* : Oscillation time of oscillator is the time that the amplitude reaches 90%.
In the crystal oscillator, the oscillation time is between several ms and to tens of ms. In FAR / ceramic oscillators, the oscillation time is between hundreds of µs to several ms. With an external clock, the oscillation time is 0 ms.

**Under normal operation:**



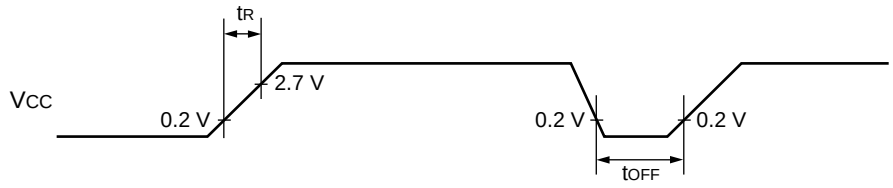

**In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode:**



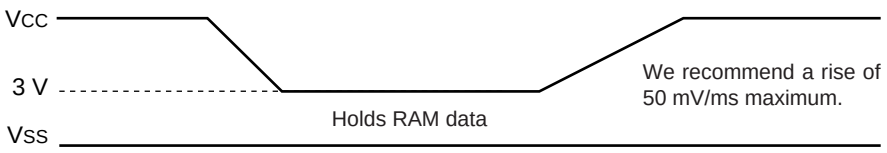
### (3) Power On Reset

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power on rise time | $t_R$ | $V_{CC}$ | — | 0.05 | 30 | ms | |
| Power off time | $t_{OFF}$ | $V_{CC}$ | | 1 | — | ms | Due to repetitive operation |



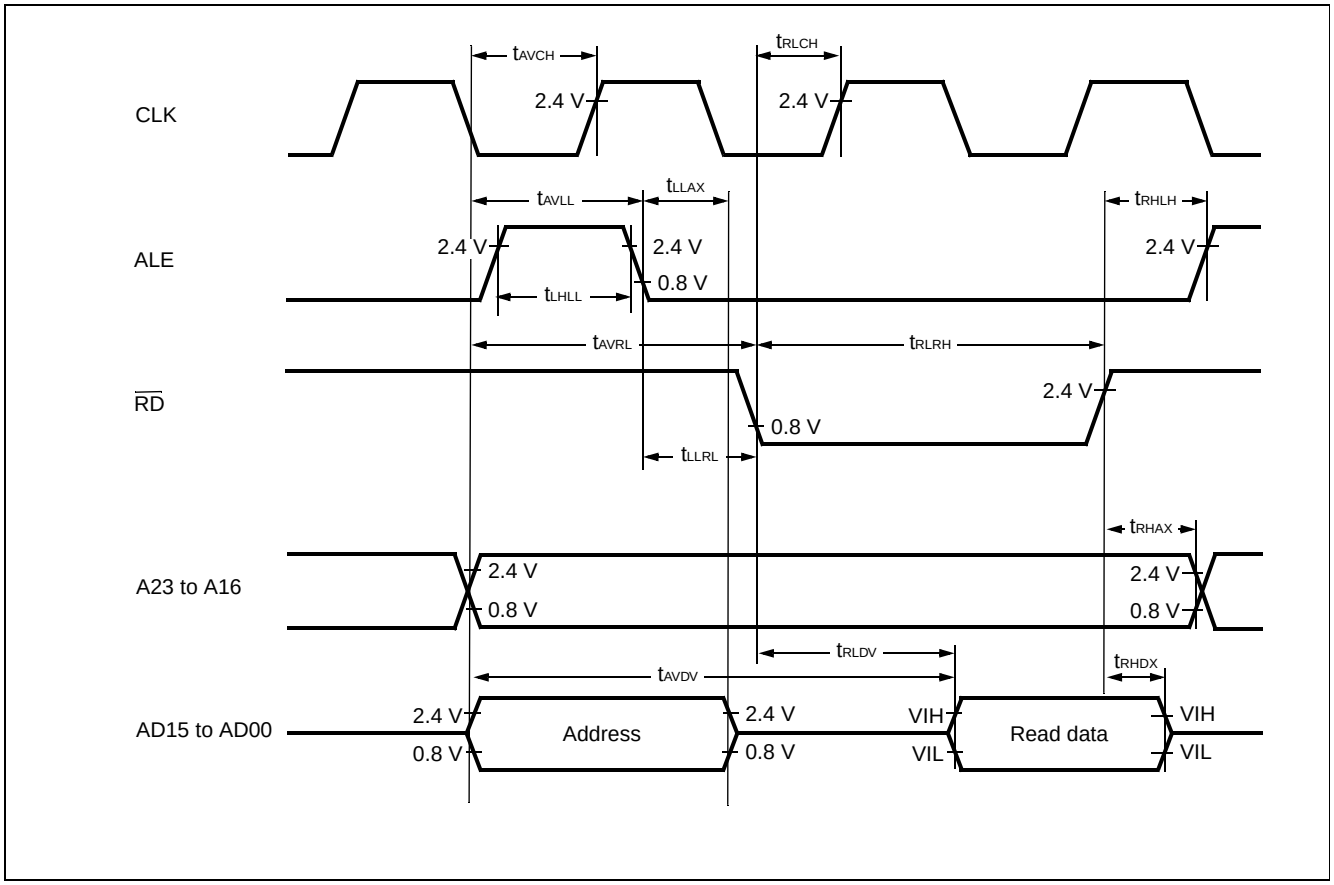

If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



### (4) Bus Timing (Read)

($T_A$ = –40°C to +85°C, $V_{CC}$ = 4.5 V to 5.5 V, $V_{SS}$ = 0.0 V, Machine Clock ≤ 16 MHz)

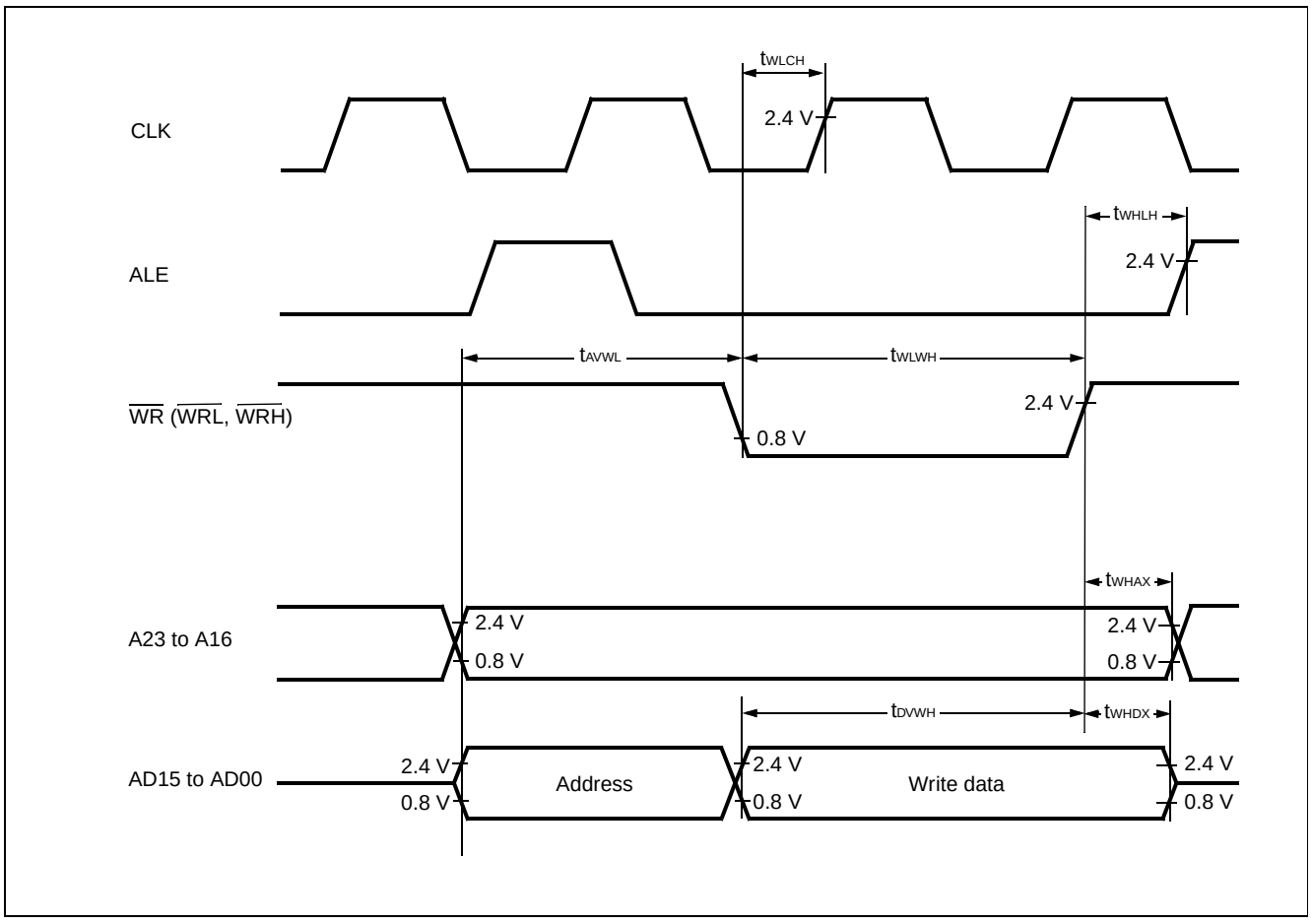
| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| ALE pulse width | $t_{LHLL}$ | ALE | — | $t_{CP}/2$ – 10 | — | ns | |
| Valid address ⇒ ALE ↓ time | $t_{AVLL}$ | ALE, A23 to A16, AD15 to AD00 | | $t_{CP}/2$ – 15 | — | ns | |
| ALE ↓ ⇒ Address valid time | $t_{LLAX}$ | ALE, AD15 to AD00 | | $t_{CP}/2$ – 15 | — | ns | |
| Valid address ⇒ $\overline{RD}$ ↓ time | $t_{AVRL}$ | A23 toA16, AD15 to AD00, $\overline{RD}$ | | $t_{CP}$ – 15 | — | ns | |
| Valid address ⇒ Valid data input | $t_{AVDV}$ | A23 to A16, AD15 to AD00 | | — | 5 $t_{CP}/2$ – 40 | ns | |
| $\overline{RD}$ pulse width | $t_{RLRH}$ | $\overline{RD}$ | | 3 $t_{CP}/2$ – 20 | — | ns | |
| $\overline{RD}$ ↓ ⇒ Valid data input | $t_{RLDV}$ | $\overline{RD}$, AD15 to AD00 | | — | 3 $t_{CP}/2$ – 50 | ns | |
| $\overline{RD}$ ↑ ⇒ Data hold time | $t_{RHDX}$ | $\overline{RD}$, AD15 to AD00 | | 0 | — | ns | |
| $\overline{RD}$ ↓ ⇒ ALE ↑ time | $t_{RHLH}$ | $\overline{RD}$, ALE | | $t_{CP}/2$ – 15 | — | ns | |
| $\overline{RD}$ ↑ ⇒ Address valid time | $t_{RHAX}$ | $\overline{RD}$, A23 to A16 | | $t_{CP}/2$ – 10 | — | ns | |
| Valid address ⇒ CLK ↑ time | $t_{AVCH}$ | A23 to A16, AD15 to AD00, CLK | | $t_{CP}/2$ – 15 | — | ns | |
| $\overline{RD}$ ↓ ⇒ CLK ↑ time | $t_{RLCH}$ | $\overline{RD}$, CLK | | $t_{CP}/2$ – 15 | — | ns | |
| ALE ↓ ⇒ $\overline{RD}$ ↓ time | $t_{LLRL}$ | ALE, $\overline{RD}$ | | $t_{CP}/2$ – 15 | — | ns | |



### (5) Bus Timing (Write)

($T_A$ = –40°C to +85°C, $V_{CC}$ = 4.5 V to 5.5 V, $V_{SS}$ = 0.0 V, Machine Clock ≤ 16 MHz)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Valid address ⇒ $\overline{WR}$ ↓ time | $t_{AVWL}$ | A23 to A16, AD15 to AD00, $\overline{WR}$ | — | $t_{CP}$–15 | — | ns | |
| $\overline{WR}$ pulse width | $t_{WLWH}$ | $\overline{WR}$ | | 3 $t_{CP}$/2 – 20 | — | ns | |
| Valid data output ⇒ $\overline{WR}$ ↑ time | $t_{DVWH}$ | AD15 to AD00, $\overline{WR}$ | | 3 $t_{CP}$/2 – 20 | — | ns | |
| $\overline{WR}$ ↑ ⇒ Data hold time | $t_{WHDX}$ | AD15 to AD00, $\overline{WR}$ | | 15 | — | ns | |
| $\overline{WR}$ ↑ ⇒ Address valid time | $t_{WHAX}$ | A23 to A16, $\overline{WR}$ | | $t_{CP}$/2 – 10 | — | ns | |
| $\overline{WR}$ ↑ ⇒ ALE ↑ time | $t_{WHLH}$ | $\overline{WR}$, ALE | | $t_{CP}$/2 – 15 | — | ns | |
| $\overline{WR}$ ↓ ⇒ CLK ↑ time | $t_{WLCH}$ | $\overline{WR}$, CLK | | $t_{CP}$/2 – 15 | — | ns | |

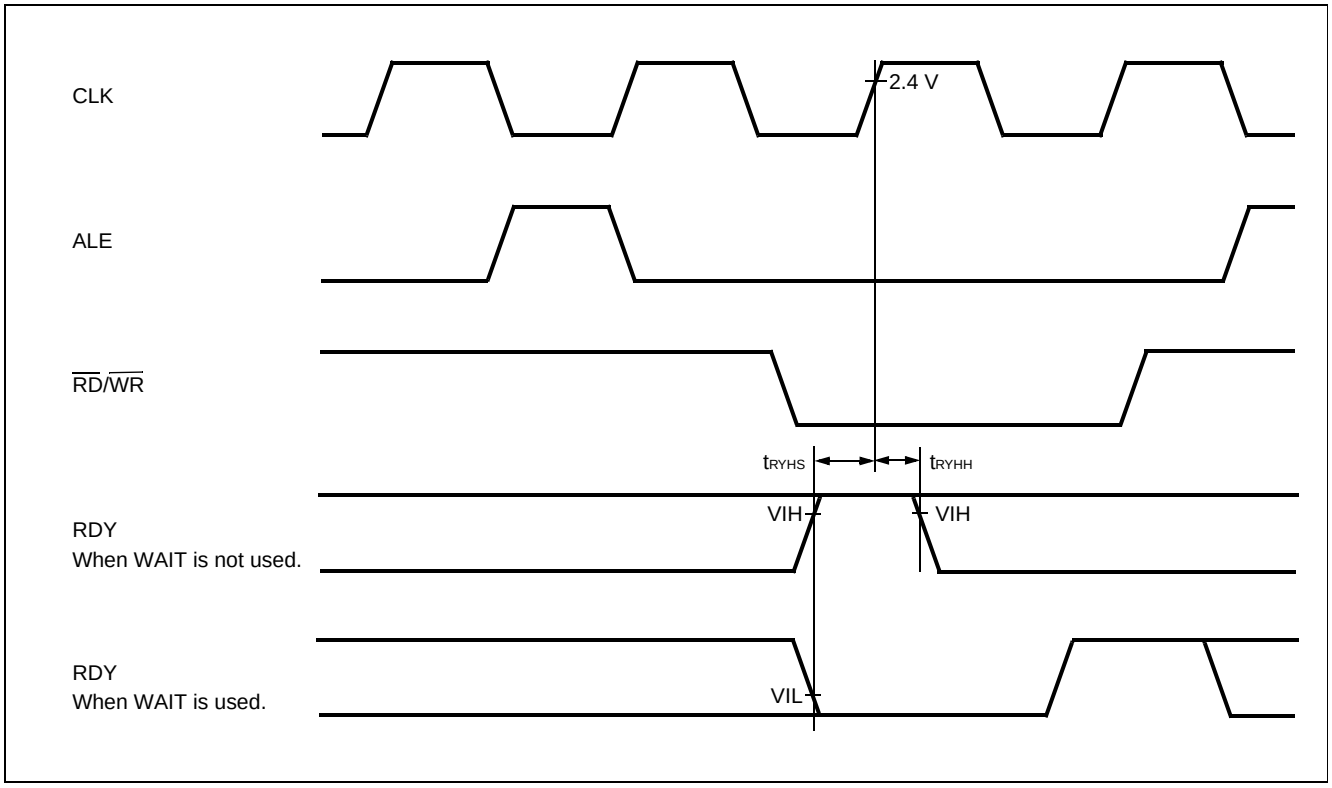


### (6) Ready Input Timing

($T_A$ = –40°C to +85°C, $V_{CC}$ = 4.5 V to 5.5 V, $V_{SS}$ = 0.0 V, Machine Clock ≤ 16 MHz)

| Parameter | Symbol | Pin | Test Condition | Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| RDY setup time | $t_{RYHS}$ | RDY | — | 45 | — | ns | |
| RDY hold time | $t_{RYHH}$ | RDY | | 0 | — | ns | |

Note : If the RDY setup time is insufficient, use the auto-ready function.

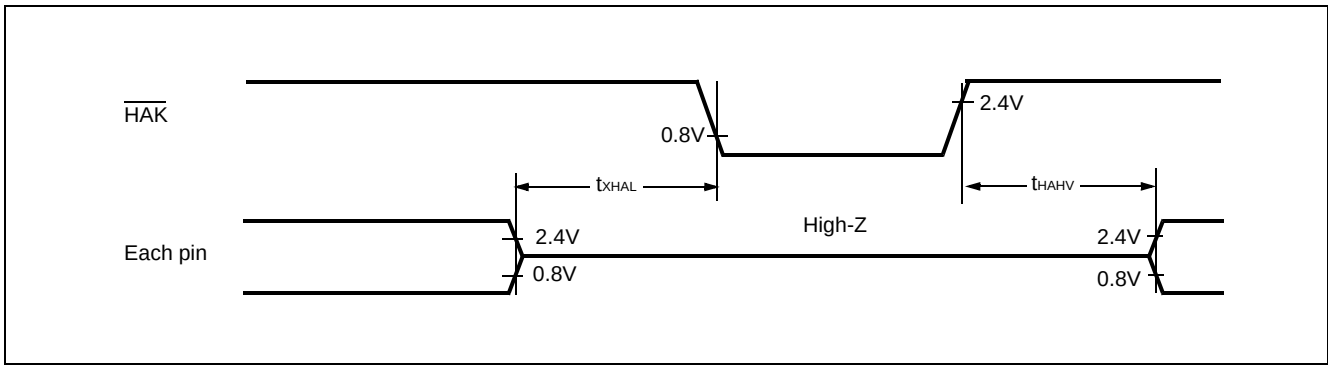


### (7) Hold Timing

($T_A$ = –40°C to +85°C, $V_{CC}$ = 4.5 V to 5.5 V, $V_{SS}$ = 0.0 V, Machine Clock ≤ 16 MHz)

| Parameter | Symbol | Pin | Condition | Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Pin floating ⇒ $\overline{HAK}$ ↓ time | $t_{XHAL}$ | $\overline{HAK}$ | — | 30 | $t_{CP}$ | ns | |
| $\overline{HAK}$ ↑ time ⇒ Pin valid time | $t_{HAHV}$ | $\overline{HAK}$ | | $t_{CP}$ | 2 $t_{CP}$ | ns | |

Note : There is more than 1 cycle from when HRQ reads in until the $\overline{HAK}$ is changed.

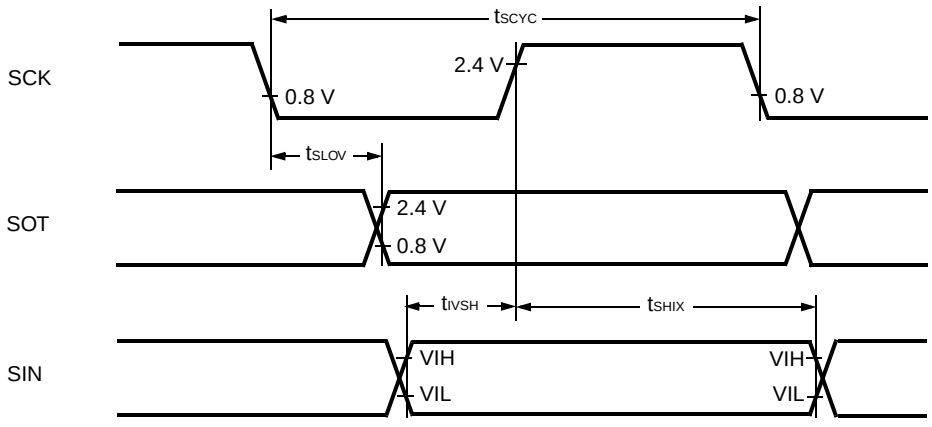


### (8) UART0/1/2/3/4

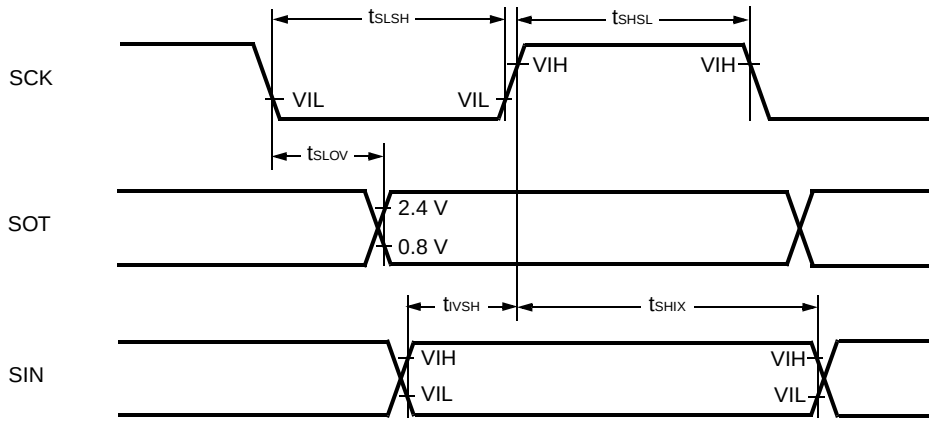
($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 4.5 V to 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK4 | Internal clock operation output pins are $C_L$ = 80 pF + 1 TTL. | 8 $t_{CP}$ | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCK0 to SCK4, SOT0 to SOT4 | | –80 | +80 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCK0 to SCK4, SIN0 to SIN4 | | 100 | — | ns | |
| SCK ↑ → Valid SIN hold time | $t_{SHIX}$ | SCK0 to SCK4, SIN0 to SIN4 | | 60 | — | ns | |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK0 to SCK4 | External clock operation output pins are $C_L$ = 80 pF + 1 TTL. | 4 $t_{CP}$ | — | ns | |
| Serial clock “L” pulse width | $t_{SLSH}$ | SCK0 to SCK4 | | 4 $t_{CP}$ | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SCK0 to SCK4, SOT0 to SOT4 | | — | 150 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SCK0 to SCK4, SIN0 to SIN4 | | 60 | — | ns | |
| SCK ↑ → Valid SIN hold time | $t_{SHIX}$ | SCK0 to SCK4, SIN0 to SIN4 | | 60 | — | ns | |

Notes : • AC characteristic in CLK synchronized mode.
• $C_L$ is load capacity value of pins when testing.
• $t_{CP}$ is the machine cycle (Unit : ns)




**Internal Shift Clock Mode**

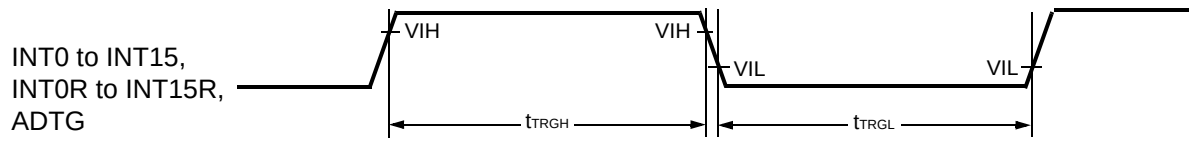



**External Shift Clock Mode**

### (9) Trigger Input Timing

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 4.5 V to 5.5 V, $V_{SS}$ = 0 V)

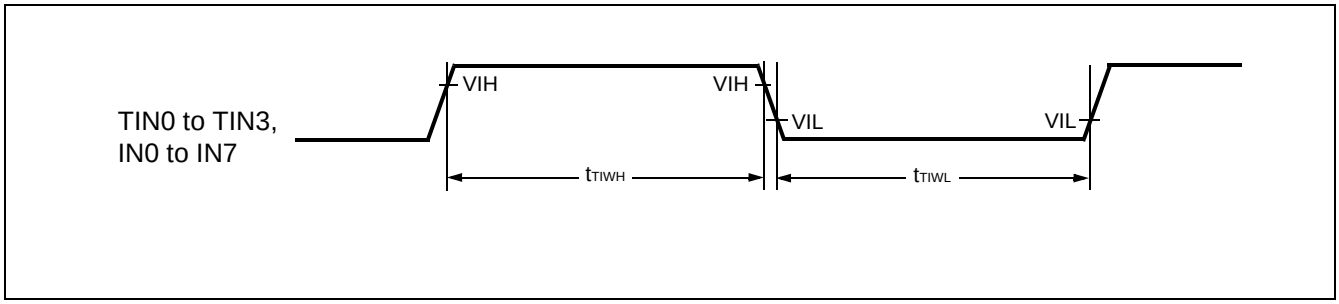
| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | INT0 to INT15, INT0R to INT15R, ADTG | — | 5 $t_{CP}$ | — | ns | |



### (10) Timer Related Resource Input Timing

($T_A$ = –40 °C to +105 °C, $V_{CC}$ = 4.5 V to 5.5 V, $V_{SS}$ = 0 V)

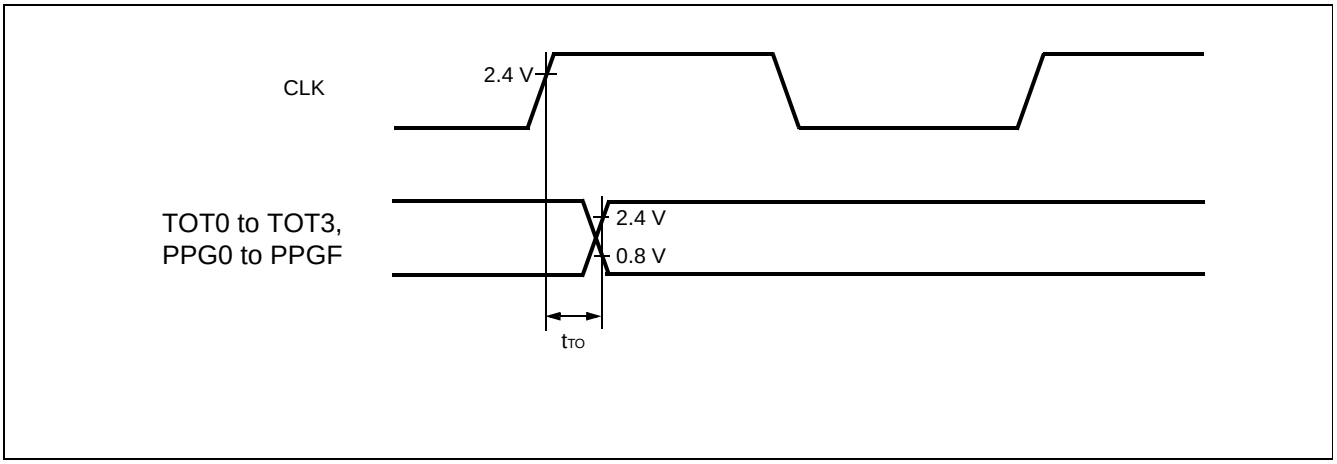
| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$<br>$t_{TIWL}$ | TIN0 to TIN3<br>IN0 to IN7 | — | 4 $t_{CP}$ | — | ns | |




### (11) Timer Related Resource Output Timing

($T_A$ = –40° to +105°C, $V_{CC}$ = 4.5 V to 5.5 V, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| CLK ↑ ⇒ $T_{OUT}$ change time | $t_{TO}$ | TOT0 to TOT3,<br>PPG0 to PPGF | — | 30 | — | ns | |



### (12) I²C Timing

($T_A$ = –40°C to +105°C, $V_{CC}$ = 4.5 V to 5.5 V, $V_{SS}$ = 0.0 V)

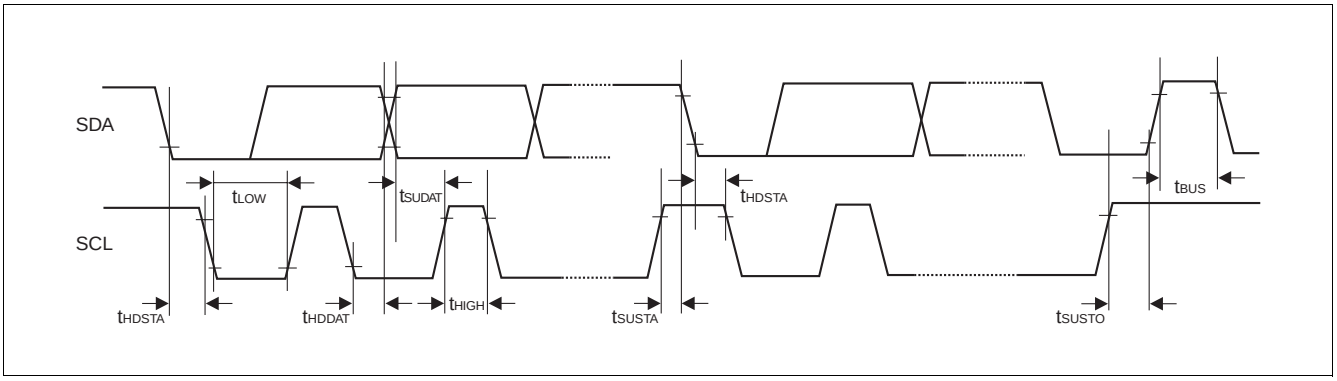
| Parameter | Symbol | Condition | Standard-mode | | Fast-mode*4 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| SCL clock frequency | $f_{SCL}$ | R = 1.7 kΩ, C = 50 pF*1 | 0 | 100 | 0 | 400 | kHz |
| Hold time (repeated) START condition SDA ↓ → SCL ↓ | $t_{HDSTA}$ | | 4.0 | — | 0.6 | — | µs |
| "L" width of the SCL clock | $t_{LOW}$ | | 4.7 | — | 1.3 | — | µs |
| "H" width of the SCL clock | $t_{HIGH}$ | | 4.0 | — | 0.6 | — | µs |
| Set-up time for a repeated START condition SCL ↑ → SDA ↓ | $t_{SUSTA}$ | | 4.7 | — | 0.6 | — | µs |
| Data hold time SCL ↓ → SDA ↓ ↑ | $t_{HDDAT}$ | | 0 | 3.45*2 | 0 | 0.9*3 | µs |
| Data set-up time SDA ↓ ↑ → SCL ↑ | $t_{SUDAT}$ | | 250 | — | 100 | — | ns |
| Set-up time for STOP condition SCL ↑ → SDA ↑ | $t_{SUSTO}$ | | 4.0 | — | 0.6 | — | µs |
| Bus free time between a STOP and START condition | $t_{BUS}$ | | 4.7 | — | 1.3 | — | µs |

*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum $t_{HDDAT}$ only has to be met if the device does not stretch the "L" width ($t_{LOW}$) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.



## 5. A/D Converter

($T_A$ = –40 °C to +105 °C, 3.0 V ≤ AVRH – AVRL, $V_{CC}$ = $AV_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | — | 10 | bit | |
| Total error | — | — | — | — | ±3.0 | LSB | |
| Nonlinearity error | — | — | — | — | ±2.5 | LSB | |
| Differential nonlinearity error | — | — | — | — | ±1.9 | LSB | |
| Zero reading voltage | $V_{OT}$ | AN0 to AN23 | AVRL – 1.5 | AVRL + 0.5 | AVRL + 2.5 | LSB | |
| Full scale reading voltage | $V_{FST}$ | AN0 to AN23 | AVRH – 3.5 | AVRH – 1.5 | AVRH + 0.5 | LSB | |
| Compare time | — | — | 1.0 | — | 16,500 | µs | 4.5 V ≤ $AV_{CC}$ ≤ 5.5 V |
| | | | 2.0 | | | | 4.0 V ≤ $AV_{CC}$ < 4.5 V |
| Sampling time | — | — | 0.5 | — | ∞ | µs | 4.5 V ≤ $AV_{CC}$ ≤ 5.5 V |
| | | | 1.2 | | | | 4.0 V ≤ $AV_{CC}$ < 4.5 V |
| Analog port input current | $I_{AIN}$ | AN0 to AN23 | –0.3 | — | +0.3 | µA | |
| Analog input voltage range | $V_{AIN}$ | AN0 to AN23 | AVRL | — | AVRH | V | |
| Reference voltage range | — | AVRH | AVRL + 2.7 | — | $AV_{CC}$ | V | |
| | — | AVRL | 0 | — | AVRH – 2.7 | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 3.5 | 7.5 | mA | |
| | $I_{AH}$ | $AV_{CC}$ | — | — | 5 | µA | * |
| Reference voltage current | $I_R$ | AVRH | — | 600 | 900 | µA | |
| | $I_{RH}$ | AVRH | — | — | 5 | µA | * |
| Offset between input channels | — | AN0 to AN23 | — | — | 4 | LSB | |

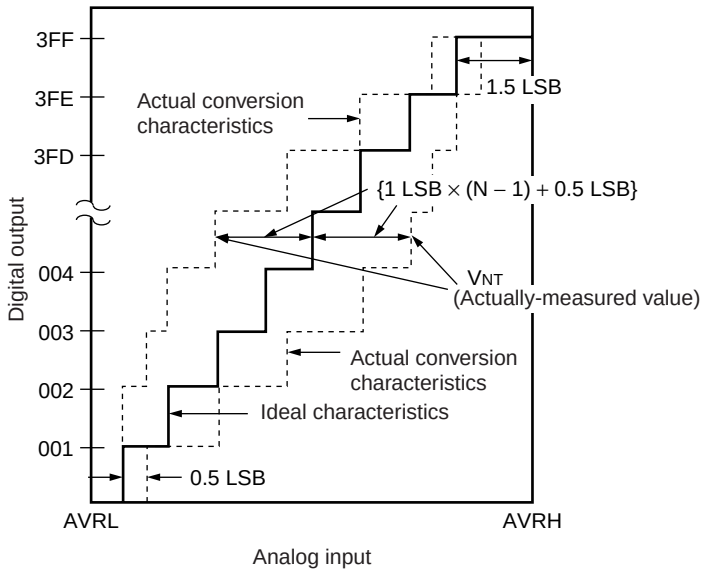
* : When not operating A/D converter, this is the current ($V_{CC}$ = $AV_{CC}$ = AVRH = 5.0 V) .

Note : The accuracy gets worse as AVRH – AVRL becomes smaller.

## 6. Definition of A/D Converter Terms

| | | |
|---|---|---|
| Resolution | : | Analog variation that is recognized by an A/D converter. |
| Non linearity error | : | Deviation between a line across zero-transition line ( “00 0000 0000” ← → “00 0000 0001” ) and full-scale transition line ( “11 1111 1110” ← → “11 1111 1111” ) and actual conversion characteristics. |
| Differential linearity error | : | Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value. |
| Total error | : | Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error. |
| Zero reading voltage | : | Input voltage which results in the minimum conversion value. |
| Full scale reading voltage | : | Input voltage which results in the maximum conversion value. |

Total error




$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

$V_{OT}$ (Ideal value) = AVRL + 0.5 LSB [V]

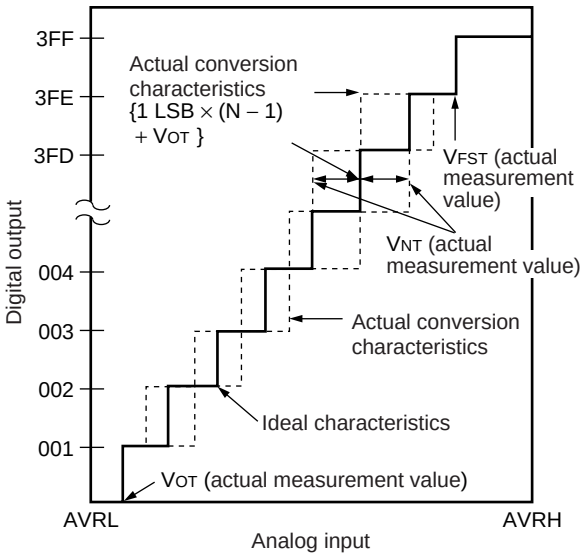
$V_{FST}$ (Ideal value) = AVRH – 1.5 LSB [V]

$V_{NT}$ : A voltage at which digital output transitions from (N – 1) to N.

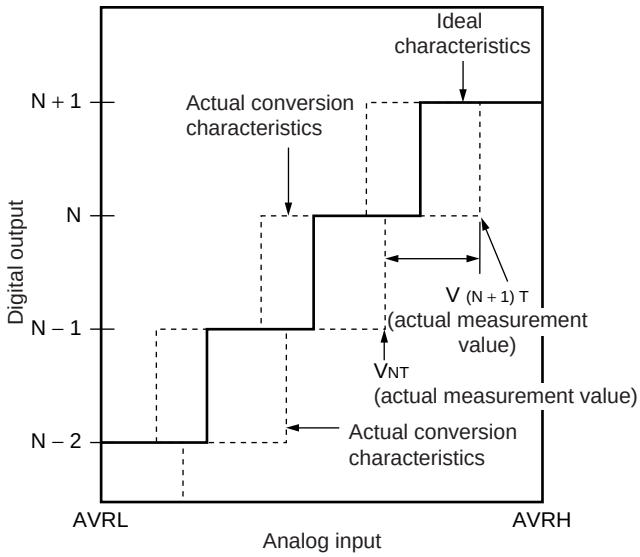
*(Continued)*

*(Continued)*

Non linearity error




Differential linearity error




$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

$V_{OT}$ : Voltage at which digital output transits from “$000_H$” to “$001_H$.”
$V_{FST}$ : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

## 7. Notes on A/D Converter Section

Use the device with external circuits of the following output impedance for analog inputs :

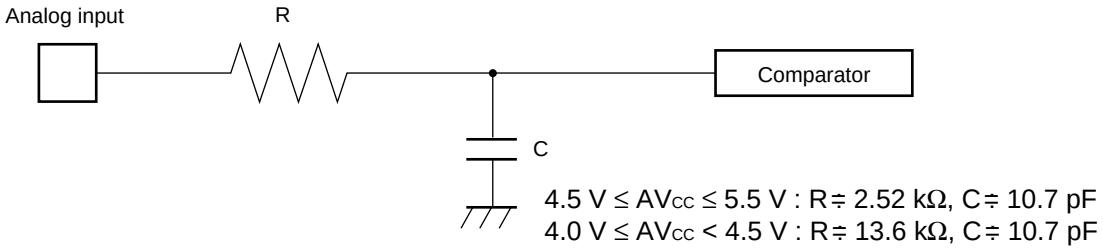
Recommended output impedance of external circuits are : Approx. 1.5 kΩ or lower (4.0 V ≤ $AV_{CC}$ ≤ 5.5 V, sampling period ≤ 0.5 µs)

if the output inpedance exceeds 1.5 kΩ, set a longer sampling time or add an external capacitor compensate the output inpedance. About setting of sampling time, please refer to hardware manual of MB90860A series.

If an external capacitor is used, in consideration of the effect by tap capacitance caused by external capacitors and on-chip capacitors, capacitance of the external one is recommended to be several thousand times as high as internal capacitor.

If output impedance of an external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model




Note : Use the values in the figure only as a guideline.

## 8. Flash Memory Program/Erase Characteristics

| Parameter | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Sector erase time | $T_A$ = +25 °C<br>$V_{CC}$ = 5.0 V | — | 1 | 15 | s | Excludes programming prior to erasure |
| Chip erase time | | — | 9 | — | s | Excludes programming prior to erasure |
| Word (16 bit width) programming time | | — | 16 | 3,600 | µs | Except for the over head time of the system |
| Programs/Erase cycle | — | 10,000 | — | — | cycle | |
| Flash Data Retention Time | Average<br>$T_A$ = +85 °C | 20 | — | — | Year | * |

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

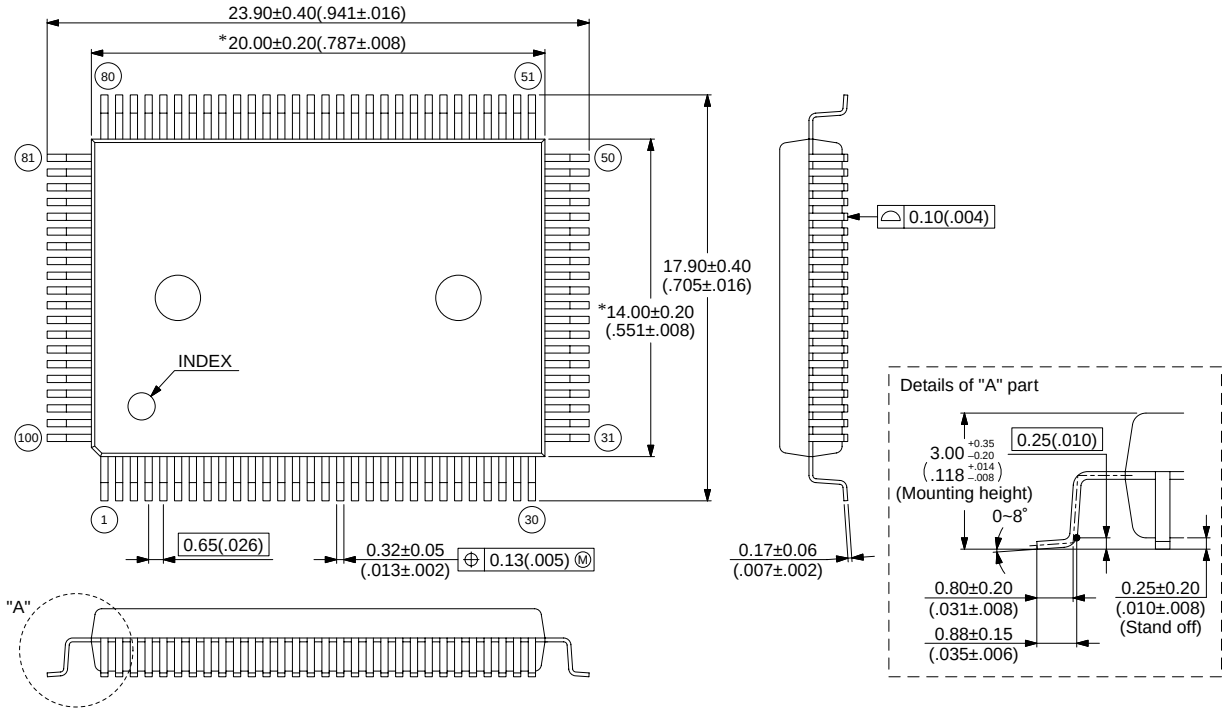
## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB90F867APF | 100-pin Plastic QFP (FPT-100P-M06) | |
| MB90F867ASPF | | |
| MB90867APF | | |
| MB90867ASPF | | |
| MB90F867APFV | 100-pin Plastic LQFP (FPT-100P-M05) | |
| MB90F867ASPFV | | |
| MB90867APFV | | |
| MB90867ASPFV | | |
| MB90V340<br>MB90V340S | 299-pin Ceramic PGA (PGA-299C-A01) | For evaluation |

## ■ PACKAGE DIMENSIONS

100-pin Plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness including plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.





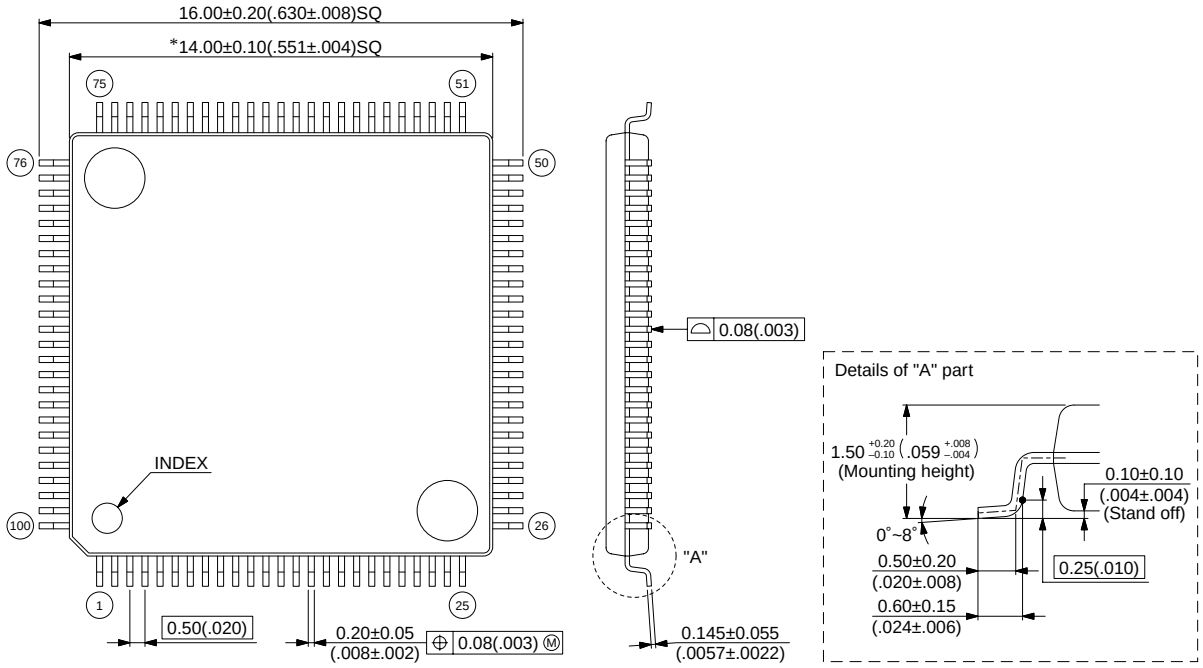

Dimensions in mm (inches)
Note : The values in parentheses are reference values.

*(Continued)*

*(Continued)*

100-pin Plastic LQFP
(FPT-100P-M05)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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