ABSOLUTE MAXIMUM RATINGS

PVDD, IN+, IN-, $\overline{SHDN}$, GAIN to PGND.................... -0.3V to 6V
All Other Pins to PGND ....-0.3V to (V_{PVDD} + 0.3V)
Continuous Current Into/Out of PVDD, PGND, OUT_... ±600mA
Continuous Input Current (all other pins)........................ ±20mA
Duration of Short Circuit Between
OUT_ and PVDD, PGND ....Continuous
OUT+ and OUT-..Continuous
Continuous Power Dissipation (T_A = +70°C) for Multilayer Board
TDFN-EP (derate 11.9mW/°C)..................................953.5mW
WLP (derate 12mW/°C) 963.8mW
Junction Temperature ....+150°C
Operating Temperature Range.......................... -40°C to +85°C
Storage Temperature Range............................ -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB (GAIN = PVDD), R_L = ∞, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AMPLIFIER CHARACTERISTICS							
Speaker Supply Voltage Range	PVDD	Inferred from PSRR test		2.6		5.5	V
Quiescent Supply Current	I_{DD}	V_{PVDD} = 5.0V			1.1	2.0	mA
		V_{PVDD} = 3.7V			0.78		
Shutdown Supply Current	I_{SHDN}	$V_{\overline{SHDN}}$ = 0V, T_A = +25°C			< 0.1	10	µA
Turn-On Time	t_{ON}				3.7	10	ms
Bias Voltage	V_{BIAS}				1.3		V
Maximum AC Input Voltage Swing	V_{IN}	Differential			2.0		V_{RMS}
		Single ended			1.0		
Input Resistance	R_{IN}	T_A = +25°C	A_V = 12dB	10	20		kΩ
			A_V = 9dB	10	20		
			A_V = 6dB	10	20		
			A_V = 3dB	15	28		
			A_V = 0dB	26	40		
Voltage Gain	A_V	Connect GAIN to PVDD		11.5	12	12.5	dB
		Connect GAIN to PVDD through 100kΩ ±5%		8.5	9	9.5	
		GAIN unconnected		5.5	6	6.5	
		Connect GAIN to PGND through 100kΩ ±5%		2.5	3	3.5	
		Connect GAIN to PGND		-0.5	0	+0.5	
Output Offset Voltage	V_{OS}	T_A = +25°C (Note 3)			±1	± 3	mV
Click and Pop	K_{CP}	Peak voltage, A-weighted, 32 samples per second, R_L = 8Ω (Notes 3, 4)	Into shutdown		-66		dBV
			Out of shutdown		-66		
Common-Mode Rejection Ratio	CMRR	f_{IN} = 1kHz, input referred			50		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB (GAIN = PVDD), R_L = ∞, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

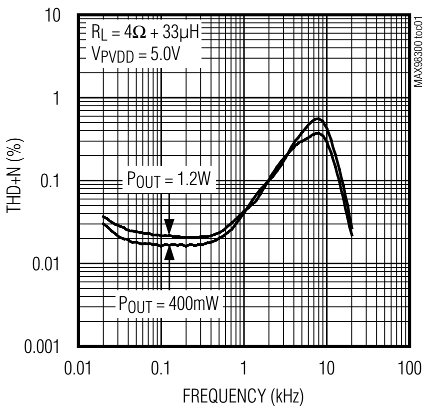
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio (Note 3)	PSRR	V_{PVDD} = 2.6V to 5.5V, T_A = +25°C		50	70		dB
		V_{RIPPLE} = 200mV_{P-P}	f = 217Hz		67		
			f = 20kHz		63		
Output Power	P_{OUT}	f_{IN} = 1kHz, R_L = 4Ω	THD+N = 1%		2.1		W
			THD+N = 10%		2.6		
		f_{IN} = 1kHz, R_L = 8Ω	THD+N = 1%		1.35		
			THD+N = 10%		1.65		
			THD+N = 1%, V_{PVDD} = 3.7V		0.71		
			THD+N = 10%, V_{PVDD} = 3.7V		0.89		
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz	R_L = 4Ω P_{OUT} = 1W		0.05		%
			R_L = 8Ω P_{OUT} = 0.5W		0.04		%
Oscillator Frequency	f_{OSC}				300		kHz
Spread-Spectrum Bandwidth					±10		kHz
Efficiency	η	P_{OUT} = 1.3W, R_L = 8Ω			89		%
Noise	V_N	A_V = 0dB, A-weighted (Note 3)			36		µV_{RMS}
Output Current Limit	I_{LIM}				2		A
Thermal Shutdown Level					+160		°C
Thermal Shutdown Hysteresis					20		°C
DIGITAL INPUT ($\overline{SHDN}$)							
Input-Voltage High	V_{INH}			1.4			V
Input-Voltage Low	V_{INL}					0.4	V
Input Leakage Current		T_A = +25°C				±10	µA

Note 1: All devices are 100% production tested at +25°C. All temperature limits are guaranteed by design.
Note 2: Testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For R_L = 4Ω, L = 33µH. For R_L = 8Ω, L = 68µH.
Note 3: Amplifier inputs AC-coupled to ground.
Note 4: Mode transitions controlled by $\overline{SHDN}$.

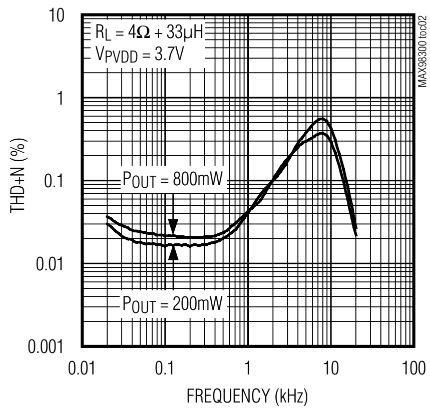
Typical Operating Characteristics

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB, R_L = ∞, unless otherwise specified, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

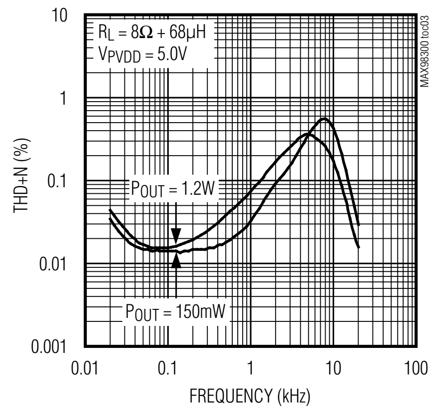
THD+N vs. FREQUENCY



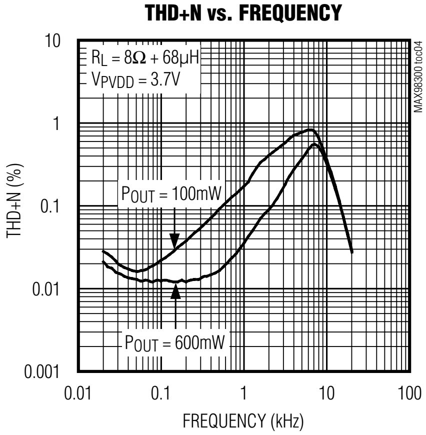
THD+N vs. FREQUENCY



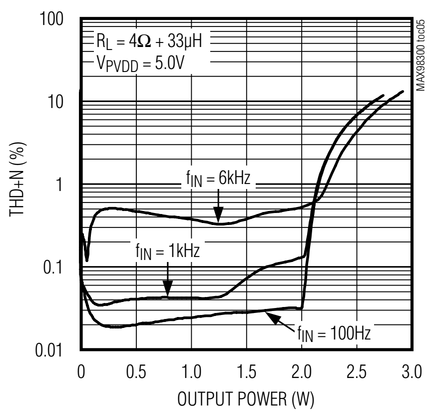
THD+N vs. FREQUENCY



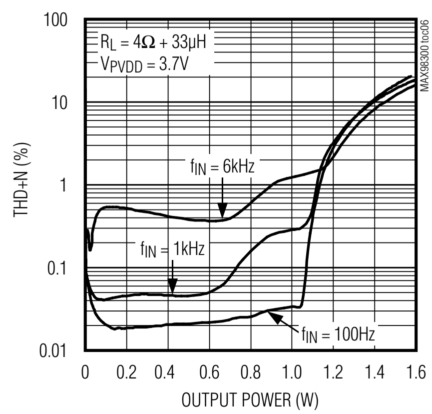
THD+N vs. FREQUENCY



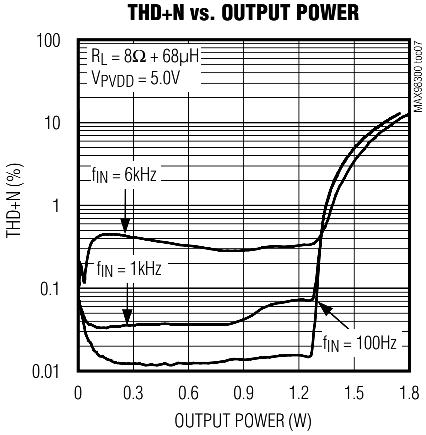
THD+N vs. OUTPUT POWER



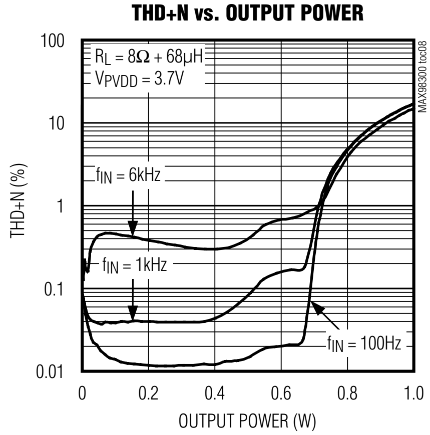
THD+N vs. OUTPUT POWER



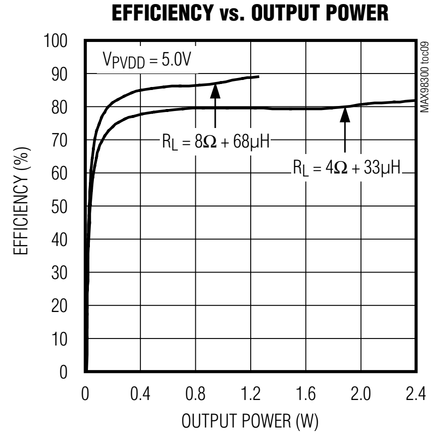
THD+N vs. OUTPUT POWER



THD+N vs. OUTPUT POWER



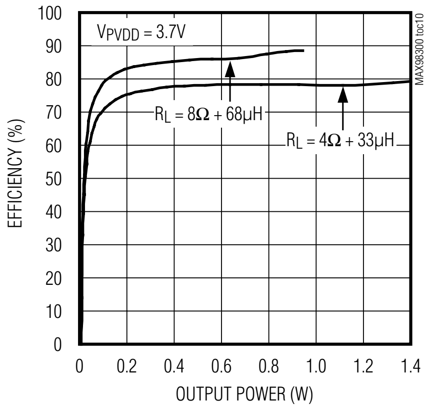
EFFICIENCY vs. OUTPUT POWER



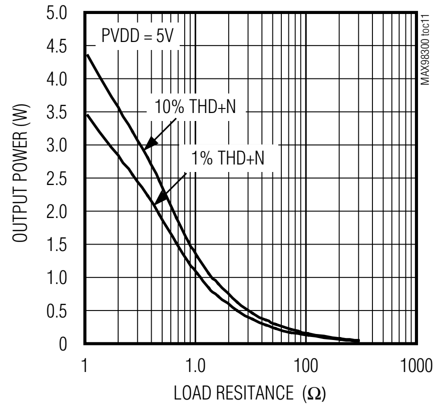
Typical Operating Characteristics (continued)

($V_{PVDD} = V_{\overline{SHDN}} = 5.0V$, $V_{PGND} = 0V$, $A_V = 12dB$, $R_L = \infty$, unless otherwise specified, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, $T_A = +25°C$, unless otherwise noted.)

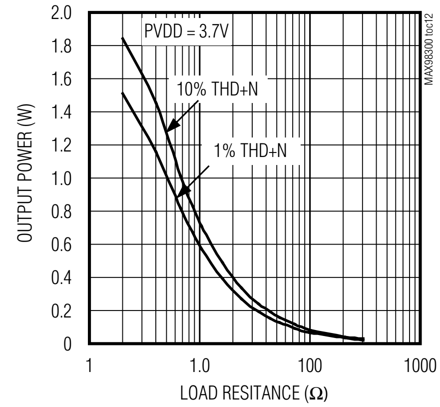
EFFICIENCY vs. OUTPUT POWER



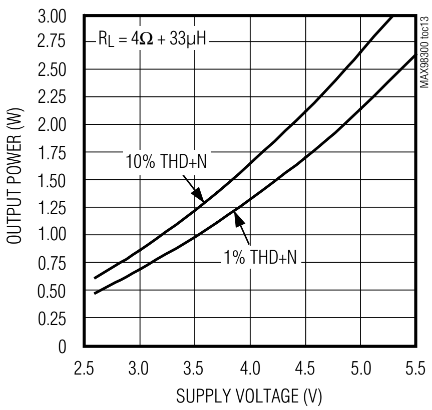
OUTPUT POWER vs. LOAD RESISTANCE



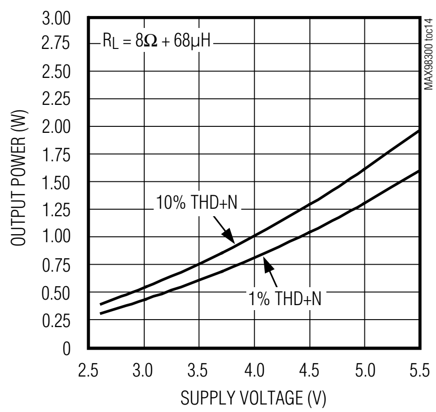
OUTPUT POWER vs. LOAD RESISTANCE



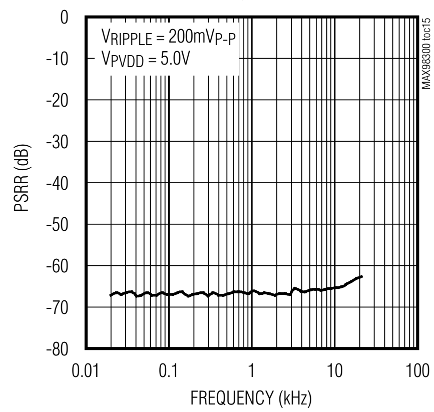
OUTPUT POWER vs. SUPPLY VOLTAGE



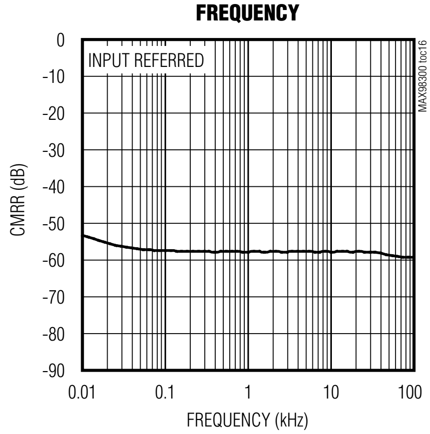
OUTPUT POWER vs. SUPPLY VOLTAGE



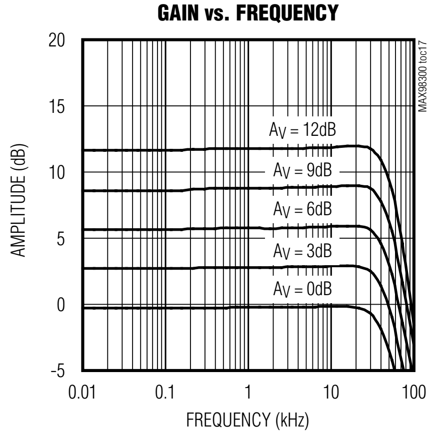
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



COMMON-MODE REJECTION RATION vs. FREQUENCY

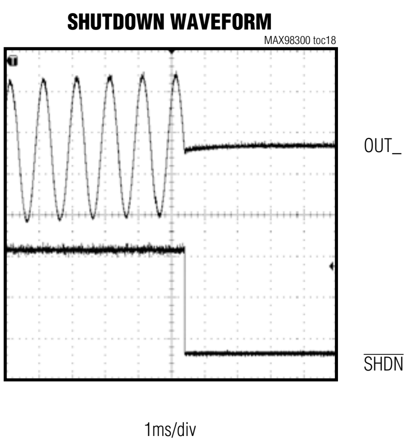


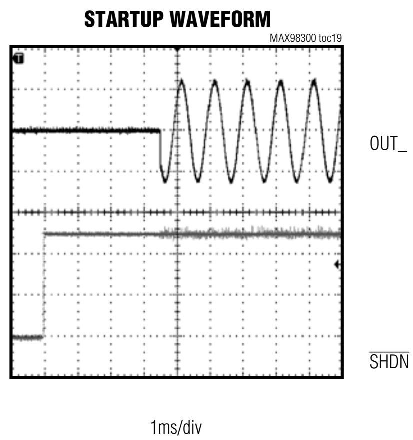
GAIN vs. FREQUENCY

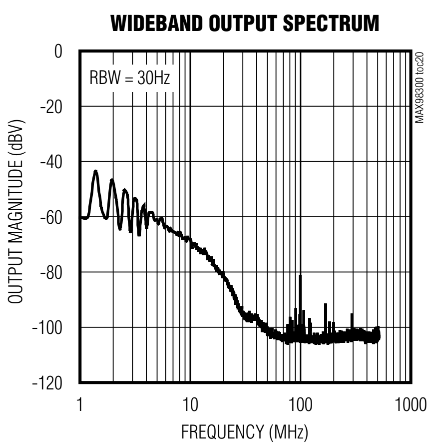


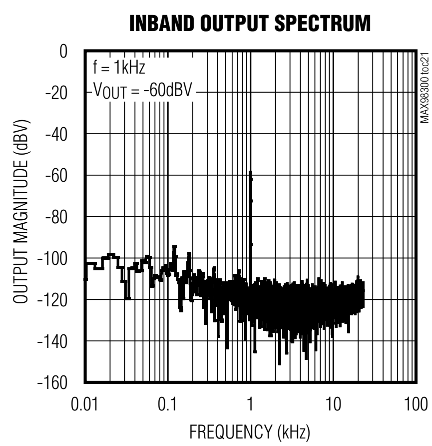
Typical Operating Characteristics (continued)

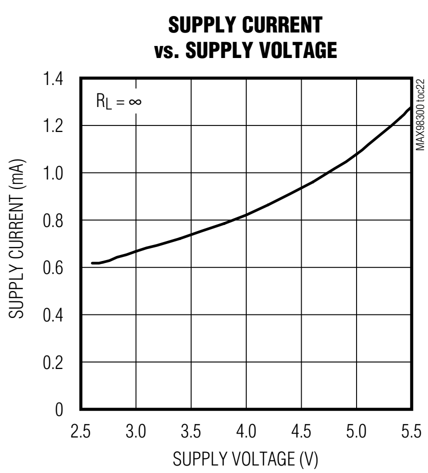
(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB, R_L = ∞, unless otherwise specified, R_L connected between OUT+ to OUT-, AC measurement bandwidth 20Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

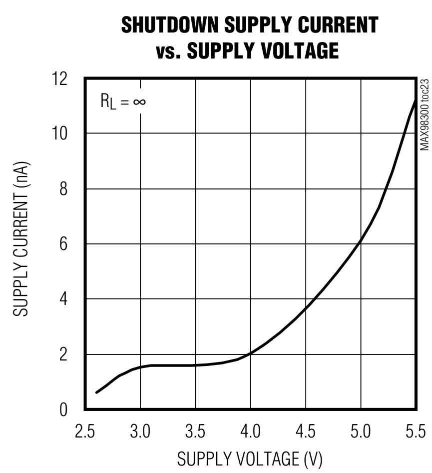




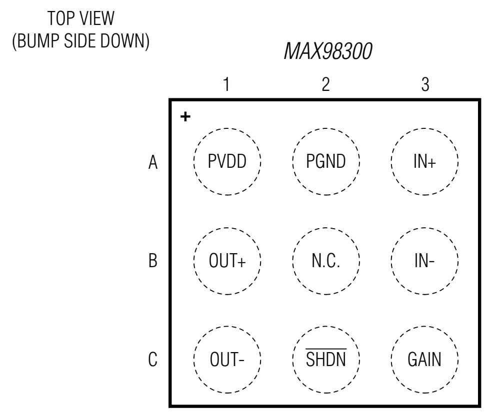




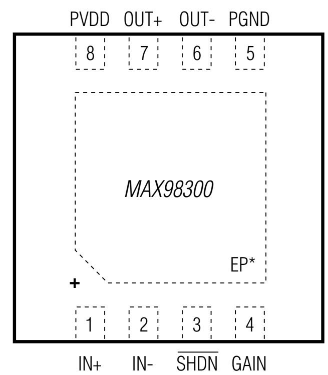




Pin Configurations



WLP
(1.2mm x 1.2mm,
0.4mm pitch)



TDFN
(2mm x 2mm)

*EP = EXPOSED PAD. CONNECT EP TO PGND TO ENHANCE THERMAL DISSIPATION

Pin Description

PIN		NAME	FUNCTION
TDFN-EP	WLP		
1	A3	IN+	Noninverting Audio Input
2	B3	IN-	Inverting Audio Input
3	C2	$\overline{\text{SHDN}}$	Active-Low Shutdown Input. Drive $\overline{\text{SHDN}}$ low to place the device in shutdown mode.
4	C3	GAIN	Gain Selection. See Table 1 for gain settings.
5	A2	PGND	Power Ground
6	C1	OUT-	Negative Speaker Output
7	B1	OUT+	Positive Speaker Output
8	A1	PVDD	Power Supply. Bypass PVDD to PGND with 0.1μF and 10μF capacitors.
—	B2	N.C.	No Connection
—	—	EP	Exposed Pad (TDFN only). Connect exposed pad to a solid ground plane.

MAX98300
Mono 2.6W Class D Amplifier

Detailed Description

The MAX98300 features industry-leading quiescent current, low-power shutdown mode, comprehensive click-and-pop suppression, and excellent RF immunity.

The device offers Class AB audio performance with Class D efficiency in a minimal board-space solution.

The Class D amplifier features spread-spectrum modulation, edge-rate, and overshoot control circuitry that offers significant improvements to switch-mode amplifier radiated emissions.

The MAX98300 amplifier features click-and-pop suppression that reduces audible transients on startup and shutdown. The amplifier includes thermal overload and short-circuit protection.

Class D Speaker Amplifier

The MAX98300 filterless Class D amplifier offers much higher efficiency than Class AB amplifiers. The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead.

Ultra-Low EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. Maxim's patented active emissions-limiting edge-rate control circuitry and spread-spectrum modulation reduces EMI emissions, while maintaining up to 89% efficiency.

Maxim's patented spread-spectrum modulation mode flattens wideband spectral components, while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The MAX98300's spread-spectrum modulator randomly varies the switching frequency by ±10kHz around the center frequency (300kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes (Figure 1).

Speaker Current Limit

If the output current of the speaker amplifier exceeds the current limit (2A typ), the MAX98300 disables the outputs for approximately 130μs. At the end of 130μs, the outputs are re-enabled. If the fault condition still exists, the MAX98300 continues to disable and re-enable the outputs until the fault condition is removed.

Selectable Gain

The MAX98300 offers five programmable gain selections through a single gain input (GAIN).

Table 1. Gain Control Configuration

GAIN PIN	MAXIMUM GAIN (dB)
Connect to PVDD	12
Connect to PVDD through 100kΩ ±5%	9
Not connected	6
Connect to PGND through 100kΩ ±5%	3
Connect to PGND	0

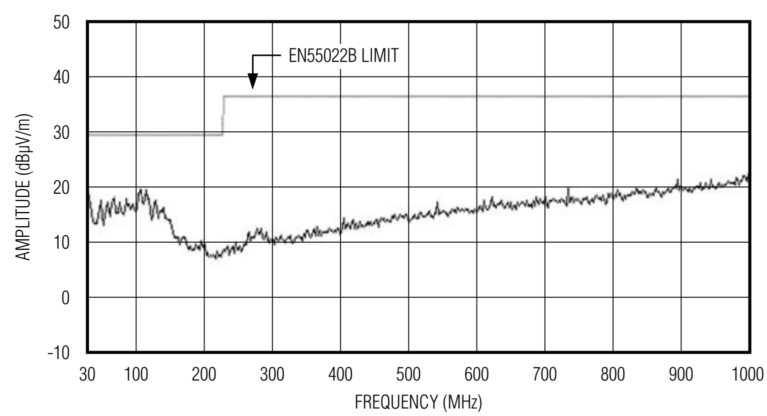


Figure 1. EMI with 60cm of Speaker Cable and No Output Filtering

Shutdown

The MAX98300 features a low-power shutdown mode, drawing less than 0.1µA of supply current. Drive $\overline{SHDN}$ low to put the MAX98300 into shutdown.

Click-and-Pop Suppression

The MAX98300 speaker amplifier features Maxim's comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transient sources internal to the device. When entering shutdown, the differential speaker outputs ramp down to PGND quickly and simultaneously.

Applications Information

Filterless Class D Operation

Traditional Class D amplifiers require an output filter. The filter adds cost, size, and decreases efficiency and THD+N performance. The MAX98300's filterless modulation scheme does not require an output filter (Figure 1).

Because the switching frequency of the MAX98300 is well beyond the bandwidth of most speakers, voice coil movement due to the switching frequency is very small. Use a speaker with a series inductance > 10µH. Typical 8Ω speakers exhibit series inductances in the 20µH to 100µH range.

Component Selection

Speaker Amplifier Power Supply Input (PVDD)

PVDD powers the speaker amplifier. PVDD ranges from 2.6V to 5.5V. Bypass PVDD with a 0.1µF and 10µF capacitor to PGND. Apply additional bulk capacitance at the device if long input traces between PVDD and the power source are used.

Input Filtering

The input-coupling capacitor (C_{IN}), in conjunction with the amplifier's internal input resistance (R_{IN}), forms a highpass filter that removes the DC bias from the incoming signal. These capacitors allow the amplifier to bias the signal to an optimum DC level.

Assuming zero source impedance with a gain setting of A_V = 6dB, 9dB, or 12dB, C_{IN} is:

$$C_{IN} = \frac{8}{f_{-3dB}}[\mu F]$$

with a gain setting of A_V = 3dB, C_{IN} is:

$$C_{IN} = \frac{5.7}{f_{-3dB}}[\mu F]$$

with a gain setting of A_V = 0dB, C_{IN} is:

$$C_{IN} = \frac{4}{f_{-3dB}}[\mu F]$$

where f_{-3dB} is the -3dB corner frequency. Use capacitors with adequately low voltage-coefficient for best low-frequency THD performance.

Layout and Grounding

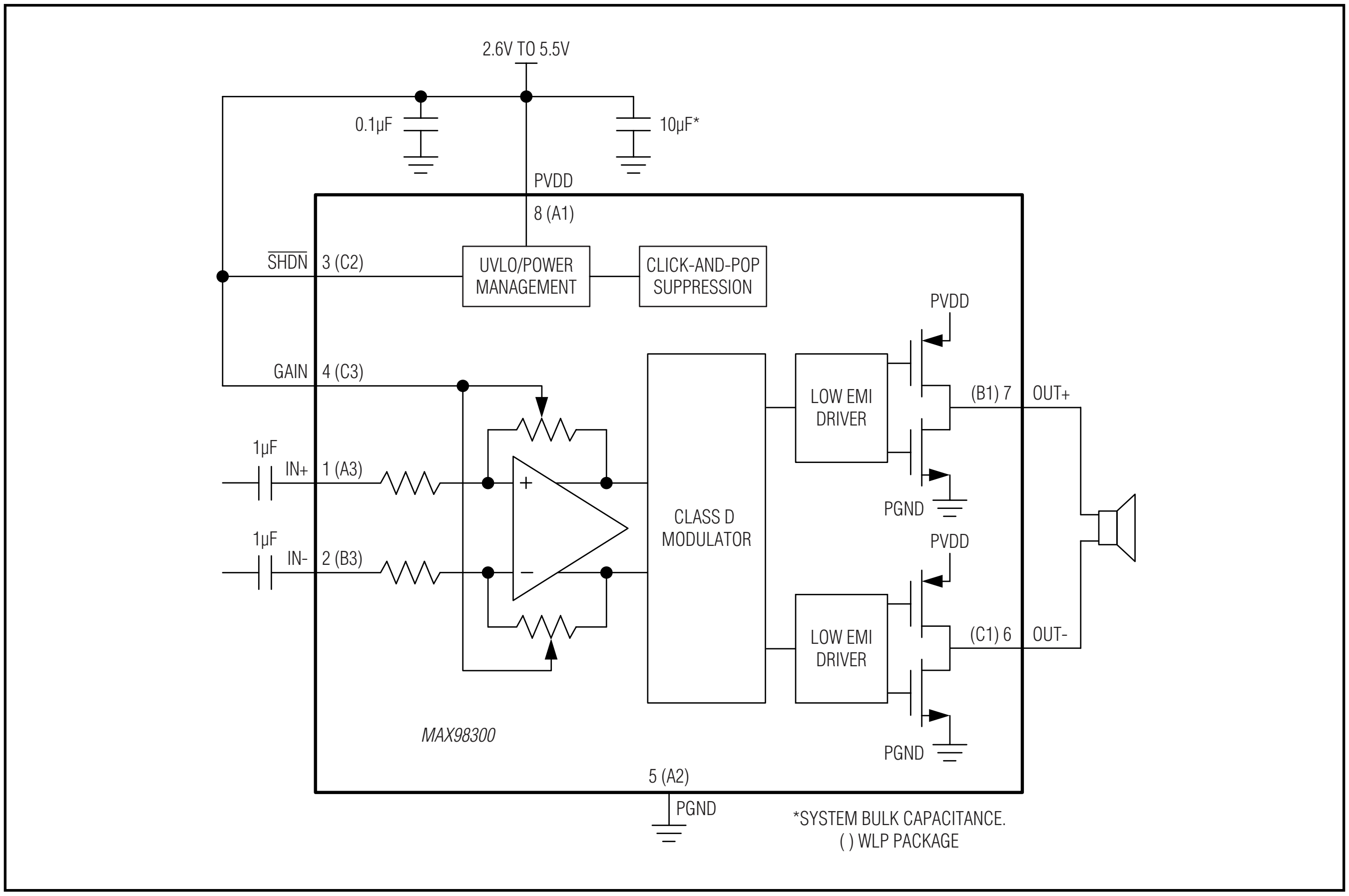
Proper layout and grounding are essential for optimum performance. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal.

Use wide, low-resistance output traces. As load impedance decreases, the current drawn from the device outputs increase. At higher current, the resistance of the output traces decreases the power delivered to the load. For example, if 2W is delivered from the speaker output to a 4Ω load through a 100mΩ trace, 49mW is consumed in the trace. If power is delivered through a 10mΩ trace, only 5mW is consumed in the trace. Wide output, supply, and ground traces also improve the power dissipation of the device.

The MAX98300 is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes.

The MAX98300 TDFN-EP package features an exposed thermal pad on its underside. This pad lowers the package's thermal resistance by providing a heat conduction path from the die to the PCB. Connect the exposed thermal pad to the ground plane by using a large pad and multiple vias.

Functional Diagram



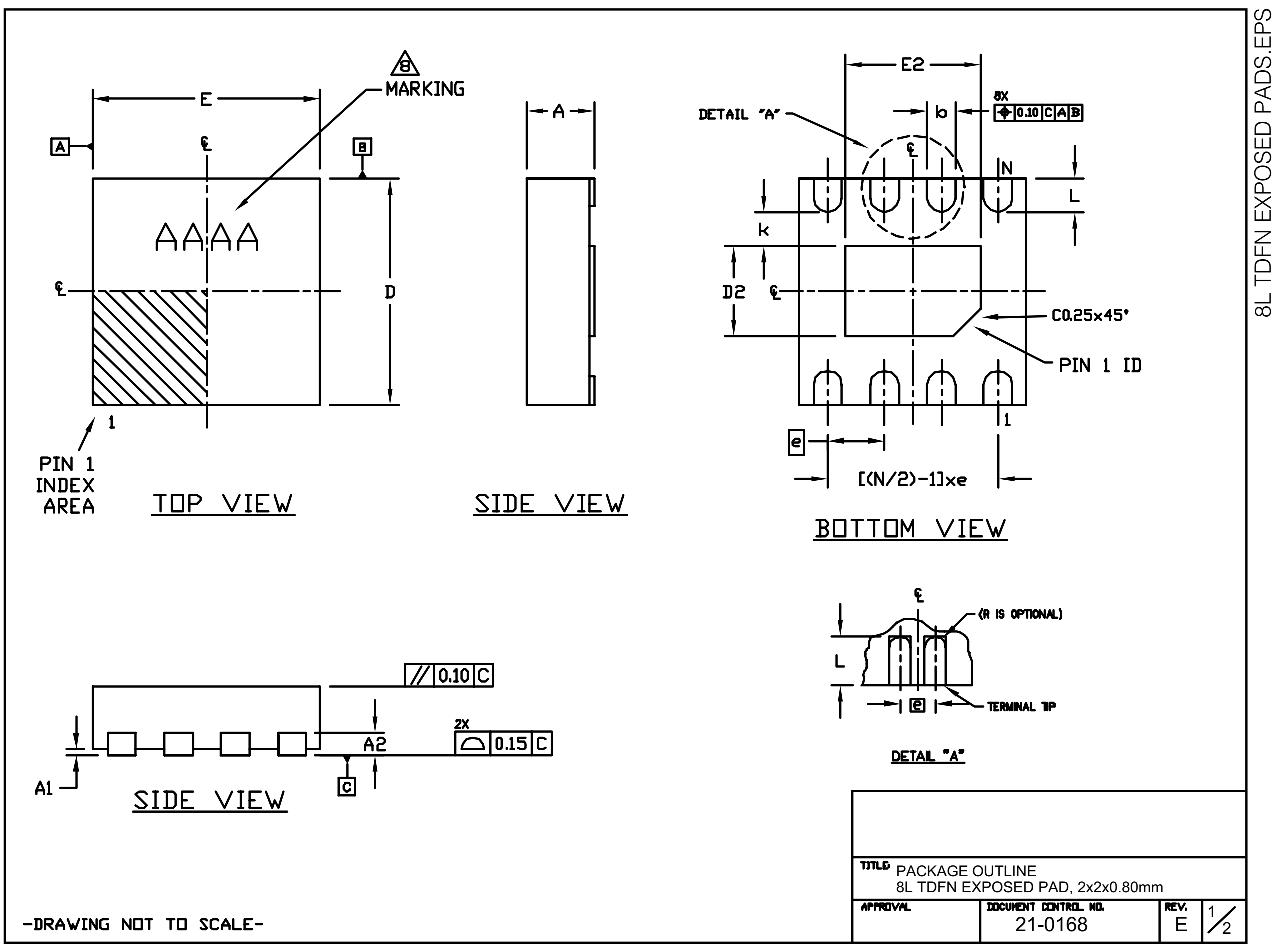
Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN-EP	T822+2	21-0168	90-0065
9 WLP	W91B1+7	21-0459	—



Package Information (continued)

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	1.90	2.10
E	1.90	2.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	b	r	[(N/2)-1] x e
T822-1	8	0.70±0.10	1.30±0.10	0.50 TYP.	0.25±0.05	0.125	1.50 REF
T822-2	8	0.80±0.10	1.20±0.10	0.50 TYP.	0.25±0.05	0.125	1.50 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.08mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. COMPLY TO JEDEC MO229 EXCEPT D2 AND E2 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE
8L TDFN EXPOSED PAD, 2x2x0.80mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0168	E	2/2

Package Information (continued)

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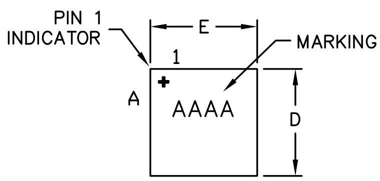
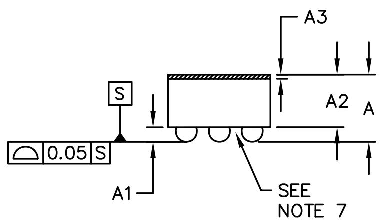


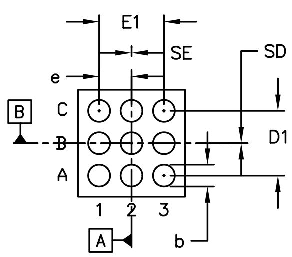
TOP VIEW



SIDE VIEW

COMMON DIMENSIONS	
A	0.64±0.05
A1	0.19±0.03
A2	0.45 REF
A3	0.025 BASIC
b	ø0.27±0.03
D1	0.80 BASIC
E1	0.80 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W91B1+7	1.22	1.30	1.22	1.30	NONE
W91C1+1	1.56	1.63	1.38	1.45	NONE



BOTTOM VIEW

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front-side finish can be either Black or Clear.

TITLE:
PACKAGE OUTLINE
9 BUMPS, WLP PKG. 0.4mm PITCH

APPROVAL | DOCUMENT CONTROL NO. 21-0459 | REV. B | 1/1

-DRAWING NOT TO SCALE-

MAX98300

Mono 2.6W Class D Amplifier

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/10	Initial release	—

Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000