10-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

MAX5741

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ....-0.3V to +6V
OUT_, SCLK, DIN, $\overline{CS}$, REF to GND...............-0.3 to (V_{DD}+0.3V)
Maximum Continuous Current Into Any Pin......................±50mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 6.9 mW/°C above +70°C) 555mW

Operating Temperature Range ....-40°C to +125°C
Junction Temperature.......................................-65°C to +150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, GND = 0, V_{REF} = V_{DD}, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are V_{DD} = +5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY (Note 1)						
Resolution	N		10			Bits
Integral Nonlinearity Error	INL	(Note 2)		±0.5	±4	LSB
Differential Nonlinearity Error	DNL	Guaranteed monotonic (Note 2)			±1	LSB
Zero-Code Error	OE	Code = 000		0.4	1.5	% of FS
Zero-Code Error Tempco				2.3		ppm/°C
Gain Error	GE	Code = 3FF hex			±3	% of FS
Gain-Error Tempco				0.26		ppm/°C
Power-Supply Rejection Ratio	PSRR	Code = 3FF hex, ΔV_{DD} = ±10%		58.8		dB
REFERENCE INPUT						
Reference Input Voltage Range	V_{REF}		0		V_{DD}	V
Reference Input Impedance	R_{REF}	In operation	32	45	63	kΩ
		In power-down mode		2		MΩ
Power-Down Reference Current		In power-down mode (Note 3)		1	10	µA
DAC OUTPUT						
Output Voltage Range		No load (Note 4)	0		V_{DD}	V
DC Output Impedance		Code = 200 hex		0.8		Ω
Short-Circuit Current		V_{DD} = +3V		15		mA
		V_{DD} = +5V		48		
Wake-Up Time		V_{DD} = +3V		8		µs
		V_{DD} = +5V		8		
Output Leakage Current		Power-down mode = output high impedance		±18		nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, GND = 0, V_{REF} = V_{DD}, R_L = 5kΩ, C_L = 200pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are V_{DD} = +5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$)						
Input High Voltage	V_{IH}	V_{DD} = +3V, +5V	0.7 × V_{DD}			V
Input Low Voltage	V_{IL}	V_{DD} = +3V, +5V			0.3 × V_{DD}	V
Input Leakage Current	I_{IN}	Digital inputs = 0 or V_{DD}		±0.1	±1	µA
Input Capacitance	C_{IN}			5		pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.5		V/µs
Voltage Output Settling Time		100 hex to 300 hex (Note 3)		4	10	µs
Digital Feedthrough		Any digital inputs from 0 to V_{DD}		0.15		nV-s
Digital-Analog Glitch Impulse		Major carry transition (Code 1FF hex to Code 200 hex)		12		nV-s
DAC-to-DAC Crosstalk				2.4		nV-s
POWER REQUIREMENTS						
Supply Voltage Range	V_{DD}		2.7		5.5	V
Supply Current with No Load	I_{DD}	All digital inputs at 0 or V_{DD} = 3.6V		230	395	µA
		All digital inputs at 0 or V_{DD} = 5.5V		270	420	
Power-Down Supply Current	I_{DDPD}	All digital inputs at 0 or V_{DD} = 5.5V		0.29	1	µA

TIMING CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Frequency	f_{SCLK}		0		20	MHz
SCLK Pulse Width High	t_{CH}		25			ns
SCLK Pulse Width Low	t_{CL}		25			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		10			ns
SCLK Fall to $\overline{CS}$ Rise Setup Time	t_{CSH}		10			ns
DIN to SCLK Fall Setup Time	t_{DS}		15			ns
DIN to SCLK Fall Hold Time	t_{DH}		0			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		80			ns

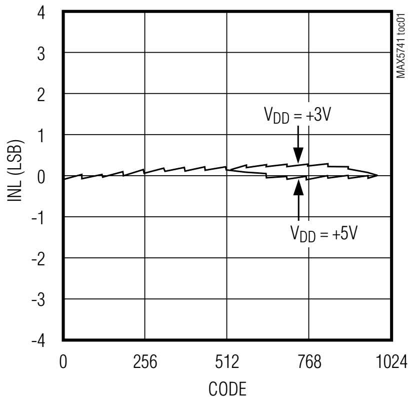
Note 1: DC specifications are tested without output loads.
Note 2: Linearity guaranteed from code 29 to code 995.
Note 3: Limited with test conditions.
Note 4: Offset and gain error limit the FSR.
Note 5: Guaranteed by design.

10-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

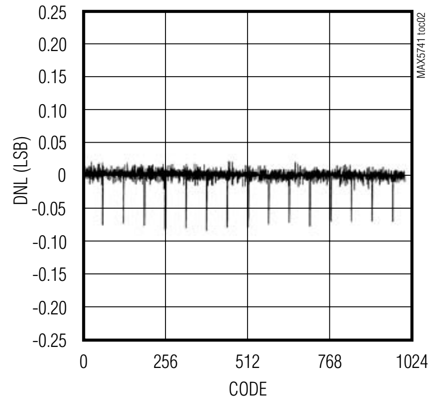
Typical Operating Characteristics

(V_{REF} = V_{DD}, T_A = +25°C, unless otherwise noted.)

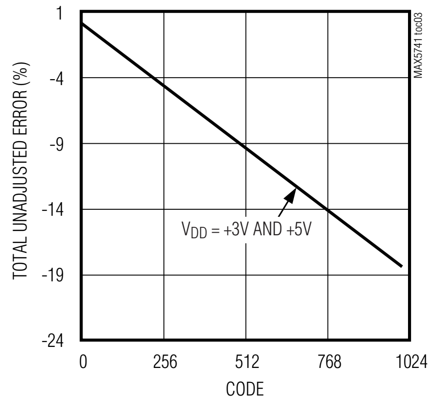
INTEGRAL NONLINEARITY vs. CODE, T_A = +25°C



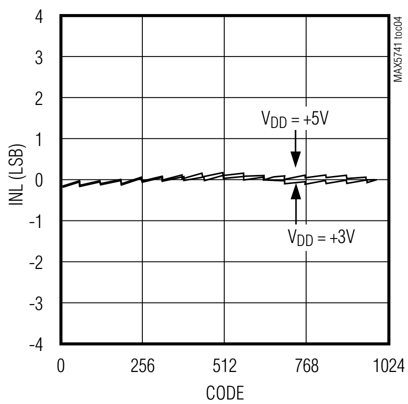
DIFFERENTIAL NONLINEARITY vs. CODE, T_A = +25°C



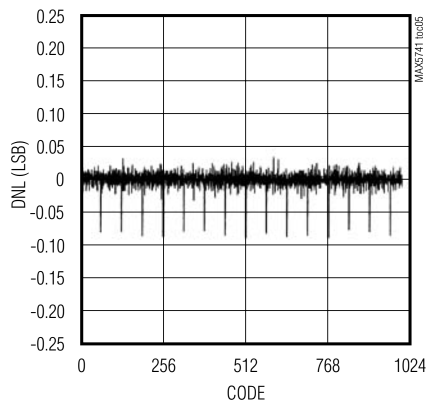
TOTAL UNADJUSTED ERROR vs. CODE, T_A = +25°C



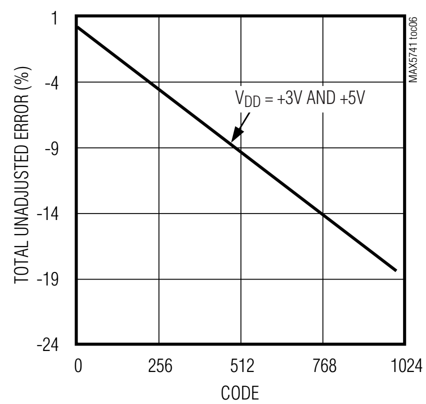
INTEGRAL NONLINEARITY vs. CODE, T_A = +40°C



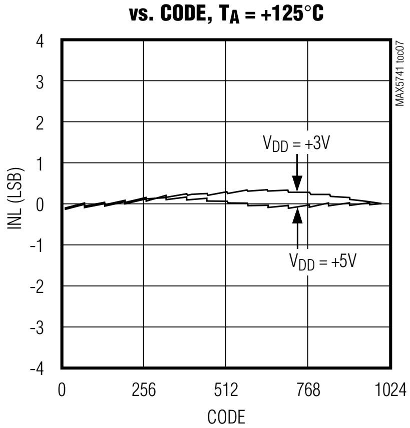
DIFFERENTIAL NONLINEARITY vs. CODE, T_A = -40°C



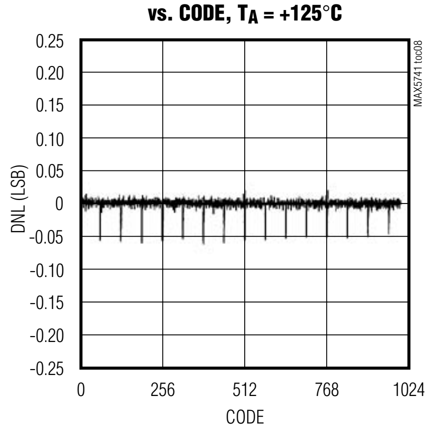
TOTAL UNADJUSTED ERROR vs. CODE, T_A = -40°C



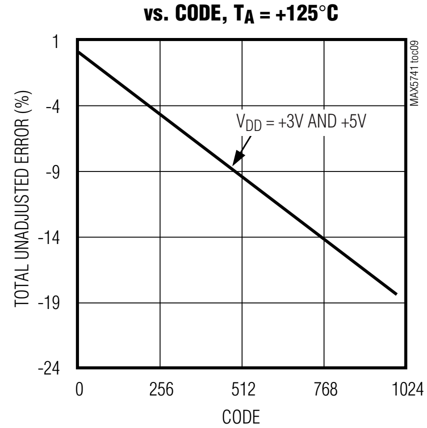
INTEGRAL NONLINEARITY vs. CODE, T_A = +125°C



DIFFERENTIAL NONLINEARITY vs. CODE, T_A = +125°C



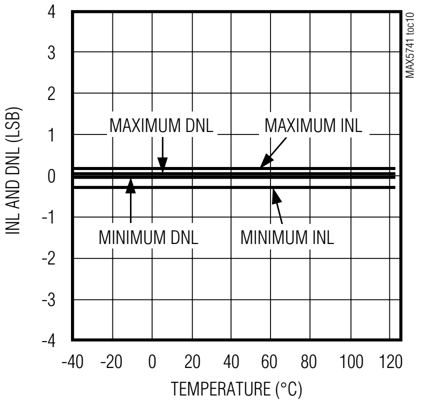
TOTAL UNADJUSTED ERROR vs. CODE, T_A = +125°C



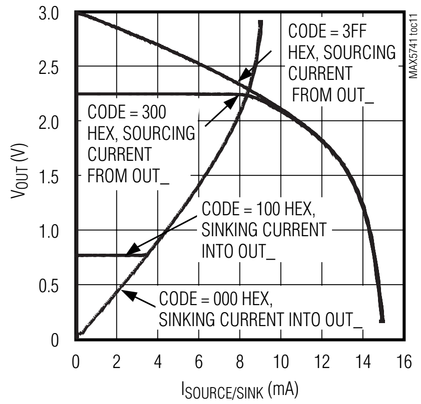
Typical Operating Characteristics (continued)

(V_{REF} = V_{DD}, T_A = +25°C, unless otherwise noted.)

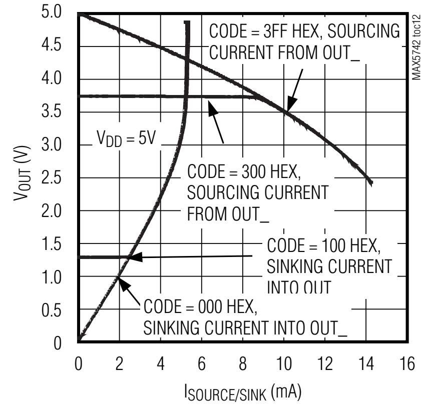
WORST-CASE INL AND DNL vs. TEMPERATURE



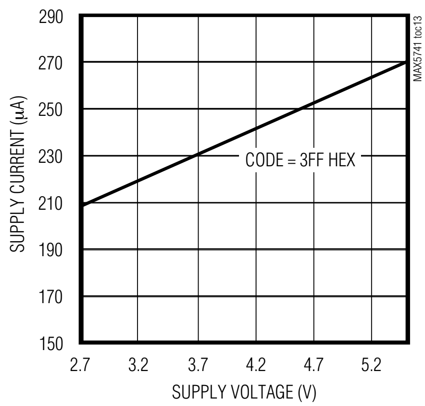
SOURCE-AND-SINK CURRENT CAPABILITY (V_{DD} = +3V)



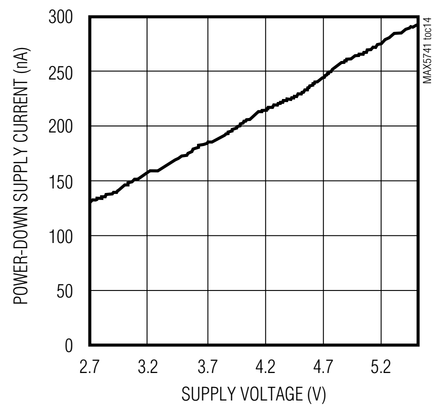
SOURCE-AND-SINK CURRENT CAPABILITY (V_{DD} = +5V)



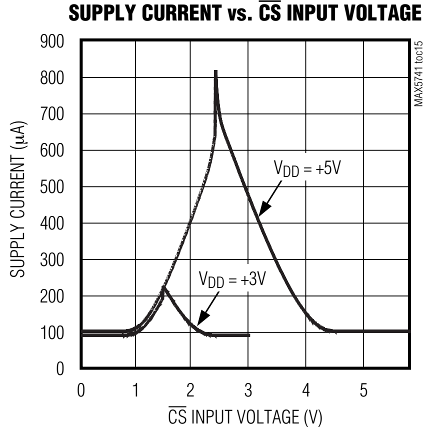
SUPPLY CURRENT vs. SUPPLY VOLTAGE



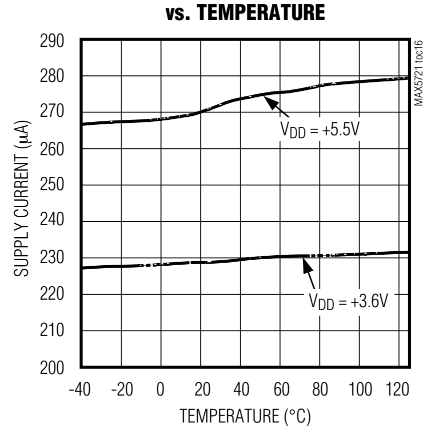
POWER-DOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. $\overline{CS}$ INPUT VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE

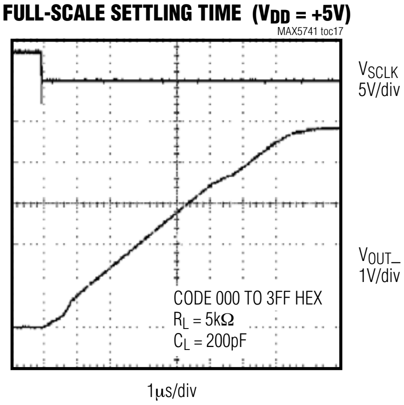


10-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

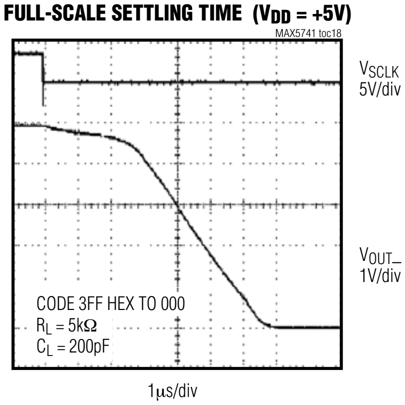
Typical Operating Characteristics (continued)

($V_{REF} = V_{DD}$, T_A = +25°C, unless otherwise noted.)

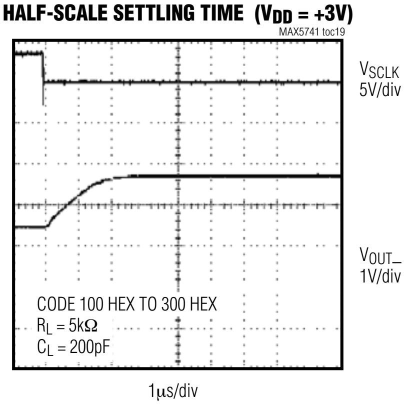
FULL-SCALE SETTLING TIME (V_{DD} = +5V)



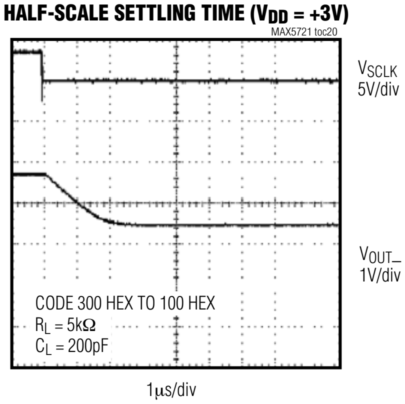
FULL-SCALE SETTLING TIME (V_{DD} = +5V)



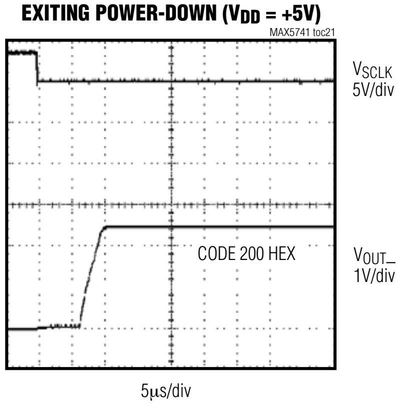
HALF-SCALE SETTLING TIME (V_{DD} = +3V)



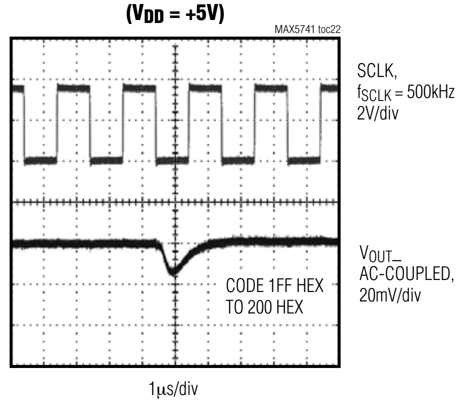
HALF-SCALE SETTLING TIME (V_{DD} = +3V)



EXITING POWER-DOWN (V_{DD} = +5V)



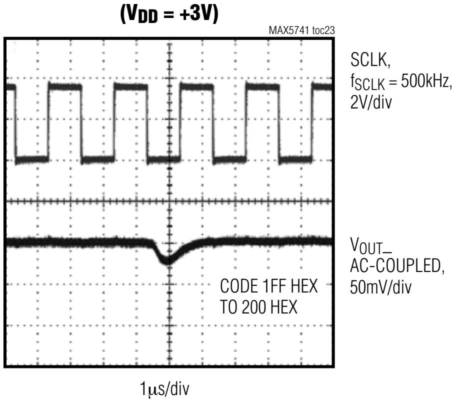
DIGITAL-TO-ANALOG GLITCH IMPULSE (V_{DD} = +5V)



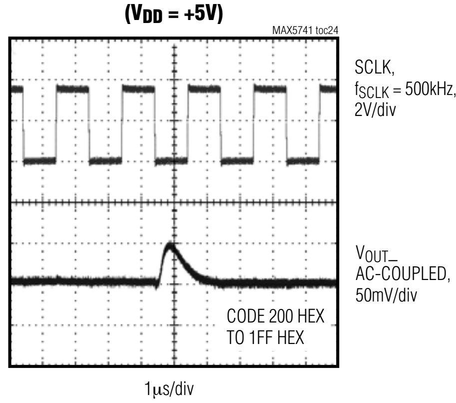
Typical Operating Characteristics (continued)

($V_{REF} = V_{DD}$, T_A = +25°C, unless otherwise noted.)

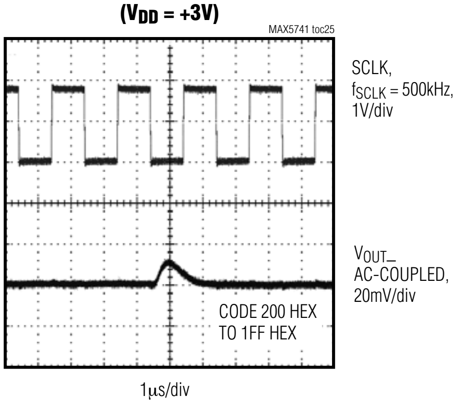
DIGITAL-TO-ANALOG GLITCH IMPULSE (V_{DD} = +3V)



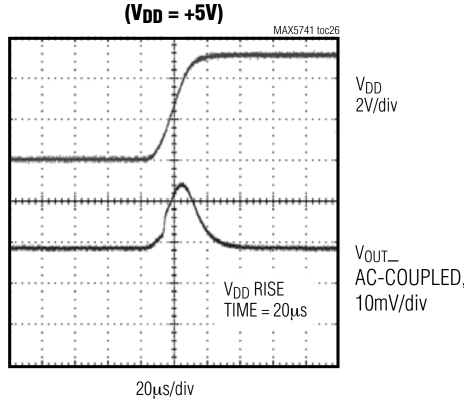
DIGITAL-TO-ANALOG GLITCH IMPULSE (V_{DD} = +5V)



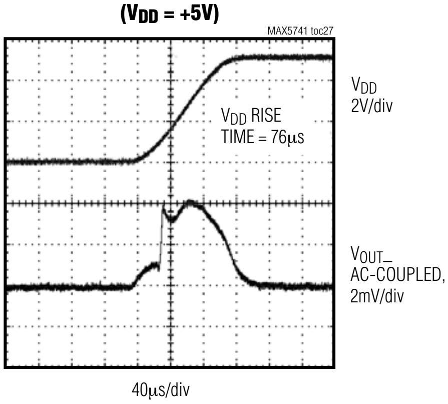
DIGITAL-TO-ANALOG GLITCH IMPULSE (V_{DD} = +3V)



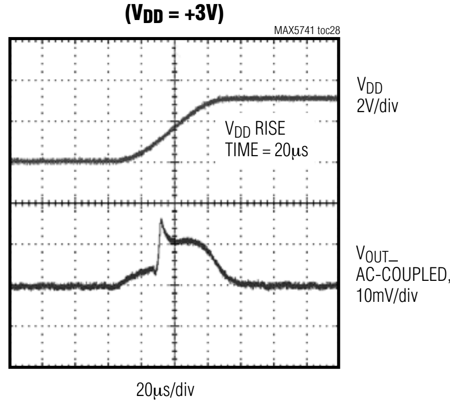
POWER-ON RESET, FAST RISE TIME (V_{DD} = +5V)



POWER-ON RESET, SLOW RISE TIME (V_{DD} = +5V)



POWER-ON RESET, FAST RISE TIME (V_{DD} = +3V)

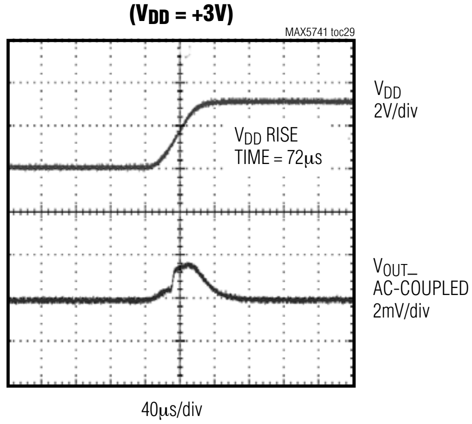


10-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

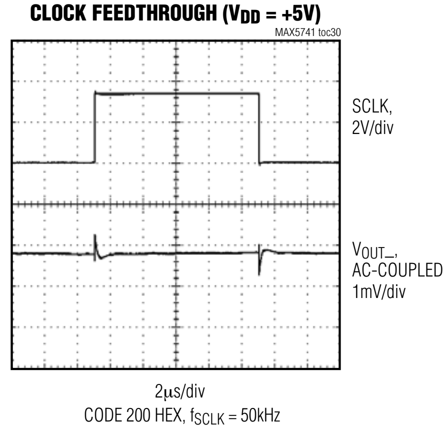
Typical Operating Characteristics (continued)

(V_{DD} = +3V, V_{REF} = V_{DD}, T_A = +25°C, unless otherwise noted.)

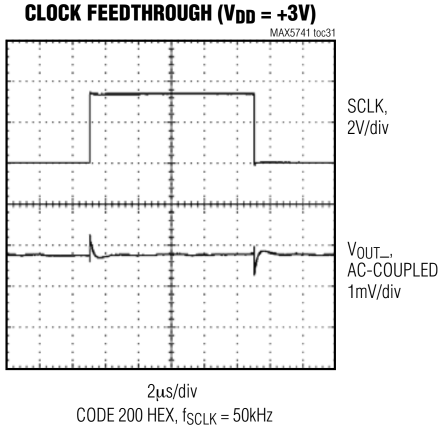
POWER-ON RESET, SLOW RISE-TIME (V_{DD} = +3V)



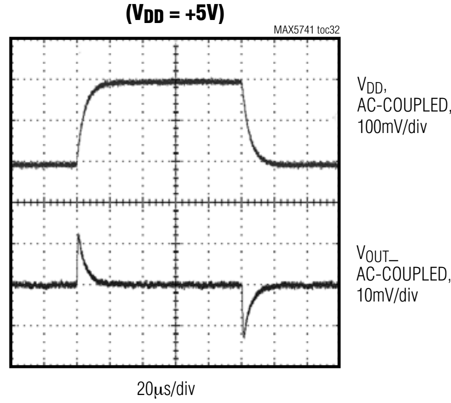
CLOCK FEEDTHROUGH (V_{DD} = +5V)



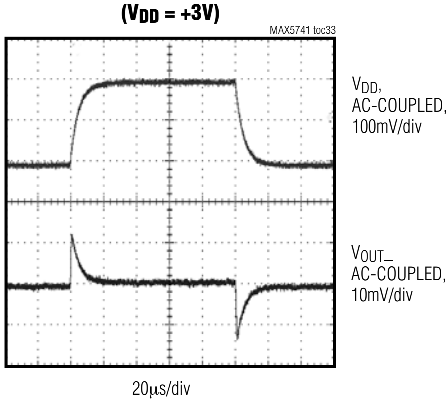
CLOCK FEEDTHROUGH (V_{DD} = +3V)



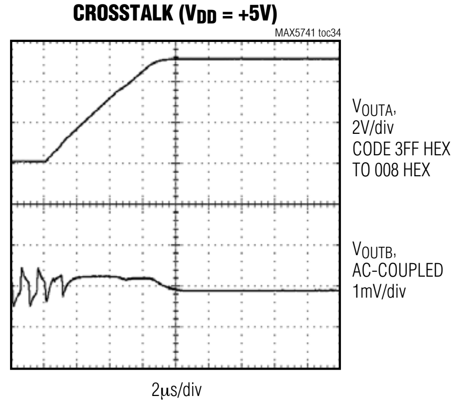
LINE TRANSIENT RESPONSE (V_{DD} = +5V)



LINE TRANSIENT RESPONSE (V_{DD} = +3V)



CROSSTALK (V_{DD} = +5V)



Pin Description

PIN	NAME	FUNCTION
1	$\overline{CS}$	Chip-Select Input
2	SCLK	Serial Clock Input
3	V_{DD}	Power-Supply Input
4	GND	Ground
5	DIN	Serial Data Input
6	REF	External Reference Voltage Input
7, 8, 9, 10	OUTA–OUTD	DAC Voltage Outputs. Power-on reset sets DAC registers to zero, and internally connects OUT to GND with 100kΩ resistor.

Detailed Description

The MAX5741 contains four 10-bit, voltage-output, low-power digital-to-analog converters (DACs). Each DAC employs a resistor word string architecture that converts a 10-bit digital input word to an equivalent analog output voltage proportional to the applied reference voltage. The MAX5741 shares one reference input (REF) between all four DACs. The MAX5741 includes rail-to-rail output buffer amplifiers for each DAC, and input logic for simple microprocessor (µP), and CMOS interfaces. The power-supply range is from +2.7V to +5.5V (*Functional Diagram*). The MAX5741's reference input accepts a voltage range from 0 to V_{DD}. In power-down mode the reference input is high impedance. The MAX5741 is compatible with the 3-wire SPI, QSPI, MICROWIRE, and DSP serial interface with Schmitt-triggered logic inputs.

Reference Input and DAC Output Range

The reference input accepts positive DC and AC signals. The voltage at REF sets the full-scale output voltage of the four DACs. The reference input voltage range is 0 to V_{DD}. The impedance at REF is 45kΩ. The voltage at REF can vary from GND to V_{DD}. The output voltages ($V_{OUT\_}$) are represented by a digitally programmable voltage source as:

$$V_{OUT\_} = (V_{REF} \times D) / 2^{10}$$

where D is the decimal equivalent of binary DAC input code ranging from 0 to 1023. V_{REF} is the voltage at REF.

Output Buffer Amplifiers

All DACs are internally buffered at the output. The buffer amplifiers have both rail-to-rail common mode and (GND to V_{REF}) output voltage range. The buffers are unity-gain stable with C_L = 200pF and R_L = 5kΩ. Buffer amplifiers are disabled during power-up and individual DAC outputs are shorted to GND through a 100kΩ resistor. Buffer amplifiers can individually or altogether be powered-down by programming the input register control bits. During power down, contents of the input and DAC registers remain the same. On wake-up all DAC outputs are restored to their pre-power down voltage values.

Power-Down Mode

In power-down mode, the DAC outputs are programmed to one of three output states, 1kΩ, 100kΩ, or floating (Table 1). The REF input is high impedance (2MΩ typ) to conserve current drain from the system reference; therefore, the system reference does not have to be powered-down. The DAC outputs return to the values contained in the registers when brought out of power-down. The recovery time, from total power-down to power-up, is 8µs. This extra time is needed to allow the internal bias to wake-up. Power-down mode reduces current consumption to 0.3µA.

3-Wire Serial Interface

The MAX5741 digital interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE/DSP interfaces. The chip-select input ($\overline{CS}$) frames the serial data loading at DIN. Immediately following $\overline{CS}$ high-to-low transition, the data is shifted synchronously and latched into the input register on the falling edge of the serial clock input (SCLK). After 16 bits have been loaded into the serial input register, it transfers its con-

Table 1. Power-Down Mode Control

EXTENDED CONTROL				DATA BITS						DESCRIPTION	FUNCTION
C3	C2	C1	C0	D9–D3	D2	D1	D0	S1	S0		
1	1	1	1	X	0	0	0	0	0	DAC A	DAC O/P, wake-up
1	1	1	1	X	0	0	0	0	1	DAC A	Floating output
1	1	1	1	X	0	0	0	1	0	DAC A	Output is terminated with 1kΩ
1	1	1	1	X	0	0	0	1	1	DAC A	Output is terminated with 100kΩ
1	1	1	1	X	0	0	1	0	0	DAC B	DAC O/P, wake-up
1	1	1	1	X	0	0	1	0	1	DAC B	Floating output
1	1	1	1	X	0	0	1	1	0	DAC B	Output is terminated with 1kΩ
1	1	1	1	X	0	0	1	1	1	DAC B	Output is terminated with 100kΩ
1	1	1	1	X	0	1	0	0	0	DAC C	DAC O/P, wake-up
1	1	1	1	X	0	1	0	0	1	DAC C	Floating output
1	1	1	1	X	0	1	0	1	0	DAC C	Output is terminated with 1kΩ
1	1	1	1	X	0	1	0	1	1	DAC C	Output is terminated with 100kΩ
1	1	1	1	X	0	1	1	0	0	DAC D	DAC O/P, wake-up
1	1	1	1	X	0	1	1	0	1	DAC D	Floating output
1	1	1	1	X	0	1	1	1	0	DAC D	Output is terminated with 1kΩ
1	1	1	1	X	0	1	1	1	1	DAC D	Output is terminated with 100kΩ
1	1	1	1	X	1	0	0	0	0	DAC A-D	DAC O/P, wake-up
1	1	1	1	X	1	0	0	0	1	DAC A-D	Floating output
1	1	1	1	X	1	0	0	1	0	DAC A-D	Output is terminated with 1kΩ
1	1	1	1	X	1	0	0	1	1	DAC A-D	Output is terminated with 100kΩ

X = Don't Care

tents to the DAC latch. $\overline{CS}$ may then either be held low or brought high. $\overline{CS}$ must be brought high for a minimum of 80ns before the next write sequence, since a write sequence is initiated on a falling edge of $\overline{CS}$. Not keeping $\overline{CS}$ low during the first 15 SCLK cycles discards input data. The serial clock (SCLK) can idle either high or low between transitions.

The MAX5741 has two internal registers per DAC, the input register and the DAC register. The input register holds the data that is waiting to be shifted to the DAC register. All four input registers can be loaded without updating the output. This function is useful when all outputs need to be updated at the same time. The input register can be made transparent. When the input register is transparent, the data written into DIN loads directly to the DAC register and the output is updated.

The DAC output is not updated until data is written to the DAC register. See Table 2 for a list of serial-interface programming commands.

Power-On Reset (POR)

The MAX5741 has an internal POR circuit. At power-up all DACs are powered-down and OUT_ is terminated to GND through 100kΩ resistors. Contents of input and DAC registers are cleared to all zero. 8µs recovery time after issuing a wake-up command is needed before writing to the DAC registers. Power-down mode control commands can be applied immediately with no recovery time.

C3–C0 are control bits. The data bits D9 to D0 are in straight binary format. Set bits S1 and S0 to zero. All zeros correspond to zero scale and all ones correspond to full scale.

CONTENTS OF INPUT SHIFT															
				D9 (MSB)									D0 (LSB)		
C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S1	S0

Figure 1. 16-Bit Input Word

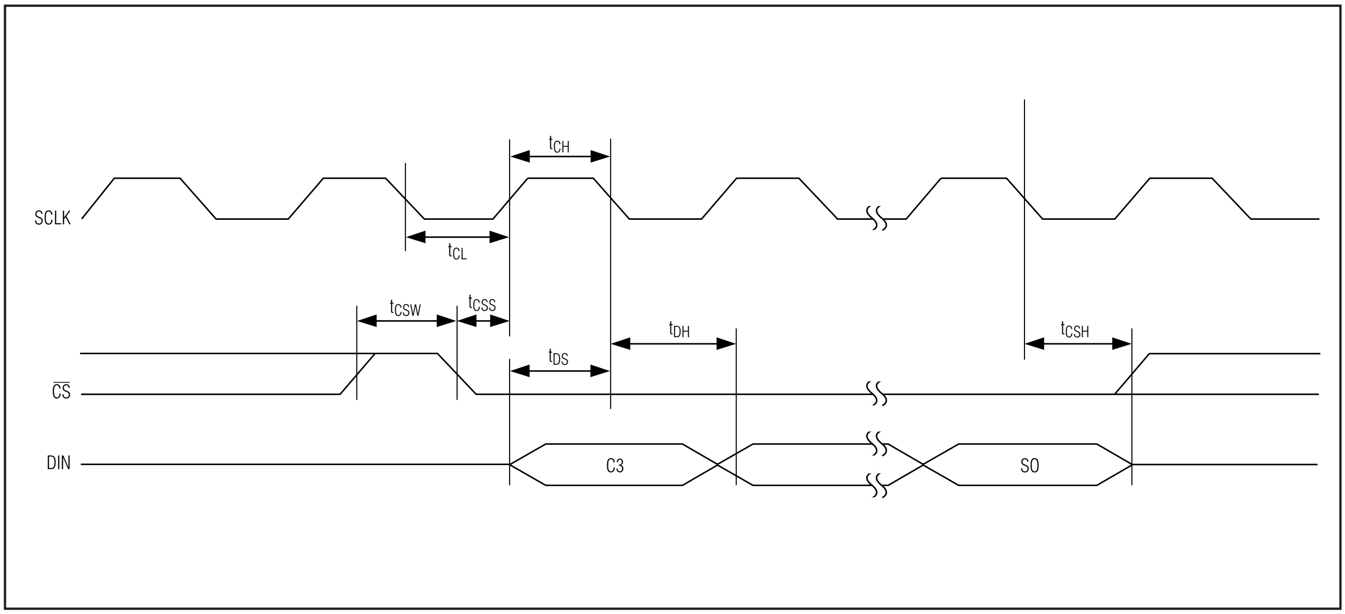


Figure 2. Timing Diagram

Digital Inputs

The digital inputs are compatible with CMOS logic. In order to save power and reduce input to output coupling, SCLK and DIN input buffers are powered down immediately after completion of shifting 16 bits into the input shift register. A high to low transition at $\overline{CS}$ powers up SCLK and DIN input buffers.

Applications Information

Unipolar Output

The typical application circuit (Figure 3) shows the MAX5741 configured for a unipolar output, where the output voltages and the reference inputs have the same polarity. Table 3 lists the unipolar output codes.

Bipolar Output

The MAX5741 can be configured for bipolar operation using a dual supply op amp (Figure 4). The transfer function for bipolar operation is:

$$V_{OUT} = V_{REF}\left[\left(\frac{2D}{1024}\right) - 1\right]$$

10-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

Table 2. Serial-Interface Programming Commands

CONTROL				DATA BITS		DAC	FUNCTION
C3	C2	C1	C0	D9–D0	S1–S0		
0	0	0	0	X	X	A	Input register transparent, data shifted directly to DAC register, OUTA updated
0	0	0	1	X	X	B	Input register transparent, data shifted directly to DAC register, OUTB updated
0	0	1	0	X	X	C	Input register transparent, data shifted directly to DAC register, OUTC updated
0	0	1	1	X	X	D	Input register transparent, data shifted directly to DAC register, OUTD updated
0	1	0	0	X	X	A	Data shifted to input register, OUTA unchanged
0	1	0	1	X	X	B	Data shifted to input register, OUTB unchanged
0	1	1	0	X	X	C	Data shifted to input register, OUTC unchanged
0	1	1	1	X	X	D	Data shifted to input register, OUTD unchanged
1	0	0	0	X	X	A	Shift data from input register to DAC register, OUTA updated
1	0	0	1	X	X	B	Shift data from input register to DAC register, OUTB updated
1	0	1	0	X	X	C	Shift data from input register to DAC register, OUTC updated
1	0	1	1	X	X	D	Shift data from input register to DAC register, OUTD updated
1	1	0	0	X	X	A–D	Input registers transparent, data shifted directly to DAC registers, OUTA–OUTD updated
1	1	0	1	X	X	A–D	Data shifted to input registers, OUTA–OUTD unchanged
1	1	1	0	X	X	A–D	Shift data from input registers to DAC registers, OUTA–OUTD updated

X = Don't Care

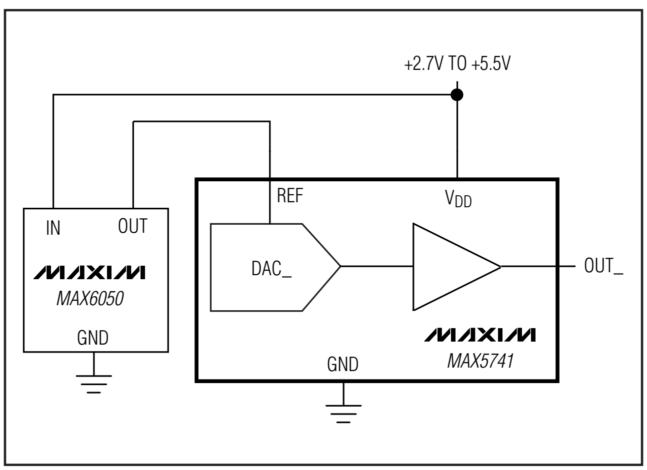


Figure 3. Typical Operating Circuit, Unipolar Output

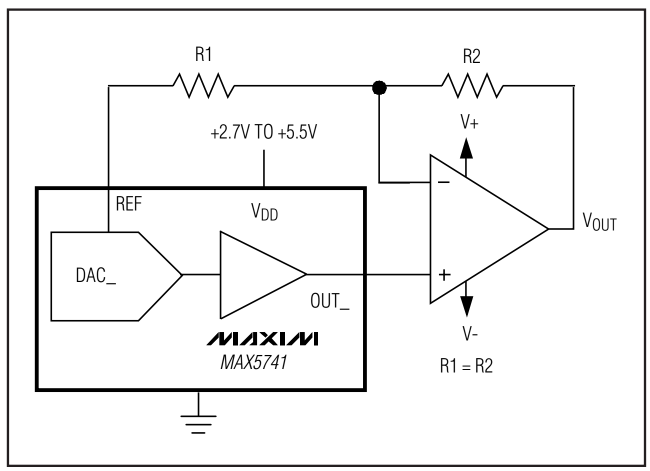


Figure 4. Bipolar Output Circuit

Table 3. Unipolar Code Table

DAC CONTENTS	ANALOG OUTPUT
1111 1111 1100	$V_{REF}\left(\frac{1023}{1024}\right)$
1000 0000 0100	$V_{REF}\left(\frac{513}{1024}\right)$
1000 0000 0000	$\frac{V_{REF}}{2}$
0111 1111 1100	$V_{REF}\left(\frac{511}{1024}\right)$
0000 0000 0100	$V_{REF}\left(\frac{1}{1024}\right)$
0000 0000 0000	0

Table 4. Bipolar Code Table

DAC CONTENTS	ANALOG OUTPUT
1111 1111 1100	$+V_{REF}\left(\frac{511}{512}\right)$
1000 0000 0100	$+V_{REF}\left(\frac{1}{512}\right)$
1000 0000 0000	0
0111 1111 1100	$-V_{REF}\left(\frac{1}{512}\right)$
0000 0000 0100	$-V_{REF}\left(\frac{511}{512}\right)$
0000 0000 0000	$-V_{REF}$

Chip Information

TRANSISTOR COUNT: 14458

PROCESS: BiCMOS

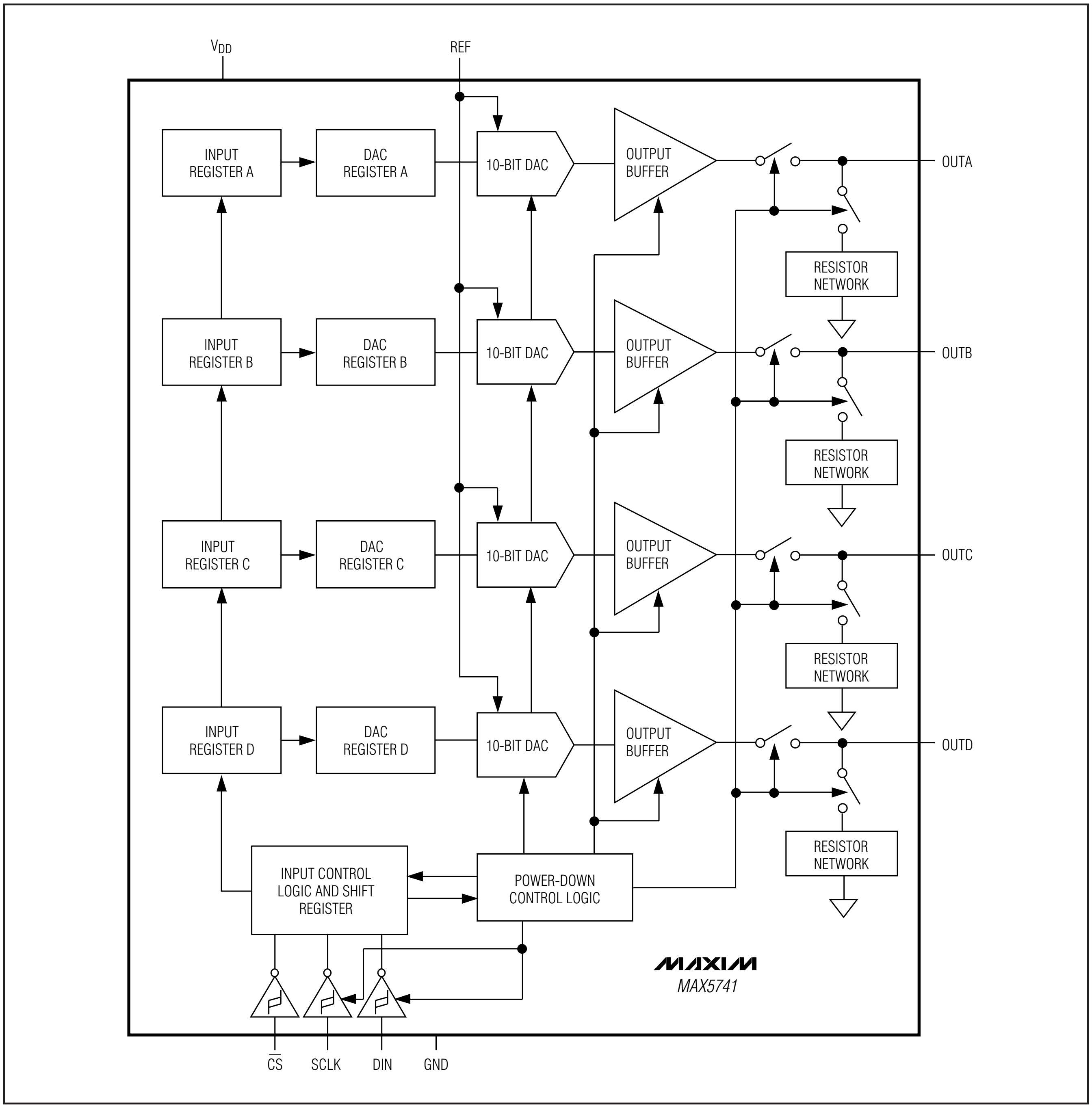
Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 µMAX	U10CN-1	**21-0061**

10-Bit, Low-Power, Quad, Voltage-Output DAC with Serial Interface

Functional Diagram



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	5/08	Corrected labeling in two TOCs	5