Absolute Maximum Ratings

Power-Supply Voltage (V_{DD} to V_{SS}).....-0.3V to +6V
All Other Pins .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Output Short-Circuit Duration
OUT Shorted to V_{SS} or V_{DD} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
5-Pin SC70 (derate 3.10mW/°C above +70°C)..... 246.90mW
5-Pin SOT23 (derate 3.90mW/°C above +70°C) ...312.60mW
6-Pin SC70 (derate 3.10mW/°C above +70°C).....245mW
8-Pin SOT23 (derate 5.10mW/°C above +70°C) 408.2mW
8-Pin µMAX (derate 4.5mW/°C above +70°C)..... 362mW
8-Pin SO (derate 5.88mW/°C above +70°C)..... 471mW
14-Pin TSSOP (derate 8.33mW/°C above +70°C) 727.30mW
14-Pin SO (derate 9.10mW/°C above +70°C)..... 667mW
Operating Temperature Range..... -40°C to +125°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

5 SC70

PACKAGE CODE	X5+1
Outline Number	21-0076
Land Pattern Number	90-0188
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	324°C/W
Junction to Case (θ_{JC})	115°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	324°C/W
Junction to Case (θ_{JC})	115°C/W

5 SOT23

PACKAGE CODE	U5+1
Outline Number	21-0057
Land Pattern Number	90-0174
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	324.30°C/W
Junction to Case (θ_{JC})	82°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	255.90°C/W
Junction to Case (θ_{JC})	81°C/W

6 SC70

PACKAGE CODE	X6SN+1
Outline Number	21-0077
Land Pattern Number	90-0189
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	326°C/W
Junction to Case (θ_{JC})	115°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	326.50°C/W
Junction to Case (θ_{JC})	115°C/W

Package Information (continued)

8 SOT23

PACKAGE CODE	K8+5, K8+5A
Outline Number	21-0078
Land Pattern Number	90-0176
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	N/A
Junction to Case (θ_{JC})	800°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	196°C/W
Junction to Case (θ_{JC})	70°C/W

8 µMAX

PACKAGE CODE	U8+1
Outline Number	21-0036
Land Pattern Number	90-0092
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	221°C/W
Junction to Case (θ_{JC})	42°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	206.30°C/W
Junction to Case (θ_{JC})	42°C/W

8 SO

PACKAGE CODE	S8+2
Outline Number	21-0041
Land Pattern Number	90-0096
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	170°C/W
Junction to Case (θ_{JC})	40°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	136°C/W
Junction to Case (θ_{JC})	38°C/W

14 TSSOP

PACKAGE CODE	U14+1
Outline Number	21-0066
Land Pattern Number	90-0113
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	110°C/W
Junction to Case (θ_{JC})	30°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	100.40°C/W
Junction to Case (θ_{JC})	30°C/W

Package Information (continued)

14 SO

PACKAGE CODE	S14+1
Outline Number	21-0041
Land Pattern Number	90-0112
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	120°C/W
Junction to Case (θ_{JC})	37°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	84°C/W
Junction to Case (θ_{JC})	34°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L = ∞ connected to V_{DD}/2, $\overline{SHDN}$ = V_{DD} (MAX4401 only), **T_A = +25°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Inferred from PSRR test		2.5		55	V
Supply Current per Amplifier	I_{DD}	V_{DD} = 2.5V			320		µA
		V_{DD} = 5.0V			410	700	
Supply Current in Shutdown	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = V_{SS} (Note 1)			0.00002	1	µA
Input Offset Voltage	V_{OS}	MAX4400/MAX4401			±0.8	±4.5	mV
		MAX4402/MAX4403			±1.0	±5.5	
Input Bias Current	I_B	(Note 2)			±0.1	±100	pA
Input Offset Current	I_{OS}	(Note 2)			±0.1	±100	pA
Input Resistance	R_{IN}	Differential or common mode			1000		GΩ
Input Common-Mode Voltage Range	V_{CM}	Inferred from CMRR test		V_{SS}		V_{DD} - 1.4	V
Common-Mode Rejection Ratio	CMRR	V_{SS} ≤ V_{CM} ≤ V_{DD} - 1.4V		68	84		dB
Power-Supply Rejection Ratio	PSRR	2.5V ≤ V_{DD} ≤ 5.5V		78	100		dB
Large-Signal Voltage Gain	A_{VOL}	V_{SS} + 0.3V ≤ V_{OUT} ≤ V_{DD} - 0.3V	R_L = 100kΩ		120		dB
			R_L = 2kΩ	90	110		
Output Voltage High	V_{OH}	Specified as $\lvert V_{DD} - V_{OH} \rvert$	R_L = 100kΩ		3		mV
			R_L = 2kΩ		55	200	
Output Voltage Low	V_{OL}	Specified as $\lvert V_{SS} - V_{OL} \rvert$	R_L = 100kΩ		2		mV
			R_L = 2kΩ		30	75	
Output Short-Circuit Current		Sourcing			12		mA
		Sinking			30		
Shutdown Mode Output Leakage	$I_{OUTSHDN}$	Device in shutdown mode, $\overline{SHDN}$ = SS, V_{SS} < V_{OUT} < V_{CC} (Note 1)				±1.0	µA
$\overline{SHDN}$ Logic-Low	V_{IL}	(Note 1)				0.3 × V_{DD}	V
$\overline{SHDN}$ Logic-High	V_{IH}	(Note 1)		0.7 × V_{DD}			V
$\overline{SHDN}$ Input Current	I_{IL}, I_{IH}	$\overline{SHDN}$ = V_{DD} or V_{SS} (Note 1)			±0.001	±500	nA
Gain-Bandwidth Product	GBW				800		kHz
Phase Margin	ϕM				70		°
Gain Margin					20		dB
Slew Rate	SR				1		V/µs
Input Voltage-Noise Density	e_n	f = 10kHz			36		nV/√Hz
Input Current-Noise Density	i_n	f = 10kHz			1		fA/√Hz
Capacitive-Load Stability	C_{LOAD}	A_V = +1V/V			400		pF
Shutdown Delay Time	t_{SHDN}	A_V = +1V/V			0.4		µs
Enable Delay Time	t_{EN}	(Note 1)			6		µs
Power-On Time	t_{ON}				5		µs
Input Capacitance	C_{IN}				2.5		pF
Total Harmonic Distortion	THD	f = 10kHz, V_{OUT} = $2V_{P-P}$, A_V = +1V/V	R_L = 100kΩ		0.009		%
			R_L = 2kΩ		0.015		
Settling Time to 0.1%	t_S	V_{OUT} = 2V step			7		µs

Electrical Characteristics

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L = ∞ connected to V_{DD}/2, **T_A = -40°C to +125°C**, unless otherwise noted.) (Note 3)

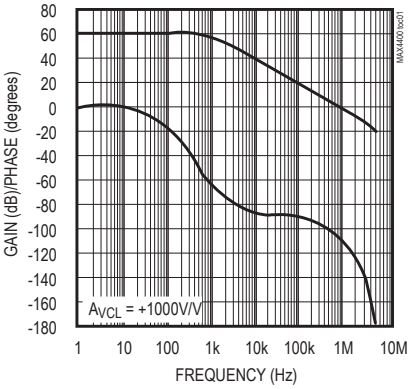
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Inferred by PSRR test		2.5		5.5	V
Supply Current per Amplifier	I_{DD}					800	µA
		MAX4400/MAX4401				±6.5	
Input Offset Voltage	V_{OS}	MAX4402/MAX4403				±8.0	mV
Input Offset Voltage Drift	TC_{VOS}				±1		µV/°C
Input Bias Current	I_B	(Note 2)				±100	pA
Input Offset Current	IOS	(Note 2)				±100	pA
Input Common-Mode Voltage Range	V_{CM}	Inferred from CMRR test		V_{SS}	V_{DD} - 1.5		V
Common-Mode Rejection Ratio	CMRR	$V_{SS} \le V_{CM} \le V_{DD}$ - 1.5V		65			dB
		$V_{SS} \le V_{CM} \le V_{DD}$ - 1.0V T_A = -20°C to +125°C		50			
Power-Supply Rejection Ratio	PSRR	2.5V ≤ V_{CC} ≤ 5.5V		74			dB
Shutdown Mode Output Leakage	$I_{OUTSHDN}$	Device in shutdown mode, $\overline{SHDN}$ = V_{SS}, $V_{SS} < V_{OUT} < V_{DD}$ (Note 1)	T_A = -40°C to +85°C			±1.0	µA
			T_A = +85°C to +125°C			±5.0	
$\overline{SHDN}$ Logic-Low	V_{IL}	(Note 1)				0.3 × V_{DD}	V
$\overline{SHDN}$ Logic-High	V_{IH}	(Note 1)		0.7 × V_{DD}			V
$\overline{SHDN}$ Input Current	I_{IL}, I_{IH}	$\overline{SHDN}$ = V_{DD} or V_{SS} (Notes 1, 2)				±1000	nA
Large-Signal Voltage Gain	A_{VOL}	V_{SS} + 0.3V ≤ V_{OUT} ≤ V_{DD} - 0.3V, R_L = 2kΩ		85			dB
Output Voltage High	V_{OH}	Specified as $\lvert V_{DD} - V_{OH}\rvert$, R_L = 2kΩ				250	mV
Output Voltage Low	V_{OL}	Specified as $\lvert V_{SS} - V_{OL}\rvert$, R_L = 2kΩ				100	mV

Note 1: Shutdown mode is only available in the 6-pin SC70 single op amp (MAX4401).
Note 2: Guaranteed by design.
Note 3: Specifications are 100% tested at T_A = +25°C (exceptions noted). All temperature limits are guaranteed by design.

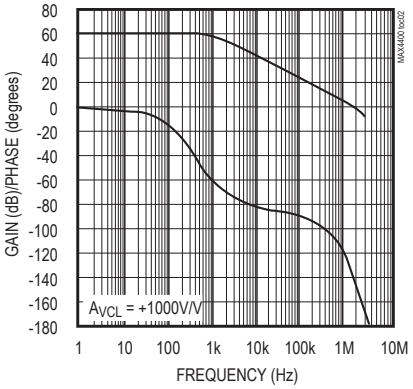
Typical Operating Characteristics

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD}/2, $V_{\overline{SHDN}}$ = 5V, R_L = ∞ connected to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

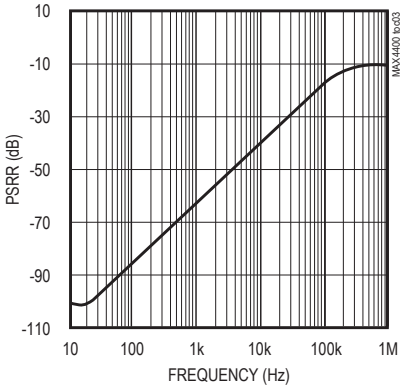
GAIN AND PHASE vs. FREQUENCY (NO LOAD)



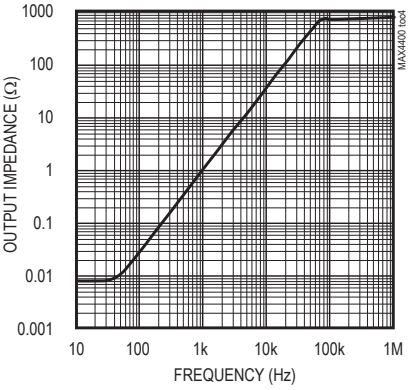
GAIN AND PHASE vs. FREQUENCY (C_L = 400pF)



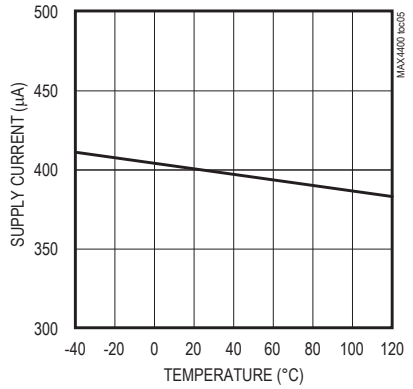
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



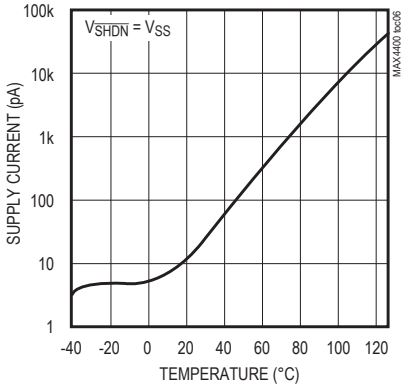
OUTPUT IMPEDANCE vs. FREQUENCY



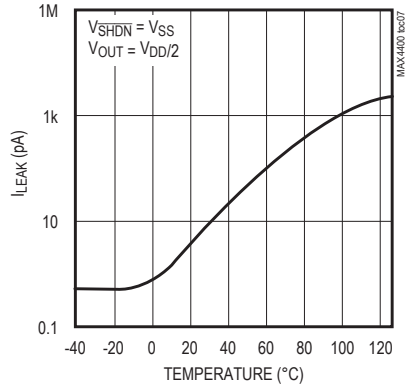
SUPPLY CURRENT vs. TEMPERATURE



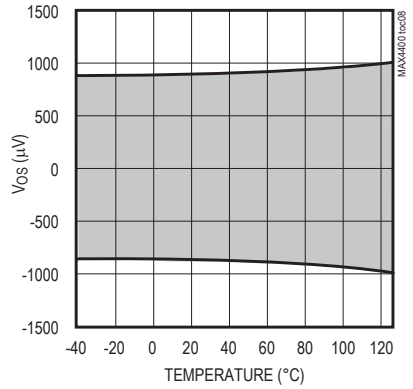
MAX4401 SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



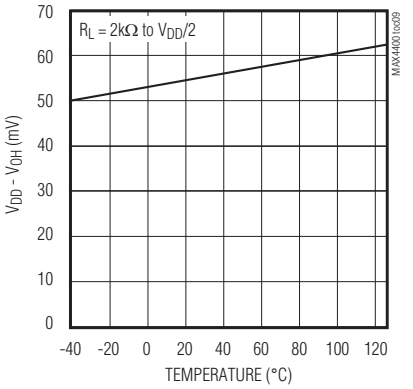
MAX4401 OUTPUT LEAKAGE CURRENT vs. TEMPERATURE



INPUT OFFSET VOLTAGE vs. TEMPERATURE



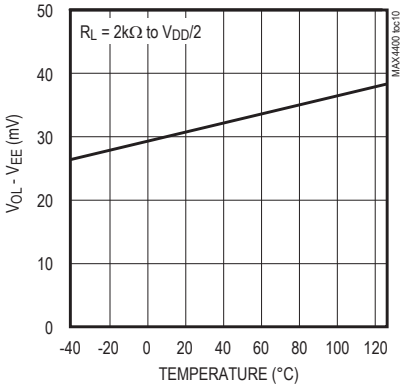
OUTPUT VOLTAGE SWING HIGH vs. TEMPERATURE



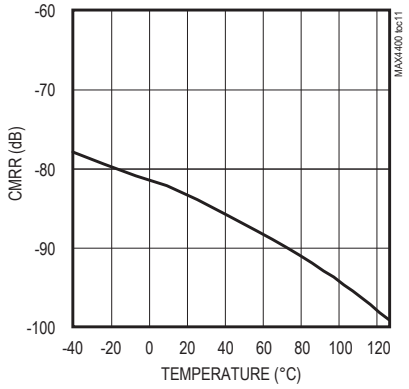
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD}/2, $V_{\overline{SHDN}}$ = 5V, R_L = ∞ connected to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

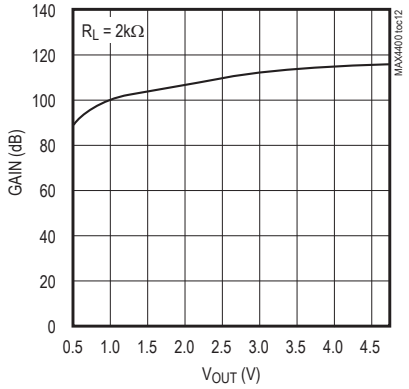
OUTPUT VOLTAGE SWING LOW vs. TEMPERATURE



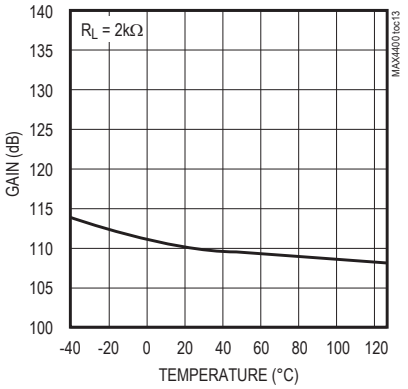
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



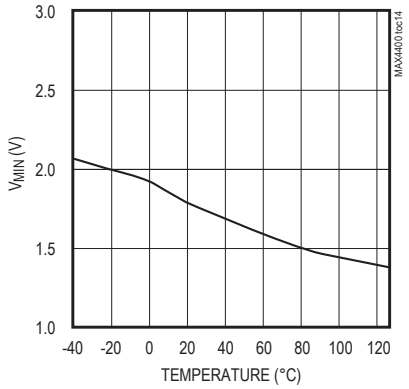
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



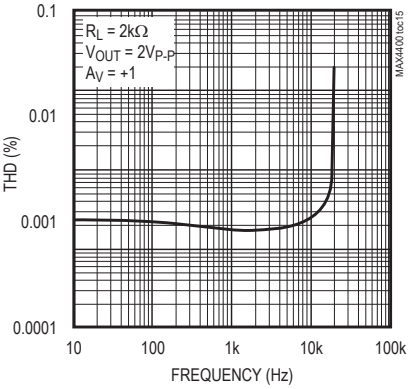
LARGE-SIGNAL GAIN vs. TEMPERATURE



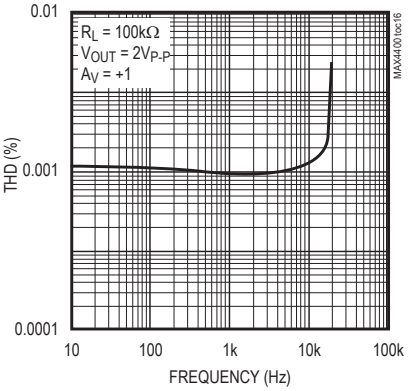
MINIMUM OPERATING VOLTAGE vs. TEMPERATURE



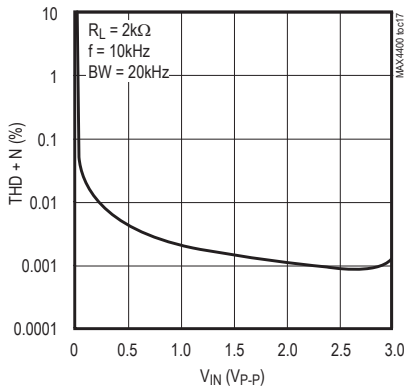
TOTAL HARMONIC DISTORTION vs. FREQUENCY



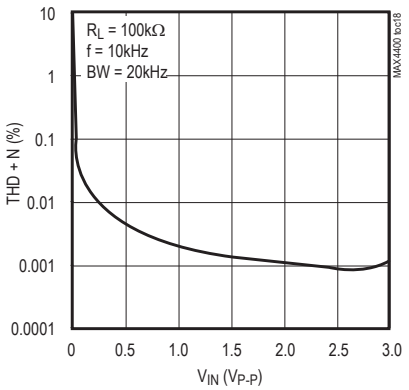
TOTAL HARMONIC DISTORTION vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. INPUT AMPLITUDE



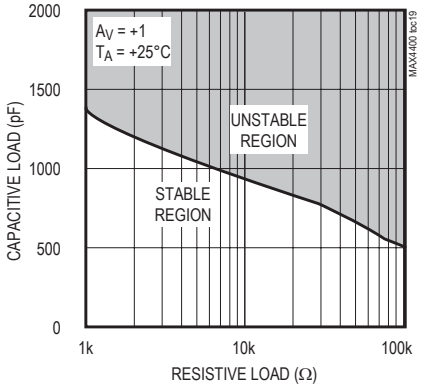
TOTAL HARMONIC DISTORTION PLUS NOISE vs. INPUT AMPLITUDE



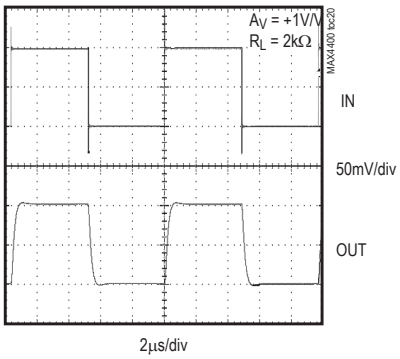
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD}/2, $V_{\overline{SHDN}}$ = 5V, R_L = ∞ connected to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

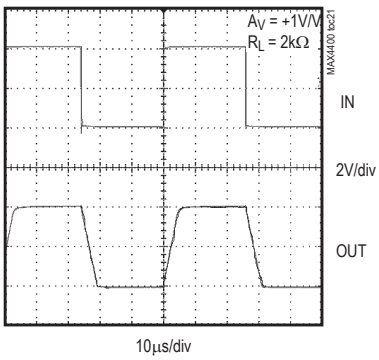
CAPACITIVE-LOAD STABILITY



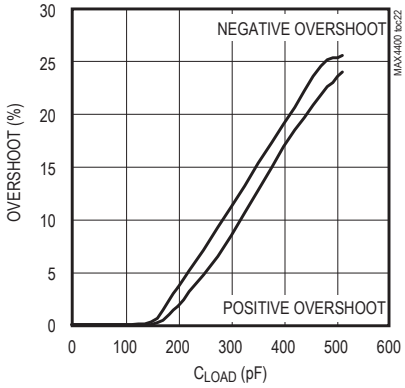
NONINVERTING SMALL-SIGNAL TRANSIENT RESPONSE



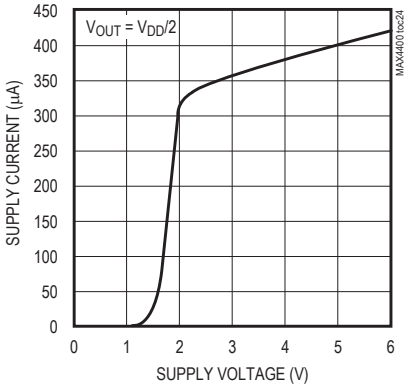
NONINVERTING LARGE-SIGNAL TRANSIENT RESPONSE



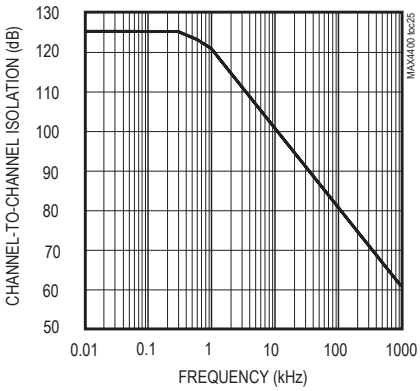
PERCENT OVERSHOOT vs. CAPACITIVE LOAD



SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAX4402/MAX4403 CHANNEL-TO-CHANNEL ISOLATION vs. FREQUENCY



Pin Description

PIN				NAME	FUNCTION
MAX4400	MAX4401	MAX4402	MAX4403		
1	1	—	—	IN+	Noninverting Amplifier Input
—	—	3	3	INA+	Noninverting Amplifier Input A
—	—	5	5	INB+	Noninverting Amplifier Input B
—	—	—	10	INC+	Noninverting Amplifier Input C
—	—	—	12	IND+	Noninverting Amplifier Input D
2	2	4	11	V_{SS}	Negative Supply. Connect to ground for single- supply operation.
3	3	—	—	IN-	Inverting Amplifier Input
—	—	2	2	INA-	Inverting Amplifier Input A
—	—	6	6	INB-	Inverting Amplifier Input B
—	—	—	9	INC-	Inverting Amplifier Input C
—	—	—	13	IND-	Inverting Amplifier Input D
4	4	—	—	OUT	Amplifier Output
—	—	1	1	OUTA	Amplifier Output A
—	—	7	7	OUTB	Amplifier Output B
—	—	—	8	OUTC	Amplifier Output C
—	—	—	14	OUTD	Amplifier Output D
5	6	8	4	V_{DD}	Positive Supply
—	5	—	—	$\overline{SHDN}$	Active-Low Shutdown Input. Connect to V_{DD} for normal operation. Do not leave unconnected.

Detailed Description

Rail-to-Rail Output Stage

The MAX4400–MAX4403 can drive a 2kΩ load and still typically swing within 55mV of the supply rails. Figure 1 shows the output voltage swing of the MAX4400 configured with A_V = +10V/V.

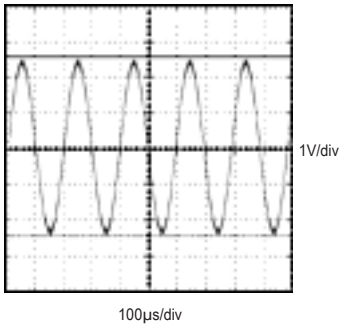


Figure 1. Rail-to-Rail Output Operation

Driving Capacitive Loads

Driving a capacitive load can cause instability in many op amps, especially those with low quiescent current. The MAX4400–MAX4403 are unity-gain stable for a range of capacitive loads to above 400pF. Figure 2 shows the response of the MAX4400 with an excessive capacitive load. Adding a series resistor between the output and the load capacitor (Figure 3) improves the circuit's response by isolating the load capacitance from the op amp's output.

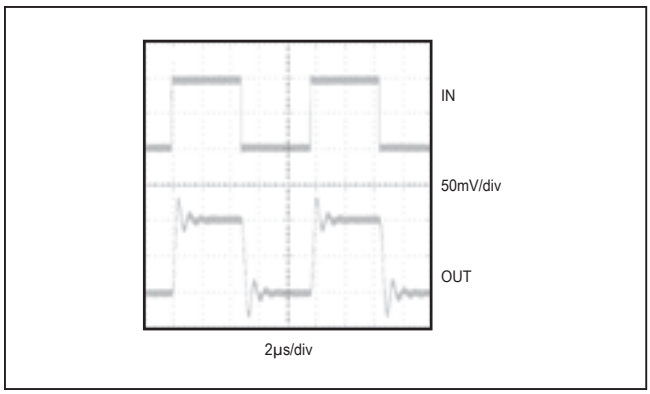


Figure 2. Small-Signal Transient Response with Excessive Capacitive Load

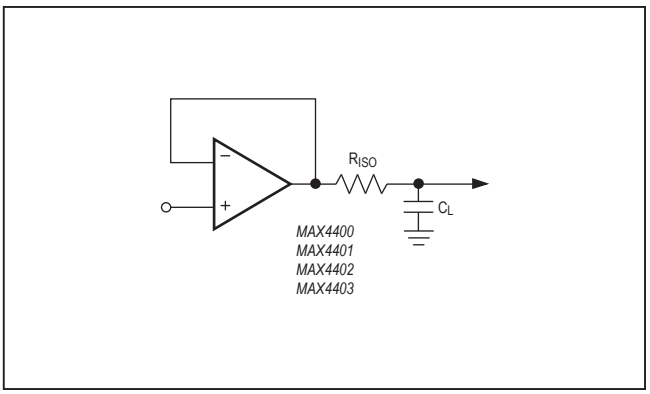


Figure 3. Capacitive-Load-Driving Circuit

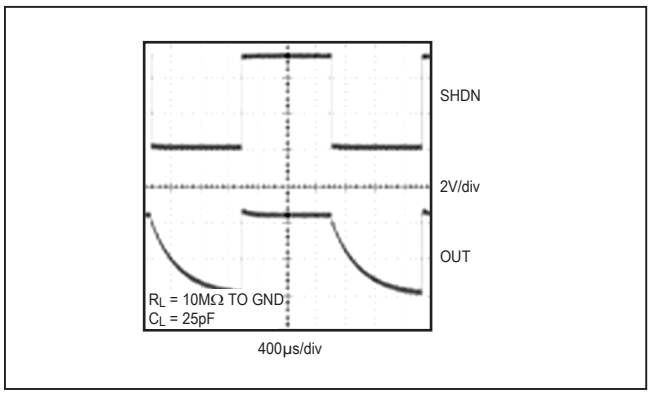


Figure 4. Shutdown Waveform

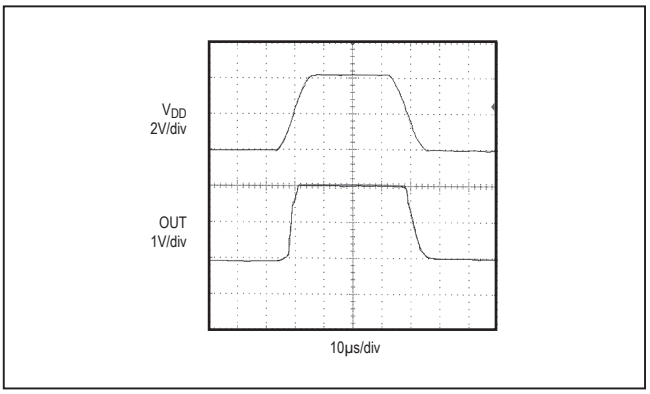


Figure 5. Power-Up/Power-Down Waveform

Applications Information

Shutdown Mode

The MAX4401 features a low-power shutdown mode. When $\overline{SHDN}$ goes low, the supply current drops to 20pA (typ) and the output enters a high-impedance state. Pull $\overline{SHDN}$ high to enable the amplifier. Do not leave $\overline{SHDN}$ unconnected. Figure 4 shows the shutdown waveform.

Power-Up

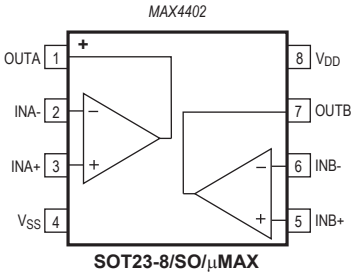
The MAX4400–MAX4403 outputs typically settle within 5µs after power-up. Figure 5 shows the output voltage on power-up and power-down.

Power Supplies and Layout

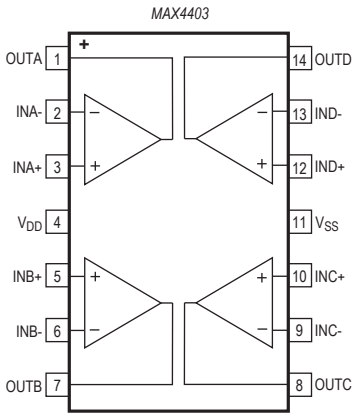
The MAX4400–MAX4403 operate from a single +2.5V to +5.5V power supply. Bypass the power supply with a 0.1µF capacitor to ground.

Good layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the op amp's pins.

Pin Configurations (continued)



SOT23-8/SO/μMAX



TSSOP/SO

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4400AXK+T	-40°C to +125°C	5 SC70	AAG
MAX4400AUK+T	-40°C to +125°C	5 SOT23	ADNP
MAX4401AXT+T	-40°C to +125°C	6 SC70	AAB
MAX4402AKA+T	-40°C to +125°C	8 SOT23	AADI
MAX4402AKA/V+T	-40°C to +125°C	8 SOT23	AETR
MAX4402AUA+	-40°C to +125°C	8 μMAX	—
MAX4402AUA/V+T	-40°C to +125°C	8 μMAX	—
MAX4402ASA+	-40°C to +125°C	8 SO	—
MAX4403AUD+	-40°C to +125°C	14 TSSOP	—
MAX4403ASD+	-40°C to +125°C	14 SO	—

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/00	Initial Release	—
1	11/00	Release of MAX4402.	1, 2, 9
2	7/00	Release of MAX4403.	1, 6, 7
3	9/01	Added µMAX package to data sheet.	1, 2, 9
4	7/12	Added automotive package for MAX4402 to data sheet.	1
5	6/14	Added MAX4402AKA/V+T automotive package to data sheet.	1
6	10/17	Added AEC qualfication statement to *Benefits and Features* section	1
7	3/18	Added *Package Information* section and updated *Absolute Maximum Ratings* section	2
8	1/19	Updated *Applications* and *Package Information* sections	1, 2–4, 12