Absolute Maximum Ratings

(Voltages relative to GND.)
Voltage Range on V_{CC} ..... -0.3V to +4.3V
Voltage Range on Any Pin ..... -0.3V to (V_{CC} + 0.3V), not to exceed +4.3V
Continuous Power Dissipation (T_A = +70°C)
μSOP (derate 4.5mW/°C above +70°C) 362mW

Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

μSOP-8

PACKAGE CODE	U8+1
Outline Number	21-0036
Land Pattern Number	90-0092
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	221°C/W
Junction to Case (θ_{JC})	42°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	206.30/W
Junction to Case (θ_{JC})	42°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Recommended Operating Conditions

(T_A = -40°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	3.0		3.6	V
Input Logic 1	V_{IH}		0.8 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0	V_{IL}		V_{GND} - 0.3		0.2 x V_{CC}	V
Input Logic Open	I_{IF}	0V < V_{IN} < V_{CC} (Note 2)			Q1	FA
Input Leakage	I_{IL}	0V < V_{IN} < V_{CC} (Note 3)			Q80	FA
SSO Load	C_{SSO}	f_{SSO} < 67MHz			15	pF
		67MHz P f_{SSO} < 101MHz			10	
		101MHz P f_{SSO} < 134MHz			7	
Crystal or Clock Input Frequency	f_{IN}		16.0		33.4	MHz
Crystal ESR	X_{ESR}				90	I
Clock Input Duty Cycle	F_{INDC}		40		60	%
Crystal Parallel Load Capacitance	C_L	(Note 4)			18	pF

DC Electrical Characteristics

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC1}	C_{SSO} = 15pF, f_{SSO} = 16MHz			15	mA
Power-Down Current	I_{CCQ}	$\overline{PDN}$ = GND, all input pins open			200	µA
Output Leakage (SSO)	I_{OZ}	$\overline{PDN}$ = GND	-1		+1	µA
Low-Level Output Voltage (SSO)	V_{OL}	I_{OL} = 4mA			0.4	V
High-Level Output Voltage (SSO)	V_{OH}	I_{OH} = -4mA	2.4			V
Input Capacitance (X1/X2)	C_{IN}	(Note 5)		5		pF

AC Electrical Characteristics

(V_{CC} = +3.0 to +3.6V, T_A = -40°C to +125°C, unless otherwise noted.)

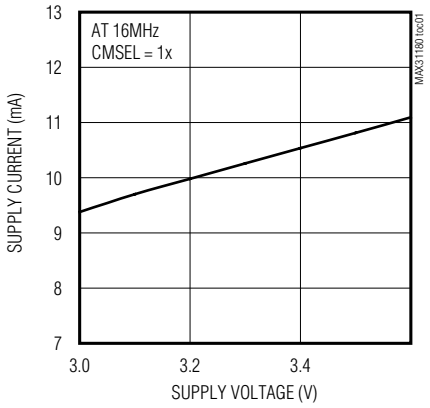
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SSO Duty Cycle	SSODC	Measured at V_{CC}/2, CMSEL = 0 or open	40		60	%
		Measured at V_{CC}/2, CMSEL = 1	30		70	
Rise Time	t_R	(Note 6)		1.6		ns
Fall Time	t_F	(Note 6)		1.6		ns
Peak Cycle-to-Cycle Jitter	t_J	f_{SSO} = 16MHz, T_A = -40 to +85°C, 10,000 cycles (Note 5)		75		ps
Power-Up Time	t_{POR}	$\overline{PDN}$ pin (Note 7)			11	ms
Power-Down Time	$t_{\overline{PDN}}$	$\overline{PDN}$ pin (Note 8)			100	ns
Dither Rate	f_{DITHER}	(Note 9)		f_{IN}/992		

Note 1: All voltages referenced to ground.
Note 2: Maximum source/sink current applied to input to be considered an open. Typical voltage range between 0.4 x V_{CC} and 0.55 x V_{CC}.
Note 3: Applicable to pins CMSEL, SMSEL, and $\overline{PDN}$.
Note 4: See information about C_{L1} and C_{L2} in the *Applications Information* section at the end of the data sheet.
Note 5: Not production tested.
Note 6: For 7pF load.
Note 7: Time between $\overline{PDN}$ deasserted to output active.
Note 8: Time between $\overline{PDN}$ asserted to output high impedance.
Note 9: Guaranteed by design.

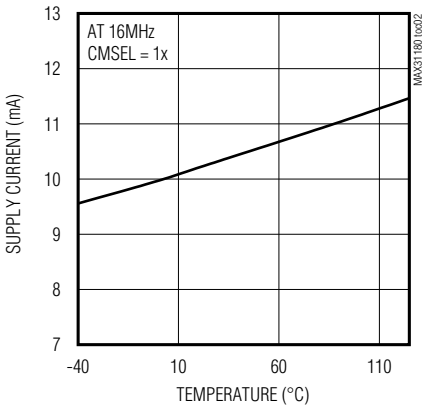
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

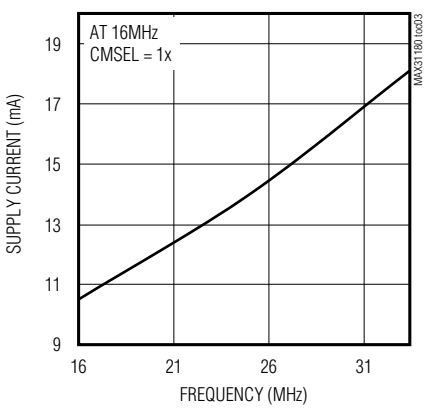
SUPPLY CURRENT vs. SUPPLY VOLTAGE



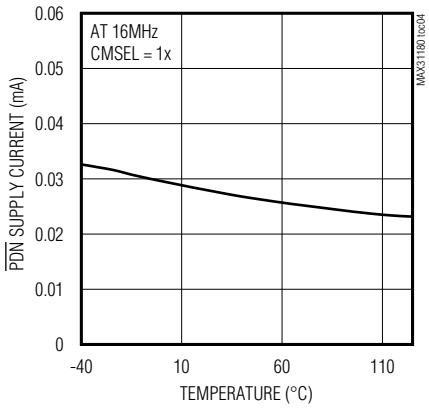
SUPPLY CURRENT vs. TEMPERATURE



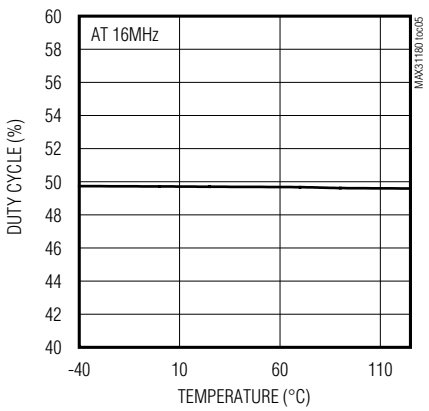
SUPPLY CURRENT vs. FREQUENCY



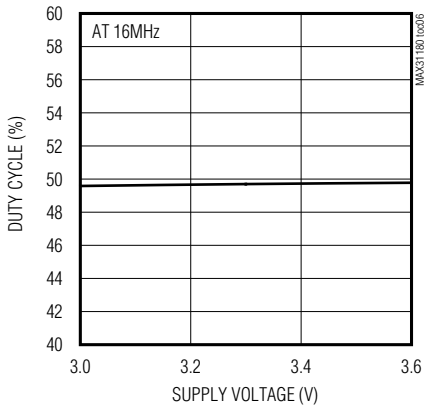
$\overline{PDN}$ SUPPLY CURRENT vs. TEMPERATURE



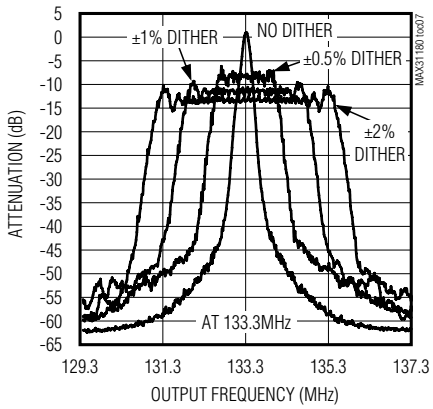
DUTY CYCLE vs. TEMPERATURE



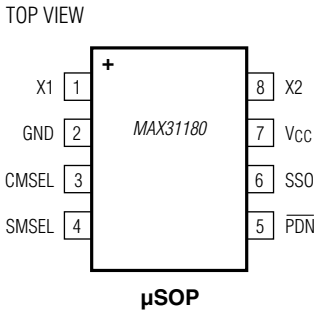
DUTY CYCLE vs. SUPPLY VOLTAGE



FREQUENCY SPECTRUM AT 133.3MHz



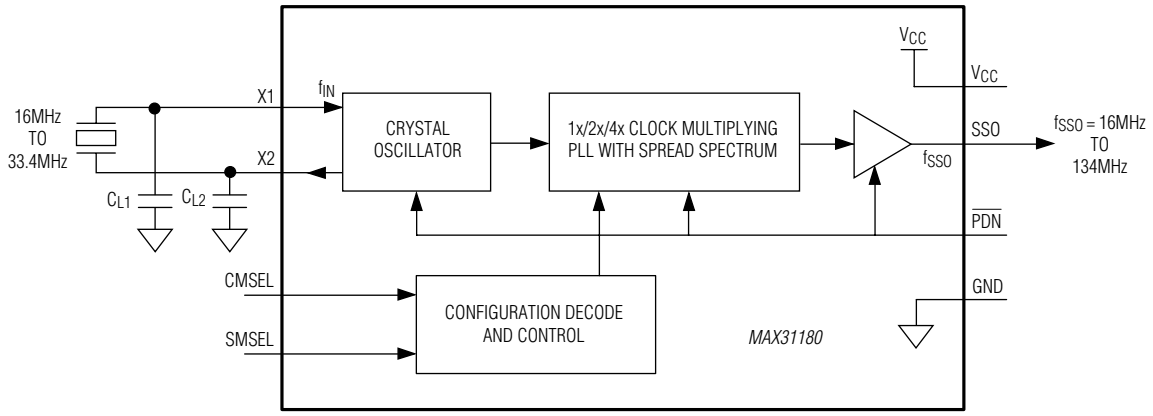
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	X1	Crystal Drive/Clock Input. A crystal with the proper loading capacitors is connected across X1 and X2. Instead of a crystal, a clock can be applied at the X1 input.
2	GND	Signal Ground
3	CMSEL	Clock Multiplier Select. Tri-level digital input. 0 = 1x Open = 2x 1 = 4x
4	SMSEL	Spread-Spectrum Magnitude Select. Tri-level digital input. 0 = ±0.5% Open = ±1.0% 1 = ±1.5%
5	$\overline{PDN}$	Active-Low Power-Down/Spread-Spectrum Disable. Tri-level digital input. 0 = Power-Down/SSO Three-Stated Open = Power-Up/Spread Spectrum Disabled 1 = Power-Up/Spread Spectrum Enabled
6	SSO	Spread-Spectrum Clock Multiplier Output. Outputs a 1x, 2x, or 4x spread-spectrum version of the crystal or clock applied at the X1/X2 pins.
7	V_{CC}	Supply Voltage
8	X2	Crystal Drive Output. A crystal with the proper loading capacitors is connected across X1 and X2. If a clock is connected to X1, then X2 should be left open circuit.

Block Diagram



NOTE: SEE INFORMATION ABOUT C_{L1} AND C_{L2} IN THE *APPLICATIONS INFORMATION* SECTION AT THE END OF THE DATA SHEET.

Detailed Description

The MAX31180 is a crystal multiplier with center spread-spectrum capability. A 16MHz to 33.4MHz crystal is connected to the X1 and X2 pins. Alternately, a 16MHz to 33.4MHz clock can be applied to X1 in place of the crystal. In such applications, X2 would be left open circuit. Using the CMSEL input, the user selects whether the attached crystal or input clock is multiplied by 1, 2, or 4. The MAX31180 is capable of generating spread-spectrum clocks from 16MHz to 134MHz.

The PLL can dither the output clock about its center frequency at a user-selectable magnitude. Using the SMSEL input, the user selects the dither magnitude. The $\overline{PDN}$ input can be used to place the device into a low-power standby mode where the SSO output is three-stated. If the $\overline{PDN}$ pin is open, the SSO output is active but the spread-spectrum dithering is disabled. The spread-spectrum dither rate is fixed at $f_{IN}/992$ to keep the dither rate above the audio frequency range. On power-up, the output clock (SSO) remains three-stated until the PLL reaches a stable frequency (f_{SSO}) and dither (f_{DITHER}).

Applications Information

Crystal Selection

The MAX31180 requires a parallel resonating crystal operating in the fundamental mode, with an ESR of less than 90Ω. The crystal should be placed very close to the device to minimize excessive loading due to parasitic capacitances.

Oscillator Input

When driving the MAX31180 using an external oscillator clock, consider the input (X1) to be high impedance.

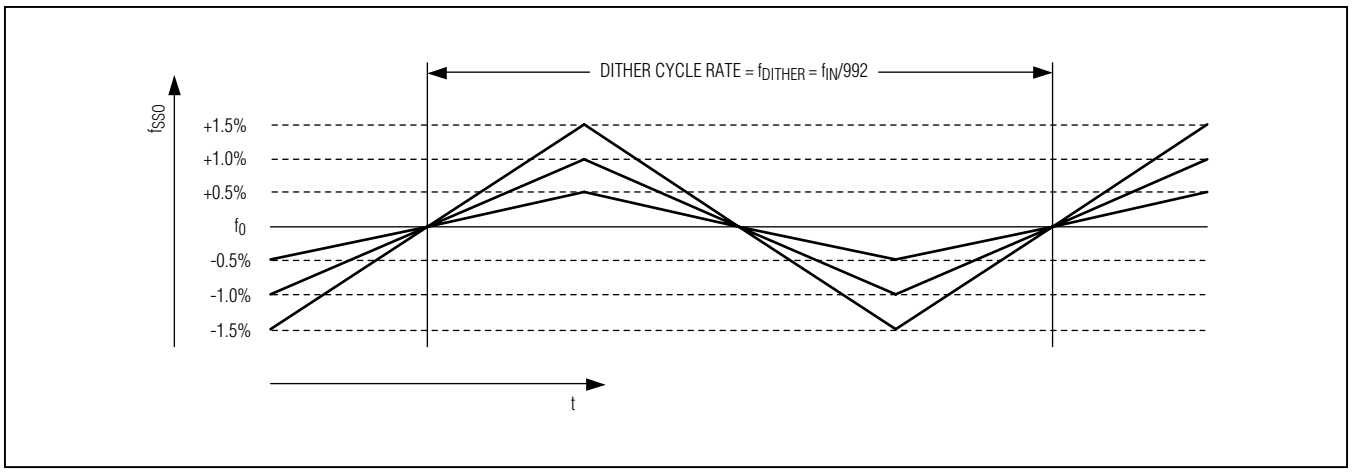


Figure 1. Spread-Spectrum Frequency Modulation

Crystal Capacitor Selection

The load capacitors C_{L1} and C_{L2} are selected based on the crystal specifications (from the data sheet of the crystal used). The crystal parallel load capacitance is calculated as follows:

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_{IN} \qquad \text{Equation 1}$$

For the MAX31180 use $C_{L1} = C_{L2} = C_{LX}$.

In this case, the equation then reduces to:

$$C_L = \frac{C_{LX}}{2} + C_{IN} \qquad \text{Equation 2}$$

where $C_{L1} = C_{L2} = C_{LX}$.

Equation 2 is used to calculate the values of C_{L1} and C_{L2} based on values on C_L and C_{IN} noted in the *Recommended Operating Conditions* and *DC Electrical Characteristics*.

Power-Supply Decoupling

To achieve best results, it is highly recommended that a decoupling capacitor is used on the IC power-supply pins. Typical values of decoupling capacitors are 0.001µF and 0.1µF. Use a high-quality, ceramic, surface-mount capacitor, and mount it as close as possible to the V_{CC} and GND pins of the IC to minimize lead inductance.

Layout Considerations

As noted earlier, the crystal should be placed very close to the device to minimize excessive loading due to parasitic capacitances. Care should also be taken to minimize loading on pins that could be open as a programming option (SMSEL and CMSEL). Coupling on inputs due to clocks should be minimized.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX31180AUA+	-40°C to +125°C	8 µSOP
MAX31180AUA+T	-40°C to +125°C	8 µSOP
MAX31180AUA/V+	-40°C to +125°C	8 µSOP
MAX31180AUA/V+T	-40°C to +125°C	8 µSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
/V denotes an automotive qualified part.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/12	Initial release	—
1	3/13	Added automotive qualified parts to *Ordering Information*	8
2	9/17	Added AEC-Q100 qualification statement to *Benefits and Features* section	1
3	2/19	Updated *Package Information* section	2

