

Current-Mode PWM Controllers with Programmable Switching Frequency

ABSOLUTE MAXIMUM RATINGS

IN to GND	-0.3V to +30V	Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
IN Clamp (Internal Shunt) Current	5mA	10-Pin μMAX (derate 5.6mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)
V_{CC} to GND	-0.3V to +13V	444.4mW
FB, COMP, UVLO/EN, RT, CS to GND	-0.3V to +6V	Operating Temperature Range
UFLG to GND	-0.3V to +30V	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
NDRV to GND	-0.3V to ($V_{CC} + 0.3\text{V}$)	Storage Temperature Range
		-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
		Junction Temperature
		+150 $^\circ\text{C}$
		Lead Temperature (soldering, 10s)
		+300 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{IN} = +12\text{V}$ (for MAX15000, bring V_{IN} up to 23.6V for startup), 10nF bypass capacitors at IN and V_{CC} , R12 = 15k Ω (MAX1500_A), R12 = 7.5k Ω (MAX1500_B), R15 = 1k Ω , C6 = 100nF (see the *Typical Application Circuit*), NDRV = open, $V_{UVLO/EN} = +1.4\text{V}$, $V_{FB} = +1.0\text{V}$, COMP = open, $V_{CS} = 0\text{V}$, $T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO/STARTUP						
Bootstrap UVLO Wake-Up Level	V_{SUVR}	V_{IN} rising (MAX15000 only)	19.68	21.6	23.60	V
Bootstrap UVLO Shutdown Level	V_{SUVF}	V_{IN} falling (MAX15000 only)	9.05	9.74	10.43	V
UVLO/EN Wake-Up Threshold	V_{ULR2}	UVLO/EN rising	1.218	1.23	1.242	V
UVLO/EN Shutdown Threshold	V_{ULF2}	UVLO/EN falling	1.14	1.17	1.20	V
UVLO/EN Input Current	I_{UVLO}	$V_{UVLO/EN} \leq 2\text{V}$	-50		+50	nA
UVLO/EN Hysteresis				60		mV
IN Supply Current In UVLO	I_{START}	$V_{IN} = 19\text{V}$, MAX15000 only when in bootstrap UVLO		50	90	μA
IN Input Voltage Range	V_{IN}	MAX15001 only	9.5		24.0	V
UVLO/EN to UFLG Propagation Delay (Figure 3)		UVLO/EN steps up from 1V to 1.4V		3		μs
		UVLO/EN steps down from 1.4V to 1V		0.6		
UVLO/EN to NDRV Propagation Delay (Figure 3)		UVLO/EN steps up from 1V to 1.4V		3	10	ms
		UVLO/EN steps down from 1.4V to 1V	150	210	300	
Bootstrap UVLO Propagation Delay		V_{IN} steps up from 9V to 24V (MAX15000 only)		5		μs
		V_{IN} steps down from 24V to 9V (MAX15000 only)		1		
UFLG Low Output Voltage	V_{UFLG}	$I_{UFLG} = 5\text{mA}$ sinking			0.8	V
UFLG High Output Leakage Current		$V_{UFLG} = 25\text{V}$		0.1	1	μA
INTERNAL SUPPLY						
V_{CC} Regulator Set Point	V_{CCSP}	$V_{IN} = 10.8\text{V}$ to 24V, sinking 1 μA to 20mA from V_{CC}	7.0		10.5	V
IN Supply Current After Startup	I_{IN}	$V_{IN} = 24\text{V}$		2	4	mA
Shutdown Supply Current		UVLO/EN = low		50	90	μA

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MAX15000/MAX15001

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = +12V$ (for MAX15000, bring V_{IN} up to 23.6V for startup), 10nF bypass capacitors at IN and V_{CC} , $R_{12} = 15k\Omega$ (MAX1500_A), $R_{12} = 7.5k\Omega$ (MAX1500_B), $R_{15} = 1k\Omega$, $C_6 = 100nF$ (see the *Typical Application Circuit*), NDRV = open, $V_{UVLO/EN} = +1.4V$, $V_{FB} = +1.0V$, COMP = open, $V_{CS} = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVER						
Driver Output Impedance	$R_{ON(LOW)}$	Measured at NDRV sinking 100mA		2	4	Ω
	$R_{ON(HIGH)}$	Measured at NDRV sourcing 20mA		4	10	
Driver Peak Sink Current				1		A
Driver Peak Source Current				0.65		A
PWM COMPARATOR						
Comparator Offset Voltage	V_{PWM}	$V_{COMP} - V_{CS}$	1.24	1.38	1.54	V
CS Input Bias Current	I_{CS}	$V_{CS} = 0V$	-4		+4	μA
Comparator Propagation Delay	t_{PWM}	Change in $V_{CS} = 0.1V$		60		ns
CURRENT-LIMIT COMPARATOR						
Current-Limit Trip Threshold	V_{CS}		900	1000	1100	mV
CS Input Bias Current	I_{CS}	$V_{CS} = 0V$	-4		+4	μA
Propagation Delay From Comparator Input to NDRV	t_{PDCS}	100mV overdrive		60		ns
IN CLAMP VOLTAGE						
IN Clamp Voltage	V_{INC}	2mA sink current (Note 2)	24.1	26.1	29.0	V
ERROR AMPLIFIER						
Voltage Gain		$R_{LOAD} = 100k\Omega$		80		dB
Unity-Gain Bandwidth		$R_{LOAD} = 100k\Omega$, $C_{LOAD} = 200pF$		2		MHz
Phase Margin		$R_{LOAD} = 100k\Omega$, $C_{LOAD} = 200pF$		65		degrees
FB Input Offset Voltage				± 1		mV
COMP High Voltage		$I_{COMP} = 0$	2.8			V
COMP Low Voltage		$I_{COMP} = 0$			1.1	
Source Current			0.5			mA
Sink Current			0.5			mA
Reference Voltage	V_{REF}	(Note 3)		1.230		V
Reference Voltage Accuracy			-1.5		+1.5	%
FB Input Bias Current			-50		+50	nA
COMP Short-Circuit Current				8		mA
DIGITAL SOFT-START						
Soft-Start Duration	t_{SS}			1984		NDRV cycles
		$f_{SW} = 350kHz$		5.6		ms
Reference Voltage Steps During Soft-Start				31		steps
Reference Voltage Step				39.67		mV

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ELECTRICAL CHARACTERISTICS (continued)

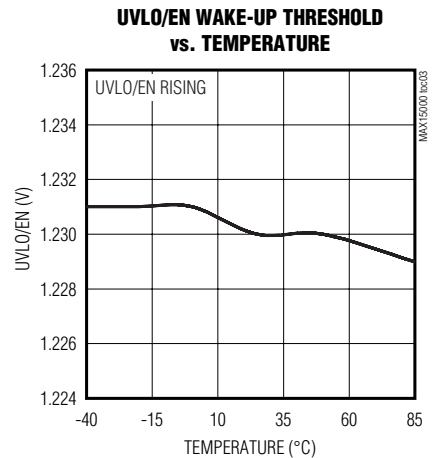
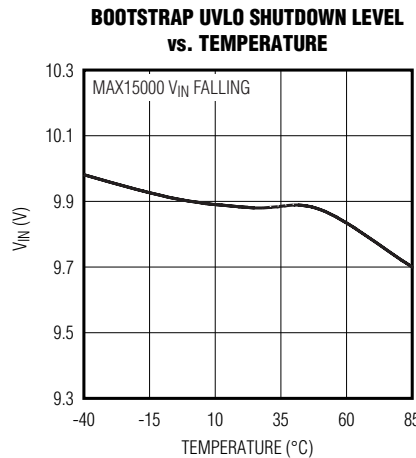
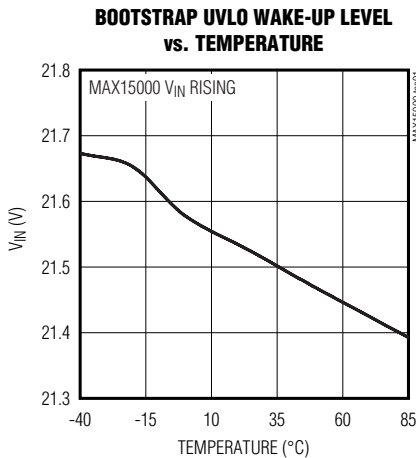
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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Oscillator Frequency Range	f_{OSC}		50		2500	kHz
Oscillator Frequency Accuracy		$f_{OSC} = 200kHz$ to $800kHz$	-10		+10	%
		$f_{OSC} = 50kHz$ to $2500kHz$	-20		+20	
NDRV Switching Frequency (Note 4)	f_{SW}	MAX1500_A, $f_{SW} = f_{OSC}/2$	25		625	kHz
		MAX1500_B, $f_{SW} = f_{OSC}/4$	12.5		625.0	
Maximum Duty Cycle	D_{MAX}	MAX1500_A		50		%
		MAX1500_B		75		

- Note 1:** All devices are 100% tested at $T_A = +85^\circ C$. All limits over temperature are guaranteed by characterization.
- Note 2:** The MAX15000 is intended for use in universal input power supplies. The internal clamp circuit at IN is used to prevent the bootstrap capacitor (C1 in Figure 1) from charging to a voltage beyond the absolute maximum rating of the device when UVLO/EN is low (shutdown mode). Externally limit the maximum current to IN (hence to clamp) to 2mA maximum when UVLO/EN is low. Clamp currents higher than 2mA may result in a clamp voltage higher than 30V, thus exceeding the absolute maximum rating for IN. For the MAX15001, do not exceed the 24V maximum operating voltage of the device.
- Note 3:** V_{REF} is measured with FB connected to COMP (see the *Functional Diagram*).
- Note 4:** The oscillator in the MAX1500_A is capable of operating up to 2500kHz. However, the NDRV switching frequency is limited to operate up to 625kHz. Thus, the oscillator frequency for MAX1500_A must be limited to 1250kHz (maximum).

Typical Operating Characteristics

($V_{UVLO/EN} = +1.4V$, $V_{FB} = +1V$, COMP = open, $V_{CS} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)

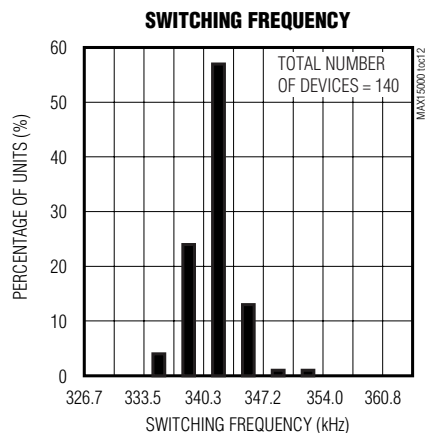
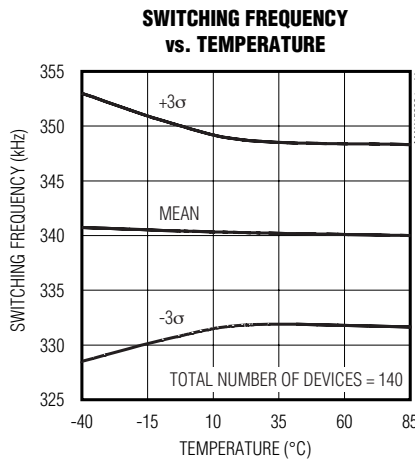
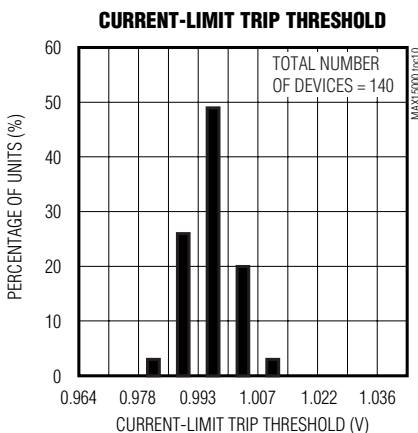
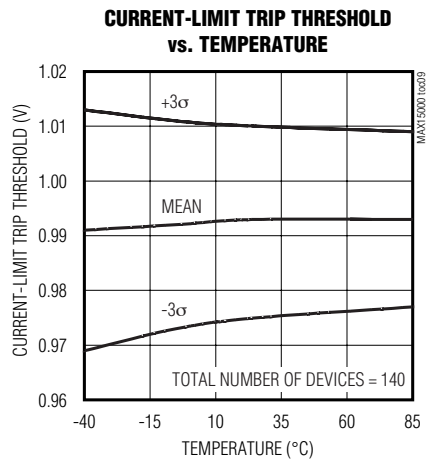
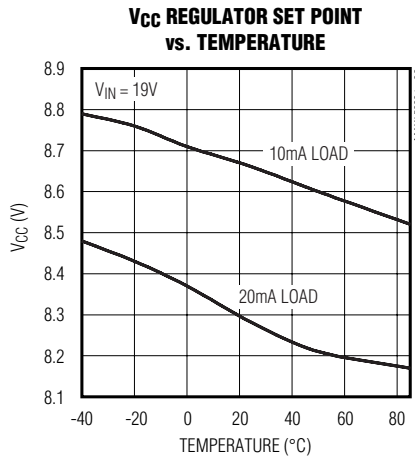
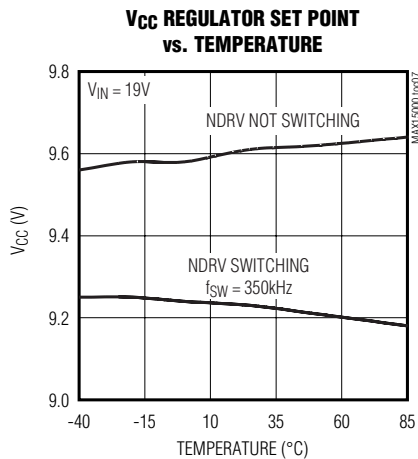
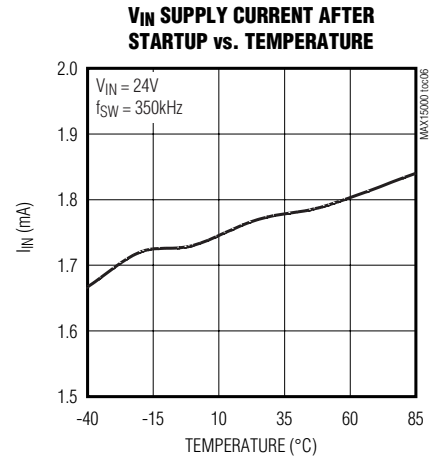
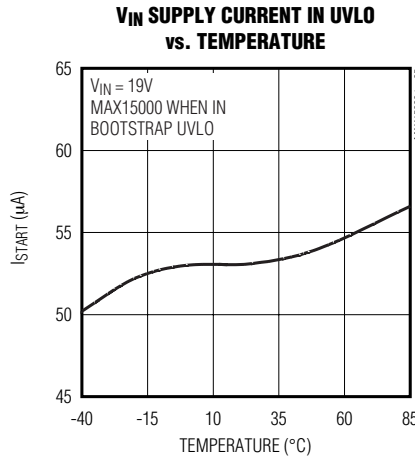
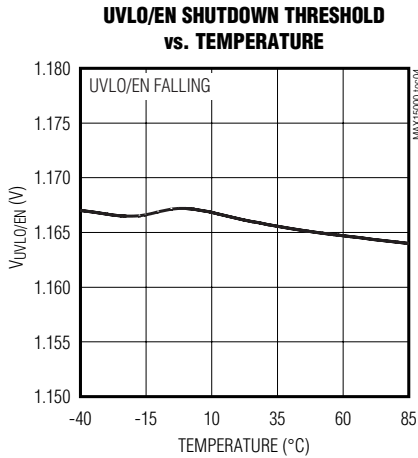


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Typical Operating Characteristics (continued)

($V_{UVLO/EN} = +1.4V$, $V_{FB} = +1V$, COMP = open, $V_{CS} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX15000/MAX15001

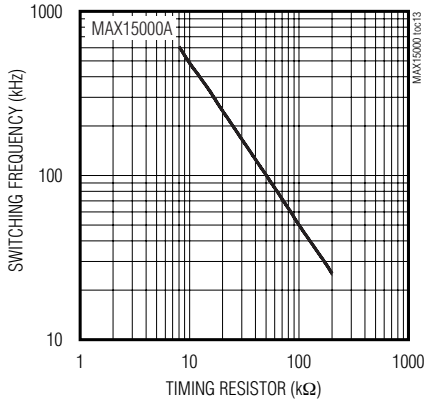


Current-Mode PWM Controllers with Programmable Switching Frequency

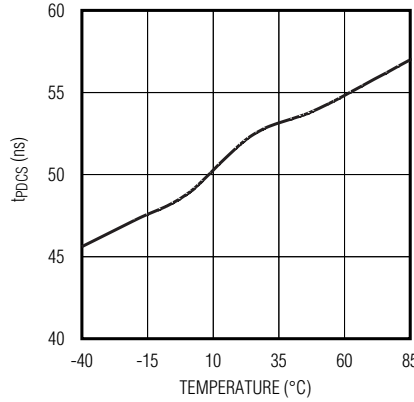
Typical Operating Characteristics (continued)

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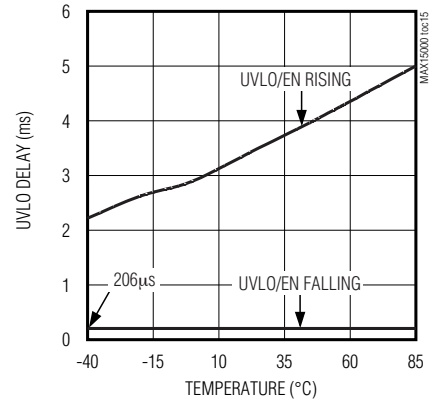
SWITCHING FREQUENCY vs. TIMING RESISTOR



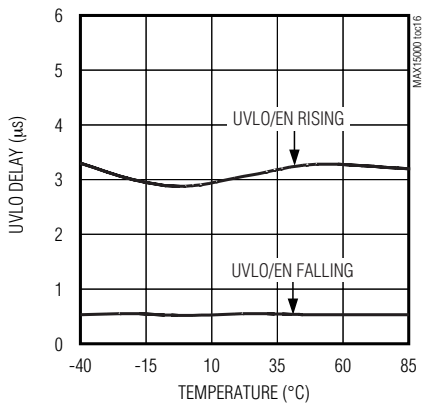
PROPAGATION DELAY FROM CURRENT-LIMIT COMPARATOR INPUT TO NDRV vs. TEMPERATURE



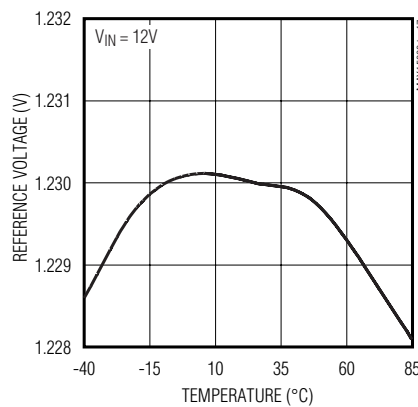
UVLO/EN TO NDRV PROPAGATION DELAY vs. TEMPERATURE



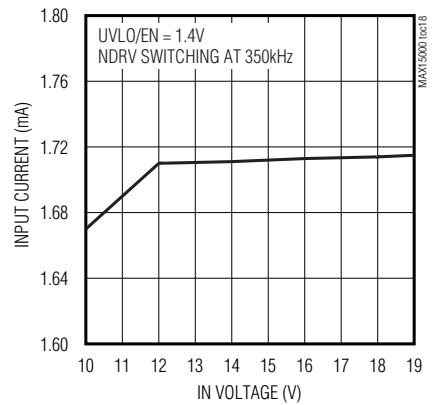
UVLO/EN TO UFLG PROPAGATION DELAY vs. TEMPERATURE



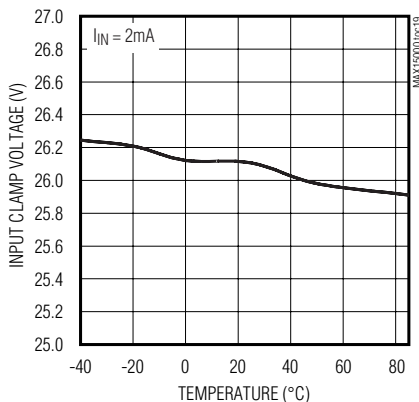
REFERENCE VOLTAGE vs. TEMPERATURE



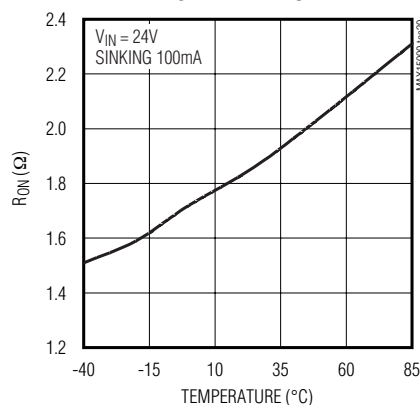
INPUT CURRENT vs. IN VOLTAGE



INPUT CLAMP VOLTAGE vs. TEMPERATURE



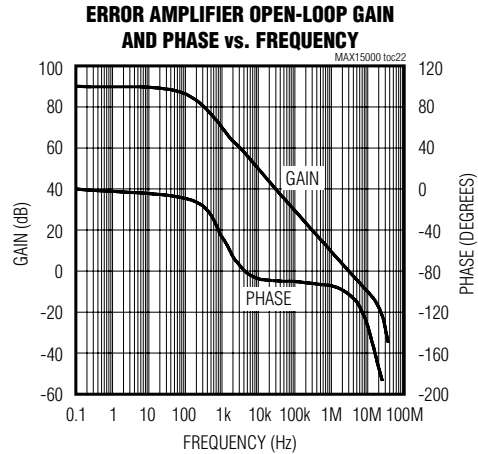
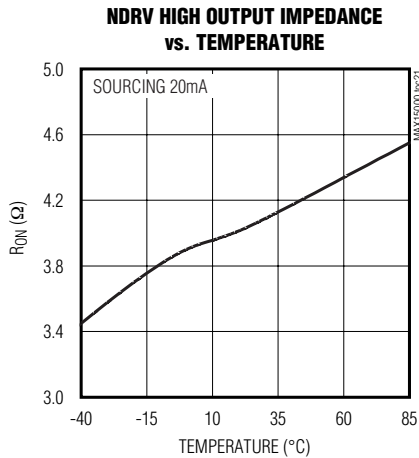
NDRV LOW OUTPUT IMPEDANCE vs. TEMPERATURE



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Typical Operating Characteristics (continued)

($V_{UVLO/EN} = +1.4V$, $V_{FB} = +1V$, COMP = open, $V_{CS} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)



MAX15000/MAX15001

Pin Description

PIN	NAME	FUNCTION
1	UVLO/EN	Externally Programmable Undervoltage Lockout. UVLO/EN programs the input start voltage. Connect UVLO/EN to GND to disable the device. NDRV stops switching approximately 210μs after the UVLO/EN voltage falls below 1.17V.
2	UFLG	Open-Drain Undervoltage Flag Output. UFLG is asserted low as soon as the UVLO/EN voltage falls below its threshold.
3	FB	Error-Amplifier Inverting Input
4	COMP	Error-Amplifier Output
5	CS	Current-Sense Input. Current-sense connection for PWM regulation and cycle-by-cycle current limit. Connect to the high side of the sense resistor. An RC filter may be necessary to eliminate leading-edge spikes. Current-limit trip voltage is 1V.
6	RT	Oscillator Timing Resistor Input. An RC network may be required to reduce jitter (see the <i>Typical Application Circuit</i>).
7	GND	Ground Connection
8	NDRV	External n-Channel MOSFET Gate Connection
9	VCC	Gate-Drive Supply. Internally generated supply from IN. Decouple VCC with a 10nF or larger capacitor to GND.
10	IN	IN Supply. Decouple with a 10nF or larger capacitor to GND. For bootstrapped operation (MAX15000), connect a startup resistor from the input supply line to IN. Connect the bias winding supply to IN also (see the <i>Typical Operating Circuit</i>). For the MAX15001, connect IN directly to the 9.5V to 24V supply.

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Detailed Description

The MAX15000/MAX15001 current-mode PWM controllers are ideal for isolated and nonisolated power-supply applications. The devices offer an accurate input startup voltage programmable through the UVLO/EN input. This feature prevents the power supply from entering a brownout condition in case the input voltage sags below its minimum value. This is important since switching power supplies increase their input supply current as the input voltage drops to keep the output power constant. In addition to this externally adjustable UVLO feature, the MAX15000 also offers a bootstrap UVLO with a large hysteresis (11.9V) and very low startup and operating current, which result in an efficient universal input power supply. The switching frequency of the MAX15000/MAX15001 is programmable with an external resistor.

The MAX15000 is well suited for universal input (rectified 85VAC to 265VAC) or telecom (-36VDC to -72VDC) power supplies. The MAX15001 is well suited for low-input voltage (9.5VDC to 24VDC) power supplies. The devices include an internal clamp at IN to prevent the input voltage from exceeding the absolute maximum rating (see Note 2 at the end of the *Electrical*

Characteristics table). The input is clamped when the devices are started with a bleed resistor (R1 in Figure 1) from a high input voltage and the UVLO/EN input is low. The clamp can safely sink up to 2mA current.

Power supplies designed with the MAX15000 use a high-value startup resistor R1 that charges a reservoir capacitor C1 (see Figure 1). During this initial period, while the voltage is less than the internal bootstrap UVLO threshold, the device typically consumes only 50 μ A of quiescent current. This low startup current and the large bootstrap UVLO hysteresis help to minimize the power dissipation across R1 even at the high end of the universal AC input voltage (265VAC).

The MAX15000/MAX15001 include a cycle-by-cycle current limit that turns off the gate drive to the external MOSFET whenever the internally set threshold of 1V is exceeded. When using the MAX15000 in the bootstrapped mode, if the power-supply output is shorted, the tertiary winding voltage will drop below the internally set threshold causing the UVLO to turn off the gate drive to the external power MOSFET. This will reinitiate a startup sequence with soft-start.

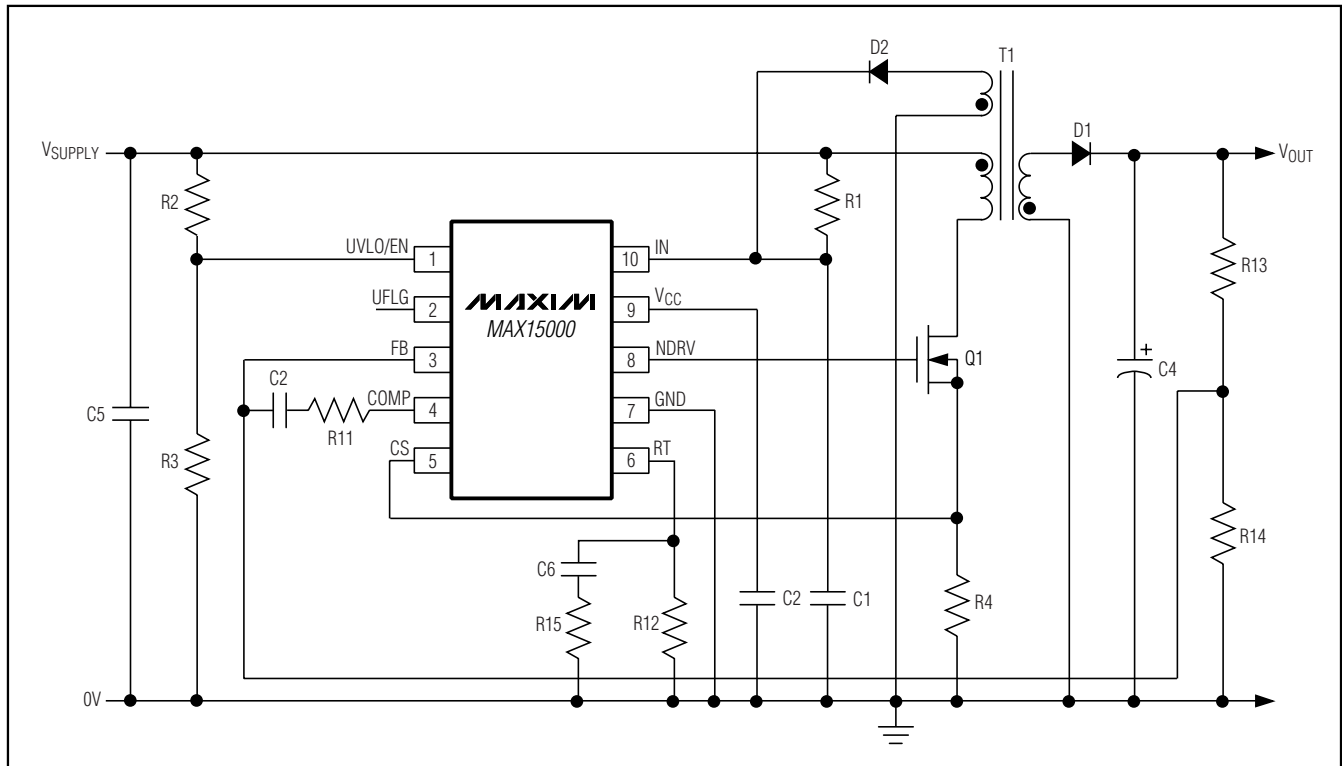


Figure 1. Nonisolated Power Supply with Programmable Input-Supply Start Voltage

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MAX15000/MAX15001

Current-Mode Control Loop

The advantages of current-mode control over voltage-mode control are twofold. First, there is the feed-forward characteristic brought on by the controller's ability to adjust for variations in the input voltage on a cycle-by-cycle basis. Secondly, the stability requirements of the current-mode controller are reduced to that of a single-pole system unlike the double pole in voltage-mode control.

The MAX15000/MAX15001 use a current-mode control loop where the output of the error amplifier (COMP) is compared to the current-sense voltage at CS. When the current-sense signal is lower than the noninverting input of the PWM comparator, the output of the CPWM comparator is low and the switch is turned on at each clock pulse. When the current-sense signal is higher than the inverting input of the CPWM, the output of the CPWM comparator goes high and the switch is turned off.

Undervoltage Lockout

The MAX15000/MAX15001 provide a UVLO/EN input. The threshold for UVLO is 1.23V with 60mV hysteresis. Before any operation can commence, the voltage on UVLO/EN has to exceed 1.23V. The UVLO circuit keeps the CPWM comparator, ILIM comparator, oscillator, and output driver shut down to reduce current consumption (see the *Functional Diagram*).

Use this UVLO/EN input to program the input-supply start voltage. For example, a reasonable start voltage for a 36V to 72V telecom range is usually 34V. Calculate the resistor-divider values, R2 and R3 (see Figure 1) by using the following formulas:

$$R3 = \frac{V_{ULR2} V_{IN}}{500I_{UVLO}(V_{IN} - V_{ULR2})}$$
$$R2 = \frac{V_{IN} - V_{ULR2}}{V_{ULR2}} R3$$

where I_{UVLO} is the UVLO/EN input current (50nA max), and V_{ULR2} is the UVLO/EN wake-up threshold (1.23V). V_{IN} is the value of the input-supply voltage where the power supply must start. The value of R3 is calculated to minimize the voltage-drop error across R2 as a result of the input bias current of the UVLO/EN input.

MAX15000 Bootstrap UVLO

In addition to the externally programmable UVLO function offered in both the MAX15000 and MAX15001, the MAX15000 includes an internal bootstrap UVLO that is very useful when designing high-voltage power supplies (see the *Functional Diagram*). This allows the device to bootstrap itself during initial power-up. The MAX15000 attempts to start when V_{IN} exceeds the bootstrap UVLO threshold of 21.6V. During startup, the UVLO circuit keeps the CPWM comparator, ILIM comparator, oscillator, and output driver shut down to reduce current consumption. Once V_{IN} reaches 21.6V, the UVLO circuit turns on the CPWM and ILIM comparators, the oscillator, and allows the output driver to switch. If V_{IN} drops below 1.17V, the UVLO circuit shuts down the CPWM comparator, ILIM comparator, oscillator, and output driver returning the MAX15000 to the low-current startup mode.

Startup Operation

The MAX15001 starts up when the voltage at IN exceeds 9.5V and the UVLO/EN input is greater than 1.23V. However, the MAX15000 requires that, in addition to meeting the specified startup conditions for the MAX15001, the voltage at IN exceeds the bootstrap UVLO threshold of 21.6V.

For the MAX15000, the voltage at IN is normally derived from a tertiary winding of the transformer. However, at startup there is no energy being delivered through the transformer, hence, a special bootstrap sequence is required. Figure 2 shows the voltages at IN and V_{CC} during startup. Initially, both V_{IN} and V_{CC} are 0V. After the line voltage is applied, C1 charges through the startup resistor, R1, to an intermediate voltage. At this point, the internal regulator begins charging C2 (see Figure 1). Only 50 μ A of the current supplied through R1 is used by the MAX15000, the remaining input current charges C1 and C2. The charging of C2 stops when the V_{CC} voltage reaches approximately 9.5V, while the voltage across C1 continues rising until it reaches the wake-up level of 21.6V. Once V_{IN} exceeds the bootstrap UVLO threshold, NDRV begins switching the MOSFET and transfers energy to the secondary and tertiary outputs. If the voltage on the tertiary output builds to higher than 9.74V (the bootstrap UVLO lower

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threshold), then startup has been accomplished and sustained operation will commence. If V_{IN} drops below 9.74V before startup is complete, the device goes back to low-current UVLO. In this case, increase the value of C1 to store enough energy to allow for the voltage at the tertiary winding to build up.

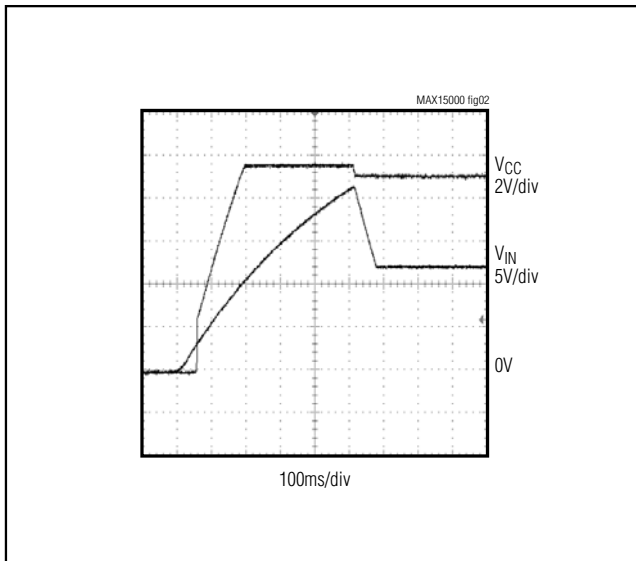


Figure 2. V_{IN} and V_{CC} During Startup When Using the MAX15000 in Bootstrapped Mode (Figure 1)

UVLO Flag (UFLG)

The MAX15000/MAX15001 have an open-drain under-voltage flag output (UFLG). When used with an optocoupler the UFLG output can serve to sequence a secondary-side controller. An internal 210 μ s delay occurs the instant the voltage on UVLO/EN drops below 1.17V until NDRV stops switching. This allows for the UFLG output to change state before the MAX15000/MAX15001 shut down (Figure 3).

When the voltage at the UVLO/EN is above the threshold, UFLG is high impedance. When UVLO/EN is below the threshold, UFLG goes low. UFLG is not affected by bootstrap UVLO (MAX15000).

Soft-Start

The MAX15000/MAX15001 soft-start feature allows the output voltage to ramp up in a controlled manner, eliminating voltage overshoot. The MAX15000/MAX15001 reference generator that is internally connected to the error amplifier soft-starts to achieve superior control of the output voltage under heavy and light load conditions. Soft-start begins after UVLO is deasserted (V_{IN} is above 21.6V for the MAX15000, V_{IN} is above 9.5V for the MAX15001, and the voltage on UVLO/EN is above 1.23V). The voltage applied to the noninverting node of the amplifier ramps from 0 to 1.23V in 1984 NDRV switching cycles. Use the following formula to calculate the soft-start time (t_{SS}):

$$t_{SS} = \frac{1984}{f_{NDRV}}$$

where f_{NDRV} is the switching frequency at the NDRV output. Figure 4 shows the soft-start regulated output of a power supply using the MAX15000 during startup.

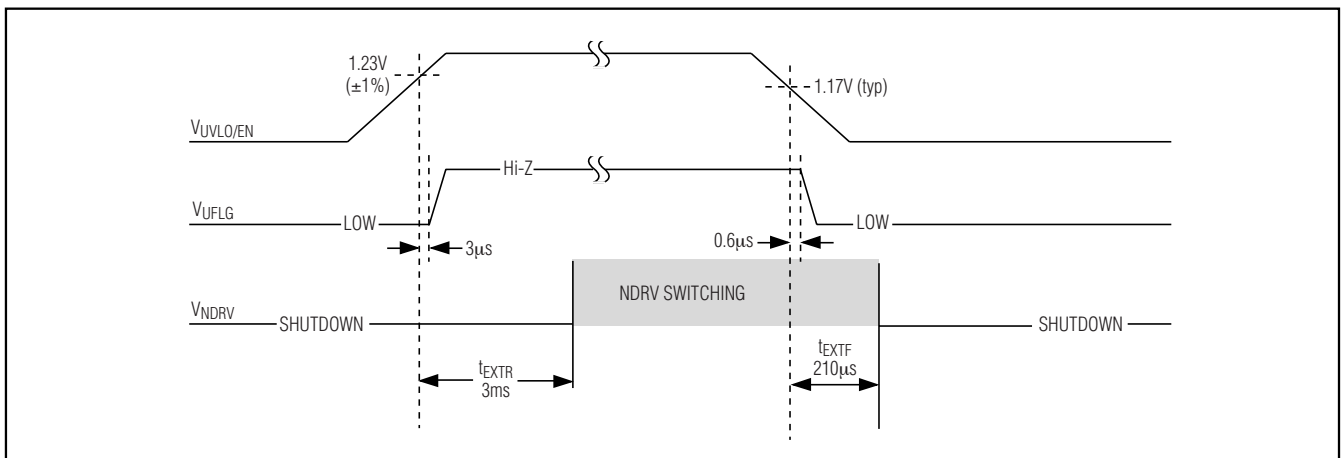


Figure 3. UVLO/EN and UFLG Operation Timing

Current-Mode PWM Controllers with Programmable Switching Frequency

n-Channel MOSFET Switch Driver

The NDRV output drives an external n-channel MOSFET. The internal regulator output (V_{CC}), set to approximately 9V, drives NDRV. For the universal input voltage range, the MOSFET used must withstand the DC level of the high-line input voltage plus the reflected voltage at the primary of the transformer. Most applications that use the discontinuous flyback topology require a MOSFET rated at 600V. NDRV can source/sink in excess of 650/1000mA peak current; therefore, select a MOSFET that will yield acceptable conduction and switching losses.

Oscillator/Switching Frequency

Use an external resistor at R_T to program the MAX15000/MAX15001 internal oscillator frequency between 50kHz and 2.5MHz. The MAX15000A/MAX15001A output switching frequency is one-half of the programmed oscillator frequency with a 50% duty cycle. The MAX15000B/MAX15001B output switching frequency is one-quarter of the programmed oscillator frequency with a 75% duty cycle.

The MAX15000A/MAX15001A and MAX15000B/MAX15001B have programmable output switching frequencies from 25kHz to 625kHz and 12.5kHz to 625kHz, respectively. Use the following formulas to determine the appropriate value of the resistor R_{12} (see Figure 1) needed to generate the desired output switching frequency (f_{SW}) at the NDRV output:

$$R_{12} = \frac{10^{10}}{2f_{SW}} \text{ for the MAX15000A/MAX15001A.}$$

$$R_{12} = \frac{10^{10}}{4f_{SW}} \text{ for the MAX15000B/MAX15001B.}$$

where R_{12} is the resistor connected from R_T to GND (see Figure 1).

Connect an RC network in parallel with R_{12} as shown in Figure 1. The RC network should consist of a 100nF capacitor C_6 (for stability) in series with resistor R_{15} which serves to further minimize jitter. Use the following formula to determine the value of R_{15} :

$$R_{15} = 88.9 \times (R_{12})^{\frac{1}{4}}$$

For example, if R_{12} is 4k Ω , R_{15} becomes 707 Ω .

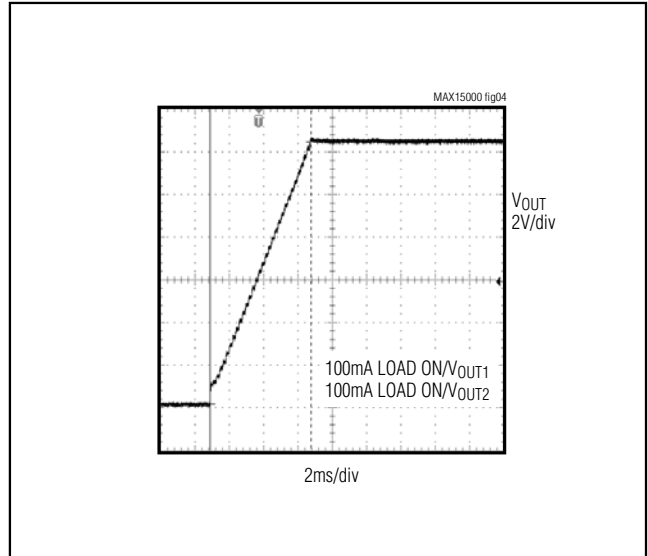


Figure 4. Primary-Side Output Voltage Soft-Start During Initial Startup for the Circuit in Figure 6

Internal Error Amplifier

The MAX15000/MAX15001 include an internal error amplifier to regulate the output voltage in the case of a nonisolated power supply (see Figure 1). For the circuit in Figure 1, calculate the output voltage using the following equation:

$$V_{OUT} = \left(1 + \frac{R_{13}}{R_{14}}\right) V_{REF}$$

where $V_{REF} = 1.23V$. The amplifier's noninverting input is internally connected to a digital soft-start circuit that gradually increases the reference voltage during start-up applied to this input. This forces the output voltage to come up in an orderly and well-defined manner under all load conditions.

The error amplifier may also be used to regulate the tertiary winding output which implements a primary-side-regulated, isolated power supply (see Figure 6). For the circuit in Figure 6, calculate the output voltage using the following equation:

$$V_{OUT} = \frac{N_S}{N_T} \left[\left(1 + \frac{R_1}{R_2}\right) V_{REF} + V_{D6} \right] - V_{D2}$$

where N_S is the number of secondary winding turns, N_T is the number of tertiary winding turns, and both V_{D6} and V_{D2} are the diode drops at the respective outputs.

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Current Limit

The current-sense resistor (R4 in Figure 1), connected between the source of the MOSFET and ground, sets the current limit. The current-limit comparator has a voltage trip level (V_{CS}) of 1V. Use the following equation to calculate the value of R4:

$$R4 = \frac{V_{CS}}{I_{PRI}}$$

where I_{PRI} is the peak current in the primary side of the transformer which also flows through the MOSFET. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (NDRV) terminates the current on-cycle within 60ns (typ). Use a small RC network to filter out the leading-edge spikes on the sensed waveform when needed. Set the corner frequency between 2MHz and 10MHz.

Applications Information

Startup Time Considerations for Power Supplies Using the MAX15000

The bypass capacitor at IN, C1, supplies current immediately after the MAX15000 wakes up (see Figure 1). The size of C1 and the connection configuration of the tertiary winding determine the number of cycles available for startup. Large values of C1 increase the startup time but also supply gate charge for more cycles during initial startup. If the value of C1 is too small, V_{IN} drops below 9.74V because NDRV does not have enough time to switch and build up sufficient voltage across the tertiary output which powers the device. The device goes back into UVLO and does not start. Use a low-leakage capacitor for C1 and C2.

Typically, offline power supplies keep startup times to less than 500ms even in low-line conditions (85VAC input for universal offline or 36VDC for telecom applications). Size the startup resistor, R1, to supply both the maximum startup bias of the device (90 μ A) and the charging current for C1 and C2. The bypass capacitor, C2, must charge to 9.5V and C1 to 24V, all within the desired time period of 500ms. Because of the internal soft-start time of the MAX15000 (approximately 5.6ms

when $f_{SW} = 350$ kHz), C1 must store enough charge to deliver current to the device for at least this much time. To calculate the approximate amount of capacitance required, use the following formula:

$$I_g = Q_{tot} f_{SW}$$

$$C1 = \frac{(I_{IN} + I_g)(t_{SS})}{V_{HYST}}$$

where I_{IN} is the MAX15000's internal supply current (2mA) after startup, Q_{tot} is the total gate charge for Q1, f_{SW} is the MAX15000's switching frequency (350kHz), V_{HYST} is the bootstrap UVLO hysteresis (approximately 12V) and t_{SS} is the internal soft-start time (5.6ms).

Example: $I_g = (8nC)(350kHz) \approx 2.8mA$

$$C1 = \frac{(2mA + 2.8mA)(5.6ms)}{12V} = 2.24\mu F$$

Choose a 2.2 μ F standard value (assuming 350kHz switching frequency).

Assuming $C1 > C2$, calculate the value of R1 as follows:

$$I_{C1} = \frac{V_{SUVR} C1}{(500ms)}$$

$$R1 \approx \frac{V_{IN(MIN)} - V_{SUVR}}{I_{C1} + I_{START}}$$

where $V_{IN(MIN)}$ is the minimum input supply voltage for the application (36V for telecom), V_{SUVR} is the bootstrap UVLO wake-up level (23.6V max), I_{START} is the IN supply current at startup (90 μ A max).

For example:

$$I_{C1} = \frac{(24V)(2.2\mu F)}{(500ms)} = 0.105mA$$

$$R1 \approx \frac{(36V) - (12V)}{(0.105mA) + (90\mu A)} = 123.07k\Omega$$

Choose a 120k Ω standard value.

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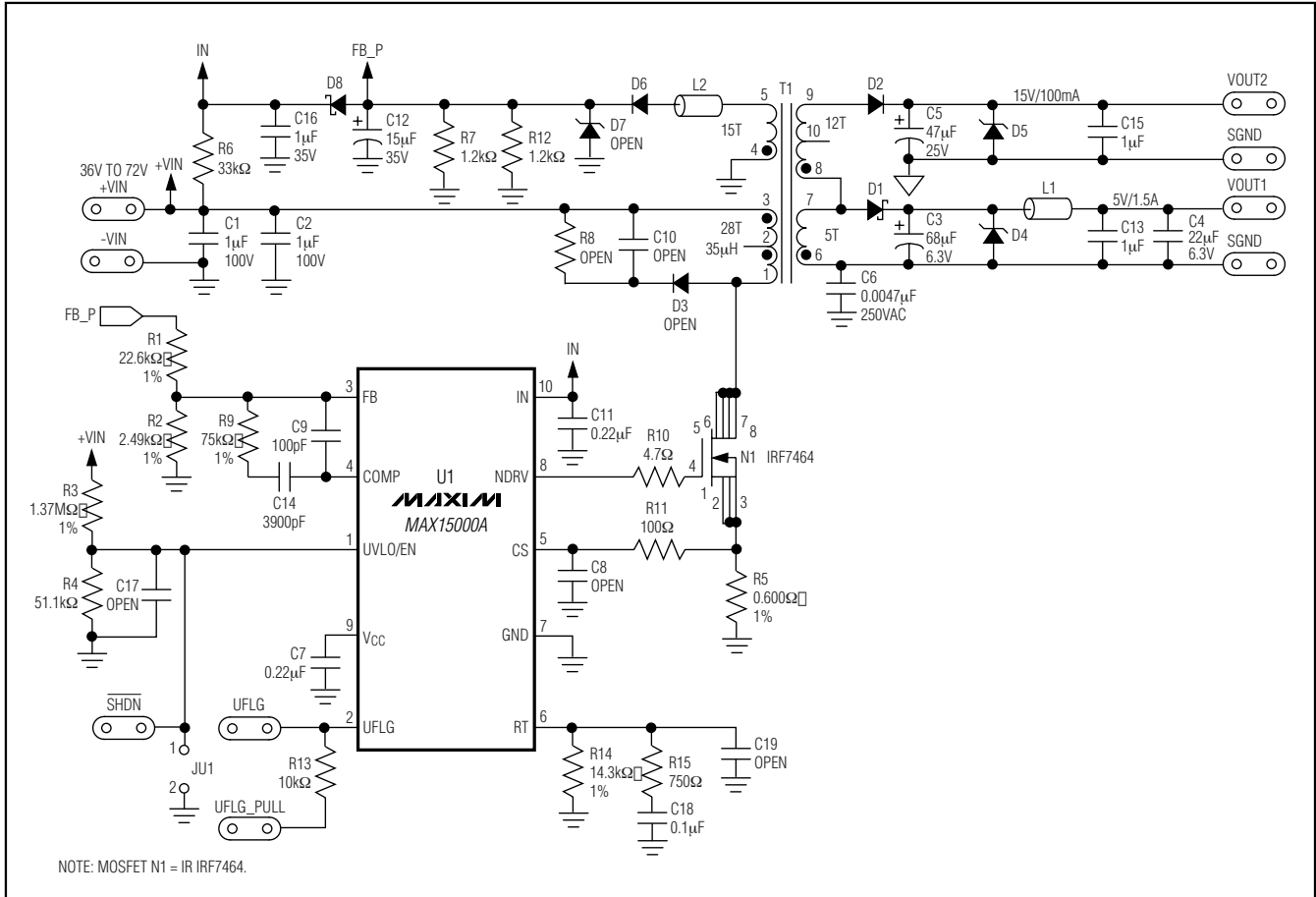


Figure 6. Primary-Side-Regulated, Dual-Output, Isolated Telecom Power Supply

Primary-Side-Regulated, Isolated Telecom Power Supply

Figure 6 shows a complete circuit of a dual-output power supply with a telecom voltage range of 36V to 72V. An important aspect of this power supply is that it is primary-side regulated. The regulation through the tertiary winding also supplies bias for the MAX15000.

In the circuit of Figure 6, cross-regulation has been improved (tertiary and 5V outputs) by using chip inductors, L1 and L2, and R7||R12 across C12. R7||R12 presents enough loading on the tertiary winding output to allow $\pm 10\%$ load regulation on the 5V output over a load current range from 150mA to 1.5A (Figure 7).

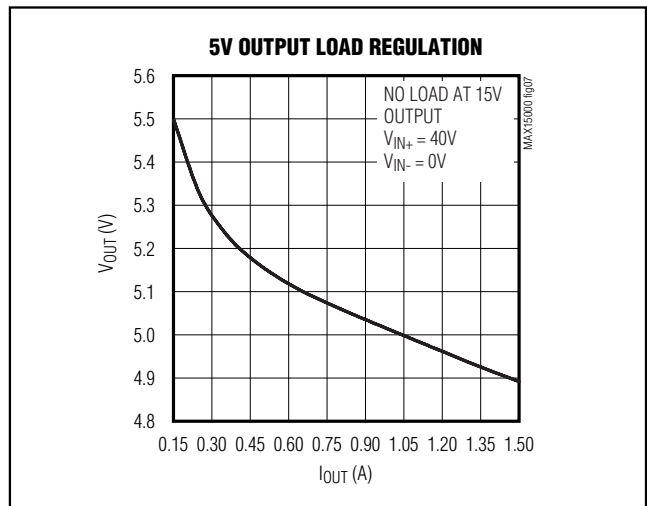


Figure 7. Output Voltage Regulation for the Circuit in Figure 6

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MAX15000/MAX15001

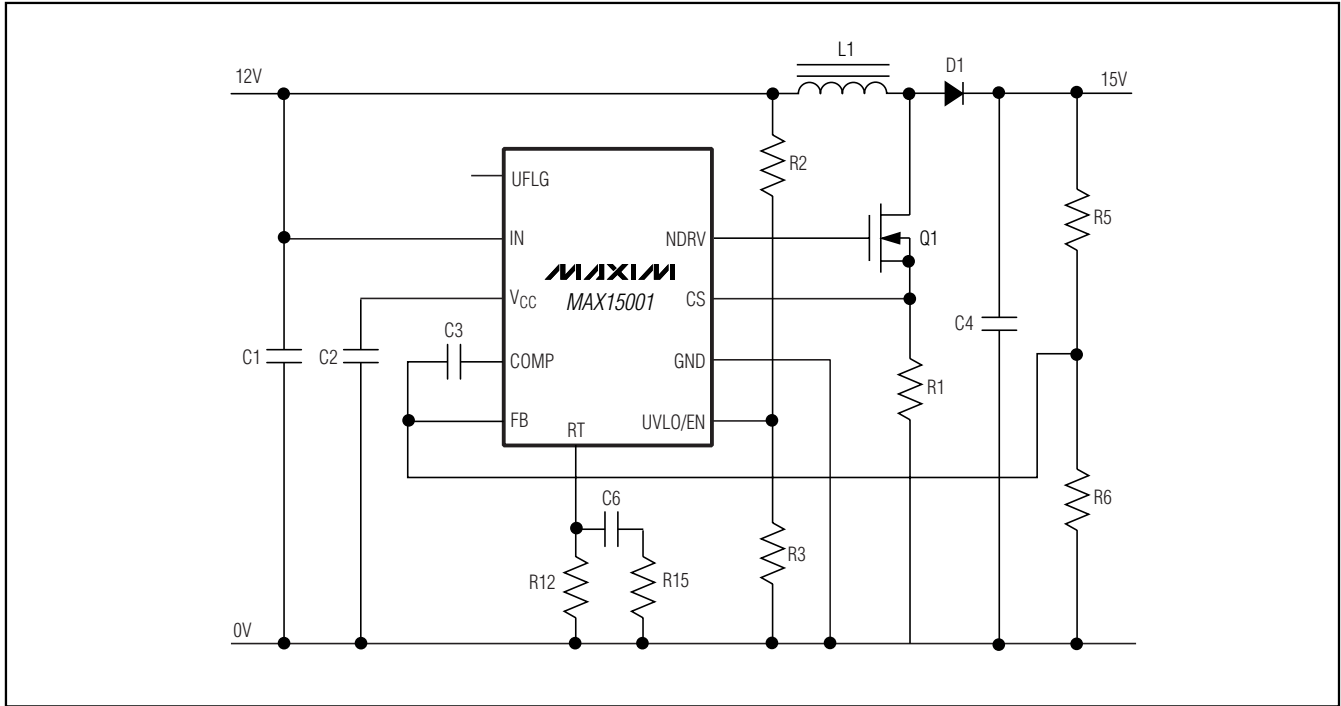


Figure 8. 12V to 15V Output Boost Regulator

Layout Recommendations

Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dv/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the MOSFET presents a dv/dt source; therefore, minimize the surface area of the heatsink as much as possible. Keep all PC board traces carrying switching currents as short as possible to minimize current loops.

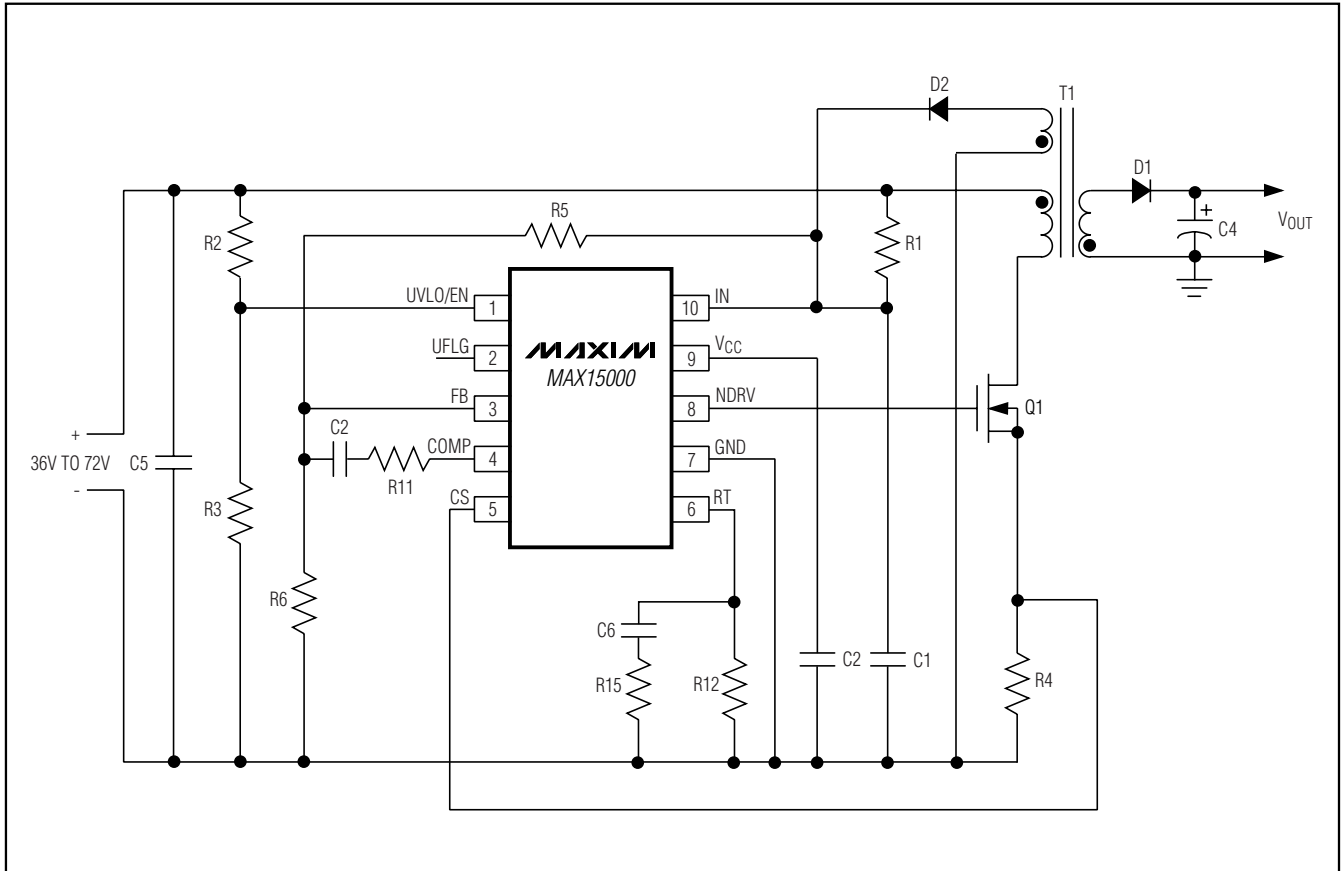
Use a ground plane for best results. The pins of the μ MAX package are positioned to allow easy interfacing to the external MOSFET.

For universal AC input design, follow all applicable safety regulations. Offline power supplies may require UL, VDE, and other similar agency approvals. To avoid noise coupling of signals from RT to NDRV, route traces from RT away from NDRV.

Current-Mode PWM Controllers with Programmable Switching Frequency

Typical Application Circuit

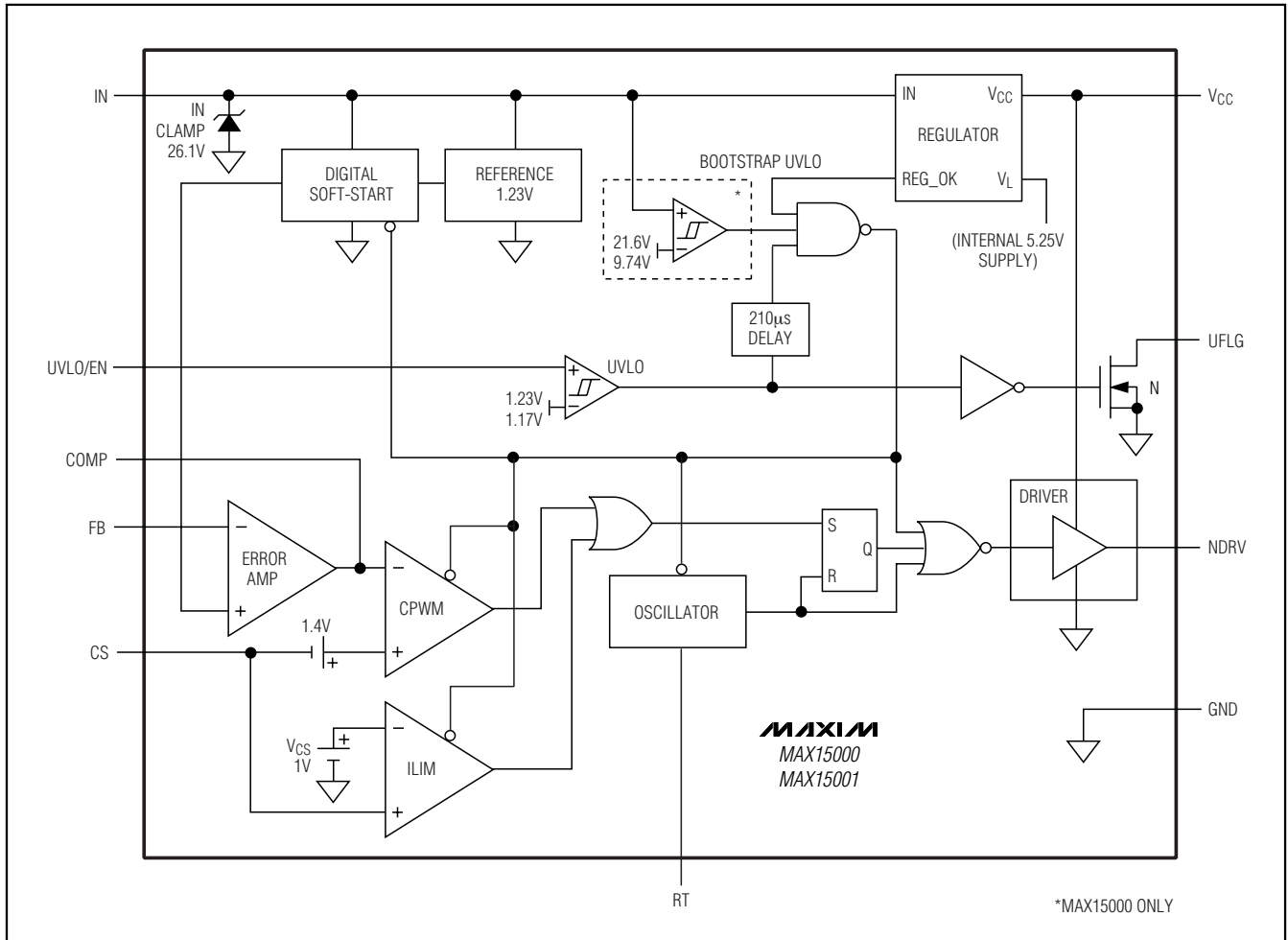
MAX15000/MAX15001



Current-Mode PWM Controllers with Programmable Switching Frequency

Functional Diagram

MAX15000/MAX15001



Selector Guide

PART	BOOTSTRAP UVLO	STARTUP VOLTAGE (V)	MAX DUTY CYCLE (%)
MAX15000A	Yes	22	50
MAX15000B	Yes	22	75
MAX15001A*	No	9.5	50
MAX15001B*	No	9.5	75

*The MAX15001 does not have an internal bootstrap UVLO. The MAX15001 starts operation as long as V_{IN} is higher than 9.5V and UVLO/EN is higher than 1.23V.

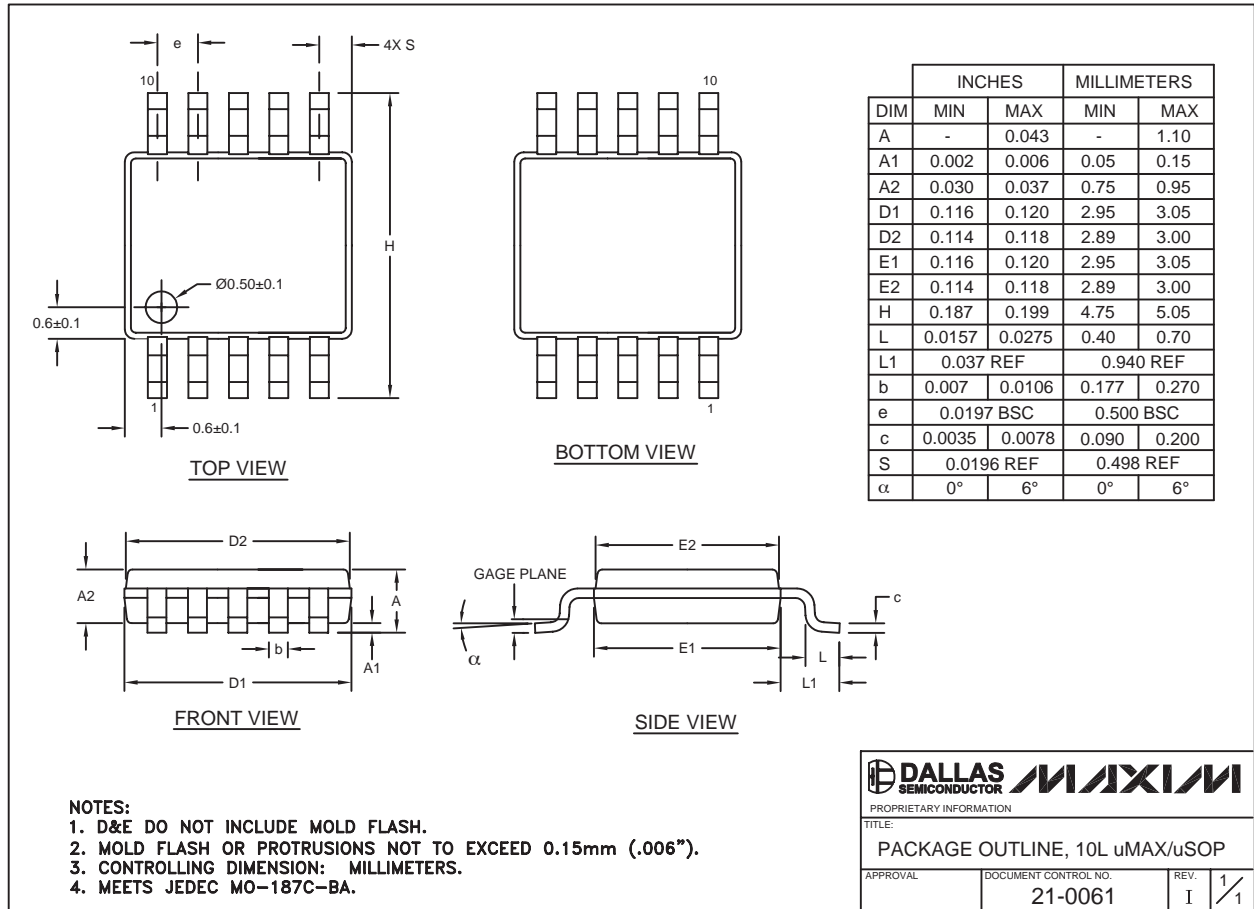
Chip Information

PROCESS: BiCMOS

Current-Mode PWM Controllers with Programmable Switching Frequency

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



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