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The LTC3880 data sheet is an essential reference document for this product.
To obtain it go to:

www.linear.com/LTC3880

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Terminal Voltages:

$V_{IN}n$ (Note 4), SV_{IN} ..... –0.3V to 28V
$V_{OUT}n$ ..... –0.3V to 6V
V_{OSNS0}^+, V_{ORB0}^+ ..... –0.3V to 4.25V
V_{OSNS1}, V_{ORB1}, $INTV_{CC}$, $I_{SNS}na^+$, $I_{SNS}nb^+$, $I_{SNS}na^-$, $I_{SNS}nb^-$ ..... –0.3V to 6V
RUN_n, SDA, SCL, $\overline{ALERT}$ ..... –0.3V to 5.5V
$F_{SWPHCFG}$, $V_{OUT}nCFG$, $V_{TRIM}nCFG$, ASEL .. –0.3V to 2.75V
V_{DD33}, $\overline{GPIO}_n$, SYNC, SHARE_CLK, WP, $TSNS_{na}$, $COMP_{na}$, $COMP_{nb}$, V_{OSNS0}^-, V_{ORB0}^- ..... –0.3V to 3.6V
SGND ..... –0.3V to 0.3V

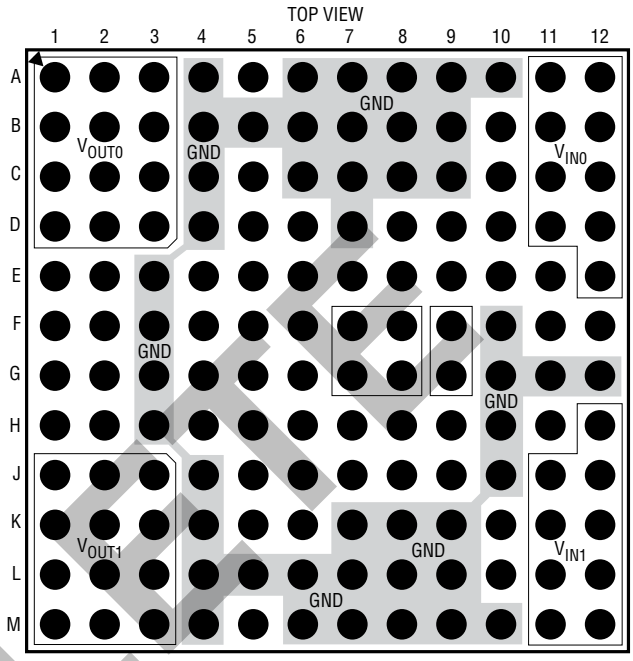
Terminal Currents

$INTV_{CC}$ Peak Output Current 100mA
V_{DD25} ..... –1.5mA to 1.5mA
$TSNS_{nb}$ ..... –1mA to 10mA

Temperatures

Internal Operating Temperature Range (Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Package Body Temperature During Reflow .. 245°C

PIN CONFIGURATION



BGA PACKAGE
144-LEAD (16mm × 16mm × 5.01mm)
T_{JMAX} = 125°C, θ_{JCtop} = 8.8°C/W, $\theta_{JCbottom}$ = 0.8°C/W, θ_{JB} = 1.3°C/W, θ_{JA} = 10.3°C/W
θ VALUES DETERMINED PER JESD51-12
WEIGHT = 3.3 GRAMS

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (See Note 2)
		DEVICE	FINISH CODE			
LTM4676EY#PBF	SAC305 (RoHS)	LTM4676Y	e1	BGA	4	–40°C to 125°C
LTM4676IY#PBF	SAC305 (RoHS)	LTM4676Y	e1	BGA	4	–40°C to 125°C
LTM4676IY	SnPb (63/37)	LTM4676Y	e0	BGA	4	–40°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 12V, RUN_n = 5V, FREQUENCY_SWITCH = 500kHz and V_{OUTn} commanded to 1.000V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage	Test Circuit 1 Test Circuit 2; VIN_OFF < VIN_ON = 4.25V	● ●	5.75 4.5		26.5 5.75	V V
V_{OUT0}	Range of Output Voltage Regulation, Channel 0	V_{OUT0} Differentially Sensed on V_{OSNS0}^+/V_{OSNS0}^- Pin-Pair; Commanded by Serial Bus or with Resistors Present at Start-Up on $V_{OUT0CFG}$ and/or $V_{TRIM0CFG}$	●	0.5		4.0	V
V_{OUT1}	Range of Output Voltage Regulation, Channel 1	V_{OUT1} Differentially Sensed on V_{OSNS1}/SGND Pin-Pair; Commanded by Serial Bus or with Resistors Present at Start-Up on $V_{OUT1CFG}$ and/or $V_{TRIM1CFG}$	●	0.5		5.4	V
$V_{OUTn(DC)}$	Output Voltage, Total Variation with Line and Load	Digital Servo Engaged (MFR_PWM_MODE$_n$[6] = 1_b) Digital Servo Disengaged (MFR_PWM_MODE$_n$[6] = 0_b) V_{OUTn} Commanded to 1.000V, V_{OUTn} Low Range (MFR_PWM_CONFIG[6-n] = 1_b), FREQUENCY_SWITCH = 250kHz (Note 5)	●	0.990 0.985	1.000 1.000	1.010 1.015	V V
Input Specifications							
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	Test Circuit 1, V_{OUTn} =1V, V_{IN} = 12V; No Load Besides Capacitors; TON_RISE_n = 3ms			400		mA
$I_{Q(SVIN)}$	Input Supply Bias Current	Forced Continuous Mode, MFR_PWM_MODE$_n$[1:0] = 10_b RUN_n = 5V, RUN_{1-n} = 0V Shutdown, RUN_0 = RUN_1 = 0V			 40 20		 mA mA
$I_{S(VINn,BURST)}$	Input Supply Current in Burst Mode® Operation	Burst Mode Operation, MFR_PWM_MODE$_n$[1:0] = 01_b, I_{OUTn} = 100mA			15		mA
$I_{S(VINn,PSM)}$	Input Supply Current in Pulse-Skipping Mode Operation	Pulse-Skipping Mode, MFR_PWM_MODE$_n$[1:0] = 00_b, I_{OUTn} = 100mA			20		mA
$I_{S(VINn,FCM)}$	Input Supply Current in Forced-Continuous Mode Operation	Forced Continuous Mode, MFR_PWM_MODE$_n$[1:0] = 10_b I_{OUTn} = 100mA I_{OUTn} = 13A			 40 1.37		 mA A
$I_{S(VINn,SHUTDOWN)}$	Input Supply Current in Shutdown	Shutdown, RUN_n = 0V			50		µA
Output Specifications							
I_{OUTn}	Output Continuous Current Range	(Note 6)		0		13	A
$\frac{\Delta V_{OUTn(LINE)}}{V_{OUTn}}$	Line Regulation Accuracy	Digital Servo Engaged (MFR_PWM_MODE$_n$[6] = 1_b) Digital Servo Disengaged (MFR_PWM_MODE$_n$[6] = 0_b) SV_{IN} and V_{INn} Electrically Shorted Together and $INTV_{CC}$ Open Circuit; I_{OUTn} = 0A, 5.75V ≤ V_{IN} ≤ 26.5V, V_{OUT} Low Range (MFR_PWM_CONFIG[6-n] = 1_b) FREQUENCY_SWITCH = 250kHz (Referenced to $12V_{IN}$) (Note 5)	 ●		0.03 0.03	 ±0.2	% %/V
$\frac{\Delta V_{OUTn(LOAD)}}{V_{OUTn}}$	Load Regulation Accuracy	Digital Servo Engaged (MFR_PWM_MODE$_n$[6] = 1_b) Digital Servo Disengaged (MFR_PWM_MODE$_n$[6] = 0_b) 0A ≤ I_{OUTn} ≤ 13A, V_{OUT} Low Range, (MFR_PWM_CONFIG[6-n] = 1_b) FREQUENCY_SWITCH = 250kHz (Note 5)	 ●		0.03 0.2	 0.5	% %
$V_{OUTn(AC)}$	Output Voltage Ripple				10		mV_{P-P}
f_S (Each Channel)	V_{OUTn} Ripple Frequency	FREQUENCY_SWITCH Set to 500kHz (0xFBE8)	●	462.5	500	537.5	kHz
$\Delta V_{OUTn(START)}$	Turn-On Overshoot	TON_RISE_n = 3ms (Note 12)			8		mV
t_{START}	Turn-On Start-Up Time	Time from V_{IN} Toggling from 0V to 12V to Rising Edge of $\overline{GPIO}_n$. TON_DELAY_n = 0ms, TON_RISE_n = 3ms, $MFR\_GPIO\_PROPAGATE_n$ = 0x0100, $MFR\_GPIO\_RESPONSE_n$ = 0x0000	●		153	170	ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 12V, RUN_n = 5V, FREQUENCY_SWITCH = 500kHz and V_{OUTn} commanded to 1.000V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{DELAY(0ms)}$	Turn-On Delay Time	Time from First Rising Edge of RUN_n to Rising Edge of $\overline{GPIO}_n$. TON_DELAY_n = 0ms, TON_RISE_n = 3ms, $MFR\_GPIO\_PROPAGATE_n$ = 0x0100, $MFR\_GPIO\_RESPONSE_n$ = 0x0000. V_{IN} Having Been Established for at Least 170ms	●	2.75	3.1	3.5	ms
$\Delta V_{OUTn(LS)}$	Peak Output Voltage Deviation for Dynamic Load Step	Load: 0A to 6.5A and 6.5A to 0A at 6.5A/µs, Figure 44 Circuit, V_{OUTn} = 1V, V_{IN} = 12V (Note 12)			50		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0A to 6.5A and 6.5A to 0A at 6.5A/µs, Figure 44 Circuit, V_{OUTn} = 1V, V_{IN} = 12V (Note 12)			35		µs
$I_{OUTn(OCL\_PK)}$	Output Current Limit, Peak	Cycle-by-Cycle Inductor Peak Current Limit Inception			22.5		A
$I_{OUTn(OCL\_AVG)}$	Output Current Limit, Time Averaged	Time-Averaged Output Inductor Current Limit Inception Threshold, Commanded by $IOUT\_OC\_FAULT\_LIMIT_n$ (Note 12)			15.6A; See $I_{O-RB-ACC}$ Specification (Output Current Readback Accuracy)		
Control Section							
V_{FBCM0}	Channel 0 Feedback Input Common Mode Range	V_{OSNS0^-} Valid Input Range (Referred to SGND) V_{OSNS0^+} Valid Input Range (Referred to SGND)	● ●	–0.1		0.3 4.25	V V
V_{FBCM1}	Channel 1 Feedback Input Common Mode Range	SGND Valid Input Range (Referred to GND) V_{OSNS1} Valid Input Range (Referred to SGND)	● ●	–0.3		0.3 5.5	V V
$V_{OUT0-RNG0}$	Channel 0 Full-Scale Command Voltage, Range 0	(Notes 7, 15) V_{OUT0} Commanded to 4.095V, $MFR\_PWM\_CONFIG[6] = 0_b$ Resolution LSB Step Size		4.015	 12 1.375	4.176	V Bits mV
$V_{OUT0-RNG1}$	Channel 0 Full-Scale Command Voltage, Range 1	(Notes 7, 15) V_{OUT0} Commanded to 2.750V, $MFR\_PWM\_CONFIG[6] = 1_b$ Resolution LSB Step Size		2.711	 12 0.6875	2.788	V Bits mV
$V_{OUT1-RNG0}$	Channel 1 Full-Scale Command Voltage, Range 0	(Notes 7, 15) V_{OUT1} Commanded to 5.500V, $MFR\_PWM\_CONFIG[5] = 0_b$ Resolution LSB Step Size		5.422	 12 1.375	5.576	V Bits mV
$V_{OUT1-RNG1}$	Channel 1 Full-Scale Command Voltage, Range 1	(Notes 7, 15) V_{OUT1} Commanded to 2.750V, $MFR\_PWM\_CONFIG[5] = 1_b$ Resolution LSB Step Size		2.711	 12 0.6875	2.788	V Bits mV
$R_{VSENSE0^+}$	V_{OSNS0^+} Impedance to SGND	$0.05V \le V_{VOSNS0^+} - V_{SGND} \le 4.1V$			41		kΩ
$R_{VSENSE1}$	V_{OSNS1} Impedance to SGND	$0.05V \le V_{VOSNS1} - V_{SGND} \le 5.5V$			37		kΩ
$t_{ON(MIN)}$	Minimum On-Time	(Note 8)			90		ns
Analog OV/UV (Overvoltage/Undervoltage) Output Voltage Supervisor Comparators (VOUT_OV/UV_FAULT_LIMIT and VOUT_OV/UV_WARN_LIMIT Monitors)							
N_{OV/UV_COMP}	Resolution, Output Voltage Supervisors, Channels 0 and 1	(Note 15)			8		Bits
VO_{OU-RNG}	Output Voltage Comparator Threshold Detection Range, Channel 0	(Note 15) High Range Scale, $MFR\_PWM\_CONFIG[6] = 0_b$ Low Range Scale, $MFR\_PWM\_CONFIG[6] = 1_b$		 1 0.5		 4.095 2.7	 V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). Specified as each individual output channel (Note 4). T_A = 25°C, V_{IN} = 12V, RUN_n = 5V, FREQUENCY_SWITCH = 500kHz and V_{OUTn} commanded to 1.000V unless otherwise noted. Configured with factory-default EEPROM settings and per Test Circuit 1, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V0_{OU-STP}$	Output Voltage Comparator Threshold Programming LSB Step Size, Channel 0	(Note 15) High Range Scale, MFR_PWM_CONFIG[6] = 0_b Low Range Scale, MFR_PWM_CONFIG[6] = 1_b			22 11		mV mV
$V0_{OU-ACC}$	Output Voltage Comparator Threshold Accuracy, Channel 0	(See Note 14) 2V ≤ $V_{VOSNS0}^+ - V_{VOSNS0}^-$ ≤ 4.095V, MFR_PWM_CONFIG[6] = 0_b 1V ≤ $V_{VOSNS0}^+ - V_{VOSNS0}^-$ ≤ 2.7V, MFR_PWM_CONFIG[6] = 1_b 0.5V ≤ $V_{VOSNS0}^+ - V_{VOSNS0}^-$ < 1V, MFR_PWM_CONFIG[6] = 1_b	 ● ● ●			 ±2 ±2 ±20	 % % mV
$V1_{OU-RNG}$	Output Voltage Comparator Threshold Detection Range, Channel 1	(Note 15) High Range Scale, MFR_PWM_CONFIG[5] = 0_b Low Range Scale, MFR_PWM_CONFIG[5] = 1_b		 1 0.5		 5.5 2.7	 V V
$V1_{OU-STP}$	Output Voltage Comparator Threshold Programming LSB Step Size, Channel 1	(Note 15) High Range Scale, MFR_PWM_CONFIG[5] = 0_b Low Range Scale, MFR_PWM_CONFIG[5] = 1_b			22 11		mV mV
$V1_{OU-ACC}$	Output Voltage Comparator Threshold Accuracy, Channel 1	(See Note 14) 2V ≤ $V_{VOSNS1} - V_{SGND}$ ≤ 5.5V, MFR_PWM_CONFIG[5] = 0_b 1.5V ≤ $V_{VOSNS1} - V_{SGND}$ ≤ 2.7V, MFR_PWM_CONFIG[5] = 1_b 0.5V ≤ $V_{VOSNS1} - V_{SGND}$ < 1.5V, MFR_PWM_CONFIG[5] = 1_b	 ● ● ●			 ±2 ±2 ±30	 % % mV
$t_{PROP-OV}$	Output OV Comparator Response Times, Channels 0 and 1	Overdrive to 10% Above Programmed Threshold				35	µs
$t_{PROP-UV}$	Output UV Comparator Response Times, Channels 0 and 1	Underdrive to 10% Below Programmed Threshold				50	µs
Analog OV/UV SV_{IN} Input Voltage Supervisor Comparators (Threshold Detectors for VIN_ON and VIN_OFF)							
$N_{SVIN-OV/UV-COMP}$	SV_{IN} OV/UV Comparator Threshold-Programming Resolution	(Note 15)			8		Bits
$SV_{IN-OU-RANGE}$	SV_{IN} OV/UV Comparator Threshold-Programming Range		●	4.5		20	V
$SV_{IN-OU-STP}$	SV_{IN} OV/UV Comparator Threshold-Programming LSB Step Size	(Note 15)			82		mV
$SV_{IN-OU-ACC}$	SV_{IN} OV/UV Comparator Threshold Accuracy	9V < SV_{IN} ≤ 20V 4.5V ≤ SV_{IN} ≤ 9V	● ●			±2.5 ±225	% mV
$t_{PROP-SVIN-HIGH-VIN}$	SV_{IN} OV/UV Comparator Response Time, High V_{IN} Operating Configuration	Test Circuit 1, and: VIN_ON = 9V; SV_{IN} Driven from 8.775V to 9.225V VIN_OFF = 9V; SV_{IN} Driven from 9.225V to 8.775V	 ● ●			 35 35	 µs µs
$t_{PROP-SVIN-LOW-VIN}$	SV_{IN} OV/UV Comparator Response Time, Low V_{IN} Operating Configuration	Test Circuit 2, and: VIN_ON = 4.5V; SV_{IN} Driven from 4.225V to 4.725V VIN_OFF = 4.5V; SV_{IN} Driven from 4.725V to 4.225V	 ● ●			 35 35	 µs µs
Channels 0 and 1 Output Voltage Readback ($READ\_VOUT_n$)							
N_{VO-RB}	Output Voltage Readback Resolution and LSB Step Size	(Note 15)			16 244		Bits µV
$V_{O-F/S}$	Output Voltage Full-Scale Digitizable Range	V_{RUNn} = 0V (Notes 7, 15)			8		V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{O-RB-ACC}$	Output Voltage Readback Accuracy	Channel 0: 0.6V ≤ $V_{VOSNS0}^+ - V_{VOSNS0}^-$ ≤ 4V Channel 1: 0.6V ≤ $V_{VOSNS1} - V_{SGND}$ ≤ 5.4V	● ●		Within ±1% of Reading Within ±1% of Reading		
$t_{CONVERT-VO-RB}$	Output Voltage Readback Update Rate	(Notes 9, 15)			100		ms
Input Voltage (SV_{IN}) Readback (READ_VIN)							
$N_{SVIN-RB}$	Input Voltage Readback Resolution and LSB Step Size	(Notes 10, 15)			10 15.625		Bits mV
$SV_{IN-F/S}$	Input Voltage Full-Scale Digitizable Range	(Notes 11, 15)			38.91		V
$SV_{IN-RB-ACC}$	Input Voltage Readback Accuracy	READ_VIN, 4.5V ≤ SV_{IN} ≤ 26.5V	●		Within ±2% of Reading		
$t_{CONVERT-SVIN-RB}$	Input Voltage Readback Update Rate	(Notes 9, 15)			100		ms
Channels 0 and 1 Output Current (READ_IOUT$_n$), Duty Cycle (READ_DUTY_CYCLE$_n$), and Computed Input Current (MFR_READ_IIN$_n$) Readback							
N_{IO-RB}	Output Current Readback Resolution and LSB Step Size	(Notes 10, 12)			10 15.6		Bits mA
$I_{O-F/S}$, $I_{I-F/S}$	Output Current Full-Scale Digitizable Range and Input Current Range of Calculation	(Note 12)			±40		A
$I_{O-RB-ACC}$	Output Current, Readback Accuracy	READ_IOUT$_n$, Channels 0 and 1, 0 ≤ I_{OUTn} ≤ 10A, Forced-Continuous Mode, MFR_PWM_MODE$_n$[1:0] = 10_b	●		Within 250mA of Reading		
$I_{O-RB(13A)}$	Full Load Output Current Readback	I_{OUTn} = 13A (Note 12). See Histograms in Typical Performance Characteristics			13.1		A
N_{II-RB}	Computed Input Current, Readback Resolution and LSB Step Size	(Notes 10, 12)			10 1.95		Bits mA
$I_{I-RB-ACC}$	Computed Input Current, Readback Accuracy, Neglecting I_{SVIN}	MFR_READ_IIN$_n$, Channels 0 and 1, 0 ≤ I_{OUTn} ≤ 10A, Forced-Continuous Mode, MFR_PWM_MODE$_n$[1:0] = 10_b, MFR_IIN_OFFSET$_n$ = 0mA	●		Within 150mA of Reading		
$t_{CONVERT-IO-RB}$	Output Current Readback Update Rate	(Notes 9, 15)			100		ms
$t_{CONVERT-II-RB}$	Computed Input Current, Readback Update Rate	(Notes 9, 15)			100		ms
$N_{DUTY-RB}$	Resolution, Duty Cycle Readback	(Notes 10, 15)			10		Bits
D_{RB-ACC}	Duty Cycle TUE	READ_DUTY_CYCLE$_n$, 16.3% Duty Cycle (Note 15)				±3	%
$t_{CONVERT-DUTY-RB}$	Duty Cycle Readback Update Rate	(Notes 9, 15)			100		ms
Temperature Readback for Channel 0, Channel 1, and Controller (Respectively: READ_TEMPERATURE_1$_0$, READ_TEMPERATURE_1$_1$, and READ_TEMPERATURE_2)							
T_{RES-RB}	Temperature Readback Resolution	Channel 0, Channel 1, and Controller (Note 15)			0.0625		°C
$T_{RB-CH-ACC(72mV)}$	Channel Temperature TUE, Switching Action Off	Channels 0 and 1, PWM Inactive, RUN_n = 0V, ΔV_{TSNSna} = 72mV	●		Within ±3°C of Reading		
$T_{RB-CH-ACC(ON)}$	Channel Temperature TUE, Switching Action On	READ_TEMPERATURE_1$_n$, Channels 0 and 1, PWM Active, RUN_n = 5V (Note 12)			Within ±3°C of Reading		

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$T_{RB-CTRL-ACC(ON)}$	Control IC Die Temperature TUE, Switching Action On	READ_TEMPERATURE_2, PWM Active, RUN_0 = RUN_1 = 5V (Note 12)			Within ±1°C of Reading		
$t_{CONVERT-TEMP-RB}$	Temperature Readback Update Rate	(Notes 9, 15)			100		ms
$INTV_{CC}$ Regulator							
V_{INTVCC}	Internal V_{CC} Voltage No Load	6V ≤ V_{IN} ≤ 26.5V	●	4.8	5	5.2	V
$\frac{\Delta V_{INTVCC(LOAD)}}{V_{INTVCC}}$	$INTV_{CC}$ Load Regulation	0mA ≤ I_{INTVCC} ≤ 50mA			0.5	±2	%
V_{DD33} Regulator							
V_{VDD33}	Internal V_{DD33} Voltage		●	3.2	3.3	3.4	V
$I_{LIM(VDD33)}$	V_{DD33} Current Limit	V_{DD33} Electrically Short-Circuited to GND			70		mA
V_{VDD33_OV}	V_{DD33} Overvoltage Threshold	(Note 15)			3.5		V
V_{VDD33_UV}	V_{DD33} Undervoltage Threshold	(Note 15)			3.1		V
V_{DD25} Regulator							
V_{VDD25}	Internal V_{DD25} Voltage		●	2.25	2.5	2.75	V
$I_{LIM(VDD25)}$	V_{DD25} Current Limit	V_{DD25} Electrically Short-Circuited to GND			50		mA
Oscillator and Phase-Locked Loop (PLL)							
f_{OSC}	Oscillator Frequency Accuracy	FREQUENCY_SWITCH = 500kHz (0xFBE8) 250kHz ≤ FREQUENCY_SWITCH ≤ 1MHz (Note 15)	●			±7.5 ±7.5	% %
f_{SYNC}	PLL SYNC Capture Range	FREQUENCY_SWITCH Set to Frequency Slave Mode (0x0000); SYNC Driven by External Clock; 3.3V_{OUT}	●	225		1100	kHz
$V_{TH,SYNC}$	SYNC Input Threshold	V_{SYNC} Rising (Note 15) V_{SYNC} Falling (Note 15)			1.5 1		V V
$V_{OL,SYNC}$	SYNC Low Output Voltage	I_{SYNC} = 3mA	●		0.3	0.4	V
I_{SYNC}	SYNC Leakage Current in Frequency Slave Mode	0V ≤ V_{SYNC} ≤ 3.6V FREQUENCY_SWITCH Set to Slave Mode (0x0000)	●			±5	µA
θ_{SYNC}-θ0	SYNC-to-Channel 0 Phase Relationship, Lag from Falling Edge of Sync to Rising Edge of Top MOSFET (MT0) Gate	(Note 15) MFR_PWM_CONFIG[2:0] = 000_b, $01X_b$ MFR_PWM_CONFIG[2:0] = 101_b MFR_PWM_CONFIG[2:0] = 001_b MFR_PWM_CONFIG[2:0] = $1X0_b$			 0 60 90 120		 Deg Deg Deg Deg
θ_{SYNC}-θ1	SYNC-to-Channel 1 Phase Relationship, Lag from Falling Edge of Sync to Rising Edge of Top MOSFET (MT1) Gate	(Note 15) MFR_PWM_CONFIG[2:0] = 011_b MFR_PWM_CONFIG[2:0] = 000_b MFR_PWM_CONFIG[2:0] = 010_b, $10X_b$ MFR_PWM_CONFIG[2:0] = 001_b MFR_PWM_CONFIG[2:0] = 110_b			 120 180 240 270 300		 Deg Deg Deg Deg Deg
EEPROM Characteristics							
Endurance	(Note 13)	0°C ≤ T_J ≤ 85°C During EEPROM Write Operations (Note 3)	●	10,000			Cycles
Retention	(Note 13)	T_J < $T_{J(MAX)}$, with Most Recent EEPROM Write Operation Having Occurred at 0°C ≤ T_J ≤ 85°C (Note 3)	●	10			Years
Mass_Write	Mass Write Operation Time	Execution of STORE_USER_ALL Command, 0°C ≤ T_J ≤ 85°C (ATE-Tested at T_J = 25°C) (Notes 3, 13)			440	4100	ms
Digital I/Os							

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Input High Threshold Voltage	SCL, SDA, RUN_n, $\overline{GPIO}_n$ (Note 15) SHARE_CLK, WP (Note 15)		2.0 1.8			V V
V_{IL}	Input Low Threshold Voltage	SCL, SDA, RUN_n, $\overline{GPIO}_n$ (Note 15) SHARE_CLK, WP (Note 15)				1.4 0.6	V V
V_{HYST}	Input Hysteresis	SCL, SDA (Note 15)			80		mV
V_{OL}	Output Low Voltage	SCL, SDA, $\overline{ALERT}$, RUN_n, $\overline{GPIO}_n$, SHARE_CLK: I_{SINK} = 3mA	●		0.3	0.4	V
I_{OL}	Input Leakage Current	SDA, SCL, $\overline{ALERT}$, RUN_n: 0V ≤ V_{PIN} ≤ 5.5V $\overline{GPIO}_n$ and SHARE_CLK: 0V ≤ V_{PIN} ≤ 3.6V	● ●			±5 ±2	µA µA
t_{FILTER}	Input Digital Filtering	RUN_n (Note 15) $\overline{GPIO}_n$ (Note 15)			10 3		µs µs
C_{PIN}	Input Capacitance	SCL, SDA, RUN_n, $\overline{GPIO}_n$, SHARE_CLK, WP (Note 15)				10	pF
PMBus Interface Timing Characteristics							
f_{SMB}	Serial Bus Operating Frequency	(Note 15)		10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start	(Note 15)		1.3			µs
$t_{HD,STA}$	Hold Time After Repeated Start Condition	Time Period After Which First Clock Is Generated (Note 15)		0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time	(Note 15)		0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time	(Note 15)		0.6			µs
$t_{HD,DAT}$	Data Hold Time	Receiving Data (Note 15) Transmitting Data (Note 15)		0 0.3		 0.9	µs µs
$t_{SU,DAT}$	Data Setup Time	Receiving Data (Note 15)		0.1			µs
$t_{TIMEOUT\_SMB}$	Stuck PMBus Timer Timeout	Measured from the Last PMBus Start Event: Block Reads (Note 15) Non-Block Reads (Note 15)			 150 32		 ms ms
t_{LOW}	Serial Clock Low Period	(Note 15)		1.3		10000	µs
t_{HIGH}	Serial Clock High Period	(Note 15)		0.6			µs

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listing under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating conditions for extended periods may affect device reliability and lifetime.

Note 2: The LTM4676 is tested under pulsed-load conditions such that $T_J \approx T_A$. The LTM4676E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4676I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The LTM4676's EEPROM temperature range for valid write commands is 0°C to 85°C. To achieve guaranteed EEPROM data retention, execution of the "STORE_USER_ALL" command—i.e., uploading RAM contents to NVM—outside this temperature range is not recommended. However, as long as the LTM4676's EEPROM temperature is less than 130°C, the LTM4676 *will* obey the STORE_USER_ALL command. Only when EEPROM temperature exceeds 130°C, the LTM4676 will not act on any STORE_USER_ALL transactions: instead, the LTM4676 NACKs the serial command and asserts its relevant CML (communications, memory, logic) fault bits. EEPROM temperature can be queried prior to commanding STORE_USER_ALL; see the Applications Information section.

Note 4: The two power inputs—V_{IN0} and V_{IN1}—and their respective power outputs—V_{OUT0} and V_{OUT1}—are tested independently in production. A shorthand notation is used in this document that allows these parameters to be referred to by "V_{INn}" and "V_{OUTn}", where *n* is permitted to take on a value of 0 or 1. This italicized, subscripted "*n*" notation and convention is extended to encompass all such pin names, as well as register names with channel-specific, i.e., paged data. For example, VOUT_COMMAND$_n$ refers to the VOUT_COMMAND command code data located in Pages 0 and 1, which in turn relate to Channels 0 (V_{OUT0}) and Channel 1 (V_{OUT1}). Registers containing non-page-specific data, i.e., whose data is "global" to the module or applies to both of the module's Channels lack the italicized, subscripted "*n*", e.g., FREQUENCY_SWITCH.

Note 5: $V_{OUTn(DC)}$ and line and load regulation tests are performed in production with digital servo disengaged (MFR_PWM_MODE$_n$[6] = 0_b) and low V_{OUTn} range selected (MFR_PWM_CONFIG[6-*n*] = 1_b. The digital servo control loop is exercised in production (setting MFR_PWM_MODE$_n$[6] = 1_b), but convergence of the output voltage to its final settling value is not necessarily observed in final test—due to potentially long time constants involved—and is instead guaranteed by the output voltage readback accuracy specification. Evaluation in application demonstrates capability; see the Typical Performance Characteristics section.

Note 6: See output current derating curves for different V_{IN}, V_{OUT}, and T_A, located in the Applications Information section.

Note 7: Even though V_{OUT0} and V_{OUT1} and their associated current-sensing pins ($I_{SNSn[a/b][+/–]}$) are specified for 6V absolute maximum and recommended for not more than 5.5V continuous, the maximum recommended command voltage to regulate output channels 0 and 1 is: 4.0V and 5.4V, respectively, when the V_{OUT} range setting for those channels—MFR_PWM_CONFIG's bits 6 and 5, respectively—are set to "high range", i.e., 0_b; and 2.5V for any channel whose respective MFR_PWM_CONFIG V_{OUT} range-setting bit is set to "low range", i.e., 1_b.

Note 8: Minimum on-time is tested at wafer sort.

Note 9: Data conversion is performed in round-robin (cyclic) fashion. All telemetry signals are continuously digitized, and reported data is based on measurements not older than 100ms, typical.

Note 10: The following telemetry parameters are formatted in PMBus-defined "Linear Data Format", in which each register contains a word comprised of 5 most significant bits—representing a signed exponent, to be raised to the power of 2—and 11 least significant bits—representing a signed mantissa: input voltage (on SV_{IN}), accessed via the READ_VIN command code; output currents (I_{OUTn}), accessed via the READ_IOUT$_n$ command codes; module input current ($I_{VIN0} + I_{VIN1} + I_{SVIN}$), accessed via the READ_IIN command code; channel input currents ($I_{VINn} + 1/2 \bullet I_{SVIN}$), accessed via the MFR_READ_IIN$_n$ command codes;and duty cycles of channel 0 and channel 1 switching power stages, accessed via the READ_DUTY_CYCLE$_n$ command codes. This data format limits the resolution of telemetry readback data to 10 bits even though the internal ADC is 16 bits and the LTM4676's internal calculations use 32-bit words.

Note 11: The absolute maximum rating for the SV_{IN} pin is 28V. Input voltage telemetry (READ_VIN) is obtained by digitizing a voltage scaled down from the SV_{IN} pin.

Note 12: These typical parameters are based on bench measurements and are not production tested.

Note 13: EEPROM endurance and retention are guaranteed by wafer-level testing for data retention. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification, and whose EEPROM data was written to at $0°C \le T_J \le 85°C$. Downloading NVM contents to RAM by executing the MFR_RESET command is valid over the entire operating temperature range and does not influence EEPROM characteristics.

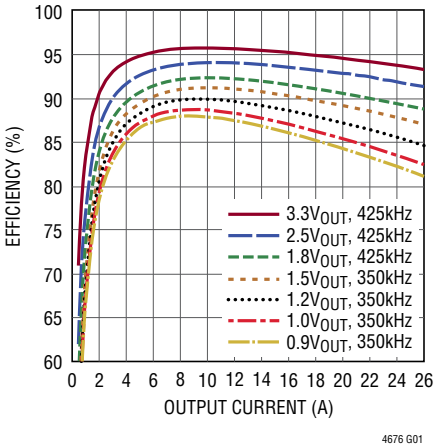
Note 14: $V0_{OU-ACC}$ OV/UV comparator threshold accuracy for MFR_PWM_CONFIG[6] = 1_b tested in ATE at $V_{VOSNS0}^+ - V_{VOSNS0}^-$ = 0.5V and 2.7V. 1V condition tested at IC-Level, only. $V1_{OU-ACC}$ OV/UV comparator threshold accuracy for MFR_PWM_CONFIG[5] = 1_b tested in ATE with V_{VOSNS1}-V_{SGND} = 0.5V and 2.7V. 1.5V condition tested at IC-level, only.

Note 15: Tested at IC-level ATE.

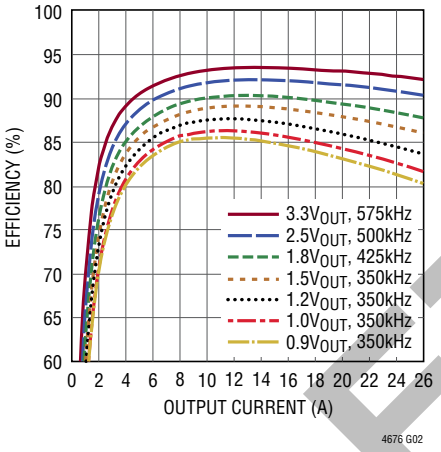
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, 12V_{IN} to 1V_{OUT}, unless otherwise noted.

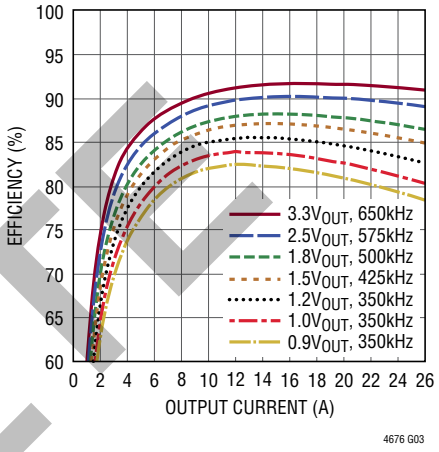
Efficiency vs Output Current, 5V_{IN}, V_{OUT0} and V_{OUT1} Paralleled, V_{IN} = SV_{IN} = V_{INn} = $INTV_{CC}$, $MFR\_PWM\_MODE_n$[1:0] = 10_b



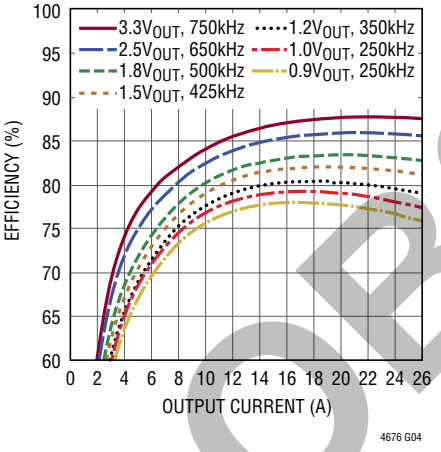
Efficiency vs Output Current, 8V_{IN}, V_{OUT0} and V_{OUT1} Paralleled, V_{IN} = SV_{IN} = V_{INn}, $INTV_{CC}$ Open, $MFR\_PWM\_MODE_n$[1:0] = 10_b



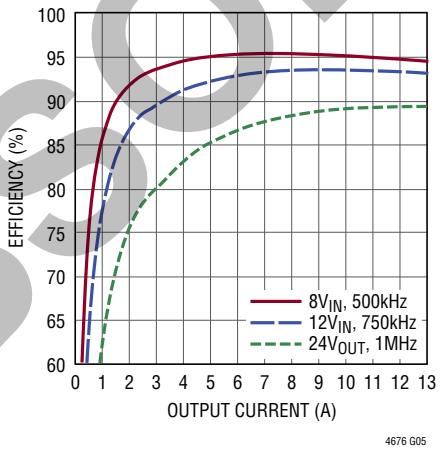
Efficiency vs Output Current, 12V_{IN}, V_{OUT0} and V_{OUT1} Paralleled, V_{IN} = SV_{IN} = V_{INn}, $INTV_{CC}$ Open, $MFR\_PWM\_MODE_n$[1:0] = 10_b



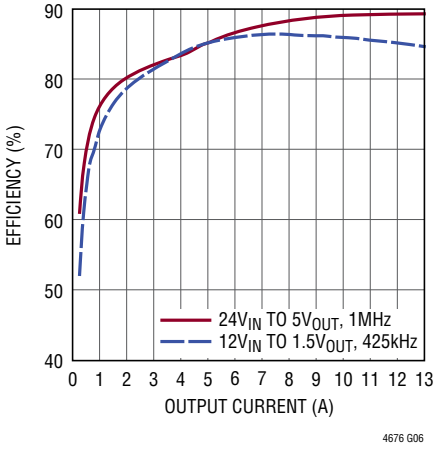
Efficiency vs Output Current, 24V_{IN}, V_{OUT0} and V_{OUT1} Paralleled, V_{IN} = SV_{IN} = V_{INn}, $INTV_{CC}$ Open, $MFR\_PWM\_MODE_n$[1:0] = 10_b



Efficiency vs Output Current, V_{OUT1} = 5V, V_{OUT0} = OFF, V_{IN} = SV_{IN} = V_{INn}, $INTV_{CC}$ Open, $MFR\_PWM\_MODE_n$[1:0] = 10_b



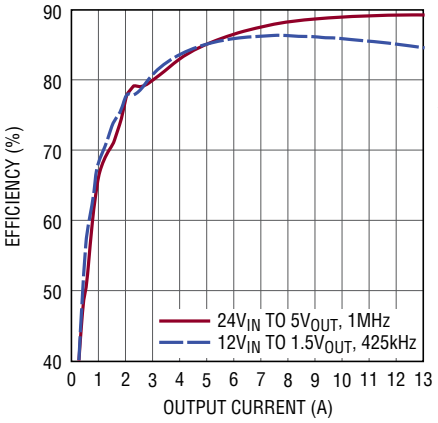
Single Phase Single Output Burst Mode Efficiency, V_{IN} = SV_{IN} = V_{INn}, $INTV_{CC}$ Open, $MFR\_PWM\_MODE_n$[1:0] = 01_b



TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $12V_{IN}$ to $1V_{OUT}$, unless otherwise noted.

Single Phase Single Output Pulse-Skipping (Discontinuous) Mode Efficiency, $V_{IN} = SV_{IN} = V_{INn}$, $INTV_{CC}$ Open, $MFR\_PWM\_MODE_n[1:0] = 00_b$



Dual Phase Single Output Load Transient Response, $12V_{IN}$ to $1V_{OUT}$

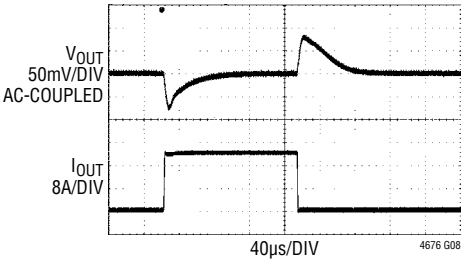


FIGURE 35 CIRCUIT AT $12V_{IN}$, $INTV_{CC}$ PIN OPEN CIRCUIT AND $VOUT\_COMMAND_n$ SET TO 1.000V. 0A TO 20A LOAD STEP AT 20A/µs

Single Phase Single Output Load Transient Response, $12V_{IN}$ to $1V_{OUT}$

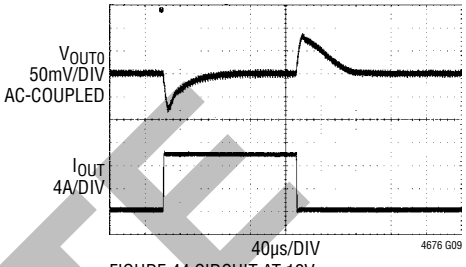


FIGURE 44 CIRCUIT AT $12V_{IN}$ 0A TO 10A LOAD STEP AT 10A/µs

Dual Phase Single Output Load Transient Response, $5V_{IN}$ to $1V_{OUT}$

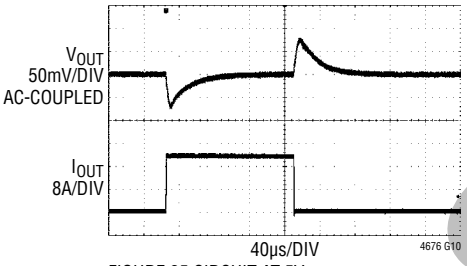


FIGURE 35 CIRCUIT AT $5V_{IN}$, $VOUT\_COMMAND_n$ SET TO 1.000V. 0A TO 20A LOAD STEP AT 20A/µs

Single Phase Single Output Load Transient Response, $24V_{IN}$ to $1V_{OUT}$

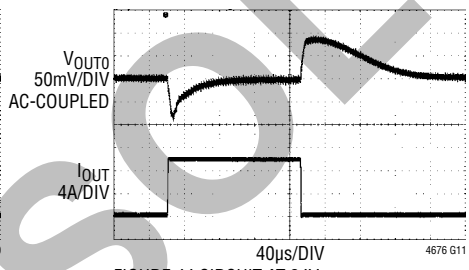


FIGURE 44 CIRCUIT AT $24V_{IN}$ 0A TO 10A LOAD STEP AT 10A/µs

Single Phase Single Output Load Transient Response, $24V_{IN}$ to $3.3V_{OUT}$

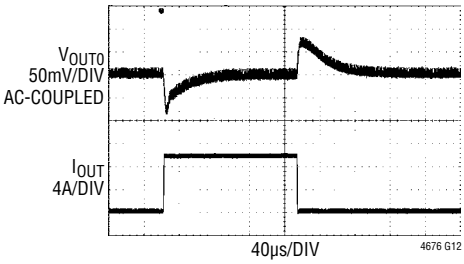


FIGURE 44 CIRCUIT AT $24V_{IN}$, C_{OUT0} = 5× 100µF AND V_{OUT0} COMMANDED TO 3.300V. 0A TO 10A LOAD STEP AT 10A/µs

Dual Output Concurrent Rail Start-Up/Shutdown

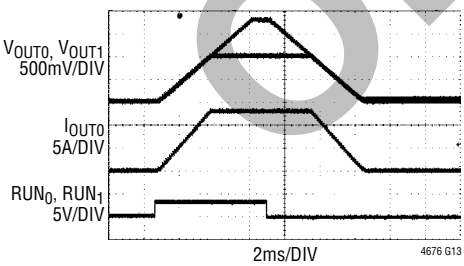


FIGURE 44 CIRCUIT AT $12V_{IN}$, 77mΩ LOAD ON V_{OUT0}, NO LOAD ON V_{OUT1}. TON_RISE_0 = 3ms, TON_RISE_1 = 5.297ms, $TOFF\_DELAY_1$ = 0ms, $TOFF\_DELAY_0$ = 2.43ms, $TOFF\_FALL_1$ = 5.328ms, $TOFF\_FALL_0$ = 3ms, $ON\_OFF\_CONFIG_n$ = 0x1E

Dual Output Start-Up/Shutdown with a Pre-Biased Load

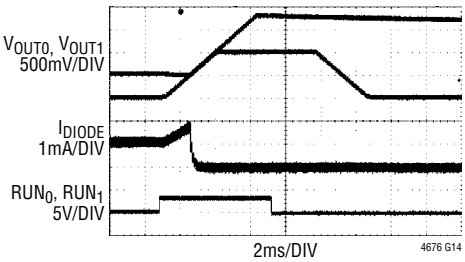


FIGURE 44 CIRCUIT AT $12V_{IN}$, 77mΩ LOAD ON V_{OUT0}, 500Ω ON V_{OUT1}. V_{OUT1} PRE-BIASED THROUGH A DIODE. TON_RISE_0 = 3ms, TON_RISE_1 = 5.297ms, $TOFF\_DELAY_1$ = 0ms, $TOFF\_DELAY_0$ = 2.43ms, $TOFF\_FALL_1$ = 5.328ms, $TOFF\_FALL_0$ = 3ms, $ON\_OFF\_CONFIG_1$ = 0x1F $ON\_OFF\_CONFIG_0$ = 0x1E

Single Phase Single Output Short-Circuit Protection at No Load

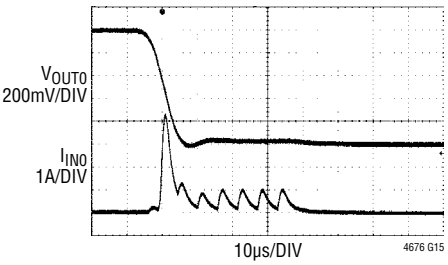


FIGURE 44 CIRCUIT AT $12V_{IN}$, NO LOAD ON V_{OUT0} PRIOR TO APPLICATION OF SHORT CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, 12V_{IN} to 1V_{OUT}, unless otherwise noted.

Single Phase Single Output Short-Circuit Protection at Full Load

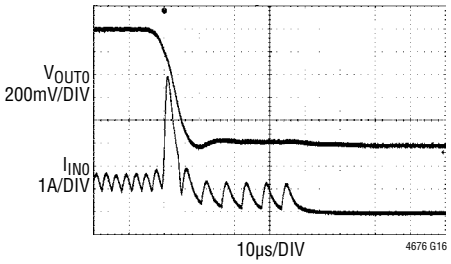
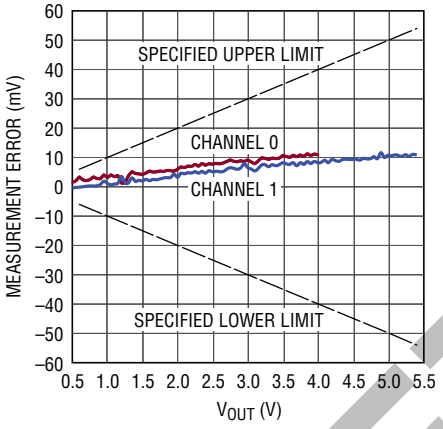
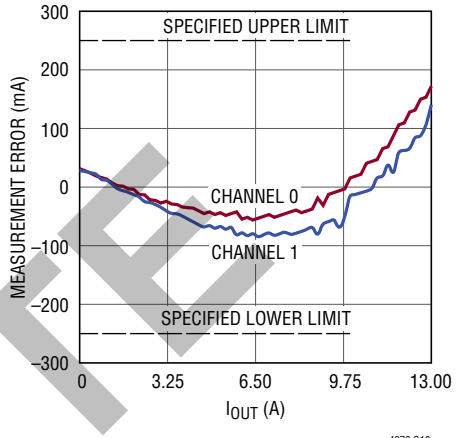


FIGURE 44 CIRCUIT AT 12V_{IN}, 77mΩ LOAD ON V_{OUT0} PRIOR TO APPLICATION OF SHORT CIRCUIT

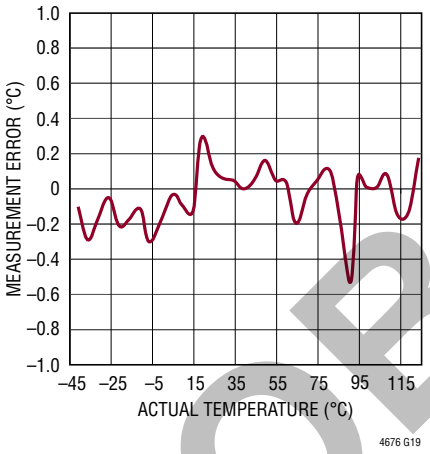
READ_VOUT$_n$ (Output Voltage Readback) Error vs V_{OUTn} I_{OUTn} = No Load, RUN_{1-n} = 0V



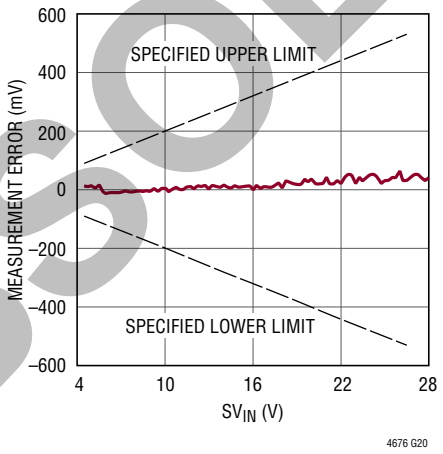
READ_IOUT$_n$ (Output Current Readback) Error vs I_{OUTn}



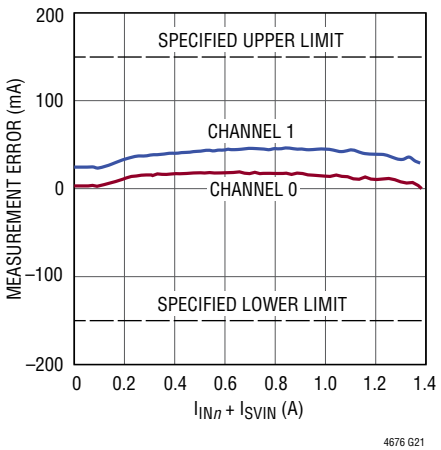
READ_TEMPERATURE_2 (Control IC Temperature Error) vs Junction Temperature, RUN_n = 0V



READ_VIN (Input Voltage Readback Telemetry) Error vs SV_{IN}, RUN_n = 0V



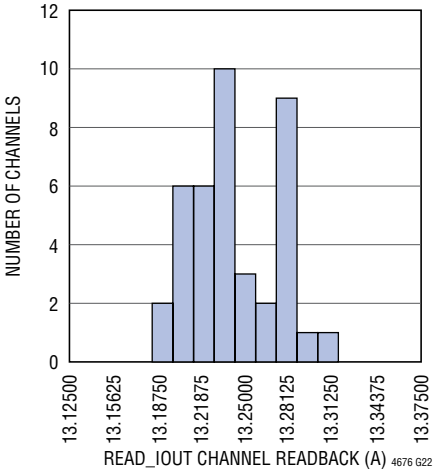
MFR_READ_IIN$_n$ (Input Current Readback) Error vs (I_{VINn} + I_{SVIN}), MFR_PWM_MODE$_n$[1:0]=10_b, I_{OUTn} Swept from 0A to 13A, One Channel at a Time, RUN_{1-n} = 0V



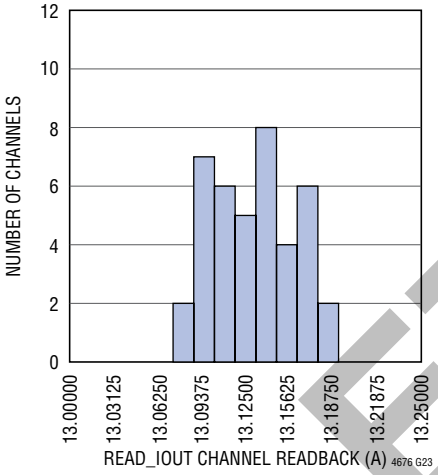
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, 12V_{IN} to 1V_{OUT}, unless otherwise noted.

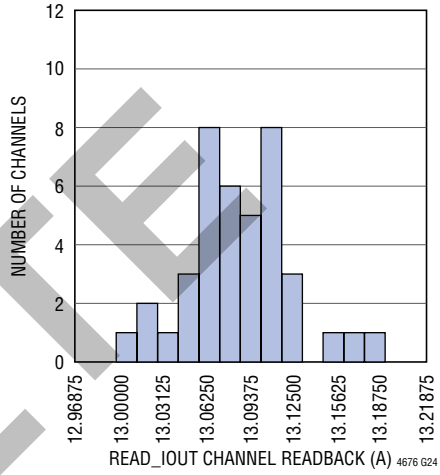
READ_OUT of 20 LTM4676s (DC1811A) 12V_{IN}, 1V_{OUT}, T_J = –40°C, I_{OUTn} = 13A, System Having Reached Thermally Steady-State Condition, No Airflow



READ_OUT of 20 LTM4676s (DC1811A) 12V_{IN}, 1V_{OUT}, T_J = 25°C, I_{OUTn} = 13A, System Having Reached Thermally Steady-State Condition, No Airflow



READ_OUT of 20 LTM4676s (DC1811A) 12V_{IN}, 1V_{OUT}, T_J = 125°C, I_{OUTn} = 13A, System Having Reached Thermally Steady-State Condition, No Airflow



PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

GND (A4, A6-10, B4-B9, C4, C6-C9, D4, D7, E3, F3, F10, G3, G10-12, H3, H10, J4, J10, K4, K7-9, L4-9, M4, M6-10): Power Ground of the LTM4676. Power return for V_{OUT0} and V_{OUT1}.

V_{OUT0} (A1-3, B1-3, C1-3, D1-3): Channel 0 Output Voltage.

V_{OSNS0}^+ (D9): Channel 0 Positive Differential Voltage Sense Input. Together, V_{OSNS0}^+ and V_{OSNS0}^- serve to kelvin-sense the V_{OUT0} output voltage at V_{OUT0}'s point of load (POL) and provide the differential feedback signal directly to Channel 0's control loop and voltage supervisor circuits. V_{OUT0} can regulate up to 4.0V output. Command V_{OUT0}'s target regulation voltage by serial bus. Its initial command value at SV_{IN} power-up is dictated by NVM (non-volatile memory) contents (factory default: 1.000V)—or, optionally, may be set by configuration resistors; see $V_{OUT0CFG}$, $V_{TRIM0CFG}$ and the Applications Information section.

V_{OSNS0}^- (E9): Channel 0 Negative Differential Voltage Sense Input. See V_{OSNS0}^+.

V_{ORB0}^+ (D10): Channel 0 Positive Readback Pin. Shorted to V_{OSNS0}^+ internal to the LTM4676. If desired, place a test point on this node and measure its impedance to V_{OUT0} on one's hardware (e.g., motherboard, during in circuit test (ICT) post-assembly process) to provide a means of verifying the integrity of the feedback signal connection between V_{OSNS0}^+ and V_{OUT0}.

V_{ORB0}^- (E10): Channel 0 Negative Readback Pin. Shorted to V_{OSNS0}^- internal to the LTM4676. If desired, place a test point on this node and measure its impedance to GND on one's hardware (e.g., motherboard, during ICT post-assembly process) to provide a means of verifying the integrity of the feedback signal connection between V_{OSNS0}^- and GND (V_{OUT0} power return).

V_{OUT1} (J1-3, K1-3, L1-3, M1-3): Channel 1 Output Voltage.

V_{OSNS1} (H9): Channel 1 Positive Voltage Sense Input. Connect V_{OSNS1} to V_{OUT1} at the POL. This provides the feedback signal for channel 1's control loop and voltage supervisor circuits. V_{OUT1} can regulate up to 5.4V output. Command V_{OUT1}'s target regulation voltage by serial bus. Its initial command value at SV_{IN} power-up is dictated by NVM (non-volatile memory) contents (factory default:

PIN FUNCTIONS

1.000V)—or, optionally, may be set by configuration resistors; see $V_{OUT1CFG}$, $V_{TRIM1CFG}$ and the Applications Information section.

SGND (F7-8, G7-8): Channel 1 Negative Voltage Sense Input. See V_{OSNS1}. Additionally, SGND is the signal ground return path of the LTM4676. If desired, one may place a test point on one of the four SGND pins and measure its impedance to GND on one's hardware (e.g., motherboard, during ICT post-assembly process) to provide a means of verifying the integrity of the feedback signal connection between the other three SGND pins and GND (V_{OUT1} power return). SGND is not electrically connected to GND internal to the LTM4676. Connect SGND to GND local to the LTM4676.

V_{ORB1} (J9): Channel 1 Positive Readback Pin. Shorted to V_{OSNS1} internal to the LTM4676. At one's option, place a test point on this node and measure its impedance to V_{OUT1} on one's hardware (e.g., motherboard, during ICT post-assembly process) to provide a means of verifying the integrity of the feedback signal connection between V_{OUT1} and V_{OSNS1}.

V_{IN0} (A11-12, B11-12, C11-12, D11-12, E12): Positive Power Input to Channel 0 Switching Stage. Provide sufficient decoupling capacitance in the form of multilayer ceramic capacitors (MLCCs) and low ESR electrolytic (or equivalent) to handle reflected input current ripple from the step-down switching stage. MLCCs should be placed as close to the LTM4676 as physically possible. See Layout Recommendations in the Applications Information section.

V_{IN1} (H12, J11-12, K11-12, L11-12, M11-12): Positive Power Input to Channel 1 Switching Stage. Provide sufficient decoupling capacitance in the form of MLCCs and low ESR electrolytic (or equivalent) to handle reflected input current ripple from the step-down switching stage. MLCCs should be placed as close to the LTM4676 as physically possible. See Layout Recommendations in the Applications Information section.

SW_0 (B10): Switching Node of Channel 0 Step-Down Converter Stage. Used for test purposes or EMI-snubbing heavier than that supported by $SNUB_0$. May be routed a short distance to a local test point to monitor switching action of Channel 0, if desired, but do not route near any sensitive signals; otherwise, leave electrically isolated (open).

SW_1 (L10): Switching Node of Channel 1 Step-Down Converter Stage. Used for test purposes or EMI-snubbing heavier than that supported by $SNUB_1$. May be routed a short distance to a local test point to monitor switching action of Channel 1, if desired, but do not route near any sensitive signals; otherwise, leave open.

$SNUB_0$ (A5): Access to Channel 0 Switching Stage Snubber Capacitor. Connecting an optional resistor from $SNUB_0$ to GND can reduce radiated EMI, with only a minor penalty towards power conversion efficiency. See the Applications Information section. Pin should otherwise be left open.

$SNUB_1$ (M5): Access to Channel 1 Switching Stage Snubber Capacitor. Connecting an optional resistor from $SNUB_0$ to GND can reduce radiated EMI, with only a minor penalty towards power conversion efficiency. See the Applications Information section. Pin should otherwise be left open.

SV_{IN} (F11-12): Input Supply for LTM4676's Internal Control IC. In most applications, SV_{IN} connects to V_{IN0} and/or V_{IN1}, in which case no external decoupling beyond that already allocated for V_{IN0}/V_{IN1} is required. If SV_{IN} is operated from an auxiliary supply separate from V_{IN0}/V_{IN1}, decouple this pin to GND with a capacitor (0.1µF to 1µF).

$INTV_{CC}$ (F9, G9): Internal Regulator, 5V Output. When operating the LTM4676 from $5.75V \le SV_{IN} \le 26.5V$, an LDO generates $INTV_{CC}$ from SV_{IN} to bias internal control circuits and the MOSFET drivers of the LTM4676. No external decoupling is required. $INTV_{CC}$ is regulated regardless of the RUN_n pin state. When operating the LTM4676 with $4.5V \le SV_{IN} < 5.75V$, $INTV_{CC}$ *must* be electrically shorted to SV_{IN}.

V_{DD33} (J7): Internally Generated 3.3V Power Supply Output Pin. This pin should only be used to provide external current for the pull-up resistors required for $\overline{GPIO}_n$, SHARE_CLK, and SYNC, and may be used to provide external current for pull-up resistors on RUN_n, SDA, SCL and $\overline{ALERT}$. No external decoupling is required.

PIN FUNCTIONS

V_{DD25} (J6): Internally Generated 2.5V Power Supply Output Pin. Do not load this pin with external current; it is used strictly to bias internal logic and provides current for the internal pull-up resistors connected to the configuration-programming pins. No external decoupling is required.

ASEL (G4): Serial Bus Address Configuration Pin. On any given I^2C/SMBus serial bus segment, every device must have its own unique slave address. If this pin is left open, the LTM4676 powers up to its default slave address of 0x4F (hexadecimal), i.e., 1001111_b (industry standard convention is used throughout this document: 7-bit slave addressing). The lower four bits of the LTM4676's slave address can be altered from this default value by connecting a resistor from this pin to SGND—hence configuring the 7-bit slave address of the LTM4676 to one of 16 supported values. Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state.

$F_{SWPHCFG}$ (H4): Switching Frequency, Channel Phase-Interleaving Angle and Phase Relationship to SYNC Configuration Pin. If this pin is left open—or, if the LTM4676 is configured to ignore pin-strap (RCONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1_b—then the LTM4676's switching frequency (FREQUENCY_SWITCH) and channel phase relationships (with respect to the SYNC clock; MFR_PWM_CONFIG[2:0]) are dictated at SV_{IN} power-up according to the LTM4676's NVM contents. Default factory values are: 500kHz operation; Channel 0 at 0°; and Channel 1 at 180°C (convention throughout this document: a phase angle of 0° means the channel's switch node rises coincident with the falling edge of the SYNC pulse). Connecting a resistor from this pin to SGND (and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0_b) allows a convenient way to configure multiple LTM4676s with identical NVM contents for different switching frequencies of operation and phase interleaving angle settings of intra- and extra-module-paralleled channels—all, without GUI intervention or the need to "custom pre-program" module NVM contents. (See the Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state.

$V_{OUT0CFG}$ (G5): Output Voltage Select Pin for V_{OUT0}, Coarse Setting. If the $V_{OUT0CFG}$ and $V_{TRIM0CFG}$ pins are both left open—or, if the LTM4676 is configured to ignore pin-strap (RCONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1_b—then the LTM4676's target V_{OUT0} output voltage setting ($VOUT\_COMMAND_0$) and associated power-good and OV/UV warning and fault thresholds are dictated at SV_{IN} power-up according to the LTM4676's NVM contents. A resistor connected from this pin to SGND—in combination with resistor pin settings on $V_{TRIM0CFG}$, and using the factory-default NVM setting of MFR_CONFIG_ALL[6] = 0_b—can be used to configure the LTM4676's Channel 0 output to power-up to a VOUT_COMMAND value (and associated output voltage monitoring and protection/fault-detection thresholds) different from those of NVM contents. (See the Applications Information section.) Connecting resistor(s) from $V_{OUT0CFG}$ to SGND and/or $V_{TRIM0CFG}$ to SGND in this manner allows a convenient way to configure multiple LTM4676s with identical NVM contents for different output voltage settings—all without GUI intervention or the need to "custom-pre-program" module NVM contents. Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of RCONFIGs on $V_{OUT0CFG}$/$V_{TRIM0CFG}$ can affect the V_{OUT0} range setting (MFR_PWM_CONFIG[6]) and loop gain.

$V_{TRIM0CFG}$ (H5): Output Voltage Select Pin for V_{OUT0}, Fine Setting. Works in combination with $V_{OUT0CFG}$ to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 0, at SV_{IN} power-up. (See $V_{OUT0CFG}$ and the Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of RCONFIGs on $V_{OUT0CFG}$/$V_{TRIM0CFG}$ can affect the V_{OUT0} range setting (MFR_PWM_CONFIG[6]) and loop gain.

$V_{OUT1CFG}$ (G6): Output Voltage Select Pin for V_{OUT1}, Coarse Setting. If the $V_{OUT1CFG}$ and $V_{TRIM1CFG}$ pins are both left open—or, if the LTM4676 is configured to ignore pin-strap (RCONFIG) resistors, i.e., MFR_CONFIG_ALL[6] = 1_b—then the LTM4676's target V_{OUT1} output voltage setting ($VOUT\_COMMAND_1$) and associated power good and OV/UV warning and fault thresholds are dictated at SV_{IN} power-up according to the LTM4676's NVM contents, in precisely the same fashion that the $V_{OUT0CFG}$ and $V_{TRIM0CFG}$ pins affect the respective settings of V_{OUT0}/Channel 0. (See $V_{OUT0CFG}$, $V_{TRIM0CFG}$ and the Applications Information

PIN FUNCTIONS

section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of RCONFIGs on $V_{OUT1CFG}$/$V_{TRIM1CFG}$ can affect the V_{OUT1} range setting (MFR_PWM_CONFIG[5]) and loop gain.

$V_{TRIM1CFG}$ (H6): Output Voltage Select Pin for V_{OUT1}, Fine Setting. Works in combination with $V_{OUT1CFG}$ to affect the VOUT_COMMAND (and associated output voltage monitoring and protection/fault-detection thresholds) of Channel 1, at SV_{IN} power-up. (See $V_{OUT1CFG}$ and the Applications Information section.) Minimize capacitance—especially when the pin is left open—to assure accurate detection of the pin state. Note that use of RCONFIGs on $V_{OUT1CFG}$/$V_{TRIM1CFG}$ can affect the V_{OUT1} range setting (MFR_PWM_CONFIG[5]) and loop gain.

SYNC (E7): PWM Clock Synchronization Input and Open-Drain Output Pin. The setting of the FREQUENCY_SWITCH register dictates whether the LTM4676 is a "sync master" or "sync slave" module. When the LTM4676 is a sync master, FREQUENCY_SWITCH contains the commanded switching frequency of Channels 0 and 1—in PMBus linear data format—and it drives its SYNC pin low for 500ns at a time, at this commanded rate. In contrast, a sync slave uses FREQUENCY_SWITCH=0x0000 and does not pull its SYNC pin low. The LTM4676's PLL synchronizes the LTM4676's PWM clock to the waveform present on the SYNC pin—and therefore, a resistor pull-up to 3.3V is required in the application, regardless of whether the LTM4676 is a sync master or slave. EXCEPTION: driving the SYNC pin with an external clock is permissible; see the Applications Information section for details.

SCL (E6): Serial Bus Clock Open-Drain Input (Can Be an Input and Output, if Clock Stretching is Enabled). A pull-up resistor to 3.3V is required in the application for digital communication to the SMBus master(s) that nominally drive this clock. The LTM4676 will never encounter scenarios where it would need to engage clock stretching unless SCL communication speeds exceed 100kHz—and even then, LTM4676 will not clock stretch unless clock stretching is enabled by means of setting MFR_CONFIG_ALL[1] = 1_b. The factory-default NVM configuration setting has MFR_CONFIG_ALL[1] = 0_b: clock stretching disabled. If communication on the bus at clock speeds above 100kHz is required, the user's SMBus master(s) need to implement clock stretching support to assure solid serial bus communications, and only then should MFR_CONFIG_ALL[1] be set to 1_b. When clock stretching is enabled, SCL becomes a bidirectional, open-drain output pin on LTM4676.

SDA (D6): Serial Bus Data Open-Drain Input and Output. A pull-up resistor to 3.3V is required in the application.

$\overline{\text{ALERT}}$ (E5): Open-Drain Digital Output. A pull-up resistor to 3.3V is required in the application only if SMBALERT interrupt detection is implemented in one's SMBus system.

SHARE_CLK (H7): Share Clock, Bidirectional Open-Drain Clock Sharing Pin. Nominally 100kHz. Used for synchronizing the time base between multiple LTM4676s (and any other Linear Technology devices with a SHARE_CLK pin)—to realize well-defined rail sequencing and rail tracking. Tie the SHARE_CLK pins of all such devices together; all devices with a SHARE_CLK pin will synchronize to the fastest clock. A pull-up resistor to 3.3V is required when synchronizing the time base between multiple devices. If synchronizing the time base between multiple devices is not needed and MFR_CHAN_CONFIG$_n$[2] = 0_b, only then is a pull-up resistor not required.

$\overline{\text{GPIO}}_0$, $\overline{\text{GPIO}}_1$ (E4 and F4, Respectively): Digital, Programmable General Purpose Inputs and Outputs. Open-drain outputs and/or high impedance inputs. The LTM4676's factory-default NVM configurations for MFR_GPIO_PROPAGATE$_n$—0x6893—and MFR_GPIO_RESPONSE$_n$—0xC0—are such that: (1) when a channel-specific fault condition is detected—such as channel OT (overtemperature) or output UV/OV—the respective $\overline{\text{GPIO}}_n$ pin pulls logic low; (2) when a non-channel specific fault condition is detected—such as input OV or control IC OT—both $\overline{\text{GPIO}}_n$ pins pull logic low; (3) the LTM4676 ceases switching action on Channel 0 and 1 when its respective $\overline{\text{GPIO}}_n$ pin is logic low. Most significantly, this default configuration provides for graceful integration and interoperation of LTM4676 with paralleled channel(s) of other LTM4676(s)—in terms of properly coordinating efforts in starting, ceasing, and resuming switching action and output voltage regulation, in unison—all without GUI intervention or the need to "custom-preprogram" module NVM contents. Pull-up resistors from $\overline{\text{GPIO}}_n$ to 3.3V are required for proper operation in the vast majority of ap-

PIN FUNCTIONS

plications. (Only if the LTM4676's MFR_GPIO_RESPONSE$_n$ value were set to 0x00 might pull-ups be unnecessary. See the Applications Information section for details.)

WP (K6): Write Protect Pin, Active High. An internal 10µA current source pulls this pin to V_{DD33}. If WP is open circuit or logic high, only I^2C writes to PAGE, OPERATION, CLEAR_FAULTS, MFR_CLEAR_PEAKS and MFR_EE_UNLOCK are supported. Additionally, individual faults can be cleared by writing 1_b's to bits of interest in registers prefixed with "STATUS". If WP is low, I^2C writes are unrestricted.

RUN_0, RUN_1 (F5 and F6, Respectively): Enable Run Input for Channels 0 and 1, Respectively. Open-drain input and output. Logic high on these pins enables the respective outputs of the LTM4676. These open-drain output pins hold the pin low until the LTM4676 is out of reset and SV_{IN} is detected to exceed VIN_ON. A pull-up resistor to 3.3V is required in the application. Do not pull RUN logic high with a low impedance source.

$TSNS_{0a}$, $TSNS_{0b}$ (D5 and C5, Respectively): Channel 0 Temperature Excitation/Measurement and Thermal Sensor Pins, Respectively. Connect $TSNS_{0a}$ to $TSNS_{0b}$. This allows the LTM4676 to monitor the power stage temperature of channel 0.

$TSNS_{1a}$, $TSNS_{1b}$ (J5 and K5, Respectively): Channel 1 Temperature Excitation/Measurement and Thermal Sensor Pins, Respectively. In most applications, connect $TSNS_{1a}$ to $TSNS_{1b}$. This allows the LTM4676 to monitor the power stage temperature of channel 1. See the Applications Information section for information on how to use $TSNS_{1a}$ to monitor a temperature sensor external to the module, e.g., a PN junction on the die of a microprocessor.

I_{SNS0a}^+, I_{SNS0b}^+ (F2 and F1, Respectively): Channel 0 Positive Current Sense and Kelvin Sense Pins, Respectively. Connect I_{SNS0a}^+ to I_{SNS0b}^+.

I_{SNS1a}^+, I_{SNS1b}^+ (H2 and H1, Respectively): Channel 1 Positive Current Sense and Kelvin Sense Pins, Respectively. Connect I_{SNS1a}^+ to I_{SNS1b}^+.

I_{SNS0a}^-, I_{SNS0b}^- (E2 and E1, Respectively): Channel 0 Negative Current Sense and Kelvin Sense Pins, Respectively. Connect I_{SNS0a}^- to I_{SNS0b}^-.

I_{SNS1a}^-, I_{SNS1b}^- (G2 and G1, Respectively): Channel 1 Negative Current Sense and Kelvin Sense Pins, Respectively. Connect I_{SNS1a}^- to I_{SNS1b}^-.

$COMP_{0a}$, $COMP_{1a}$ (E8 and H8, Respectively): Current Control Threshold and Error Amplifier Compensation Nodes for Channels 0 and 1, Respectively. The trip threshold of each channel's current comparator increases with a respective rise in $COMP_{na}$ voltage. Small filter capacitors (22pF) internal to the LTM4676 on these COMP pins (terminated to SGND) introduce high frequency roll off of the error-amplifier response, yielding good noise rejection in the control loop. See $COMP_{0b}$/$COMP_{1b}$.

$COMP_{0b}$, $COMP_{1b}$ (D8 and J8, Respectively): Internal Loop Compensation Networks for Channels 0 and 1, Respectively. For the vast majority of applications, the internal, default loop compensation of the LTM4676 is suitable to apply "as is", and yields very satisfactory results: apply the default loop compensation to the control loops of Channels 0 and 1 by simply connecting $COMP_{0a}$ to $COMP_{0b}$ and $COMP_{1a}$ to $COMP_{1b}$, respectively. In contrast, when more specialized applications require a personal touch the optimization of control loop response, this can be easily accomplished by connecting (an) R-C network(s) from $COMP_{0a}$ and/or $COMP_{1a}$—terminated to SGND—and leaving $COMP_{0b}$ and/or $COMP_{1b}$ open, as desired.

DNC (C10, E11, H11, K10): Do not connect these pins to external circuitry. Solder these pins only to mounting pads on the PC board for mechanical integrity. These pads must remain electrically open circuit.

SIMPLIFIED BLOCK DIAGRAM

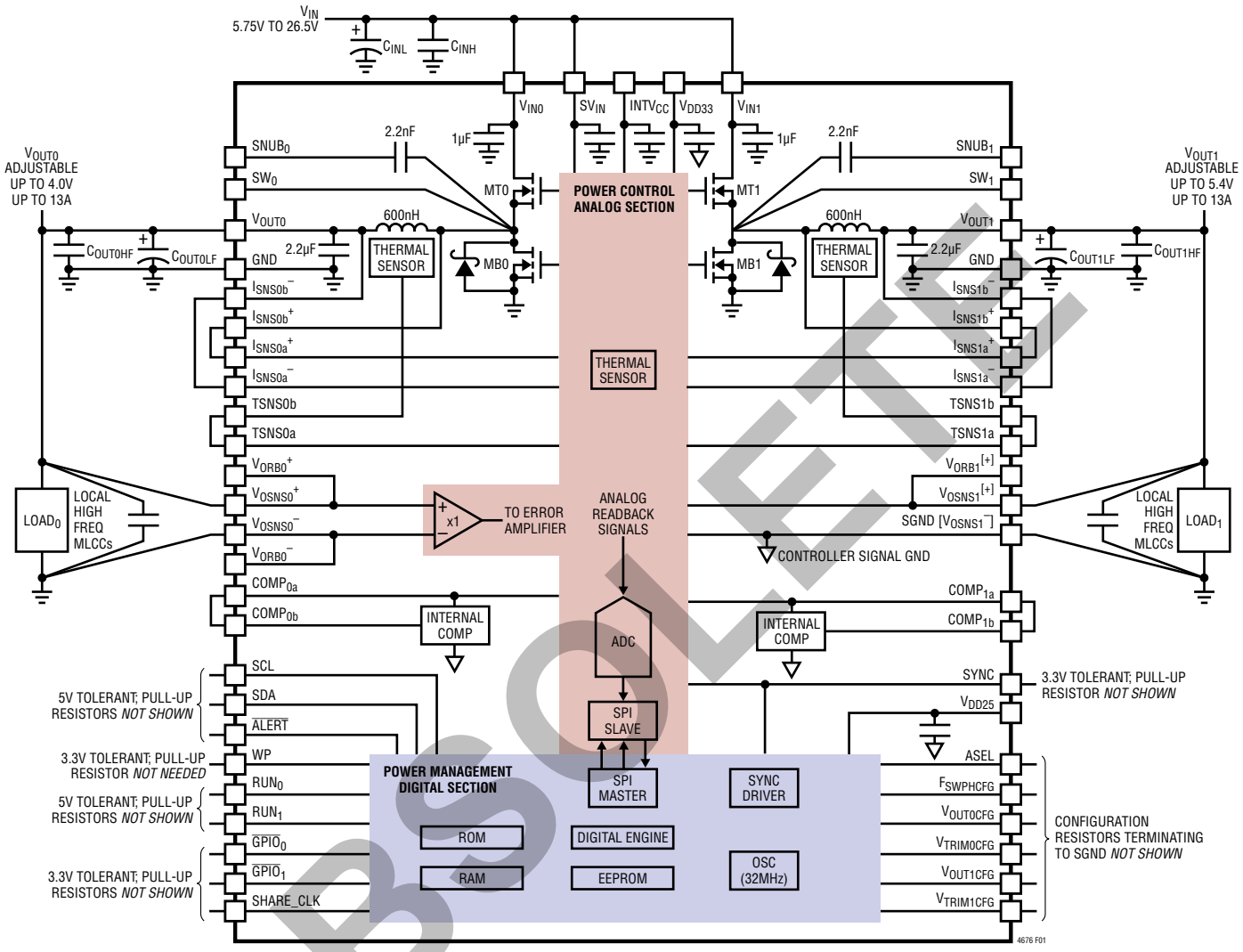


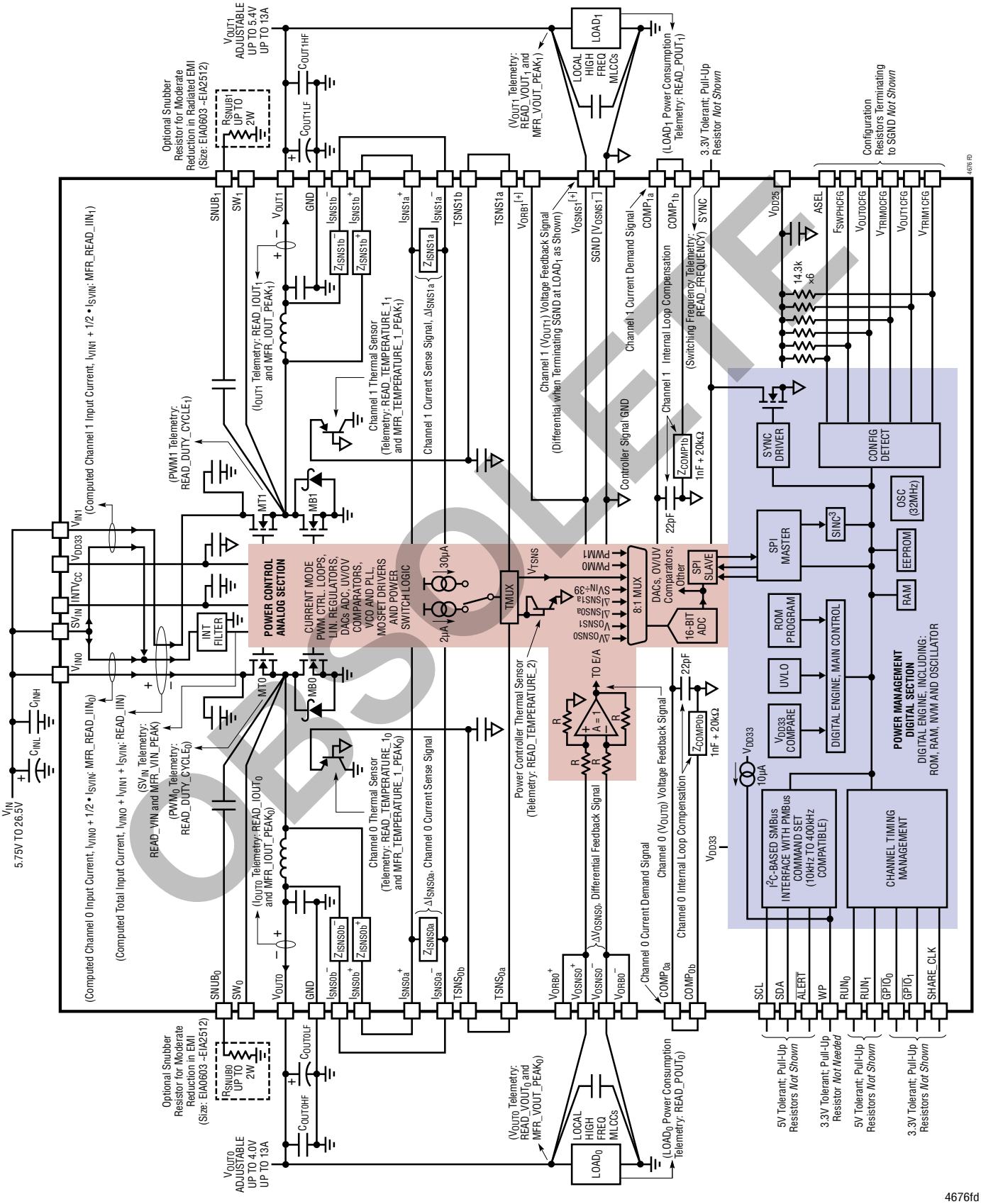
Figure 1. Simplified LTM4676 Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Using Figure 1 configuration.

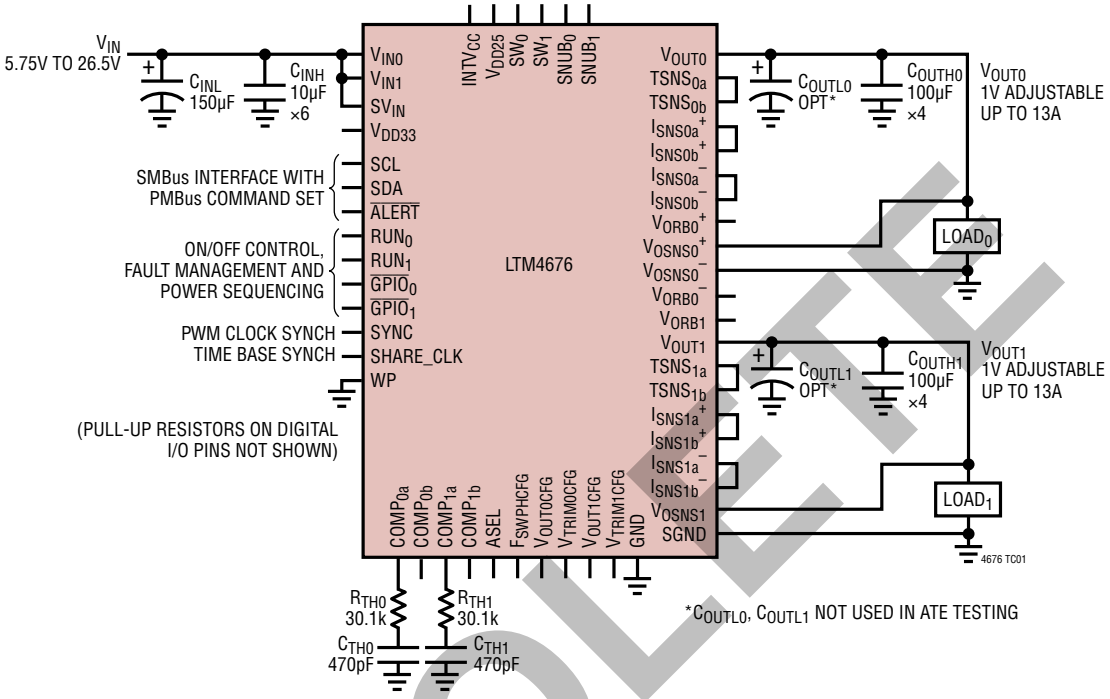
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{INH}	External High Frequency Input Capacitor Requirement ($5.75V \le V_{IN} \le 26.5V$, V_{OUTn} Commanded to 1.000V)	I_{OUT0} = 13A, 3 × 22µF, or 4 × 10µF I_{OUT1} = 13A, 3 × 22µF, or 4 × 10µF	40	66		µF
$C_{OUTn HF}$	External High Frequency Output Capacitor Requirement ($5.75V \le V_{IN} \le 26.5V$, V_{OUTn} Commanded to 1.000V)	I_{OUT0} = 13A I_{OUT1} = 13A		400 400		µF µF

FUNCTIONAL DIAGRAM

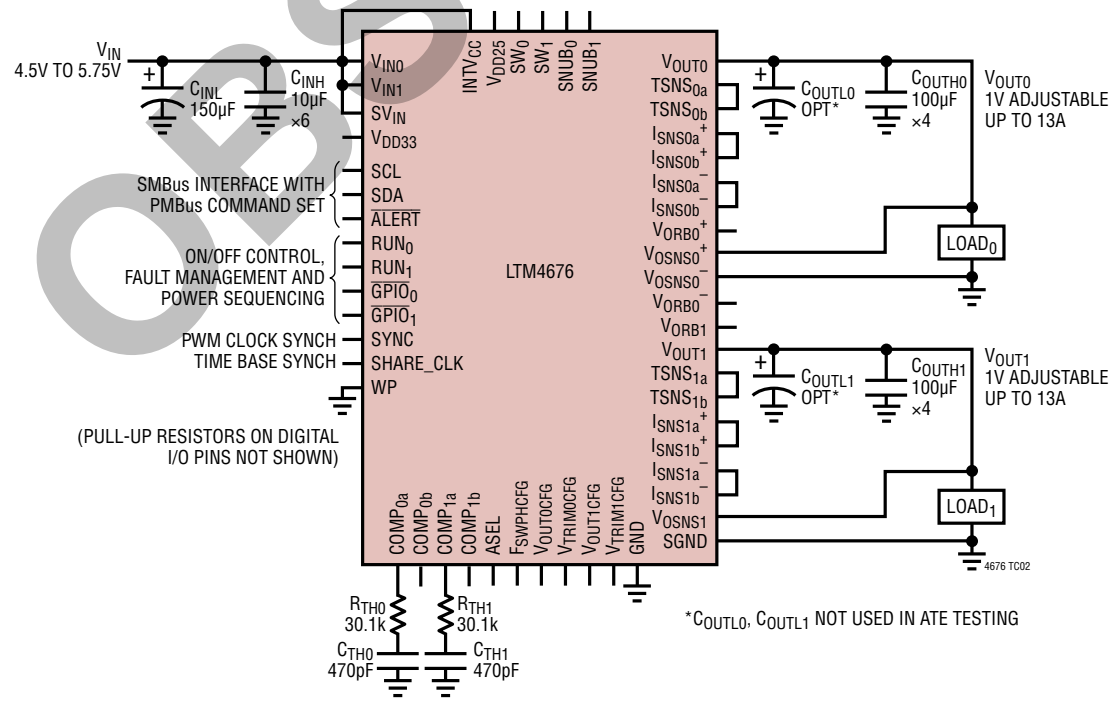


TEST CIRCUITS

Test Circuit 1. LTM4676 ATE High V_{IN} Operating Range Configuration, 5.75V ≤ V_{IN} ≤ 26.5V



Test Circuit 2. LTM4676 ATE Low V_{IN} Operating Range Configuration, 4.5V ≤ V_{IN} ≤ 5.75V



OPERATION

The LTC3880 data sheet is an essential reference document for this product. To obtain it go to:

www.linear.com/LTC3880

POWER MODULE INTRODUCTION

The LTM4676 is a highly configurable dual 13A output standalone nonisolated switching mode step-down DC/DC power supply with built-in EEPROM NVM (nonvolatile memory) and I²C-based PMBus/SMBus 2-wire serial communication interface capable of 400kHz SCL bus speed. Two output voltages can be regulated (V_{OUT0}, V_{OUT1}—collectively, V_{OUTn}) with a few external input and output capacitors and pull-up resistors. Readback telemetry data of average input and output voltages and currents, Channel PWM duty cycles, and module temperatures are continually digitized cyclically by an integrated 16-bit ADC (analog-to-digital converter). Many fault thresholds and responses are customizable. Data can be autonomously saved to EEPROM when a fault occurs, and the resulting fault log can be retrieved over I²C at a later time, for analysis.

The LTM4676 provides precisely regulated output voltages (±1%) between 0.6VDC to 4VDC (V_{OUT0}) and between 0.6VDC to 5.4VDC (V_{OUT1}). The target output voltage can be set according to pin-strapping resistors ($V_{OUTnCFG}$ and/or $V_{TRIMnCFG}$ pins), NVM/register settings, and/or can be altered on the fly via the I²C interface. The output voltage can be modified by the user at any time with a write to PMBus VOUT_COMMAND. Executing this command has a typical latency less than 10ms. Writes to PMBus OPERATION have a typical latency less than 1ms. The NVM factory-default switching frequency is 500kHz and the phase-interleaving angle between its two channels is 180°. Channel switching frequency, phase angle, and phase relationship with the falling edge of the SYNC pin waveform can be configured according to a pin-strap resistor ($F_{SWPHCFG}$ pin) and NVM/register settings—though, not on the fly during regulation. The 7-bit I²C slave address of the module defaults to 0x4F, but the least significant four bits of the address can be altered by the presence of the ASEL resistor—yielding 16 possible slave addresses. With the exception of the ASEL pin, the module can be configured to ignore all pin-strap resistors, if desired (see MFR_CONFIG_ALL[6]). The slave address cannot be changed over I²C.

The LTM4676 control IC is a slightly modified version of the LTC®3880; differences between the LTC3880 and the LTM4676's control IC are outlined in Table 1 of this data sheet—in the Applications Information section.

An indexed list of supported PMBus (I²C) and manufacturer-specific transaction command codes, register map documentation, register-by-register factory-default settings and the corresponding communication protocols, payload size and data formats for the LTM4676's control IC are provided in the LTC3880 data sheet—again, with exceptions noted in Table 1 of this data sheet. Therefore, the LTC3880 data sheet is an essential reference for all LTM4676 users.

Major features of the LTM4676 strictly from a DC/DC converter power delivery point of view are as follows:

- Up to 13A Output Current Delivery from Each of Two Integrated Power Stages (See Front Page Figure)—or Up to 26A Output, Combined (See Figure 35).
- Wide Input Voltage Range: DC/DC Step-Down Conversion from 5.75V to 26.5V Input (See Figure 44).
- DC/DC Step-Down Conversion from 4.5V to 5.75V Input, Connecting SV_{IN} to $INTV_{CC}$ (See Figure 35).
- DC/DC Step-Down Conversion Possible from Less Than 4.5V Input When an Auxiliary 5V Bias Supply Powers SV_{IN} and $INTV_{CC}$ (See Figure 37).
- Output Voltage Range: 0.5V to 4V on V_{OUT0}, 0.5V to 5.4V on V_{OUT1}. (See Figure 42 for Dual Phase Single 5V Output Operation with Reduced Telemetry.)
- Differential Remote Sensing of V_{OUT0} (V_{OSNS0}^+/V_{OSNS0}^-).
- Start-Up Into a Pre-Biased Load Without Sinking Current.
- Four LTM4676s Can Be Paralleled to Deliver Up to 100A (See Figure 39).
- One LTM4676 Can Be Paralleled with Three LTM4620A or LTM4630 Modules to Deliver Up to 130A; Infer Rail Status and Telemetry of Paralleled LTM4620A or LTM4630 via the Sole LTM4676 (See Figure 40.)

OPERATION

- Discontinuous Mode and Burst Mode Operation Available for Higher Light-Load Efficiency (MFR_PWM_MODE$_n$[1:0]).
- Output Current Limit and Overvoltage Protection.
- Three Integrated Temperature Sensors, Over/Undertemperature Protection.
- Constant Frequency Peak Current Mode Control.
- Configurable Switching Frequency, 250kHz to 1MHz; Synchronizable to External Clock; Seven Configurable Channel Phase Interleaving Settings.
- Internal Loop Compensation Provided; External Loop Compensation Can Be Applied, if Preferred.
- Integrated Snubber Capacitors Enable EMI Reduction by Placing External Snubber Resistors Adjacent to the Module (see Figures 32 and 33).
- Low Profile (16mm × 16mm × 5.01mm) BGA Package Power Solution Requires Only Input and Output Capacitors; at Most, Nine Pull-Up Resistors for Open-Drain Digital Signals; at Most, Six Pull-Down Resistors to Configure All Possible Pin-Strapping Options.

Features of the LTM4676 that enable power system management, rail sequencing, and fault monitoring and reporting are as follows:

- I^{2}C-based PMBus/SMBus 2-Wire Serial Communication Interface (SDA, SCL) with $\overline{\text{ALERT}}$ Interrupt Pin, SCL Clock Capable of 400kHz Bus Communication Speeds with Clock Low Extending—or 100kHz, Otherwise.
- Configurable Output Voltage.
- Configurable Input Undervoltage Comparators (UVLO Rising, UVLO Falling).
- Configurable Switching Frequency.
- Configurable Current Limit.
- Configurable Output Over/Undervoltage Comparators.
- Configurable Turn-On and Turn-Off Delay Times.
- Configurable Output Ramp Rise and Fall Times.
- Non-Volatile Configuration Memory (NVM EEPROM) to Configure Aforementioned Settings, and More—Yielding Standalone Operation, if Desired, and Also Enabling In-Situ Changes to the LTM4676's Configuration in Embedded Designs.
- Monitoring and Reporting of Telemetry Data: Average Output and Input Currents and Voltages, Internal Temperatures, and Power Stage Duty Cycles—Continuously Digitized Cyclically by a 16-Bit ADC.
  - Peak Observed Output Current and Voltage, Input Voltage, and Module Temperatures Can Be Polled and Cleared/Reset.
  - ADC Latency Not Greater Than 100ms, Nominal.
  - Option to Monitor One External Temperature in Lieu of Channel 1 (V_{OUT1}) Module Power Stage Temperature.
- Monitoring, Reporting, and Configurable Response to Latching and Non-Latching Individual Fault and/or Warning Status, Including but Not Limited to:
  - Output Over/Undervoltages.
  - Input (SV_{IN}) Over/Undervoltages.
  - Module Input and Power Stage Output Overcurrents.
  - Module Power Stage Over/Undertemperatures.
  - Internal Control IC Overtemperature.
  - Communication, Memory and Logic (CML) Faults.
- Fault Logging Upon Detection of a Fault Condition. The LTM4676 Can Be Configured to Automatically Upload a Fault Log to Its NVM, Consisting of: an Uptime Counter, Peak Observed Telemetry, Telemetry Gathered from the Six Most Recent Rounds of Cyclical ADC Data Leading Up to the Detection of the Fault That Triggered Fault Log Writing, and Fault Status Associated with That ADC History.
- Two Configurable Open-Drain General Purpose Input/Output Pins ($\overline{\text{GPIO}}_0$, $\overline{\text{GPIO}}_1$), Which Can Be Used for:
  - Fault Reporting, e.g., as a System Interrupt Signal.
  - Coordinating Turn-On/Off of the LTM4676 in Multiphase/Multirail Systems.
  - Propagating an Unfiltered Power Good Signal (Output of a V_{OUTn} Undervoltage Comparator) to Command Turn-On/Off of a Downstream Rail.

OPERATION

- A Write Protect (WP) Pin and Configurable WRITE_PROTECT Register to Protect the Internal Configuration of RAM and NVM Against Unintended Changes via I^2C.
- Time-Base Interconnect (SHARE_CLK, 100kHz Heartbeat) for Synchronization in the Time Domain Between Multiple LTM4676s.
- Optional External Configuration Resistors (RCONFIGs) for Setting Start-Up Output Voltages, Switching Frequency and Channel-to-Channel Phase Interleaving Angle.
- 16 Supported Slave Addresses (0x4F Default), Configured by Resistor Pin Strapping the ASEL Pin.

POWER MODULE CONFIGURABILITY AND READBACK DATA

This section of the data sheet describes in detail all the configurable features and readable data of the LTM4676 accessible via I^2C. The relevant command code name(s) are indicated by use of all capital letters, e.g., "VIN_ON". Refer to the LTC3880 data sheet and Table 1 of this data sheet in order to identify the associated command code, payload size, data format and factory-default value for each register name of interest. Specific register bits of some registers are indicated with the use of brackets, i.e., "[" and "]". The least significant bit (LSB) of a register is bit number zero, indicated by "[0]". The most significant bit of a byte-long (8-bit-long) register is bit number seven, indicated by "[7]". The most significant bit (MSB) of a word-long (16-bit-long) register is bit number fifteen, indicated by "[15]". Multiple bits of a register can be alluded to with the use of a colon, e.g., bits 2, 1 and 0 of the MFR_PWM_CONFIG register are indicated by "MFR_PWM_CONFIG[2:0]". Bits can take on values of 0_b or 1_b. The subscripted "$_b$" suffix indicates the number's value is in binary. Values in hexadecimal are indicated with a "0x" prefix. For example, decimal value "89" is indicated by 0x59 and 01011001_b (8-bit-long values), as well as 0x0059 and 0000000001011001_b (16-bit-long values).

One further shorthand notion the reader will notice is the italicized "*n*" or "*n*". "*n*" can take on a value of 0 or 1—and provides an easy way to refer to registers which are paged commands, i.e., register names which have the same command code value but can be configured independently (or yield channel-specific telemetry) for Channel 0 (Page 0, or 0x00) vs Channel 1 (Page 1, or 0x01). Registers lacking an "*n*" are therefore easily identified as being global in nature, i.e., common to both Channels/Outputs. For example, the switching frequency setting commanded by register FREQUENCY_SWITCH is common to both channels, and lacks "*n*". Another example: the READ_VIN register contains the digitized input voltage as seen at the SV_{IN} pin, and SV_{IN} is unique, i.e., common to both Channels. In contrast, the nominal commanded output voltage is indicated by the register VOUT_COMMAND*n*. The "*n*" indicates that VOUT_COMMAND can be set differently for Channel 0 vs Channel 1. Executing the PAGE Command (Command Code 0x00) with payload 0x00 sets the LTM4676 to write/read data pertaining to Channel 0 in all subsequent I^2C transactions until the Page is changed. Executing the PAGE Command with payload 0x01 sets the LTM4676 to write/read data pertaining to Channel 1 in all subsequent I^2C transactions until the Page is changed. Executing the PAGE Command with payload 0xFF sets the LTM4676 to write data pertaining to Channels 0 and 1 in all subsequent I^2C write transactions until the Page is changed. Reads from and writes to global registers do not require setting the Page to 0xFF. Reads from channel-specific (i.e., non-global) registers when the Page is set to 0xFF result in the LTM4676 reporting the value on Page 0x00 (i.e., Channel 0-specific data).

The list below itemizes aspects of the LTM4676 relating to power supply functions that are configurable by I^2C communications—provided the state of the WP (write protect) pin and the WRITE_PROTECT register value permit the I^2C writes—and by EEPROM settings:

OPERATION

- Output Start-Up Voltages (VOUT_COMMAND$_n$), the Maximum Commandable Output Voltages (VOUT_MAX$_n$), Output Voltage Power Good "On" (VOUT_PGOOD_ON$_n$) and "Off" (POWER_GOOD_OFF$_n$) Thresholds, Output Margin High (VOUT_MARGIN_HIGH$_n$) and Margin Low (VOUT_MARGIN_LOW$_n$) Command Voltages, and Output Over/Undervoltage Warning and Fault Thresholds (VOUT_OV_WARN_LIMIT$_n$, VOUT_OV_FAULT_LIMIT$_n$, VOUT_UV_WARN_LIMIT$_n$, and VOUT_UV_FAULT_LIMIT$_n$). Additionally, these Values Can Be Configured at SV_{IN} Power-Up According to Resistor-Pin Strapping of the $V_{OUT0CFG}$, $V_{TRIM0CFG}$, $V_{OUT1CFG}$ and/or $V_{TRIM1CFG}$ Pins, Provided MFR_CONFIG_ALL[6] = 0_b.
- Output Voltages, On the Fly, Including Transition Rate ($\Delta V/\Delta t$), VOUT_TRANSITION_RATE$_n$—Either by I^2C Writes to the VOUT_COMMAND$_n$, VOUT_MARGIN_HIGH$_n$, or VOUT_MARGIN_LOW$_n$ Registers, and/or to the OPERATION$_n$ Register.
- Input Undervoltage-Lockout, Rising (VIN_ON) and Input Undervoltage Lockout, Falling (VIN_OFF), Based on the SV_{IN} Pin Voltage.
- Switching Frequency (FREQUENCY_SWITCH) and Channel Phase-Interleaving Angle (MFR_PWM_CONFIG[2:0]). However, these Parameters Can Be Changed via I^2C Communications Only When the LTM4676's Channels are Off, i.e., not Switching. Additionally, These Parameters Can Be Configured at SV_{IN} Power-Up According to Resistor-Pin Strapping of the $F_{SWPHCFG}$ Pin, Provided MFR_CONFIG_ALL[6] = 0_b.
- Output Voltage Turn On and Turn Off Sequencing and Associated Watchdog Timers, Namely:
  - Output Voltage Turn-On Delay Time (the Time Delay from the LTM4676 Being Commanded to Turn On, e.g., by the RUN$_n$ Pin Toggling from Logic Low to High, Before Switching Action Commences. TON_DELAY$_n$).
  - Output Voltage Soft-Start Ramp-Up Time (TON_RISE$_n$).
  - The Amount of Time (TON_MAX_FAULT_LIMIT$_n$) Permitted to Elapse After the LTM4676 is Commanded to Turn On, e.g., by the RUN$_n$ Pin Toggling from Logic Low to High, After Which, If the Output Voltage Fails to Exceed the Output Undervoltage Fault Threshold (VOUT_UV_FAULT_LIMIT$_n$), the LTM4676's Output (V_{OUTn}) is Declared to Have Not Come Up in a Timely Manner.
  - The LTM4676's Response to Any Such Aforementioned TON_MAX_FAULT_LIMIT$_n$ Event (TON_MAX_FAULT_RESPONSE$_n$).
  - Output Voltage Soft-Stop Ramp-Down Time (TOFF_FALL$_n$).
  - Output Voltage Turn-Off Delay Time (the Time Delay from the LTM4676 Being Commanded to Turn Off, e.g., by the RUN$_n$ Pin Toggling from Logic High to Low, Before Switching Action Ceases. TOFF_DELAY$_n$).
  - When Commanded to Turn Off it Output—or, When Turning Off its Output in Response to a Fault—Configuring Whether the LTM4676's Output (V_{OUTn}) Becomes High Impedance ("High-Z" or "Three State"—turning off both MTn and MBn in the Power Stage). ("Immediate Off", ON_OFF_CONFIG$_n$[0] = 1_b vs Configuring the Output Voltage to Be Ramped Down According to TOFF_FALL$_n$ and/or TOFF_DELAY$_n$ Settings, ON_OFF_CONFIG$_n$[0] = 0_b).
  - The Amount of Time (TOFF_MAX_WARN_LIMIT$_n$) Permitted to Elapse After the LTM4676 is Supposed to Have Turned Off its Output, i.e., at the End of the Period Dictated by TOFF_FALL$_n$, After Which, If the Output Voltage Has Not Fallen Below 12.5% of the Former Target Voltage of Regulation, the LTM4676's Output (V_{OUTn}) is Declared to Have Not Powered Down in a Timely Manner.

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- Configurable Output Voltage Restart Time. Subsequent to the RUN_n Pin Being Pulled Low, the LTM4676 Pulls RUN_n Logic Low, Itself, and the Output Cannot Be Restarted Until a Minimum Time Has Elapsed—the Restart Delay Time. This Delay Assures Proper Sequencing of All System Rails. The Minimum Restart Delay Processed By the LTM4676 is the Longer of ($TOFF\_DELAY_n$ + $TOFF\_FALL_n$ + 136ms) vs the Commanded $MFR\_RESTART\_DELAY_n$ Register Value. At the End of This Delay, the LTM4676 Releases its RUN_n Pin.
- Configurable Fault-Hiccup Retry Delay Time. When a Fault Occurs in Which the LTM4676's Fault Response Behavior to That Fault Is to Reattempt Power-Up of its Output Voltage After Said Fault Ceases to Be Present (e.g., "Infinite Retry"), the Delay Time for the LTM4676 to Re-engage Switching Action Is the Longer of the $MFR\_RETRY\_DELAY_n$ Time vs the Time Required for the Output to Decay Below 12.5% of the Formerly Commanded Output Voltage Value (Unless This Lattermost Criteria, i.e., Requiring the Output to Decay Below 12.5% Is Negated By the Setting of $MFR\_CHAN\_CONFIG_n$[0] to "1_b"—Which is the LTM4676's Factory-NVM Default Setting).
- Output Over/Undervoltage Fault Responses ($VOUT\_OV\_FAULT\_RESPONSE_n$, $VOUT\_UV\_FAULT\_RESPONSE_n$).
- Time-Averaged Current Limit Warning and Instantaneous Peak (Cycle-by-Cycle) Fault Thresholds, and Fault Response ($IOUT\_OC\_WARN\_LIMIT_n$, $IOUT\_OC\_FAULT\_LIMIT_n$, $IOUT\_OC\_FAULT\_RESPONSE_n$).
- Channel (V_{OUT0}, V_{OUT1}) Overtemperature Warning and Fault Thresholds, and Fault Response ($OT\_WARN\_LIMIT_n$, $OT\_FAULT\_LIMIT_n$, $OT\_FAULT\_RESPONSE_n$).
- Channel (V_{OUT0}, V_{OUT1}) Undertemperature Fault Thresholds and Fault Response ($UT\_FAULT\_LIMIT_n$, $UT\_FAULT\_RESPONSE_n$).
- Input Overvoltage Fault Threshold and Response (VIN_OV_FAULT_LIMIT, VIN_OV_FAULT_RESPONSE), Based on the SV_{IN} Pin Voltage.
- Input Undervoltage Warning Threshold (VIN_UV_WARN_LIMIT) Based on the SV_{IN} Pin Voltage.
- Module Input Overcurrent Warning Threshold (IIN_OC_WARN_LIMIT)

The control IC within the LTM4676 module ceases switching action if control IC temperature exceeds 160°C (Note 12). The control IC resumes operation after a 10°C cool-down hysteresis. Note that these typical parameters are based on measurements in a lab oven and are not production tested. This overtemperature protection is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

TIME-AVERAGED AND PEAK READBACK DATA

Time-averaged telemetry readback data accessible via I^2C communications follow:

- Channel Output Current ($READ\_IOUT_n$) and Peak Observed Value of $READ\_IOUT_n$ ($MFR\_IOUT\_PEAK_n$).
- Channel Output Voltage ($READ\_VOUT_n$) and Peak Observed Value of $READ\_VOUT_n$ ($MFR\_VOUT\_PEAK_n$).
- Channel Output Power ($READ\_POUT_n$).
- Channel Input Current ($MFR\_READ\_IIN_n$) and Module Input Current (READ_IIN).
- Channel Temperatures ($READ\_TEMPERATURE\_1_n$) and Peak Observed Values of $READ\_TEMPERATURE\_1_n$ ($MFR\_TEMPERATURE\_1\_PEAK_n$).
- Control IC Temperature (READ_TEMPERATURE_2) and Peak Observed Value (MFR_TEMPERATURE_2_PEAK).
- Input Voltage (READ_VIN), Based on the Voltage of the SV_{IN} Pin, and Peak Observed Value of READ_VIN (MFR_VIN_PEAK).
- Channel Topside Power MOSFET (MT*n*) Duty Cycle ($READ\_DUTY\_CYCLE_n$)

Peak observed values of telemetry readback data can be cleared with the MFR_CLEAR_PEAKS I^2C command, provided the WRITE_PROTECT register value permits it. (Executing MFR_CLEAR_PEAKS can be performed regardless of the state of the WP pin.)

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Details on the LTM4676's Fault Log Feature follow:

- Fault Logging is Enabled When MFR_CONFIG_ALL[7] = 1_b.
- A Fault Log is Present in NVM When STATUS_MFR_SPECIFIC$_n$[3]Reports "1_b", Which Is Propagated to the MFR Bit (Bit 12) of the STATUS_WORD Register.
- Retrieving Fault Log Data, if Present, Is Performed with the MFR_FAULT_LOG Command. 147 Bytes of Data are Retrieved Using the PMBus-Defined Variant to the SMBus Block Read Protocol.
- The Fault Log Contents in NVM, if Present, Are Cleared By Executing the MFR_FAULT_LOG_CLEAR Command.
- The Fault Log Will Not Be Written if a Fault Log Is Already Present in NVM.
- The LTM4676 Can Be Forced to Write a Fault Log to Its NVM by Executing the MFR_FAULT_LOG_STORE Command; the LTM4676 Will Behave as if a Channel Faulted Off. Note the command is NACKed and a CML fault is reported if a Fault Log is already present at the time of executing MFR_FAULT_LOG_STORE.

When an external stimulus pulls the LTM4676's $\overline{GPIO}_n$ pin(s) logic low, the respective channel ($V_{OUT}n$) either: takes no action on it, i.e., ignores it completely—if MFR_GPIO_RESPONSE$_n$ = 0x00; or, turns off immediately, i.e., the power stage(s) become high impedance ("inhibited")—if MFR_GPIO_RESPONSE$_n$ = 0xC0.

The MFR_GPIO_PROPAGATE$_n$ register contents configure which fault(s) cause the LTM4676 to pull its $\overline{GPIO}_n$ pin(s) logic low.

I^{2}C communications are originated by the user's (system's) I^{2}C master device. Writes/reads to/from Channel 0 of the LTM4676 (V_{OUT0}: PAGE 0x00), to/from Channel 1 of the LTM4676 (V_{OUT1}: PAGE 0x01), or writes to both Channels 0 and 1 of the LTM4676 (V_{OUT0} and V_{OUT1}: PAGE 0xFF) are possible. The target channel(s) of interest are selected by the I^{2}C master by executing the PAGE command and sending the appropriate argument (0x00, 0x01, 0xFF) in the payload. The PAGE command is unrestricted, i.e., not affected by the WP pin or WRITE_PROTECT register settings.

The LTM4676 always responds to its global slave addresses, 0x5A and 0x5B. Commands sent to the global address 0x5A act the same as if the PAGE command were set to 0xFF, i.e., received commands are written to both channels simultaneously. Commands sent to the global address 0x5B are applied to the PAGE active at the time of the global address transaction, i.e., allows channel-specific command of all LTM4676 devices on the bus.

I^{2}C commands not listed above that relate to Fault Status and EEPROM NVM Operations follow. Writing of the following is possible provided the state of the WP (write protect) pin and the WRITE_PROTECT register value permits the I^{2}C writes:

- Soliciting (Reading) Module Fault Status and Clearing (Writing) Module Fault Status (CLEAR_FAULTS, STATUS_BYTE$_n$, STATUS_WORD$_n$, STATUS_VOUT$_n$, STATUS_IOUT$_n$, STATUS_INPUT, STATUS_TEMPERATURE$_n$, STATUS_CML [Communications, Memory, and/or Logic], and STATUS_MFR_SPECIFIC$_n$ [Miscellaneous]).
- Storing the LTM4676's User-Writable RAM Register Data to the EEPROM NVM (STORE_USER_ALL).
- An Alternate Means to the STORE_USER_ALL Command to Directly Erase and Write the LTM4676's EEPROM Contents, Protected by Unlock Keys, to Facilitate Programming of the LTM4676 EEPROM in Environments Such as ICT (In-Circuit Test) and Bulk Programming by, e.g., Embedded Hardware or by the LTpowerPlay GUI. Also, a Means to Directly Read the LTM4676 EEPROM Contents (MFR_EE_UNLOCK, MFR_EE_ERASE, MFR_EE_DATA).
- Instigating a Soft Reset of the LTM4676 without Power-Cycling SV_{IN} Power (MFR_RESET). The MFR_RESET Command Triggers the Download of EEPROM NVM Data to RAM Registers, as if SV_{IN} Power had been cycled.

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Other data that can be obtained from the LTM4676 via I²C communications are as follows:

- Soliciting the LTM4676 for its PMBus Capabilities, as Defined by PMBus (CAPABILITY):
  - PEC (Packet Error Checking). Note, the LTM4676 Requires Valid PEC in I²C Communications when MFR_CONFIG_ALL[2] = 1_b. The NVM Factory-Default Configuration is MFR_CONFIG_ALL[2] = 0_b, i.e., PEC Not Required.
  - I²C Communications Can Be Supported at Up to 400kHz SCL Bus Speed. Note, Clock Low Extending (Clock Stretching) Must Be Enabled On the LTM4676 to Ensure Robust Communications Above 100kHz SCL Bus Speeds, i.e., MFR_CONFIG_ALL[1] = 1_b. The NVM Factory-Default Configuration is MFR_CONFIG_ALL[1] = 0_b, i.e. Clock Stretching is Disabled.
  - The LTM4676 Has an $\overline{\text{SMBALERT}}$ ($\overline{\text{ALERT}}$) Pin and Does Support the SMBus ARA (Alert Response Address) Protocol.
- Soliciting the Module for the Maximum Output Voltage It Can Be Commanded to Produce (MFR_VOUT_MAX$_n$).
- Soliciting the Device for the Data Format of Its Output Voltage-Related Registers (VOUT_MODE$_n$).
- Soliciting the Device for the Revisions of PMBus Specifications That It Supports (Part I: Rev. 1.1; Part II: Rev 1.1).
- Soliciting the Device for the Identification of the Manufacturer of the LTM4676, "LTC" (MFR_ID) and the Manufacturer Code Representing the LTM4676 and Revision, 0x448X or 0x440X (MFR_SPECIAL_ID).
- Soliciting the Device for Its Part Number, "LTM4676" (MFR_MODEL).
- Soliciting the Module for Its Serial Number (MFR_SERIAL).
- The Digital Status of the LTM4676's I/O Pads and Validity of the ADC (MFR_PADS) and WP Pin Status (MFR_COMMON[0]).

The following list indicates other aspects of the LTM4676 relating to power system management and power sequencing that are configurable by I²C communications—provided the state of the WP (write protect) pin and the WRITE_PROTECT register value permit the I²C writes—and by EEPROM settings:

- Providing Multiple Means to Read/Write Data Directly to a Particular Channel of the LTM4676 By Assigning Additional Slave Address for Channels 0 and 1 (MFR_CHANNEL_ADDRESS$_n$, MFR_RAIL_ADDRESS$_n$), the Benefit of Which Is That It Reduces Page Command Usage and Associated I²C Traffic. It Also Facilitates Altering the Same Register of Multiple LTM4676 in Unison without Invoking the PMBus Group Command Protocol.
- Configuring the Output Voltage to Be On or Off by Means Other Than the RUN$_n$ Pin (ON_OFF_CONFIG$_n$[3], OPERATION commands)
- Configuring Whether the LTM4676 Masks PLL (Phase-Locked Loop) Out-of-Lock Faults. (MFR_CONFIG_ALL[3]).
- Configuring Whether the LTM4676 Performs a CLEAR_FAULTS Command Upon Itself When Either RUN$_n$ Pin Toggles from Logic Low to Logic High. (MFR_CONFIG_ALL[0]).
- Configuring Whether the LTM4676 Pulls RUN$_n$ Logic Low When the LTM4676 is Commanded Off By Other Means (MFR_CHAN_CONFIG$_n$[4]).
- Configuring the Response of the LTM4676 When It Is Commanded to Turn On Its Output Prior to the Completion of Processing TOFF_DELAY$_n$ and TOFF_FALL$_n$ Power-Down Sequencing (MFR_CHAN_CONFIG$_n$[3]).
- Configuring Whether the LTM4676's Output Is Disabled When SHARE_CLK Is Held Low (MFR_CHAN_CONFIG$_n$[2]).
- Configuring Whether the $\overline{\text{ALERT}}$ Pin is Pulled Low When $\overline{\text{GPIO}}_n$ Is Pulled Low by External Stimulus (MFR_CHAN_CONFIG$_n$[1]).

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- Setting the Value of the MFR_IIN_OFFSET$_n$ Registers, Representing an Estimate of the Current Drawn by the SV_{IN} Pin. The SV_{IN} Pin Current Is Not Measured by the LTM4676 but the MFR_IIN_OFFSET$_n$ Is Used in Computing and Reporting Channel and Total Module Input Currents (MFR_READ_IIN$_n$, READ_IIN).
- Three Words (Six Bytes) of the LTM4676's EEPROM That Are Available for Storing User Data. (USER_DATA_03$_n$, USER_DATA_04).
- Invoking or Releasing Several Levels of I^2C Write Protection (WRITE_PROTECT).
- Determining Whether the User-Editable RAM Register Values Are Identical to the Contents of the User NVM (MFR_COMPARE_USER_ALL).
- Setting the Programmable Output Voltage Range of V_{OUT} to a Narrower Range (0.5V to 2.75V) in Order to Achieve a Higher Resolution of V_{OUT} Adjustment Than Is Available by Default (MFR_PWM_CONFIG[6:5]). MFR_PWM_CONFIG Cannot Be Changed On the Fly; Switching Action Must Be Off. Note that Altering the V_{OUT} Range Alters the Gain of the Control Loop and May Therefore Require Loop Compensation to Be Adjusted.
- Altering the Temperature Coefficient of the LTM4676's Current Sensing Elements, if Needed (MFR_IOUT_CAL_GAIN_TC$_n$) (Uncommon to Alter This Parameter from its NVM-Factory Default Setting).
- Altering the Gain or Offset of the Power Stage Sensors (MFR_TEMP_1_GAIN$_n$ and MFR_TEMP_1_OFFSET$_n$)—or That of the External Temperature Sensor, When an External Temperature Sensor Is Used On the $TSNS_{1a}$ Pin. (Uncommon to Alter This Parameter from its NVM-Factory Default Setting).
- Configuring Whether the LTM4676 Pulls SHARE_CLK Logic Low When SV_{IN} Has Fallen Outside Its UVLO Thresholds (MFR_PWM_CONFIG[4]). MFR_PWM_CONFIG Cannot Be Changed On the Fly; Switching Action Must Be Off (Uncommon to Alter This Parameter from its NVM-Factory Default Setting).
- Configuring Whether the LTM4676's Output Voltage Digital Servos Are Active vs Disengaged (MFR_PWM_MODE$_n$[6]. Uncommon to Alter This Parameter from its NVM-Factory Default Settings).
- Configuring Whether the LTM4676's Current Limit Range is Set to High Range vs Low Range. (MFR_PWM_MODE$_n$[7]. Not Recommended to Alter This Parameter from its NVM-Factory Default Settings).

Remaining LTM4676 status that can be queried over I^2C communications follow:

- Access to Three "Hand-Shaking" Status Bits (MFR_COMMON[6:4]) to Ease Implementation of PMBus Busy Protocols, i.e., Enabling Fast and Robust System Level Communication Through Polling of These Bits to Infer LTM4676's Readiness to Act on Subsequent I^2C Writes. (See PMBus Communication and Command Processing, in the Applications Information Section.)
- Providing a Means to Determine Whether the LTM4676 NVM Download to RAM Has Occurred ("NVM Initialized", MFR_COMMON[3]).
- Providing a Means Other Than ARA Protocol to Determine Whether the LTM4676 is Pulling ALERT Low (MFR_COMMON[7]).
- Detecting a SHARE_CLK Timeout Event (MFR_COMMON[1]).
- Verifying the Slave Address of the LTM4676 (MFR_ADDRESS).

POWER MODULE OVERVIEW

A dedicated remote-sense amplifier precisely kelvin-senses V_{OUT0}'s load via the differential pin-pair formed by V_{OSNS0}^+ and V_{OSNS0}^-. V_{OUT0} can be commanded to between 0.5VDC and 4.0VDC. V_{OUT1} is sensed via the pin-pair formed by V_{OSNS1} and signal ground of the module's internal control IC, SGND. V_{OUT1} can be commanded to between 0.5VDC and 5.4VDC. Output voltage readback telemetry is available over I^2C (READ_VOUT$_n$ registers). Peak output voltage readback telemetry is accessible

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in the MFR_READ_VOUT_PEAK$_n$ registers. If V_{OSNS0}^- exceeds V_{OSNS}^+, no phase reversal of the differentially-sensed output voltage feedback signal occurs (Note 12). Similarly, no phase reversal occurs when SGND exceeds V_{OSNS1}(Note 12).

The typical application schematic is shown in Figure 44 on the back page of this data sheet.

The LTM4676 can operate from input voltages between 5.75V and 26.5V (see front page figure). In this configuration, $INTV_{CC}$ MOSFET driver and control IC bias is generated internally by an LDO fed from SV_{IN} to produce 5V at up to 100mA peak output current. Additional internal LDOs—3.3V (V_{DD33}), derived from $INTV_{CC}$, and 2.5V (V_{DD25}), derived from V_{DD33}—bias the LTM4676's digital circuitry. When $INTV_{CC}$ is connected to SV_{IN}, the LTM4676 can operate from input voltages between 4.5V and 5.75V (see Figure 35). Control IC bias (SV_{IN}) is routed independent of the inputs to the power stages (V_{IN0}, V_{IN1}); this enables step-down DC/DC conversion from less than 4.5V input (see Figure 37), so long as auxiliary power (4.5V ~ 26.5V) is available to bias the control IC appropriately. Furthermore, the inputs of the two power stages are not connected together internal to the module; therefore, DC/DC step-down conversion from two different source power supplies can be performed.

Per Note 6 of the Electrical Characteristics section, the output current may require derating for some operating scenarios. Detailed derating guidance is provided in the Applications Information section.

The LTM4676 contains dual integrated constant frequency current mode control buck regulators (Channel 0 and Channel 1) whose built-in power MOSFETs are capable of fast switching speed. The factory NVM-default switching frequency clocks SYNC at 500kHz, to which the regulators synchronize their switching frequency. The default phase-interleaving angle between the channels is 180°. A pin-strapping resistor on $F_{SWPHCFG}$ configures the frequency of the SYNC clock (switching frequency) and the channel phase relationship of the channels to each other and with respect to the falling edge of the SYNC signal. (Not all possible combinations of switching frequency and phase-angle assignments are settable by resistor pin programming; see Table 4. Configure the LTM4676's NVM to implement settings not available by resistor-pin strapping.) When a $F_{SWPHCFG}$ pin-strap resistor sets the channel phase relationship of the LTM4676's channels, the SYNC clock is not driven by the module; instead, SYNC becomes strictly a high impedance input and channel switching frequency is then synchronized to SYNC provided by an externally-generated clock or sibling LTM4676 with pull-up resistor to V_{DD33}. Switching frequency and phase relationship can be altered via the I^2C interface, but only when switching action is off, i.e., when the module is not regulating either output. See the Applications Information section for details.

Internal feedback loop compensation for Regulator 0 is available by connecting $COMP_{0a}$ to $COMP_{0b}$. (For Regulator 1, the connection is from $COMP_{1a}$ to $COMP_{1b}$.) With current mode control and internal feedback loop compensation, the LTM4676 module has sufficient stability margins and good transient performance with a wide range of output capacitors—even all-ceramic MLCCs. Table 20 provides guidance on input and output capacitors recommended for many common operating conditions. The Linear Technology µModule Power Design Tool is available for transient and stability analysis. Furthermore, expert users who prefer to not make use of the module's internal feedback loop compensation—but instead, tailor the feedback loop compensation specifically for his/her application—may do so by not connecting $COMP_{na}$ to $COMP_{nb}$: the personalized loop compensation network can be applied externally, i.e., from $COMP_{na}$ to SGND, and leaving $COMP_{nb}$ open circuit.

The LTM4676 has two general purpose input/output pins, named $\overline{GPIO}_0$ and $\overline{GPIO}_1$. The behavior of these pins is configurable via registers MFR_GPIO_PROPAGATE$_n$ and MFR_GPIO_RESPONSE$_n$. The $\overline{GPIO}_n$ pins are high impedance during NVM-download-to-RAM initialization. These pins are intended to perform one of two primary functions, or a hybrid of the two: behave as open- drain, active low fault/warning indicators; and/or, behave as auxiliary RUN pins for their respective V_{OUT}s. In the former case, the pins can be configured as interrupt pins, pulling active low when output under/overvoltage, input under/overvoltage, input/output overcurrent, overtemperature, and/or communication, memory or logic (CML) fault or warning events are detected by the LTM4676. Factory

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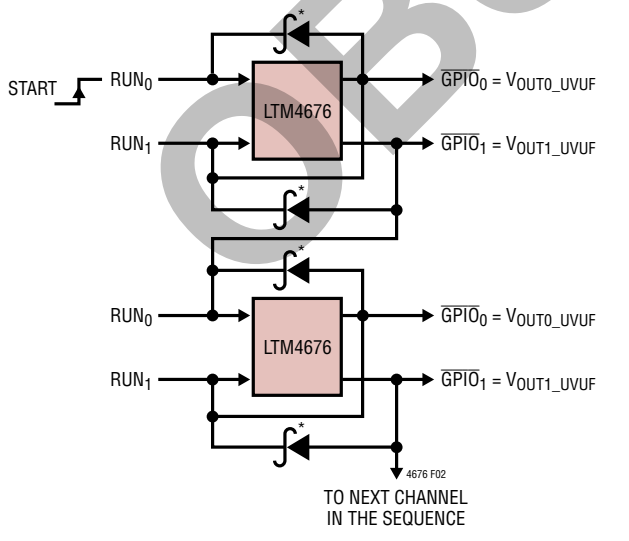
NVM-default settings configure the LTM4676 for the latter case, enabling the $\overline{GPIO}_n$ to be bussed to paralleled siblings (paralleled LTM4676 channels and/or modules), for purposes of coordinating orderly power-up and power-down, i.e., in unison. The LTM4676 DC/DC regulator does not feature a traditional "power good" (PGOOD) indicator pin to indicate when the output voltage is within a few percent of the target regulation point. However, the $\overline{GPIO}_n$ pin can be configured as a PGOOD indicator. If used for event-based sequencing of downstream rails, configure $\overline{GPIO}_n$ as the unfiltered output of the VOUT_UV_FAULT_LIMIT$_n$ comparator, setting Bit 12 of MFR_GPIO_PROPAGATE$_n$ to "1_b"; do not set Bits 9 and 10 of MFR_GPIO_PROPAGATE$_n$ for this purpose, since the propagation of power good in those latter instances is subject to the ADC's latency of up to 100ms, nominal. If it is necessary to have the desired PGOOD polarity appear on the $\overline{GPIO}_n$ pin immediately upon SV_{IN} power-up—given that the pin will initially be high impedance, until NVM contents have downloaded to RAM—a pull-down Schottky diode is needed between the RUN$_n$ pin of the LTM4676 and the respective $\overline{GPIO}_n$ pin. (See Figure 2.) If the $\overline{GPIO}_n$ pin is configured as a PGOOD indicator, the MFR_GPIO_RESPONSE$_n$ must be set to "ignore" (0x00), or else the LTM4676 cannot start up due to the latch-off conditions imposed.

Voltage Based Sequencing by Cascading $\overline{GPIO}_n$ Pins Into RUN$_n$ Pins (MFR_GPIO_PROPAGATE = XXX1X00XX00XXXX$_b$ and MFR_GPIO_RESPONSE = 0x00)



NOTE: RESISTOR OR RC PULL-UPS ON RUN$_n$ AND $\overline{GPIO}_n$ PINS NOT SHOWN
*OPTIONAL SIGNAL SCHOTTKY DIODE. ONLY NEEDED WHEN ACCURATE PGOOD (POWER GOOD) INDICATION IS REQURED BY THE SYSTEM/USER IMMEDIATELY AT SV_{IN} POWER UP

Figure 2. Event (Voltage) Based Sequencing

The RUN$_n$ pin is a bidirectional open-drain pin. This means it should never be driven logic high from a low impedance source. Instead, simply provide a 10k pull-up resistor from the RUN$_n$ pins to V_{DD33}. The LTM4676 pulls its RUN$_n$ pin logic low during NVM-download-to-RAM initialization, when SV_{IN} is below the commanded undervoltage lockout voltage (VIN_ON, rising and VIN_OFF, falling), and subsequent to external stimulus pulling RUN low—for a minimum time dictated by MFR_RESTART_DELAY$_n$. Bussing the respective RUN$_n$ and $\overline{GPIO}_n$ pins to sibling LTM4676 modules enables coordinated power-up/power-down to be well orchestrated, i.e., performing turn-on and turn-off in a unified fashion.

When RUN$_n$ exceeds 2V, the LTM4676 initially idles for a time dictated by the TON_DELAY$_n$ register. After the TON_DELAY$_n$ time expires, the module begins ramping up the respective control loop's internal reference, starting from 0V. In the absence of a pre-biased V_{OUTn} condition, the output voltage is ramped linearly from 0V to the commanded target voltage, with a ramp-up time dictated by the TON_RISE$_n$ register. In the presence of a pre-biased V_{OUTn} condition, the output voltage is brought into regulation in the same manner as aforementioned, with the exception that inductor current is prevented from going negative (the module's controller is operated in discontinuous mode operation during start-up). In both cases, the output voltage reaches regulation in a consistent time, as measured with respect to RUN$_n$ toggling high. See start-up oscilloscope shots in the Typical Performance Characteristics section.

Pulling the RUN$_n$ pin below 1.4V turns off the DC/DC converter, i.e., forces the respective regulator into a shutdown state. Factory NVM-default settings configure the LTM4676 to turn off its power stage MOSFETs immediately, thereby becoming high impedance. The output voltage then decays according to whatever output capacitance and load impedance is present. Alternatively, NVM/register settings can configure the LTM4676 to actively discharge V_{OUTn} when RUN$_n$ is pulled logic low, according to prescribed TOFF_DELAY$_n$ delay and TOFF_FALL$_n$ ramp-down times. See the Applications Information section for details. The LTM4676 does not feature an explicit, analog TRACK pin. Rail-to-rail tracking and sequencing is handled digitally, as explained previously.

OPERATION

Bussing the open-drain SHARE_CLK pins of all LTM4676s (and providing a pull-up resistor to V_{DD33}) provides a means for all LTM4676s in the system to synchronize their time-base (or "heartbeat") to the fastest SHARE_CLK clock. Sharing the heartbeat amongst all LTM4676 ensures that all rails are sequenced according to expectations; it negates timing errors that could otherwise materialize due to SHARE_CLK (time-base) tolerance and part-to-part variation.

Electrically connect adjacent pins I_{SNS0a}^+ to I_{SNS0b}^+; I_{SNS0a}^- to I_{SNS0b}^-; I_{SNS1a}^+ to I_{SNS1b}^+; and I_{SNS1a}^- to I_{SNS01b}^-. Current sense information is derived from across the power inductors (I_{SNSnb}^+/I_{SNSnb}^- pin-pairs) internal to the LTM4676 and made available to the internal control IC's current control loops and ADC sensors (I_{SNSna}^+/I_{SNSna}^-) by the aforementioned connections. Output current readback telemetry is available over I²C (READ_IOUT$_n$ registers). Peak output current readback telemetry is available in the MFR_READ_IOUT_PEAK$_n$ registers.

Output power readback is computed by the LTM4676 according to:

$$READ\_POUT_n = READ\_VOUT_n \bullet READ\_IOUT_n$$

Alternating excitation currents of 2µA and 30µA are sourced from each of the $TSNS_{0a}$ and $TSNS_{1a}$ pins. Connecting $TSNS_{0a}$ to $TSNS_{0b}$, and then $TSNS_{1a}$ to $TSNS_{1b}$, temperature sensing of the Channel 0 and Channel 1 power stages is realized by the LTM4676 digitizing the voltages that appear at the PNP transistor temperature sensors that reside at pins $TSNS_{0b}$ and $TSNS_{1b}$, respectively. The LTM4676 performs what is known in the industry as delta VBE (ΔVBE) computations and makes channel (power stage) temperature telemetry available over I²C (READ_TEMPERATURE_1$_n$). The junction temperature of the control IC within the LTM4676 is also available over I²C (READ_TEMPERATURE_2). Observed peak Channel temperatures can be read back in registers READ_MFR_TEMPERATURE_1_PEAK$_n$. Observed peak temperature of the control IC can be read back in register MFR_READ_TEMPERATURE_2_PEAK.

For a fixed load current, the amplitude of the current sense information changes over temperature due to the temperature coefficient of copper (inductor DCR), which is approximately 3900ppm/°C. This would introduce significant current readback error over the operating range of the module if not for the fact that the LTM4676's temperature readback information is used in conjunction with the perceived current sense signal to yield temperature-corrected current readback data.

If desired, it is possible to use only the temperature readback information derived from the $TSNS_{0a}/TSNS_{0b}$ pins to yield temperature-corrected current readback data for both Channels 0 and 1. This frees up the Channel 1 temperature sensor to monitor a temperature sensor external to the LTM4676. This is achieved by setting MFR_PWM_MODE$_0$[4] = 1_b (the NVM-factory default value is 0_b). This degrades the current readback accuracy of Channel 1—more so when Channel 0 and Channel 1 are not paralleled outputs. However, the $TSNS_{1a}$ pin becomes available to be connected to an external diode-connected small-signal PNP transistor (such as 2N3906) and 10nF X7R capacitor, i.e., an external temperature sensor, whose temperature readback data and peak value are available over I²C (READ_TEMPERATURE_1$_1$, MFR_READ_TEMPERATURE_1_PEAK$_1$). Details on how to connect an external temperature sensor and 10nF capacitor to the $TSNS_{1a}$ pin are detailed in the LTC3880 data sheet (the $TSNS_{1a}$ pin of the LTM4676 is the $TSNS_1$ pin of LTM4676's internal control IC).

Power stage duty cycle readback telemetry is available over I²C (READ_DUTY_CYCLE$_n$ registers). Computed channel input current readback is computed by the LTM4676 as:

$$MFR\_READ\_IIN_n = READ\_DUTY\_CYCLE_n \bullet READ\_IOUT_n + MFR\_IIN\_OFFSET_n$$

Computed module input current readback is computed by the LTM4676 as:

$$READ\_IIN = MFR\_READ\_IIN_0 + MFR\_READ\_IIN_1$$

where MFR_IIN_OFFSET$_n$ is a register value representing the SV_{IN} input bias current. The SV_{IN} current is not digitized by the module. The factory NVM-default value of MFR_IIN_OFFSET$_n$ is 30.5mA, representing the contribution of current drawn by each of the module's channels

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on the SV_{IN} pin, when the power stages are operating in forced continuous mode at the factory-default switching frequency of 500kHz. See Table 8 in the Applications Information section for recommended MFR_IIN_OFFSET$_n$ setting vs Switching Frequency. The aforementioned method by which input current is calculated yields an accurate current readback value even at light load currents, but only as long as the module is configured for forced continuous operation (NVM-factory default). SV_{IN} and peak SV_{IN} readback telemetry is accessible via I^2C in the READ_VIN and MFR_VIN_PEAK registers, respectively.

The power stage switch nodes are brought out on the SW_n pin for functional operation monitoring and for optional installation of a resistor-capacitor snubber circuit (terminated to GND) for reduced EMI. Internal 2.2nF snubber capacitors connected directly to the switch nodes further facilitate implementation of a snubber network, if desired. See the Application Information section for details.

The LTM4676 features a write protect (WP) pin. If WP is open circuit or logic high, I^2C writes are severely restricted: only I^2C writes to the PAGE, OPERATION, CLEAR_FAULTS, MFR_CLEAR_PEAKS, and MFR_EE_UNLOCK commands are supported, with the exception that individual fault bits can be cleared by writing a "1_b" to the respective bits in the STATUS_* registers. Register reads are never restricted. Not to be confused with the WP pin, the LTM4676 features a WRITE_PROTECT register, which is also used to restrict I^2C writes to register contents. Refer to the LTC3880 data sheet for details. The WP pin and the WRITE_PROTECT register provide a level of protection against accidental changes to RAM and EEPROM contents.

The LTM4676 supports up to 16 possible slave addresses. The factory NVM-default slave address is 0x4F. The lower four bits of the LTM4676's slave address can be altered from this default value by connecting a resistor from this pin to SGND. See Table 5 in the Applications Information section for details.

Up to four LTM4676 modules (8 channels) can be paralleled, suitable for powering ~100A loads such as CPUs and GPUs. (See Figure 39.) The LTM4676 can be paralleled with LTM4620A or LTM4630 modules, as well (see Figures 40 and 41).

EEPROM

The LTM4676's control IC contains an internal EEPROM (non-volatile memory, NVM) to store configuration settings and fault log information. EEPROM endurance retention and mass write operation time are specified in the Electrical Characteristics and Absolute Maximum Ratings sections. Write operations at $T_J < 0°C$ or at $T_J > 85°C$ are possible although the Electrical Characteristics are not guaranteed and the EEPROM retention characteristics may be degraded. Read operations performed at junction temperatures between –40°C and 125°C do not degrade the EEPROM. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log-specific EEPROM locations (partitions). If occasional writes to these registers occur above 85°C junction, the slight degradation in the data retention characteristics of the fault log does not undermine the usefulness of the function.

It is recommended that the EEPROM not be written when the control IC die temperature is greater than 85°C. If the die temperature exceeds 130°C, the LTM4676's control IC disables all EEPROM write operations. EEPROM write operations are subsequently re-enabled when the die temperature drops below 125°C.

ADDITIONAL INFORMATION

An even more detailed account of the operation of the LTM4676's internal control IC can be perused in the LTC3880 data sheet. Be reminded of the differences between the LTM4676's control IC and the LTC3880, per Table 1.

Operational topics discussed in the LTC3880 data sheet not covered here—but are equally applicable to the LTM4676—follow:

- Bus Timeout Failure.
- Similarities Between PMBus, SMBus, and I^2C 2-Wire Interface.
- The PMBus Serial Digital Interface and Timing Diagrams.
- PMBus Data Format Terminology.
- Protocols for Reading/Writing to PMBus Registers of the LTM4676/LTC3880 Control ICs, Over I^2C/SMBus.

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The LTC3880 data sheet is an essential reference document for this product. To obtain it go to:

www.linear.com/LTC3880

LTM4676 CONTROL IC DIFFERENCES FROM LTC3880

The LTM4676 control IC is a slightly modified version of the LTC3880; differences between the LTC3880 and the LTM4676's control IC are summarized in Table 1. As such, it should stand to reason that the LTC3880 data sheet is a valuable reference document for the LTM4676 user, especially for newcomers to the PMBus suite of commands/command codes (registers) and working with I^2C/SMBus 2-wire interface.

Apart from exceptions noted in Table 1, the PMBus commands codes (registers) supported by the LTM4676 are identical in scope and data format to that of the LTC3880's. Refer to LTC3880's PMBus Command Summary and PMBus Command Details data sheet sections for detailed information on the supported command codes.

Note that the LTC3880 RCONFIG (resistor pin-strappable) pins require resistor networks from V_{DD25} to SGND, whereas the LTM4676 integrates the "top" resistors and therefore only requires pull-down (termination) resistors to SGND. As a result, the resistor pin-strap tables for the LTM4676 differ from the LTC3880. Additionally, the LTM4676's $F_{SWPHCFG}$ pin-strap options have been slightly modified compared to LTC3880's FREQ_CFG pin-strap options. Refer to Tables 2 to 5 in this data sheet for details.

The typical LTM4676 application circuit is shown in Figure 44 on the back page of this data sheet.

External capacitor selection is primarily determined by the maximum load current and output voltage. Refer to Table 20 for specific external capacitor requirements for particular applications.

Note that up to nine pull-up resistors are required for proper operation of the LTM4676:

- Three for the SMBus/I^2C interface (the SCL, SDA, and $\overline{\text{ALERT}}$ pins); two, only if the system SMBus host does not make use of the $\overline{\text{ALERT}}$ interrupt.
- One each for the RUN_0 and RUN_1 pins (or, just one to RUN_0 and RUN_1, if RUN_0 and RUN_1 are electrically connected together).
- One each for $\overline{GPIO}_0$ and $\overline{GPIO}_1$ (or, just one to $\overline{GPIO}_0$ and $\overline{GPIO}_1$, if $\overline{GPIO}_0$ and $\overline{GPIO}_1$ are electrically connected together).
- One on SHARE_CLK, required, for the LTM4676 to establish a heartbeat time base for timing-related operations and functions (output voltage ramp-up timing, voltage margining transition timing, SYNC open-drain drive frequency).
- One on SYNC, in order for the LTM4676 to phase lock to the frequency generated by the open-drain output of its digital engine. EXCEPTION: in some applications, it is desirable to drive the LTM4676's SYNC pin with a hard-driven (low impedance) external clock. This is the only scenario where the LTM4676 does not require a pull-up resistor on SYNC. However, be aware that the SYNC pin can be low impedance during NVM initialization, i.e., during download of EEPROM contents to RAM (for ~50ms [Note 12] after SV_{IN} power is applied). Therefore, the hard-driven clock signal should only be applied to the LTM4676 SYNC pin through a series resistor whose impedance limits current into the SYNC pin during NVM initialization to less than 10mA. Furthermore, any clock signal should be provided prior to the RUN_n pins toggle from logic low to logic high, or else the switching frequency of the LTM4676 will start off at the low end of its PLL-capture range (~225kHz) until the SYNC clock becomes established.

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Table 1. Summary of Supported Commands and Differences Between the LTM4676's Control IC and the LTC3880 (Items of Greatest Significance Indicated by Gray-Shaded Cells; Common Commands, Values and Attributes Indicated by Non-Shaded, Merged Cells)

PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTC3880 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	LTM4676 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES
$FREQ_{CFG}$ (or $F_{SWPHCFG}$) Pin-Strap Options	N/A	Switching frequency and phase-angle pin-strap table.	Look-up table for pin-strapping options on setting Channel phase angles and power-up switching frequency is different. $FREQ_{CFG}$ pin on the LTC3880; $F_{SWPHCFG}$ pin on the LTM4676. See Table 4 of this data sheet.	
PAGE	0x00	Channel or page currently targeted for paged communications.	No difference: 0x00, read/write, non-paged, not stored in NVM.	
$OPERATION_n$	0x01	Operating mode control. On/off, margin high and margin low.	No difference: 0x80, read/write, paged, stored in user-editable NVM.	
$ON\_OFF\_CONFIG_n$	0x02	RUN_n pin and On/Off Configuration.	0x1E, read/write, paged, stored in user-editable NVM.	0x1F, read/write, paged, stored in user-editable NVM.
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	No difference: default value not applicable, send byte only, non-paged, not stored in NVM.	
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	No difference: 0x00, read/write, non-paged, stored in user-editable NVM.	
STORE_USER_ALL	0x15	Store user operating memory to EEPROM (user-editable NVM).	No difference: default value not applicable, send byte only, non-paged, not stored in NVM.	
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Default value not applicable, send byte only, non-paged, not stored in NVM.	Reserved. Execute MFR_RESET command (0xFD), instead.
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	No difference: 0xB0, read-only, non-paged, not stored in NVM.	
$VOUT\_MODE_n$	0x20	Output voltage format/exponent.	No difference: 0x14 (2^{-12}), read-only, paged, not stored in NVM.	
$VOUT\_COMMAND_n$	0x21	Nominal output voltage set point.	No difference: 0x1000 (1.000V), read/write, paged, stored in user-editable NVM.	
$VOUT\_MAX_n$	0x24	The upper limit on the commandable output voltage.	Page 0x00: 0x4189 (4.096V). Page 0x01: 0x5800 (5.500V). Read/write, paged, stored in user-editable NVM.	Page 0x00: 0x4000 (4.000V). Page 0x01: 0x5666 (5.400V). Read/write, paged, stored in user-editable NVM.
$VOUT\_MARGIN\_HIGH_n$	0x25	Margin high output voltage set point. Must be greater than $VOUT\_COMMAND_n$.	No difference: 0x10CD (1.050V), read/write, paged, stored in user-editable NVM.	
$VOUT\_MARGIN\_LOW_n$	0x26	Margin low output voltage set point. Must be less than $VOUT\_COMMAND_n$.	No difference: 0x0F33 (0.950V), read/write, paged, stored in user-editable NVM.	
$VOUT\_TRANSITION\_RATE_n$	0x27	The rate at which the output voltage changes when $VOUT_n$ is commanded to a new value via I^2C.	0xAA00 (0.25V/ms), read/write, paged, stored in user-editable NVM.	0x8042 (0.001V/ms). Read/write, paged, stored in user-editable NVM.
FREQUENCY_SWITCH	0x33	The switching frequency setting.	0xFABC (350kHz), read/write, non-paged, stored in user-editable NVM.	0xFBE8 (500kHz), read/write, non-paged, stored in user-editable NVM.
VIN_ON	0x35	The undervoltage lockout (UVLO)-rising threshold.	0xCB40 (6.5V), as monitored on the LTC3880's "V_{IN}" pin, read/write, non-paged, stored in user-editable NVM.	0xCAC0 (5.500V), as monitored on the LTM4676's "SV_{IN}" pin, read/write, non-paged, stored in user-editable NVM.

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PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTC3880 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	LTM4676 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES
VIN_OFF	0x36	The undervoltage lockout (UVLO)-falling threshold.	0xCB00 (6.0V) , as monitored on the LTC3880's "V_{IN}" pin, read/write, non-paged, stored in user-editable NVM.	0xCAA0 (5.250V) , as monitored on the LTM4676's "SV_{IN}" pin, read/write, non-paged, stored in user-editable NVM.
IOUT_CAL_GAIN$_n$	0x38	The ratio of the voltage at the control IC's current-sense pins to the sensed current, in mΩ, at 25°C.	1.8mΩ, read/write, paged, stored in user-editable NVM.	Trimmed at ATE, read-only, stored in factory-only NVM.
VOUT_OV_FAULT_LIMIT$_n$	0x40	Output overvoltage fault limit.	No difference: 0x119A (1.100V), read/write, paged, stored in user-editable NVM.	
VOUT_OV_FAULT_RESPONSE$_n$	0x41	Action to be taken by the device when an output overvoltage fault is detected.	0xB8 (non-latching shutdown; autonomous restart upon fault removal), read/write, paged, stored in user-editable NVM.	0x7A (non-latching shutdown; autonomous restart upon fault removal; 20µs glitch filter), read/write, paged, stored in user-editable NVM.
VOUT_OV_WARN_LIMIT$_n$	0x42	Output overvoltage warning threshold.	0x1133 (1.075V), read/write, paged, stored in user-editable NVM.	0x111F (1.070V), read/write, paged, stored in user-editable NVM.
VOUT_UV_WARN_LIMIT$_n$	0x43	Output undervoltage warning threshold.	0x0ECD (0.925V), read/write, paged, stored in user-editable NVM.	0x0EE1 (0.930V), read/write, paged, stored in user-editable NVM.
VOUT_UV_FAULT_LIMIT$_n$	0x44	Output undervoltage fault limit.	No difference: 0x0E66 (0.900V), read/write, paged, stored in user-editable NVM.	
VOUT_UV_FAULT_RESPONSE$_n$	0x45	Action to be taken by the device when an output undervoltage fault is detected.	No difference: 0xB8 (non-latching shutdown; autonomous restart upon fault removal), read/write, paged, stored in user-editable NVM.	
IOUT_OC_FAULT_LIMIT$_n$	0x46	Output overcurrent fault threshold (cycle-by-cycle inductor peak current).	0xDBB8 (29.75A), read/write, paged, stored in user-editable NVM.	0xDADB (22.84A), read/write, paged, stored in user-editable NVM.
IOUT_OC_FAULT_RESPONSE$_n$	0x47	Action to be taken by the device when an output overcurrent fault is detected.	No difference: 0x00 (try to regulate through the fault condition/event; limit the cycle-by-cycle peak of the inductor current to not exceed the commanded IOUT_OC_FAULT_LIMIT), read/write, paged, stored in user-editable NVM.	
IOUT_OC_WARN_LIMIT$_n$	0x4A	Output overcurrent warning threshold (time-averaged inductor current).	0xDA80 (20.00A), read/write, paged, stored in user-editable NVM.	0xD3E6 (15.59A), read/write, paged, stored in user-editable NVM.
OT_FAULT_LIMIT$_n$	0x4F	Overtemperature fault threshold.	0xEB20 (100°C), read/write, paged, stored in user-editable NVM.	0xF200 (128°C), read/write, paged, stored in user-editable NVM.
OT_FAULT_RESPONSE$_n$	0x50	Action to be taken by the device when an overtemperature fault is detected via TSNS$_{na}$ (TSNSn).	No difference: 0xB8 (non-latching shutdown; autonomous restart upon fault removal), read/write, paged, stored in user-editable NVM.	
OT_WARN_LIMIT$_n$	0x51	Overtemperature warning threshold.	0xEAA8 (85°C), read/write, paged, stored in user-editable NVM.	0xEBE8 (125°C), read/write, paged, stored in user-editable NVM.
UT_FAULT_LIMIT$_n$	0x53	Undertemperature fault threshold.	0xE580 (–40°C), read/write, paged, stored in user-editable NVM.	0xE530 (–45°C), read/write, paged, stored in user-editable NVM.
UT_FAULT_RESPONSE$_n$	0x54	Response to undertemperature fault events.	0xB8 (non-latching shutdown; autonomous restart upon fault removal), read/write, paged, stored in user-editable NVM.	0x00 (ignore; continue without interruption), read/write, paged, stored in user-editable NVM, read/write, paged, stored in user-editable NVM.
VIN_OV_FAULT_LIMIT	0x55	Input supply (SV_{IN}) overvoltage fault limit.	0xD3E0 (15.5V), read/write, non-paged, stored in user-editable NVM.	0xDB60 (27.0V), read/write, non-paged, stored in user-editable NVM.

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PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTC3880 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	LTM4676 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES
VIN_OV_FAULT_RESPONSE$_n$	0x56	Response to input overvoltage fault events.	0x80 (latched-off shutdown), read/write, paged, stored in user-editable NVM.	0xB8 (non-latching shutdown; autonomous restart upon fault removal), read/write, paged, stored in user-editable NVM.
VIN_UV_WARN_LIMIT	0x58	Input undervoltage warning threshold.	0xCB26 (6.297V), read/write, non-paged, stored in user-editable NVM.	0xCAA6 (5.297V), read/write, non-paged, stored in user-editable NVM.
IIN_OC_WARN_LIMIT	0x5D	Input supply overcurrent warning threshold.	0xD280 (10A), read/write, non-paged, stored in user-editable NVM.	0xD300 (12A), read/write, non-paged, stored in user-editable NVM.
POWER_GOOD_ON$_n$	0x5E	Output voltage at or above which a power good should be asserted.	No difference: 0x0EE1 (0.9299V), read/write, paged, stored in user-editable NVM.	
POWER_GOOD_OFF$_n$	0x5F	Output voltage at or below which a power good should be de-asserted.	No difference: 0x0EB8 (0.9199V), read/write, paged, stored in user-editable NVM.	
TON_DELAY$_n$	0x60	Time from RUN$_n$ and/or OPERATION$_n$ on to output rail turn-on.	No difference: 0x8000 (0ms), read/write, paged, stored in user-editable NVM.	
TON_RISE$_n$	0x61	Time from when the output voltage reference starts to rise until it reaches its commanded setting.	0xD200 (8ms), read/write, paged, stored in user-editable NVM.	0xC300 (3ms), read/write, paged, stored in user-editable NVM.
TON_MAX_FAULT_LIMIT$_n$	0x62	Turn-on watchdog timeout fault threshold (time permitted for VOUT$_n$ to reach or exceed VOUT_UV_FAULT_LIMIT$_n$ after turn-on command is received).	0xD280 (10ms), read/write, paged, stored in user-editable NVM.	0xCA80 (5ms), read/write, paged, stored in user-editable NVM.
TON_MAX_FAULT_RESPONSE$_n$	0x63	Action to be taken by the device when a TON_MAX_FAULT$_n$ event is detected.	No difference: 0xB8 (non-latching shutdown; autonomous restart upon fault removal), read/write, paged, stored in user-editable NVM.	
TOFF_DELAY$_n$	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL$_n$ ramp.	No difference: 0x8000 (0ms), read/write, paged, stored in user-editable NVM.	
TOFF_FALL$_n$	0x65	Time from when the output voltage reference starts to fall until it reaches 0V.	0xD200 (8ms), read/write, paged, stored in user-editable NVM.	0xC300 (3ms), read/write, paged, stored in user-editable NVM.
TOFF_MAX_WARN_LIMIT$_n$	0x66	Turn-off watchdog timeout fault threshold (time permitted for VOUT$_n$ to decay to or below 12.5% of the commanded VOUT$_n$ value at the time of receiving a turn-off command).	0xF258 (150ms), read/write, paged, stored in user-editable NVM.	0x8000 (no limit; warning is disabled), read/write, paged, stored in user-editable NVM.
STATUS_BYTE$_n$	0x78	One byte summary of the unit's fault condition.	No difference: default value not applicable, read/write, paged, not stored in NVM.	
STATUS_WORD$_n$	0x79	Two byte summary of the unit's fault condition.	No difference: default value not applicable, read/write, paged, not stored in NVM.	
STATUS_VOUT$_n$	0x7A	Output voltage fault and warning status.	No difference: default value not applicable, read/write, paged, not stored in NVM.	
STATUS_IOUT$_n$	0x7B	Output current fault and warning status.	No difference: default value not applicable, read/write, paged, not stored in NVM.	
STATUS_INPUT	0x7C	Input supply (SV_{IN}) fault and warning status.	No difference: default value not applicable, read/write, non-paged, not stored in NVM.	

APPLICATIONS INFORMATION

PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTC3880 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	LTM4676 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES
STATUS_ TEMPERATURE$_n$	0x7D	TSNS$_{na}$ (TSNSn)-sensed temperature fault and warning status for READ_TEMERATURE_1$_n$.	No difference: default value not applicable, read/write, paged, not stored in NVM.	
STATUS_CML	0x7E	Communication and memory fault and warning status.	No difference: default value not applicable, read/write, non-paged, not stored in NVM.	
STATUS_MFR_ SPECIFIC$_n$	0x80	Manufacturer specific fault and state information.	No difference: default value not applicable, read/write, paged, not stored in NVM.	
READ_VIN	0x88	Measured input supply (SV_{IN}) voltage.	No difference: default value not applicable, read-only, non-paged, not stored in NVM.	
READ_IIN	0x89	Calculated total input supply current.	No difference: default value not applicable, read-only, non-paged, not stored in NVM.	
READ_VOUT$_n$	0x8B	Measured output voltage.	No difference: default value not applicable, read-only, paged, not stored in NVM.	
READ_IOUT$_n$	0x8C	Measured output current.	No difference: default value not applicable, read-only, paged, not stored in NVM.	
READ_ TEMPERATURE_1$_n$	0x8D	Measurement of TSNS$_{na}$ (TSNSn)-sensed temperature.	No difference: default value not applicable, read-only, paged, not stored in NVM.	
READ_ TEMPERATURE2	0x8E	Measured control IC junction temperature.	No difference: default value not applicable, read-only, non-paged, not stored in NVM.	
READ_DUTY_ CYCLE$_n$	0x94	Measured duty cycle of MT$_n$.	No difference: default value not applicable, read-only, paged, not stored in NVM.	
READ_POUT$_n$	0x96	Calculated output power.	No difference: default value not applicable, read-only, paged, not stored in NVM.	
PMBUS_REVISION	0x98	PMBus revision supported by this device.	No difference: 0x11 (Revision 1.1 of Part I and Revision 1.1 of Part II of PMBus Specification documents), read-only, non-paged, not stored in NVM.	
MFR_ID	0x99	Manufacturer identification, in ASCII	No difference: “LTC”, read-only, non-paged.	
MFR_MODEL	0x9A	Manufacturer’s part number, in ASCII	“LTC3880”, read-only, non-paged.	“LTM4676”, read-only, non-paged.
MFR_SERIAL	0x9E	Serial number of this specific unit.	No difference: Up to nine bytes of custom-formatted data that identify the unit’s configuration, read-only, non-paged.	
MFR_VOUT_MAX$_n$	0xA5	Maximum allowed output voltage.	No difference: 0x4189 (4.096V) on Channel 0, 0x5800 (5.500V) on Channel 1. Read-only, paged, not stored in user-editable NVM.	
USER_DATA_00	0xB0	OEM reserved data.	Read/write, non-paged, stored in user-editable NVM. Recommended against altering.	Read/write, non-paged, stored in user-editable NVM. Recommended against altering.
USER_DATA_01$_n$	0xB1	OEM reserved data.	Read/write, paged, stored in user-editable NVM. Recommended against altering.	Read/write, paged, stored in user-editable NVM. Recommended against altering.
USER_DATA_02	0xB2	OEM reserved data.	Read/write, non-paged, stored in user-editable NVM. Recommended against altering.	Read/write, non-paged, stored in user-editable NVM. Recommended against altering.
USER_DATA_03$_n$	0xB3	User-editable words available for the user.	No difference: 0x0000, read/write, paged, stored in user-editable NVM.	
USER_DATA_04	0xB4	A user-editable word available for the user.	No difference: 0x0000, read/write, non-paged, stored in user-editable NVM.	

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PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTC3880 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	LTM4676 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	No difference: default value not applicable, read/write, non-paged, not stored in NVM.	
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	No difference: default value not applicable, read/write, non-paged, not stored in NVM.	
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	No difference: default value not applicable, read/write, non-paged, not stored in NVM.	
MFR_CHAN_CONFIG_*$_n$	0xD0	Channel-specific configuration bits.	0x1F, read/write, paged, stored in user-editable NVM. Register is named “MFR_CHAN_CONFIG_LTC3880”.	0x1F, read/write, paged, stored in user-editable NVM. Register is named “MFR_CHAN_CONFIG” and referred to as “MFR_CHAN_CONFIG_LTM467X” in LTpowerPlay.
MFR_CONFIG_ALL_*	0xD1	Global configuration bits, i.e., common to both V_{OUT} channels 0 and 1.	0x09, read/write, non-paged, stored in user-editable NVM. Register is named “MFR_CONFIG_ALL_LTC3880”.	0x09, read/write, non-paged, stored in user-editable NVM. Register is named “MFR_CONFIG_ALL” and referred to as “MFR_CONFIG_ALL_LTM467X” in LTpowerPlay.
MFR_GPIO_PROPAGATE_*$_n$	0xD2	Configuration bits for propagating faults to the GPIO$_n$ pins.	0x2997, read/write, paged, stored in user-editable NVM. Register is named “MFR_GPIO_PROPAGATE_LTC3880”.	0x6893, read/write, paged, stored in user-editable NVM. Register is named “MFR_GPIO_PROPAGATE” and referred to as “MFR_GPIO_PROPAGATE_LTM467X” in LTpowerPlay.
MFR_PWM_MODE_*$_n$	0xD4	Configuration for the PWM engine of each V_{OUT} channel.	0xC2, read/write, paged, stored in user-editable NVM. Bit 4 is reserved and should be 0_b. Register is named “MFR_PWM_MODE_LTC3880”.	0xC2, read/write, paged, stored in user-editable NVM. When bit 4 of Page 0 (MFR_PWM_MODE_LTM4676$_0$[4]) is 0_b, Channel temperature-sensing is performed per LTC3880 documentation. When MFR_PWM_MODE_LTM4676$_0$[4]= 1_b, T_{SNS1A} monitors a temperature sensor external to the LTM4676, per the Operation section. Register is named “MFR_PWM_MODE” and referred to as “MFR_PWM_MODE_LTM467X” in LTpowerPlay.
MFR_GPIO_RESPONSE$_n$	0xD5	Action to be taken by the device when the GPIO$_n$ pin is asserted low by circuitry external to the unit.	No difference: 0xC0 (make the respective output’s power stage high impedance, i.e., three-stated; autonomous restart upon fault removal), read/write, paged, stored in user-editable NVM.	
MFR_OT_FAULT_RESPONSE	0xD6	Action to be taken by the device when a control IC junction overtemperature fault is detected.	No difference: 0xC0 (make the respective output’s power stage high impedance, i.e., three-stated; autonomous restart upon fault removal), read-only, non-paged, not stored in user-editable NVM.	
MFR_IOUT_PEAK$_n$	0xD7	Maximum measured value of READ_IOUT$_n$ since the last MFR_CLEAR_PEAKS.	No difference: default value not applicable, read-only, paged, not stored in NVM.	
MFR_CHANNEL_ADDRESS$_n$	0xD8	Address to the PAGE-activated channel.	No difference: 0x80, read/write, paged, stored in user-editable NVM.	

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PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTC3880 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	LTM4676 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES
MFR_RETRY_DELAY$_n$	0xDB	Retry interval during fault-retry mode.	0xFABC (350ms), read/write, paged, stored in user-editable NVM.	0xF3E8 (250ms), read/write, paged, stored in user-editable NVM.
MFR_RESTART_DELAY$_n$	0xDC	Minimum interval (nominal) the RUN$_n$ pin is pulled logic low by internal circuitry.	0xFBE8 (500ms), read/write, paged, stored in user-editable NVM.	0xF258 (150ms), read/write, paged, stored in user-editable NVM.
MFR_VOUT_PEAK$_n$	0xDD	Maximum measured value of READ_VOUT$_n$ since the last MFR_CLEAR_PEAKS.	No difference: default value not applicable, read-only, paged, not stored in NVM.	
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since the last MFR_CLEAR_PEAKS.	No difference: default value not applicable, read-only, non-paged, not stored in NVM.	
MFR_TEMPERATURE_1_PEAK$_n$	0xDF	Maximum value of TSNS$_{na}$ (TSNSn)-measured temperature since the last MFR_CLEAR_PEAKS.	No difference: default value not applicable, read-only, paged, not stored in NVM.	
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	No difference: default value not applicable, send byte only, non-paged, not stored in NVM.	
MFR_PADS	0xE5	Digital status of the I/O pads.	No difference: default value not applicable, read-only, non-paged, not stored in NVM.	
MFR_ADDRESS	0xE6	The 7 bits of the LTM4676's I^{2}C slave address.	0x4F, read/write, non-paged, stored in user-editable NVM. Least significant four bits augmented by ASEL resistor network. Can take on value 0x80 to disable device-specific addressing.	0x4F, read-only, non-paged, stored in factory-only NVM. Least significant four bits augmented by ASEL resistor pin-strap. Cannot take on value 0x80; device-specific addressing cannot be disabled.
MFR_SPECIAL_ID	0xE7	Manufacturer code representing IC silicon and revision	0x40XX, read-only, non-paged.	0x448X or 0x440X, read-only, non-paged.
MFR_IIN_OFFSET$_n$	0xE9	Coefficient used in calculations of READ_IIN and MFR_READ_IIN$_n$, representing the contribution of input current drawn by the control IC, including the MOSFET drivers.	0x9333 (0.0500A), read/write, paged, stored in user-editable NVM.	0x8BE7 (0.0305A), read/write, paged, stored in user-editable NVM.
MFR_FAULT_LOG_STORE	0xEA	Commands a transfer of the fault log from RAM to EEPROM. This causes the part to behave as if a channel has faulted off.	No difference: default value not applicable, send byte only, non-paged, not stored in NVM.	
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	No difference: default value not applicable, send byte only, non-paged, not stored in NVM.	

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PMBus COMMAND NAME, OR FEATURE	CMD CODE (REGISTER)	COMMAND OR FEATURE DESCRIPTION	LTC3880 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES	LTM4676 NVM FACTORY-DEFAULT VALUE AND/OR ATTRIBUTES
MFR_READ_IIN$_n$	0xED	Calculated input current, by channel.	No difference: default value not applicable, read-only, paged, not stored in NVM.	
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	No difference: default value not applicable, read-only, non-paged, stored in fault-log NVM.	
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple LTC ICs/ modules.	No difference: default value not applicable, read-only, non-paged, not stored in NVM.	
MFR_COMPARE_ USER_ALL	0xF0	Compares current command contents (RAM) with NVM.	No difference: default value not applicable, send byte only, non-paged, not stored in NVM.	
MFR_ TEMPERATURE_2_ PEAK	0xF4	Maximum measured control IC junction temperature since last MFR_CLEAR_PEAKS.	No difference: default value not applicable, read-only, non-paged, not stored in NVM.	
MFR_PWM_ CONFIG_*	0xF5	Configuration bits for setting the phase interleaving angles and output voltage ranges of Channels 0 and 1, and SHARE_CLK behavior in UVLO.	0x10, read/write, non-paged, stored in user-editable NVM. Register is named “MFR_PWM_CONFIG_ LTC3880”.	0x10, read/write, non-paged, stored in user-editable NVM. Register is named “MFR_PWM_CONFIG” and referred to as “MFR_PWM_CONFIG_LTM467X” in LTpowerPlay.
MFR_IOUT_CAL_ GAIN_TC$_n$	0xF6	Temperature coefficient of the current sensing element.	0x0F3C (3900ppm/°C), read/write, paged, stored in user-editable NVM.	0x0F14 (3860ppm/°C), read/write, paged, stored in user-editable NVM.
MFR_TEMP_1_ GAIN$_n$	0xF8	Sets the slope of the temperature sensors that interface to TSNS$_{na}$ (TSNS*n*).	No difference: 0x4000 (1.0, in custom units), read/write, paged, stored in NVM.	
MFR_TEMP_1_ OFFSET$_n$	0xF9	Sets the offset of the TSNS$_{na}$ (TSNS*n*) temperature sensor with respect to –273.1°C.	No difference: 0x8000 (0.0), read/write, paged, stored in NVM.	
MFR_RAIL_ ADDRESS$_n$	0xFA	Common address for PolyPhase outputs to adjust common parameters.	No difference: 0x80, read/write, paged, stored in NVM.	
MFR_RESET	0xFD	Commanded reset without requiring a power down.	No difference: default value not applicable, send byte only, non-paged, not stored in NVM.	

APPLICATIONS INFORMATION

Table 2. $V_{OUTnCFG}$ Pin Strapping Look-Up Table for the LTM4676's Output Voltage, Coarse Setting (Not Applicable if MFR_CONFIG_ALL[6] = 1_b)

$R_{VOUTnCFG}$* (kΩ)	V_{OUTn} (V) SETTING COARSE	MFR_PWM_CONFIG[6-*n*] BIT
Open	NVM	NVM
32.4	See Table 3	See Table 3
22.6	3.3	0
18.0	3.1	0
15.4	2.9	0
12.7	2.7	0
10.7	2.5	0, if V_{TRIMn} > 0mV 1, if V_{TRIMn} ≤ 0mV
9.09	2.3	1
7.68	2.1	1
6.34	1.9	1
5.23	1.7	1
4.22	1.5	1
3.24	1.3	1
2.43	1.1	1
1.65	0.9	1
0.787	0.7	1
0	0.5	1

*$R_{VOUTnCFG}$ value indicated is nominal. Select $R_{VOUTnCFG}$ from a resistor vendor such that its value is always within 3% of the value indicated in the table. Take into account resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect $R_{VOUTnCFG}$'s value over time. All such effects must be taken into account in order for resistor pin strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET, over the lifetime of one's product.

Table 3. $V_{TRIMnCFG}$ Pin Strapping Look-Up Table for the LTM4676's Output Voltage, Fine Adjustment Setting (Not Applicable if MFR_CONFIG_ALL[6] = 1_b)

$R_{VTRIMnCFG}$* (kΩ)	V_{TRIM} (mV) FINE ADJUSTMENT TO V_{OUTn} SETTING WHEN RESPECTIVE $R_{VOUTnCFG} \neq$ 32.4kΩ	V_{OUTn} OUTPUT VOLTAGE SETTING (V) WHEN $V_{OUTnCFG}$ PIN USES R_{CFG} = 32.4kΩ	MFR_PWM_CONFIG[6-*n*] BIT
Open	0	NVM	0, if VOUT_OV_FAULT_LIMIT$_n$ > 2.75V 1, if VOUT_OV_FAULT_LIMIT$_n$ ≤ 2.75V
32.4	99		
22.6	86.625		
18.0	74.25		
15.4	61.875		
12.7	49.5		
10.7	37.125	5.50	0
9.09	24.75	5.25	0
7.68	12.375	5.00	0
6.34	–12.375	4.75	0
5.23	–24.75	4.50	0
4.22	–37.125	4.25	0
3.24	–49.5	4.00	0
2.43	–61.875	3.75	0
1.65	–74.25	3.63	0
0.787	–86.625	3.50	0
0	–99	3.46	0

*$R_{VTRIMnCFG}$ value indicated is nominal. Select $R_{VTRIMnCFG}$ from a resistor vendor such that its value is always within 3% of the value indicated in the table. Take into account resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect $R_{VTRIMnCFG}$'s value over time. All such effects must be taken into account in order for resistor pin strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET, over the lifetime of one's product.

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Table 4. $F_{SWPHCFG}$ Pin Strapping Look-Up Table to Set the LTM4676's Switching Frequency and Channel Phase-Interleaving Angle (Not Applicable if MFR_CONFIG_ALL[6] = 1_b)

$R_{FSWPHCFG}$* (kΩ)	SWITCHING FREQUENCY (kHz)	θ_{SYNC} TO θ_0	θ_{SYNC} TO θ_1	bits [2:0] of MFR_PWM_CONFIG
Open	NVM; LTM4676 Default = 500	NVM; LTM4676 Default = 0°	NVM; LTM4676 Default = 180°	NVM; LTM4676 Default = 000_b
32.4	250	0°	180°	000_b
22.6	350	0°	180°	000_b
18.0	425	0°	180°	000_b
15.4	575	0°	180°	000_b
12.7	650	0°	180°	000_b
10.7	750	0°	180°	000_b
9.09	1000	0°	180°	000_b
7.68	500	120°	240°	100_b
6.34	500	90°	270°	001_b
5.23	External**	0°	240°	010_b
4.22	External**	0°	120°	011_b
3.24	External**	60°	240°	101_b
2.43	External**	120°	300°	110_b
1.65	External**	90°	270°	001_b
0.787	External**	0°	180°	000_b
0	External**	120°	240°	100_b

*$R_{FSWPHCFG}$ value indicated is nominal. Select $R_{FSWPHCFG}$ from a resistor vendor such that its value is always within 3% of the value indicated in the table. Take into account resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock/cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect $R_{FSWPHCFG}$'s value over time. All such effects must be taken into account in order for resistor pin-strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET, over the lifetime of one's product.

**"External" setting corresponds to FREQUENCY_SWITCH (Register 0x33) value set to 0x0000; the device synchronizes its switching frequency to that of the clock provided on the SYNC pin.

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Table 5. ASEL Pin Strapping Look-Up Table to Set the LTM4676's Slave Address (Applicable Regardless of MFR_CONFIG_ALL[6] Setting)

R_{ASEL}* (kΩ)	SLAVE ADDRESS
Open	100_1111_R/W
32.4	100_1111_R/W
22.6	100_1110_R/W
18.0	100_1101_R/W
15.4	100_1100_R/W
12.7	100_1011_R/W
10.7	100_1010_R/W
9.09	100_1001_R/W
7.68	100_1000_R/W
6.34	100_0111_R/W
5.23	100_0110_R/W
4.22	100_0101_R/W
3.24	100_0100_R/W
2.43	100_0011_R/W
1.65	100_0010_R/W
0.787	100_0001_R/W
0	100_0000_R/W

where:

R/W = Read/Write bit in control byte.
All PMBus device addresses listed in the specification are 7 bits wide unless otherwise noted.
Note: The LTM4676 will always respond to slave address 0x5A and 0x5B regardless of the NVM or ASEL resistor configuration values.

*R_{CFG} value indicated is nominal. Select R_{CFG} from a resistor vendor such that its value is always within 3% of the value indicated in the table. Take into account resistor initial tolerance, T.C.R. and resistor operating temperatures, soldering heat/IR reflow, and endurance of the resistor over its lifetime. Thermal shock cycling, moisture (humidity) and other effects (depending on one's specific application) could also affect R_{CFG}'s value over time. All such effects must be taken into account in order for resistor pin-strapping to yield the expected result at every SV_{IN} power-up and/or every execution of MFR_RESET, over the lifetime of one's product.

Table 6. LTM4676 MFR_ADDRESS Command Examples Expressed in 7- and 8-Bit Addressing

DESCRIPTION	HEX DEVICE ADDRESS 7 BIT	8 BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	R/W
Rail[4]	0x5A	0xB4	0	1	0	1	1	0	1	0	0
Global[4]	0x5B	0xB6	0	1	0	1	1	0	1	1	0
Default	0x4F	0x9E	0	1	0	0	1	1	1	1	0
Example 1	0x40	0x80	0	1	0	0	0	0	0	0	0
Example 2	0x41	0x82	0	1	0	0	0	0	0	1	0
Disabled[2,3]			1	0	0	0	0	0	0	0	0

Note 1: This table can be applied to the $MFR\_CHANNEL\_ADDRESS_n$ and $MFR\_RAIL\_ADDRESS_n$ commands, but not the MFR_ADDRESS command.

Note 2: A disabled value in one command does not disable the device, nor does it disable the Global address.

Note 3: A disabled value in one command does not inhibit the device from responding to device addresses specified in other commands.

Note 4: It is not recommended to write the value 0x00, 0x0C (7 bit), or 0x5A (7 bit) or 0x5B (7 bit) to the $MFR\_CHANNEL\_ADDRESS_n$ or the $MFR\_RAIL\_ADDRESS_n$ commands.

APPLICATIONS INFORMATION

V_{IN} TO V_{OUT} STEP-DOWN RATIOS

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage. Each output of the LTM4676 is capable of 95% duty cycle at 500kHz, but the V_{IN} to V_{OUT} minimum dropout is still a function of its load current and will limit output current capability related to high duty cycle on the topside switch. Minimum on-time $t_{ON(MIN)}$ is another consideration in operating at a specified duty cycle while operating at a certain frequency due to the fact that $t_{ON(MIN)} < D/f_{SW}$, where D is duty cycle and f_{SW} is the switching frequency. $t_{ON(MIN)}$ is specified in the electrical parameters as 90ns. See Note 6 in the Electrical Characteristics section for output current guideline.

INPUT CAPACITORS

The LTM4676 module should be connected to a low ac-impedance DC source. For the regulator input four 22µF input ceramic capacitors are used to handle the RMS ripple current. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated as:

$$D_n = \frac{V_{OUTn}}{V_{INn}}$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CINn(RMS)} = \frac{I_{OUTn(MAX)}}{\eta\%} \bullet \sqrt{D_n \bullet (1-D_n)}$$

In the above equation, $\eta\%$ is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor, or a Polymer capacitor.

OUTPUT CAPACITORS

The LTM4676 is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range for each output is from 400µF to 700µF. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spikes is required. Table 20 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 6.5A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 20 matrix, and the Linear Technology µModule Power Design Tool will be provided for stability analysis. Multiphase operation reduces effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The Linear Technology µModule Power Design Tool can calculate the output ripple reduction as the number of implemented phases increases by N times. A small value 10Ω resistor can be placed in series from V_{OUTn} to the V_{OSNS0}^+ or V_{OSNS1} pin to allow for a bode plot analyzer to inject a signal into the control loop and validate the regulator stability.

LIGHT LOAD CURRENT OPERATION

The LTM4676 has three modes of operation including high efficiency Burst Mode operation, discontinuous conduction mode or forced continuous conduction mode. Mode selection is done using the MFR_PWM_MODE$_n$ command (discontinuous conduction is always the start-up mode, forced continuous is the default running mode).

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In Burst Mode operation, the peak current in the inductor is set to approximately one-third of the maximum sense voltage even though the voltage on the $COMP_{na}$ pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the $COMP_{na}$ pin. When the $COMP_{na}$ voltage drops below approximately 0.5V, the internal Burst Mode operation asserts and both power stage MOSFETs are turned off. In Burst Mode operation, the load current is supplied by the output capacitor. As the output voltage decreases, the EA output begins to rise. When the output voltage drops sufficiently, Burst Mode operation is deasserted, and the controller resumes normal operation by turning on the top MOSFET (MT*n*) on the next PWM cycle.

If a channel is enabled for Burst Mode or discontinuous mode operation, the inductor current is not allowed to reverse. The reverse current comparator, I_{REV}, turns off the bottom MOSFET (MB*n*) just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller can operate in discontinuous (pulse-skippng)operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined solely by the voltage on the $COMP_{na}$ pin. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode exhibits lower output ripple and less interference with audio circuitry. Forced continuous conduction mode may result in reverse inductor current, which can cause the input supply to boost. The VIN_OV_FAULT_LIMIT can detect this (if SV_{IN} is connected to V_{IN0} and/or V_{IN1}) and turn off the offending channel. However, this fault is based on an ADC read and can nominally take up to 100ms to detect. If there is a concern about the input supply boosting, keep the part in discontinuous conduction or Burst Mode operation.

If the part is set to Burst Mode operation, as the inductor average current increases, the controller automatically modifies the operation from Burst Mode operation, to discontinuous mode to continuous mode.

SWITCHING FREQUENCY AND PHASE

The switching frequency of the LTM4676's channels is established by its analog phase-locked-loop (PLL) locking on to the clock present at the module's SYNC pin. The clock waveform on the SYNC pin can be generated by the LTM4676's internal circuitry when an external pull-up resistor to 3.3V (e.g., V_{DD33}) is provided, in combination with the LTM4676 control IC's FREQUENCY_SWITCH register being set to one of the following supported values: 250kHz, 350kHz, 425kHz, 500kHz, 575kHz, 650kHz, 750kHz, 1MHz (see Table 8 for hexadecimal values). In this configuration, the module is called a "sync master": SYNC becomes a bidirectional open-drain pin, and the LTM4676 pulls SYNC logic low for nominally 500ns at a time, at the prescribed clock rate. The SYNC signal can be bused to other LTM4676 modules (configured as "sync slaves"), for purposes of synchronizing switching frequencies of multiple modules within a system—but only one LTM4676 should be configured as a "sync master"; the other LTM4676(s) should be configured as "sync slaves". To configure an LTM4676 as a "sync slave", set its FREQUENCY_SWITCH register to 0x0000. In that configuration, the LTM4676's SYNC pin becomes a high impedance input, only—i.e., it does not drive SYNC low.

The FREQUENCY_SWITCH register can be altered via I^2C commands, but only when switching action is disengaged, i.e., the module's outputs are turned off. The FREQUENCY_SWITCH register takes on the value stored in NVM at SV_{IN} power-up, but is overridden according to a resistor pin-strap applied between the $F_{SWPHCFG}$ pin and SGND only if the module is configured to respect resistor pin-strap settings (MFR_CONFIG_ALL[6] = 0_b). Table 4 highlights available resistor pin-strap and corresponding FREQUENCY_SWITCH settings.

The relative phasing of all active channels in a PolyPhase® rail should be optimally phased. The relative phasing of each rail is 360°/n, where n is the number of phases in the rail. MFR_PWM_CONFIG[2:0] configures channel relative phasing with respect to the SYNC pin. Phase

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relationship values are indicated with 0° corresponding to the falling edge of SYNC being coincident with the turn-on of the top MOSFETs, MT*n*.

The MFR_PWM_CONFIG register can be altered via I^2C commands, but only when switching action is disengaged, i.e., the module's outputs are turned off. The MFR_PWM_CONFIG register takes on the value stored in NVM at SV_{IN} power-up, but is overridden according to a resistor pin-strap applied between the $F_{SWPHCFG}$ pin and SGND only if the module is configured to respect resistor pin-strap settings (MFR_CONFIG_ALL[6] = 0_b). Table 4 highlights available resistor pin-strap and corresponding MFR_PWM_CONFIG[2:0] settings.

Some combinations of FREQUENCY_SWITCH and MFR_PWM_CONFIG[2:0] are not available by resistor pin-strapping the $F_{SWPHCFG}$ pin. All combinations of supported values for FREQUENCY_SWITCH and MFR_PWM_CONFIG[2:0] can be configured by NVM programming—or, I^2C transactions, provided switching action is disengaged, i.e., the module's outputs are turned off.

Care must be taken to minimize capacitance on SYNC to assure that the pull-up resistor versus the capacitor load has a low enough time constant for the application to form a "clean" clock. (See "Open-Drain Pins", later in this section.)

When an LTM4676 is configured as a sync slave, it is permissible for external circuitry to drive the SYNC pin from a current-limited source (less than 10mA), rather than using a pull-up resistor. Any external circuitry must not drive high with arbitrarily low impedance at SV_{IN} power-up, because the SYNC output can be low impedance until NVM contents have been downloaded to RAM.

Recommended LTM4676 switching frequencies of operation for many common V_{IN}-to-V_{OUT} applications are indicated in Table 7. When the two channels of an LTM4676 are stepping input voltage(s) down to output voltages whose recommended switching frequencies in Table 7 are significantly different, operation at the higher of the two recommended switching frequencies is preferable, but minimum on-time must be considered. (See Minimum On-Time Considerations section.) For example, consider an application in which it is desired for an LTM4676 to step-down $12V_{IN}$ to $1V_{OUT}$ on Channel 0, and $12V_{IN}$ to $3.3V_{OUT}$ on Channel 1: according to Table 7, the recommended switching frequency is 350kHz and 650kHz, respectively. However, the switching frequency setting of the LTM4676 is common to both channels. Based on the aforementioned guidance, operation at 650kHz would be preferred—in order to keep inductor ripple currents reasonable—however, it is then realized that the on-time for a $12V_{IN}$-to-$1V_{OUT}$ condition at 650kHz is only 128ns, which is marginal. Therefore, for this particular example, the recommended switching frequency becomes 575kHz.

Table 7. Recommended Switching Frequency for Various V_{IN}-to-V_{OUT} Step-Down Scenarios.

	$5V_{IN}$	$8V_{IN}$	$12V_{IN}$	$24V_{IN}$
$0.9V_{OUT}$	350kHz	350kHz	350kHz	250kHz
$1.0V_{OUT}$	350kHz	350kHz	350kHz	250kHz
$1.2V_{OUT}$	350kHz	350kHz	350kHz	350kHz
$1.5V_{OUT}$	350kHz	350kHz	425kHz	425kHz
$1.8V_{OUT}$	425kHz	425kHz	500kHz	500kHz
$2.5V_{OUT}$	425kHz	500kHz	575kHz	650kHz
$3.3V_{OUT}$	425kHz	575kHz	650kHz	750kHz
$5.0V_{OUT}$	N/A	500kHz	750kHz	1MHz

The current drawn by the SV_{IN} pin of the LTM4676 is not digitized or computed. A value representing the estimated SV_{IN} current is located in the MFR_IIN_OFFSET$_n$ register, and is used in the computations of input current readback telemetry, namely READ_IIN and and MFR_READ_IIN$_n$. The recommended setting of MFR_IIN_OFFSET$_n$ is found in Table 8. The same value should be used for MFR_IIN_OFFSET$_0$ and MFR_IIN_OFFSET$_1$ (i.e., Pages 0x00 and 0x01).

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Table 8. Recommended MFR_IIN_OFFSET$_n$ Setting vs Switching Frequency Setting

SWITCHING FREQUENCY (kHz)	FREQUENCY_ SWITCH REGISTER VALUE (HEX.)	RECOMMENDED MFR_IIN_ OFFSET$_n$ SETTING (mA)	RECOMMENDED MFR_IIN_ OFFSET$_n$ SETTING (HEX.)
250	0xF3E8	20.3	0x8A99
350	0xFABC	24.4	0x8B20
425	0xFB52	27.4	0x8B82
500	0xFBE8	30.5	0x8BE7
575	0x023F	33.6	0x9227
650	0x028A	36.7	0x9259
750	0x02EE	40.8	0x929C
1000	0x03E8	51.0	0x9344
Sync. to External Clock, f_{SYNC}	0x0000	0.041 • f_{SYNC} + 10.037	*

*See LTC3880 data sheet, L11 data format.

MINIMUM ON-TIME CONSIDERATIONS

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTM4676 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUTn}}{V_{INn} \bullet f_{OSC}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTM4676 is 90ns, nominal, guardband to 130ns.

VARIABLE DELAY TIME, SOFT-START AND OUTPUT VOLTAGE RAMPING

The LTM4676 must enter its run state prior to soft-start. The RUN$_n$ pins are released after the part initializes and SV_{IN} is greater than the VIN_ON threshold. If multiple LTM4676s are used in an application, they should be configured to share the same RUN$_n$ pins. They all hold their respective RUN$_n$ pins low until all devices initialize and SV_{IN} exceeds the VIN_ON threshold for all devices. The SHARE_CLK pin assures all the devices connected to the signal use the same time base.

After the RUN$_n$ pin releases, the controller waits for the user-specified turn-on delay (TON_DELAY$_n$) prior to initiating an output voltage ramp. Multiple LTM4676s and other LTC parts can be configured to start with variable delay times. To work correctly, all devices use the same timing clock (SHARE_CLK) and all devices must share the RUN$_n$ pin. This allows the relative delay of all parts to be synchronized. The actual variation in the delay will be dependent on the highest clock rate of the devices connected to the SHARE_CLK pin (all Linear Technology ICs are configured to allow the fastest SHARE_CLK signal to control the timing of all devices). The SHARE_CLK signal can be ±7.5% in frequency, thus the actual time delays will have some variance.

Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set point. The rise time of the voltage ramp can be programmed using the TON_RISE$_n$ command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting TON_RISE$_n$ to any value less than 0.250ms. The LTM4676 performs the necessary math internally to assure the voltage ramp is controlled to the desired slope. However, the voltage slope can not be any faster than the fundamental limits of the power stage. The number of steps in the ramp is equal to TON_RISE/0.1ms. Therefore, the shorter the TON_RISE$_n$ time setting, the more jagged the soft-start ramp appears.

The LTM4676 PWM always operates in discontinuous mode during the TON_RISE$_n$ operation. In discontinuous mode, the bottom MOSFET (MBn) is turned off as soon as reverse current is detected in the inductor. This allows the regulator to start up into a pre-biased load.

There is no analog tracking feature in the LTM4676; however, two outputs can be given the same TON_RISE$_n$ and TON_DELAY$_n$ times to achieve ratiometric rail tracking. Because the RUN$_n$ pins are released at the same time and both units use the same time base (SHARE_CLK), the outputs track very closely. If the circuit is in a PolyPhase configuration, all timing parameters must be the same.

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Coincident rail tracking can be achieved by setting two outputs to have the same turn-on/off slew rates, identical turn-on delays, and appropriately chosen turn-off delays:

$$\frac{VOUT\_COMMAND_{RAIL1}}{TON\_RISE_{RAIL1}} = \frac{VOUT\_COMMAND_{RAIL2}}{TON\_RISE_{RAIL2}}$$

and

$$\frac{VOUT\_COMMAND_{RAIL1}}{TOFF\_FALL_{RAIL1}} = \frac{VOUT\_COMMAND_{RAIL2}}{TOFF\_FALL_{RAIL2}}$$

and

$$TON\_DELAY_{RAIL1} = TON\_DELAY_{RAIL2}$$

and (if $VOUT\_COMMAND_{RAIL2} \geq VOUT\_COMMAND_{RAIL1}$)

$$TOFF\_DELAY_{RAIL1} = TOFF\_DELAY_{RAIL2} + \left(1 - \frac{VOUT\_COMMAND_{RAIL1}}{VOUT\_COMMAND_{RAIL2}}\right) \bullet TOFF\_FALL_{RAIL2}$$

or else ($VOUT\_COMMAND_{RAIL2} < VOUT\_COMMAND_{RAIL1}$)

$$TOFF\_DELAY_{RAIL2} = TOFF\_DELAY_{RAIL1} + \left(1 - \frac{VOUT\_COMMAND_{RAIL2}}{VOUT\_COMMAND_{RAIL1}}\right) \bullet TOFF\_FALL_{RAIL1}$$

The described method of start-up sequencing is time based. For concatenated events it is possible to control the RUN pin based on the $\overline{GPIO}_n$ pin of a different controller (see Figure 2). The $\overline{GPIO}_n$ pin can be configured to release when the output voltage of the converter is greater than the $VOUT\_UV\_FAULT\_LIMIT_n$. It is recommended to use the unfiltered V_{OUT} UV fault limit because there is little appreciable time delay between the converter crossing the UV threshold and the $\overline{GPIO}_n$ pin releasing. The unfiltered output can be enabled by the $MFR\_GPIO\_PROPAGATE_n$[12] setting. (Refer to the MFR section of the PMBus commands in the LTC3880 data sheet). The unfiltered signal may have some glitching as the V_{OUT} signal transitions through the comparator threshold. A small digital filter of 250µs internally deglitches the $\overline{GPIO}_n$ pins. If the TON_RISE time is greater than 100ms, the deglitch filter should be complimented with an externally applied capacitor between $\overline{GPIO}_n$ and ground—to further filter the waveform. The RC time-constant of the filter should be set sufficiently fast to assure no appreciable delay is incurred. For most applications, a value of 300µs to 500µs will provide sufficient filtering without significantly delaying the trigger event.

DIGITAL SERVO MODE

For maximum accuracy in the regulated output voltage, enable the digital servo loop by asserting bit 6 of the $MFR\_PWM\_MODE_n$ command. In digital servo mode, the LTM4676 adjusts the regulated output voltage based on the ADC voltage reading. Every 100ms the digital servo loop steps the LSB of the DAC (nominally 1.375mV or 0.6875mV depending on the voltage range bit, MFR_PWM_CONFIG[6-*n*]) until the output is at the correct ADC reading. At power-up this mode engages after $TON\_MAX\_FAULT\_LIMIT_n$ unless the limit is set to 0 (infinite). If the $TON\_MAX\_FAULT\_LIMIT_n$ is set to 0 (infinite), the servo begins after TON_RISE_n is complete and V_{OUTn} has exceeded $VOUT\_UV\_FAULT\_LIMIT_n$ and $IOUT\_OC_n$ is not present. This same point in time is when the output changes from discontinuous to the mode commanded by $MFR\_PWM\_MODE_n$[1:0]. Refer to Figure 3 for details on the V_{OUTn} waveform under time based sequencing.

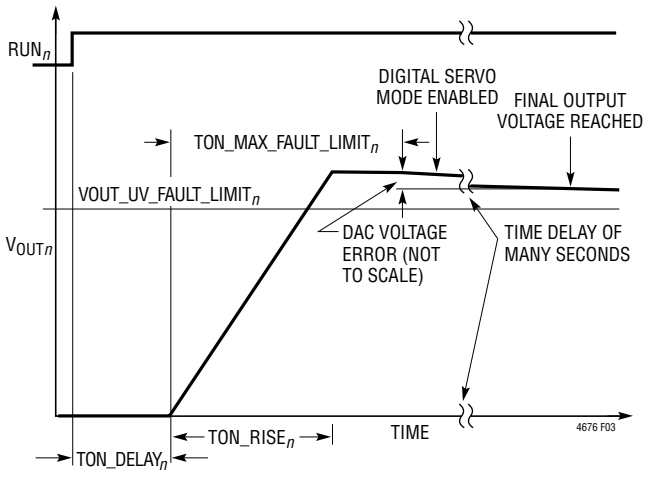

Figure 3. Timing Controlled V_{OUT} Rise

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If the TON_MAX_FAULT_LIMIT$_n$ is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE$_n$ is set to ignore (0x00), the servo begins:

1. After the TON_RISE$_n$ sequence is complete
2. After the TON_MAX_FAULT_LIMIT$_n$ time is reached; and
3. After the VOUT_UV_FAULT_LIMIT$_n$ has been exceed or the IOUT_OC_FAULT_LIMIT$_n$ is no longer active.

If the TON_MAX_FAULT_LIMIT$_n$ is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE$_n$ is not set to ignore (0X00), the servo begins:

1. After the TON_RISE$_n$ sequence is complete;
2. After the TON_MAX_FAULT_LIMIT$_n$ time has expired and both VOUT_UV_FAULT$_n$ and IOUT_OC_FAULT$_n$ are not present.

The maximum rise time is limited to 1.3 seconds.

In a PolyPhase configuration it is recommended only one of the control loops have the digital servo mode enabled. This will assure the various loops do not work against each other due to slight differences in the reference circuits.

SOFT OFF (SEQUENCED OFF)

In addition to a controlled start-up, the LTM4676 also supports controlled turn-off. The TOFF_DELAY$_n$ and TOFF_FALL$_n$ functions are shown in Figure 4. TOFF_FALL$_n$ is processed when the RUN$_n$ pin goes low or if the module is commanded off. If the module faults off or $\overline{\text{GPIO}}_n$ is pulled low externally and the module is programmed to respond to this (MFR_GPIO_RESPONSE$_n$ = 0xC0), the output three-states (becomes high impedance) rather than exhibiting a controlled ramp. The output then decays as a function of the load.

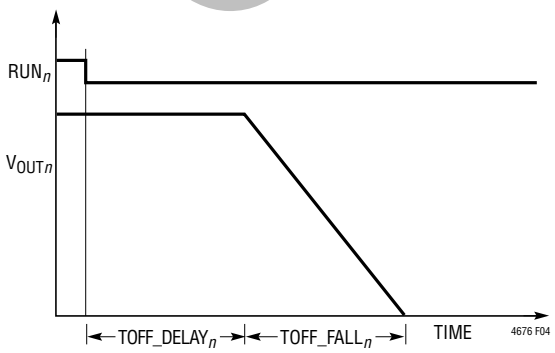

Figure 4. TOFF_DELAY$_n$ and TOFF_FALL$_n$

The output voltage operates as shown in Figure 4 so long as the part is in forced continuous mode and the TOFF_FALL$_n$ time is sufficiently slow that the power stage can achieve the desired slope. The TOFF_FALL$_n$ time can only be met if the power stage and controller can sink sufficient current to assure the output is at zero volts by the end of the fall time interval. If the TOFF_FALL$_n$ time is set shorter than the time required to discharge the load capacitance, the output will not reach the desired zero volt state. At the end of TOFF_FALL$_n$, the controller ceases to sink current and V$_{OUT}$$_n$ decays at the natural rate determined by the load impedance. If the controller is in discontinuous mode, the controller does not pull negative current and the output becomes pulled low by the load, not the power stage. The maximum fall time is limited to 1.3 seconds. The number of steps in the ramp is equal to TOFF_FALL/0.1ms. Therefore, the shorter the TOFF_FALL$_n$ setting, the more jagged the TOFF_FALL$_n$ ramp appears.

UNDERVOLTAGE LOCKOUT

The LTM4676 is initialized by an internal threshold-based UVLO where SV$_{IN}$ must be approximately 4V and INTV$_{CC}$, V$_{DD33}$, V$_{DD25}$ must be within approximately 20% of the regulated values. In addition, V$_{DD33}$ must be within approximately 7% of the targeted value before the LTM4676 releases its RUN$_n$ pins. After the part has initialized, an additional comparator monitors SV$_{IN}$. The VIN_ON threshold must be exceeded before the power sequencing can begin. When SV$_{IN}$ drops below the VIN_OFF threshold, the LTM4676 pulls its RUN$_n$ pins low and SV$_{IN}$ must increase above the VIN_ON threshold before the controller will restart. The normal start-up sequence will be allowed after the VIN_ON threshold is crossed.

It is possible to program the contents of the NVM in the application if the V$_{DD33}$ supply is externally driven. This activates the digital portion of the LTM4676 without engaging the high voltage sections. PMBus communications are valid in this supply configuration. If SV$_{IN}$ has not been applied to the LTM4676,

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MFR_COMMON[3] will be asserted low, indicating that NVM has not initialized. If this condition is detected, the part will only respond to addresses 0x5A and 0x5B. To initialize the part issue the following set of commands: global address 0x5B command 0xBD data 0x2B followed by global address 0x5B command 0xBD and data 0xC4. The part will now respond to the correct address. Configure the part as desired then issue a STORE_USER_ALL. When SV_{IN} is applied a MFR_RESET command must be issued to allow the PWM to be enabled and valid ADC conversions to be read.

FAULT CONDITIONS

The LTM4676 $\overline{GPIO}_n$ pins are configurable to indicate a variety of faults including OV/UV, OC, OT, timing faults, peak overcurrent faults. In addition the $\overline{GPIO}_n$ pins can be pulled low by external sources to indicate to the LTM4676 the presence of a fault in some other portion of the system. The fault response is configurable and allow the following options:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in $MFR\_RETRY\_DELAY_n$

Refer to the PMBus section of the LTC3880 data sheet and the PMBus specification for more details.

The OV response is automatic and rapid. If an OV is detected, MT*n* is turned off and BG*n* is turned on, until the OV condition clears.

Fault logging is available on the LTM4676. The fault logging is configurable to automatically store data when a fault occurs that causes the unit to fault off. The header portion of the fault logging table contains peak values. It is possible to read these values at any time. This data will be useful while troubleshooting the fault.

If the LTM4676 internal temperature is in excess of 85°C or below 0°C, the write into the NVM is not recommended. The data will still be held in RAM, unless the 3.3V supply UVLO threshold is reached. If the die temperature exceeds 130°C all NVM communication is disabled until the die temperature drops below 125°C.

OPEN-DRAIN PINS

The LTM4676 has the following open-drain pins:

3.3V Pins

1. $\overline{GPIO}_n$
2. SYNC
3. SHARE_CLK

5V Pins (compatible with 3.3V digital logic thresholds)

1. RUN_n
2. $\overline{ALERT}$
3. SCL
4. SDA

All the above pins have on-chip pull-down transistors that can sink 3mA at 0.4V. The low threshold on the pins is 1.4V; thus, plenty of margin on the digital signals with 3mA of current. For 3.3V pins, 3mA of current is a 1.1k resistor. Unless there are transient speed issues associated with the RC time constant of the resistor pull-up and parasitic capacitance to ground, a 10k resistor or larger is generally recommended.

For high speed signals such as the SDA, SCL and SYNC, a lower value resistor may be required. The RC time constant should be set to 1/3 to 1/5 the required rise time to avoid timing issues. For a 100pF load and a 400kHz PMBus communication rate, the rise time must be less than 300ns. The resistor pull-up on the SDA and SCL pins with the time constant set to 1/3 the rise time:

$$R_{PULLUP} = \frac{t_{RISE}}{3 \bullet 100pF} = 1k$$

Be careful to minimize parasitic capacitance on the SDA and SCL pins to avoid communication problems. To estimate the loading capacitance, monitor the signal in question and measure how long it takes for the desired signal to reach approximately 63% of the output value. This is one time constant.

The SYNC pin has an on-chip pull-down transistor with the output held low for nominally 500ns. If the internal oscillator is set for 500kHz and the load is 100pF and a

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3x time constant is required, the resistor calculation is as follows:

$$R_{PULLUP} = \frac{2\mu s - 500ns}{3 \bullet 100pF} = 5k$$

The closest 1% resistor is 4.99k.

If timing errors are occurring or if the SYNC frequency is not as fast as desired, monitor the waveform and determine if the RC time constant is too long for the application. If possible reduce the parasitic capacitance. If not reduce the pull up resistor sufficiently to assure proper timing.

PHASE-LOCKED LOOP AND FREQUENCY SYNCHRONIZATION

The LTM4676 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. The PLL is locked to the falling edge of the SYNC pin. The phase relationship between channel 0, channel 1 and the falling edge of SYNC is controlled by the lower 3 bits of the MFR_PWM_CONFIG command. For PolyPhase applications, it is recommended all the phases be spaced evenly. Thus for a 2-phase system the signals should be 180° out of phase and a 4-phase system should be spaced 90°.

The phase detector is an edge-sensitive digital type that provides a known phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. The PLL lock range is guaranteed between 225kHz and 1.1MHz.

The PLL has a lock detection circuit. If the PLL should lose lock during operation, bit 4 of the STATUS_MFR_SPECIFIC command is asserted and the $\overline{\text{ALERT}}$ pin is pulled low. The fault can be cleared by writing a 1 to the bit. If the user does not wish to see the PLL_FAULT, even if a synchronization clock is not available at power up, bit 3 of the MFR_CONFIG_ALL command must be asserted.

If the SYNC signal is not clocking in the application, the PLL runs at the lowest free running frequency of the VCO. This will be well below the intended PWM frequency of the application and may cause undesirable operation of the converter.

If the PWM (SW*n*) signal appears to be running at too high a frequency, monitor the SYNC pin. Extra transitions on the falling edge will result in the PLL trying to lock on to noise instead of the intended signal. Review routing of digital control signals and minimize crosstalk to the SYNC signal to avoid this problem. Multiple LTM4676s are required to share the SYNC pin in PolyPhase configurations; for other configurations, it is optional. If the SYNC pin is shared between LTM4676s, only one LTM4676 can be programmed with a frequency output. All the other LTM4676s must be configured for external clock (FREQUENCY_SWITCH = 0x0000, and/or see Table 4).

RCONFIG PIN-STRAPS (EXTERNAL RESISTOR CONFIGURATION PINS)

The LTM4676 default NVM is programmed to respect the RCONFIG pins. If a user wishes the output voltage, PWM frequency and phasing and the address to be set without programming the part or purchasing specially programmed parts, the RCONFIG pins can be used to establish these parameters—provided MFR_CONFIG_ALL[6] = 0_b. The RCONFIG pins only require a resistor terminating to SGND of the LTM4676. The RCONFIG pins are only monitored at initial power up and during a reset (MFR_RESET) so modifying their values perhaps using a DAC after the part is powered will have no effect. To assure proper operation, the value of RCONFIG resistors applied to the LTM4676 pin-strapping pins must not deviate more than ±3% away from the target nominal values indicated in lookup Tables 2 to 5, over the lifetime of the product. Thin film, 1% tolerance (or better), ±50ppm/°C-T.C.R. rated (or better) resistors from vendors such as KOA Speer, Panasonic, Vishay and Yageo are good candidates. Noisy clock signals should not be routed near these pins.

VOLTAGE SELECTION

When an output voltage is set using the RCONFIG pins on VOUT*n*_CFG and VTRIM*n*_CFG (MFR_CONFIG_ALL[6] =

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0_b), the following parameters are set as a percentage of the output voltage:

- VOUT_OV_FAULT_LIMIT +10%
- VOUT_OV_WARN +7.5%
- VOUT_MAX +7.5%
- VOUT_MARGIN_HI +5%
- POWER_GOOD_ON –7%
- POWER_GOOD_OFF –8%
- VOUT_MARGIN_LO –5%
- VOUT_UV_WARN –6.5%
- VOUT_UV_FAULT_LIMIT –7%

CONNECTING THE USB TO THE I²C/SMBus/PMBus CONTROLLER TO THE LTM4676 IN SYSTEM

The LTC USB to I²C/SMBus/PMBus controller can be interfaced to the LTM4676 on the user's board for programming, telemetry and system debug. The controller, when used in conjunction with LTpowerPlay, provides a powerful way to debug an entire power system. Faults are quickly diagnosed using telemetry, fault status registers and the fault log. The final configuration can be quickly developed and stored to the LTM4676 EEPROM.

Figures 5 and 6 illustrate the application schematics for powering, programming and communicating with one or more LTM4676s via the LTC I²C/SMBus/PMBus controller regardless of whether or not system power is present. If system power is not present the dongle will power the LTM4676 through the V_{DD33} supply pin. To initialize the part when SV_{IN} is not applied and the V_{DD33} pin is powered use global address 0x5B command 0xBD data 0x2B followed by address 0x5B command 0xBD data 0xC4. The part can now be communicated with, and the project file updated. To write the updated project file to the NVM issue a STORE_USER_ALL command. When SV_{IN} is applied, a MFR_RESET must be issued to allow the PWM to be enabled and valid ADCs to be read.

Because of the controllers limited current sourcing capability, only the LTM4676s, their associated pull-up resistors and the I²C pull-up resistors should be powered from the ORed 3.3V/3.4V supply. In addition, any device sharing the I²C bus connections with the LTM4676 must not have body diodes between the SDA/SCL pins and

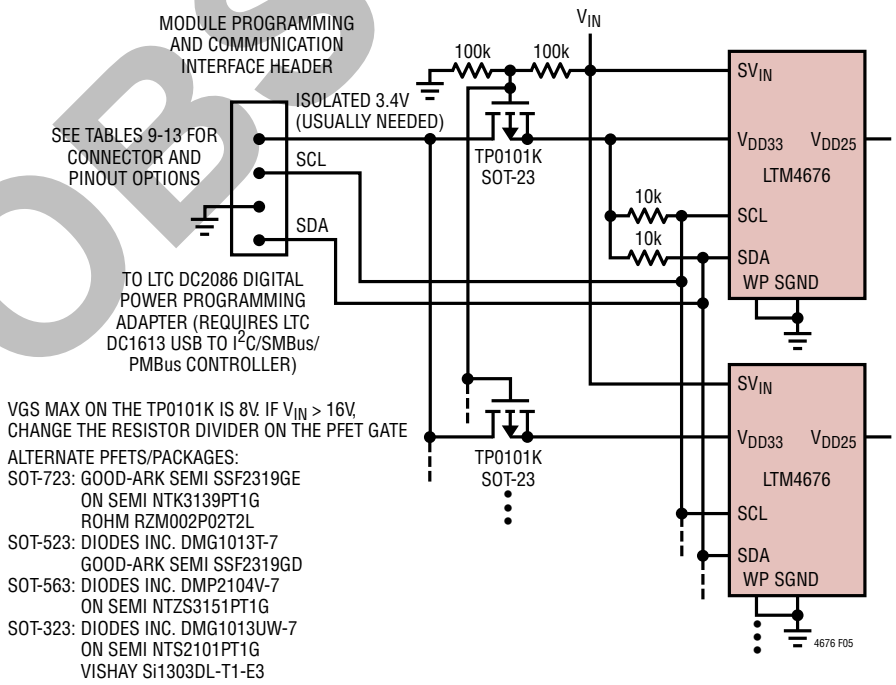

Figure 5. Circuit Suitable for Programming EEPROM/NVM of LTM4676 and Other LTC PSM Modules/ICs in Vast Systems, Even When V_{IN} Power Is Absent, 0°C < T_J ≤ 85°C

APPLICATIONS INFORMATION

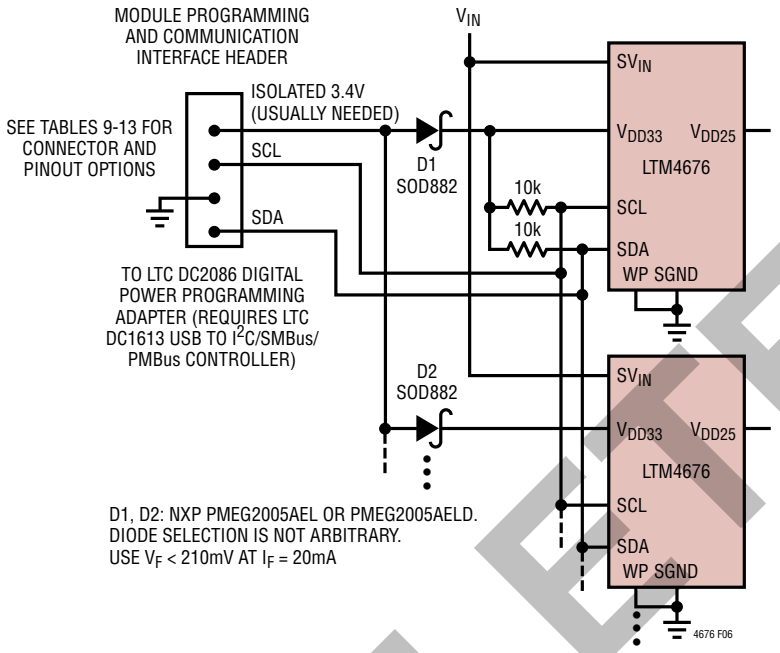

Figure 6. Circuit Suitable for Programming EEPROM/NVM of LTM4676 and Other LTC PSM Modules/ICs in Vast Systems, Even When V_{IN} Power Is Absent, T_A > 20°C and T_J < 85°C

their respective V_{DD} node because this will interfere with bus communication in the absence of system power. In Figure 5, the dongle will not bias the LTM4676s when SV_{IN} is present. It is recommended the RUN_n pins be held low to avoid providing power to the load until the part is fully configured.

The LTC controller/adapter I^2C connections are opto-isolated from the PC USB. The 3.3V/3/4V from the controller/adapter and the LTM4676 V_{DD33} pin must be driven to each LTM4676 with a separate PFET or diode, according to Figures 5 and 6. Only when SV_{IN} is not applied is it permissible for the V_{DD33} pins to be electrically in parallel because the $INTV_{CC}$ LDO is off. The DC1613's 3.3V current limit is 100mA but typical V_{DD33} currents are under 15mA. The V_{DD33} does back drive the $INTV_{CC}$ pin. Normally this is not an issue if SV_{IN} is open. The DC2086 is capable of delivering 3.4V at 2A.

Using a 4-pin header in Figure 5 or 6 maximizes flexibility to alter the LTM4676's NVM contents at any stage of the user's product development and production cycles. If the LTM4676's NVM is "pre-programmed", i.e., contains its finalized configuration, prior to being soldered to the user's PCB/motherboard—or, if other means have been provided for altering the LTM4676's NVM contents in the user's system—then the 3.3V/3.4V pin on the header is not needed, and a 3-pin header is sufficient to establish GUI communications. The LTM4676 can be purchased with customized NVM contents; consult factory for details. Alternatively, the NVM contents of the LTM4676 can be configured in a mass production environment by designing for it in ICT (in-circuit test), or by providing a means of applying SV_{IN} while holding the LTM4676's RUN pins low. Communication to the module must be made possible via the SCL and SDA pins/nets in all NVM programming scenarios. Recommended headers are found in Tables 9 and 10.

LTpowerPlay: AN INTERACTIVE GUI FOR DIGITAL POWER SYSTEM MANAGEMENT

LTpowerPlay is a powerful Windows-based development environment that supports Linear Technology digital power ICs including the LTM4676. The software supports a variety of different tasks. LTpowerPlay can be used to evaluate Linear Technology ICs by connecting to a demo board or the user application. LTpowerPlay can also be used in an offline mode (with no hardware pres-

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Table 9. 4-Pin Headers, 2mm Pin-to-Pin Spacing, Gold Flash or Plating, Compatible with DC2086 Cables

MOUNTING STYLE	INSERTION ANGLE	INTERFACE STYLE	VENDOR	PART NUMBER	PINOUT STYLE (SEE TABLE 11)
Surface Mount	Vertical	Shrouded and Keyed Header	Hirose	DF3DZ-4P-2V(51) DF3DZ-4P-2V(50) DF3Z-4P-2V(50)	Type A
		Non Shrouded, Non-Keyed Header	3M	951104-2530-AR-PR	Type A and B Supported. Reversible/Not Keyed
	Right Angle	Shrouded and Keyed Header	Hirose	DF3DZ-4P-2H(51) DF3DZ-4P-2H(50)	Type A
		Non Shrouded. Cable-to-Header/PCB Mechanics Yield Keying Effect	FCI	10112684-G03-04ULF	Type B. Keying Achieved by PCB Surface
Through-Hole	Vertical	Shrouded and Keyed Header	Hirose	DF3-4P-2DSA(01)	Type A
		Non Shrouded, Non-Keyed Header	Harwin	M22-2010405	Type A and B Supported. Reversible/Not Keyed
			Samtec	TMM-104-01-LS	
			Sullins	NRPN041PAEN-RC	
	Right Angle	Shrouded and Keyed Header	Hirose	DF3-4P-2DS(01)	Type A
		Non Shrouded. Cable-to-Header/PCB Mechanics Yield Keying Effect	Norcomp	27630402RP2	Type B. Keying Achieved by Intentional PCB Interference
			Harwin	M22-2030405	
			Samtec	TMM-104-01-L-S-RA	

Table 10. 3-Pin Headers, 2mm Pin-to-Pin Spacing, Gold Flash or Plating, Compatible with DC2086 Cables

MOUNTING STYLE	INSERTION ANGLE	INTERFACE STYLE	VENDOR	PART NUMBER	PINOUT STYLE (SEE TABLE 12)
Surface Mount	Vertical	Shrouded and Keyed Header	Hirose	DF3DZ-3P-2V(51) DF3DZ-3P-2V(50) DF3Z-3P-2V(50)	Type A
		Non Shrouded, Non-Keyed Header	3M	951103-2530-AR-PR	Type A and B Supported. Reversible/Not Keyed
	Right Angle	Shrouded and Keyed Header	Hirose	DF3DZ-3P-2H(51) DF3DZ-3P-2H(50)	Type A
		Non Shrouded. Cable-to-Header/PCB Mechanics Yield Keying Effect	FCI	10112684-G03-03LF	Type B. Keying Achieved by PCB Surface
Through-Hole	Vertical	Shrouded and Keyed Header	Hirose	DF3-3P-2DSA(01)	Type A
		Non Shrouded, Non-Keyed Header	Harwin	M22-2010305	Type A and B Supported. Reversible/Not Keyed
			Samtec	TMM-103-01-LS	
			Sullins	NRPN031PAEN-RC	
	Right Angle	Shrouded and Keyed Header	Hirose	DF3-3P-2DS(01)	Type A
		Non Shrouded. Cable-to-Header/PCB Mechanics Yield Keying Effect	Norcomp	27630302RP2	Type B. Keying Achieved by Intentional PCB Interference
			Harwin	M22-2030305	
			Samtec	TMM-103-01-L-S-RA	

Table 11. Recommended 4-Pin Header Pinout (Pin Numbering Scheme Adheres to Hirose Conventions). Interfaces to DC2086 Cables

PIN NUMBER	PINOUT STYLE "A" (SEE TABLE 9)	PINOUT STYLE "B" (SEE TABLE 9)
1	SDA	Isolated 3.3V/3.4V
2	GND	SCL
3	SCL	GND
4	Isolated 3.3V/3.4V	SDA

Table 12. Recommended 3-Pin Header Pinout (Pin Numbering Scheme Adheres to Hirose Conventions). Interfaces to DC2086 Cables

PIN NUMBER	PINOUT STYLE "A" (SEE TABLE 10)	PINOUT STYLE "B" (SEE TABLE 10)
1	SDA	SCL
2	GND	GND
3	SCL	SDA

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Table 13. 4-Pin Male-to-Male Shrouded and Keyed Adapter (Optional. Eases Creation of Adapter Cables, if Deviating from Recommended Connectors/Connector Pinouts). Interfaces to DC2086 Cables

Vendor	Part Number	Website
Hirose	DF3-4EP-2A	www.hirose.com, www.hirose.co.jp

ent) in order to build multiple IC configuration files that can be saved and reloaded at a later time. LTpowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program or tweak the power system or to diagnose power issues when bringing up rails. LTpowerPlay utilizes Linear Technology's USB-to-I^{2}C/SMBus/PMBus controller to communication with one of the many potential targets including the DC1811A (single LTM4676) or DC1989 (dual, triple, quad LTM4676) demo boards, or a customer target system. The software also provides an automatic update feature to keep the revisions current with the latest set of device drivers and documentation. A great deal of context sensitive help is available with LTpowerPlay along with several tutorial demos. Complete information is available at http://www.linear.com/ltpowerplay

PMBus COMMUNICATION AND COMMAND PROCESSING

The LTM4676 has one deep buffer to hold the last data written for each supported command prior to processing as shown in Figure 8; Write Command Data Processing. When the part receives a new command from the bus, it copies the data into the Write Command Data Buffer, indicates to the internal processor that this command data needs to be fetched, and converts the command to its internal format so that it can be executed.

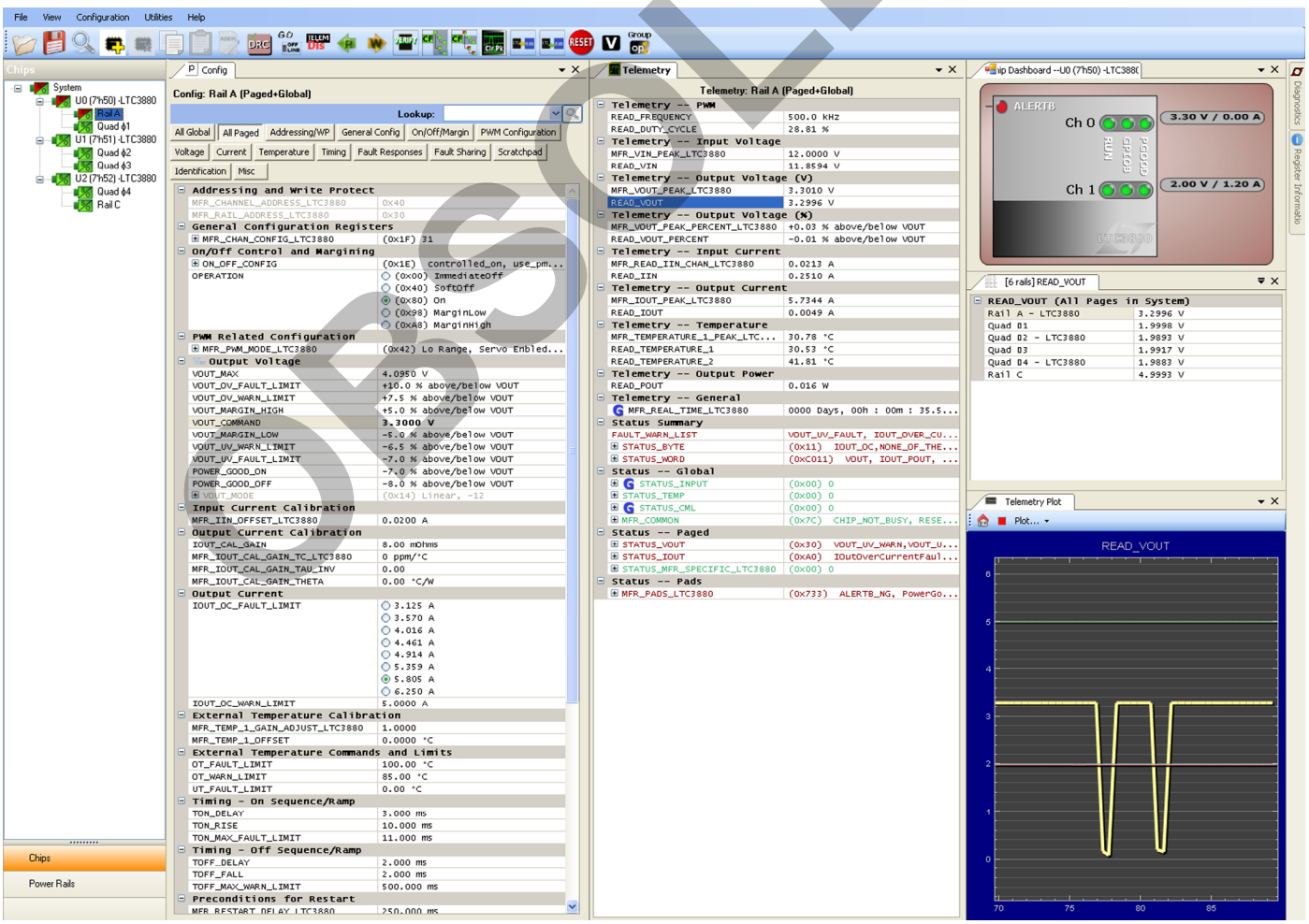

Figure 7

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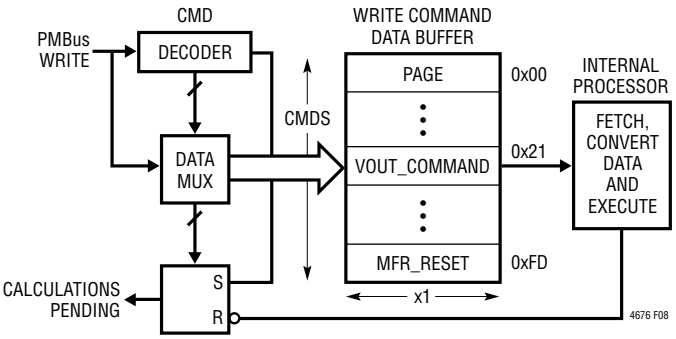

Figure 8. Write Command Data Processing

Two distinct parallel blocks manage command buffering and command processing (fetch, convert, and execute) to ensure the last data written to any command is never lost. Command data buffering handles incoming PMBus writes by storing the command data to the Write Command Data Buffer and marking these commands for future processing. The internal processor runs in parallel and handles the sometimes slower task of fetching, converting and executing commands marked for processing.

Some computationally intensive commands (e.g., timing parameters, temperatures, voltages and currents) have internal processor execution times that may be long relative to PMBus timing. If the part is busy processing a command, and new command(s) arrive, execution may be delayed or processed in a different order than received. The part indicates when internal calculations are in process via bit 5 of MFR_COMMON ('calculations not pending'). When the part is busy calculating, bit 5 is cleared. When this bit is set, the part is ready for another command. An example polling loop is provided in Figure 8 which ensures that commands are processed in order while simplifying error handling routines.

When the part receives a new command while it is busy, it will communicate this condition using standard PMBus protocol. Depending on part configuration it may either NACK the command or return all ones (0xFF) for reads. It may also generate a BUSY fault and $\overline{\text{ALERT}}$ notification, or stretch the SCL clock low. For more information refer to PMBus Specification v1.1, Part II, Section 10.8.7 and SMBus v2.0 section 4.3.3. Clock stretching can be enabled by asserting bit 1 of MFR_CONFIG_ALL. Clock stretching will only occur if enabled and the bus communication speed exceeds 100kHz.

PMBus busy protocols are well accepted standards, but can make writing system level software somewhat complex. The part provides three 'hand shaking' status bits which reduce complexity while enabling robust system level communication.

The three hand shaking status bits are in the MFR_COMMON register. When the part is busy executing an internal operation, it will clear bit 6 of MFR_COMMON ('module not busy'). When the part is busy specifically because it is in a transitional VOUT state (margining hi/lo, power off/on, moving to a new output voltage set point, etc.) it will clear bit 4 of MFR_COMMON ('output not in transition'). When internal calculations are in process, the part will clear bit 5 of MFR_COMMON ('calculations not pending'). These three status bits can be polled with a PMBus read byte of the MFR_COMMON register until all three bits are set. A command immediately following the status bits being set will be accepted without NACKing or generating a BUSY fault/$\overline{\text{ALERT}}$ notification. The part can NACK commands for other reasons, however, as required by the PMBus spec (for instance, an invalid command or data). An example of a robust command write algorithm for the VOUT_COMMAND$_n$ register is provided in Figure 9.

```
// wait until bits 6, 5, and 4 of MFR_COMMON are all set
do
{
        mfrCommonValue = PMBUS_READ_BYTE(0xEF);
        partReady = (mfrCommonValue & 0x68) == 0x68;
}while(!partReady)

// now the part is ready to receive the next command
PMBUS_WRITE_WORD(0x21, 0x2000); //write VOUT_COMMAND to 2V
```

Figure 9. Example of a Command Write of VOUT_COMMAND

It is recommended that all command writes (write byte, write word, etc.) be preceded with a polling loop to avoid the extra complexity of dealing with busy behavior and unwanted $\overline{\text{ALERT}}$ notification. A simple way to achieve this is by creating SAFE_WRITE_BYTE() and SAFE_WRITE_WORD() subroutines. The above polling mechanism allows one's software to remain clean and simple while robustly communicating with the part. For a detailed discussion of these topics and other special cases please refer to the application note section located at www.linear.com/designtools/app_notes.

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When communicating using bus speeds at or below 100kHz, the polling mechanism shown here provides a simple solution that ensures robust communication without clock stretching. At bus speeds in excess of 100kHz, it is strongly recommended that the part be configured to enable clock stretching. This requires a PMBus master that supports clock stretching. System software that detects and properly recovers from the standard PMBus NACK/BUSY faults as described in the PMBus Specification v1.1, Part II, Section 10.8.7 is required to communicate above 100kHz without clock stretching. Clock stretching will not extend the PMBus speed beyond the specified 400kHz.

THERMAL CONSIDERATIONS AND OUTPUT CURRENT DERATING

The thermal resistances reported in the Pin Configuration section of this data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance. Instead, the derating curves provided later in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12. These coefficients are quoted or paraphrased as follows:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which may not reflect an actual application.

2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule regulator and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD51-9.

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A graphical representation of the aforementioned thermal resistances is given in Figure 10; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package. Granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4676, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4676 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4676 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves provided in later sections of this data sheet, along with well-correlated JESD51-12-defined θ values provided in the Pin Configuration section of this data sheet.

The 1V, 1.8V and 3.3V power loss curves in Figures 11, 12 and 13 respectively can be used in coordination with the load current derating curves in Figures 14 to 31 for calculating an approximate θ_{JA} thermal resistance for the LTM4676 with various heat sinking and air flow conditions. These thermal resistances represent demonstrated performance of the LTM4676 on DC1811A hardware; a 4-layer FR4 PCB measuring 99mm × 113mm × 1.6mm using outer and inner copper weights of 2oz and 1oz, respectively. The power loss curves are taken at room temperature, and are increased with multiplicative factors with ambient temperature. These approximate factors are listed in Table 14.

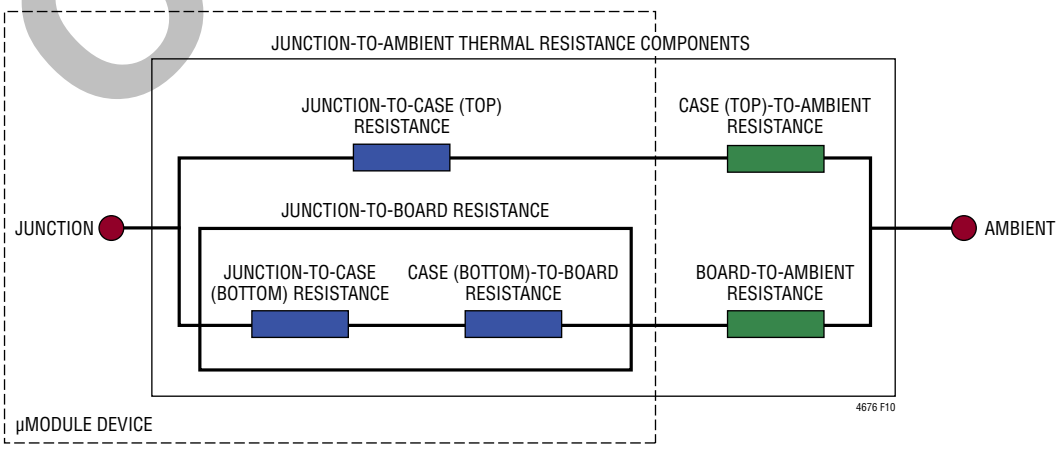

Figure 10. Graphical Representation of JESD51-12 Thermal Coefficients

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(Compute the factor by interpolation, for intermediate temperatures.) The derating curves are plotted with the LTM4676's paralleled outputs initially sourcing up to 26A and the ambient temperature at 30°C. The output voltages are 1V, 1.8V and 3.3V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without air flow, and with and without a heat sink attached with thermally conductive adhesive tape. The BGA heat sinks evaluated in Table 18 (and attached to the LTM4676 with thermally conductive adhesive tape listed in Table 19) yield very comparable performance in laminar airflow despite being visibly different in construction and form factor. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current decreases the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 15, the load current is derated to ~19A at ~80°C ambient with 400LFM airflow and no heat sink and the room temperature (25°C) power loss for this $12V_{IN}$ to $1V_{OUT}$ at $19A_{OUT}$ condition is ~4W. A 4.8W loss is calculated by multiplying the ~4W room temperature loss from the $12V_{IN}$ to $1V_{OUT}$ power loss curve at 19A (Figure 11), with the 1.2 multiplying factor at 80°C ambient (from Table 14). If the 80°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 40°C divided by 4.8W yields a thermal resistance, θ_{JA}, of 8.3°C/W—in good agreement with Table 15. Tables 15, 16 and 17 provide equivalent thermal resistances for 1V, 1.8V and 3.3V outputs with and without air flow and heat sinking. The derived thermal resistances in Tables 15, 16 and 17 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with ambient temperature multiplicative factors from Table 14.

Table 14. Power Loss Multiplicative Factors vs Ambient Temperature

AMBIENT TEMPERATURE	POWER LOSS MULTIPLICATIVE FACTOR
Up to 40°C	1.00
50°C	1.05
60°C	1.10
70°C	1.15
80°C	1.20
90°C	1.25
100°C	1.30
110°C	1.35
120°C	1.40

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Table 15. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 14, 15, 16	5, 12, 24	Figure 11	0	None	10.6
Figures 14, 15, 16	5, 12, 24	Figure 11	200	None	9.5
Figures 14, 15, 16	5, 12, 24	Figure 11	400	None	8.5
Figures 17, 18, 19	5, 12, 24	Figure 11	0	BGA Heat Sink	9.8
Figures 17, 18, 19	5, 12, 24	Figure 11	200	BGA Heat Sink	8.2
Figures 17, 18, 19	5, 12, 24	Figure 11	400	BGA Heat Sink	7.1

Table 16. 1.8V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 20, 21, 22	5, 12, 24	Figure 12	0	None	10.7
Figures 20, 21, 22	5, 12, 24	Figure 12	200	None	9.4
Figures 20, 21, 22	5, 12, 24	Figure 12	400	None	8.4
Figures 23, 24, 25	5, 12, 24	Figure 12	0	BGA Heat Sink	9.9
Figures 23, 24, 25	5, 12, 24	Figure 12	200	BGA Heat Sink	8.3
Figures 23, 24, 25	5, 12, 24	Figure 12	400	BGA Heat Sink	7.1

Table 17. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 26, 27, 28	5, 12, 24	Figure 13	0	None	10.6
Figure 26, 27, 28	5, 12, 24	Figure 13	200	None	9.3
Figure 26, 27, 28	5, 12, 24	Figure 13	400	None	8.4
Figure 29, 30, 31	5, 12, 24	Figure 13	0	BGA Heat Sink	10.0
Figure 29, 30, 31	5, 12, 24	Figure 13	200	BGA Heat Sink	8.4
Figure 29, 30, 31	5, 12, 24	Figure 13	400	BGA Heat Sink	7.3

Table 18. Heat Sink Manufacturer (Thermally Conductive Adhesive Tape Pre-Attached)

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Aavid Thermalloy	375424B00034G	www.aavid.com
Cool Innovations	4-050503PT411	www.coolinnovations.com
Wakefield Engineering	LTN20069	www.wakefield.com

Table 19. Thermally Conductive Adhesive Tape Vendor

THERMALLY CONDUCTIVE ADHESIVE TAPE MANUFACTURER	PART NUMBER	WEBSITE
Chomerics	T411	www.chomerics.com

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Table 20. LTM4676 Channel Output Voltage Response vs Component Matrix. 6.5A Load-Stepping at 6.5A/µs. Typical Measured Values

C_{OUTH} VENDORS	PART NUMBER	C_{OUTL} VENDORS	PART NUMBER
AVX	12106D107MAT2A (100µF, 6.3V, 1210 Case Size)	Sanyo POSCAP	6TPF330M9L (330µF, 6.3V, 9mΩ ESR, D3L Case Size)
Murata	GRM32ER60J107ME20L (100µF, 6.3V, 1210 Case Size)	Sanyo POSCAP	6TPD470M (470µF, 6.3V, 10mΩ ESR, D4D Case Size)
Taiyo Yuden	JMK325BJ107MM-T (100µF, 6.3V, 1210 Case Size)	Sanyo POSCAP	2R5TPE470M9 (470µF, 2.5V, 9mΩ ESR, D2E Case Size)
TDK	C3225X5R0J107MT (100µF, 6.3V, 1210 Case Size)		

V_{OUTn} (V)	V_{INn} (V)	REF. CIRCUIT*	C_{OUTHn} (CERAMIC OUTPUT CAP)	C_{OUTLn} (BULK OUTPUT CAP)	CONNECT $COMP_{na}$ TO $COMP_{nb}$? (INTERNAL LOOP COMP)	R_{THn} (EXT LOOP COMP) (kΩ)	C_{THn} (EXT LOOP COMP) (nF)	f_{SW} (kHz)	$F_{SWPHCFG}$ PIN-STRAP, RESISTOR TO SGND (Table 4) (kΩ)	$V_{OUTn\ CFG}$ PIN-STRAP RESISTOR TO SGND (Table 2) (kΩ)	$V_{TRIMnCFG}$ PIN-STRAP, RESISTOR TO SGND (Table 3) (kΩ)	TRANSIENT DROOP (0A TO 6.5A) (mV)	PK-PK DEVIATION (0A TO 6.5A TO 0A) (mV)	RECOVERY TIME (µs)
0.9	5	Test Ckt. 2	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	350	22.6	1.65	None	42	79	45
0.9	5	Test Ckt. 2	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.12	2.2	350	22.6	1.65	None	91	162	40
0.9	12	Test Ckt. 1	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	350	22.6	1.65	None	42	79	45
0.9	12	Test Ckt. 1	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.12	2.2	350	22.6	1.65	None	91	162	40
0.9	24	Test Ckt. 1	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	250	32.4	1.65	None	45	85	45
0.9	24	Test Ckt. 1	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.12	2.2	350	22.6	1.65	None	94	165	40
1	5	Test Ckt. 2	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	350	22.6	2.43	0	44	85	45
1	5	Test Ckt. 2	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.22	2.2	350	22.6	2.43	0	90	160	40
1	12	Test Ckt. 1	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	350	22.6	2.43	0	44	85	45
1	12	Test Ckt. 1	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.22	2.2	350	22.6	2.43	0	90	160	40
1	24	Test Ckt. 1	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	250	32.4	2.43	0	47	90	45
1	24	Test Ckt. 1	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.22	2.2	350	22.6	2.43	0	93	164	40
1.2	5	Test Ckt. 2	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	350	22.6	3.24	0	45	85	45
1.2	5	Test Ckt. 2	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.42	2.2	350	22.6	3.24	0	89	149	40
1.2	12	Test Ckt. 1	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	350	22.6	3.24	0	45	85	45
1.2	12	Test Ckt. 1	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.42	2.2	350	22.6	3.24	0	89	149	40
1.2	24	Test Ckt. 1	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	350	22.6	3.24	0	48	81	45
1.2	24	Test Ckt. 1	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.42	2.2	350	22.6	3.24	0	92	154	40
1.5	5	Test Ckt. 2	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	350	22.6	4.22	None	45	85	45
1.5	5	Test Ckt. 2	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.75	2.2	350	22.6	4.22	None	89	149	40
1.5	12	Test Ckt. 1	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	350	22.6	4.22	None	45	85	45
1.5	12	Test Ckt. 1	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.75	2.2	350	22.6	4.22	None	89	149	40
1.5	24	Test Ckt. 1	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	425	18.0	4.22	None	48	91	45
1.5	24	Test Ckt. 1	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.75	2.2	350	22.6	4.22	None	93	156	40
1.8	5	Test Ckt. 2	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	425	18.0	6.34	0	45	85	45
1.8	5	Test Ckt. 2	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.99	2.2	500	None	6.34	0	88	144	40
1.8	12	Test Ckt. 1	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	500	None	6.34	0	45	85	45
1.8	12	Test Ckt. 1	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.99	2.2	500	None	6.34	0	88	144	40
1.8	24	Test Ckt. 1	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	500	None	6.34	0	48	92	45

APPLICATIONS INFORMATION

Table 20. LTM4676 Channel Output Voltage Response vs Component Matrix. 6.5A Load-Stepping at 6.5A/µs. Typical Measured Values

V_{OUTn} (V)	V_{INn} (V)	REF. CIRCUIT*	C_{OUTHn} (CERAMIC OUTPUT CAP)	C_{OUTLn} (BULK OUTPUT CAP)	CONNECT $COMP_{na}$ TO $COMP_{nb}$? (INTERNAL LOOP COMP)	R_{THn} (EXT LOOP COMP) (kΩ)	C_{THn} (EXT LOOP COMP) (nF)	f_{SW} (kHz)	$F_{SWPHCFG}$ PIN-STRAP, RESISTOR TO SGND (Table 4) (kΩ)	$V_{OUTn\ CFG}$ PIN-STRAP RESISTOR TO SGND (Table 2) (kΩ)	$V_{TRIMnCFG}$ PIN-STRAP, RESISTOR TO SGND (Table 3) (kΩ)	TRANSIENT DROOP (0A TO 6.5A) (mV)	PK-PK DEVIATION (0A TO 6.5A TO 0A) (mV)	RECOVERY TIME (µs)
1.8	24	Test Ckt. 1	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	4.99	2.2	500	None	6.34	0	94	158	40
2.5	5	Test Ckt. 2	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	425	18.0	10.7	None	46	86	45
2.5	5	Test Ckt. 2	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	5.62	2.2	575	15.4	10.7	None	89	148	40
2.5	12	Test Ckt. 1	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	575	15.4	10.7	None	46	86	45
2.5	12	Test Ckt. 1	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	5.62	2.2	575	15.4	10.7	None	90	150	40
2.5	24	Test Ckt. 1	100µF × 7	None	Yes, cf. Fig. 44	N/A	N/A	650	12.7	10.7	None	48	94	45
2.5	24	Test Ckt. 1	100µF × 3	330µF	No. Use R_{TH}, C_{TH}	5.62	2.2	650	12.7	10.7	None	92	154	40
3.3	5	Test Ckt. 2	100µF × 5	None	Yes, cf. Fig. 44	N/A	N/A	425	18.0	22.6	None	56	110	45
3.3	12	Test Ckt. 1	100µF × 5	None	Yes, cf. Fig. 44	N/A	N/A	650	12.7	22.6	None	60	112	45
3.3	24	Test Ckt. 1	100µF × 5	None	Yes, cf. Fig. 44	N/A	N/A	750	10.7	22.6	None	62	115	45
5**	12	Test Ckt. 1	100µF × 5	None	Yes, cf. Fig. 44	N/A	N/A	750	10.7	32.4	7.68	62	125	50
5**	24	Test Ckt. 1	100µF × 5	None	Yes, cf. Fig. 44	N/A	N/A	1000	9.09	32.4	7.68	65	130	50

*For all conditions: C_{INH} input capacitance is 10µF × 3, per channel (V_{IN0}, V_{IN1}). C_{INL} bulk input capacitance of 150µF is optional if V_{IN} has very low input impedance.

**$5V_{OUT}$ supported on V_{OUT1} channel output, only. V_{OUT0} channel supported range of output voltage regulation is limited to $4V_{OUT}$, max. Exception for dual phase single output operation shown in Figure 42.

APPLICATIONS INFORMATION—DERATING CURVES

See also Figure 43, $12V_{IN}$ to $5V_{OUT}$ derating curves.

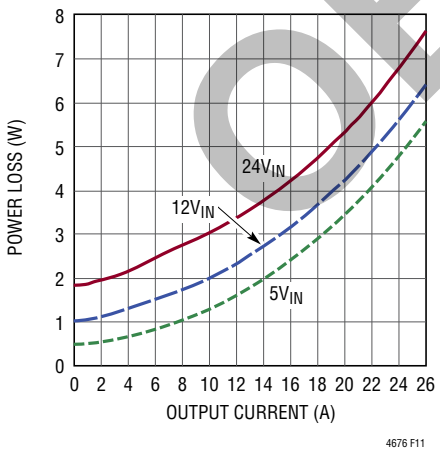


Figure 11. $1V_{OUT}$ Power Loss Curve

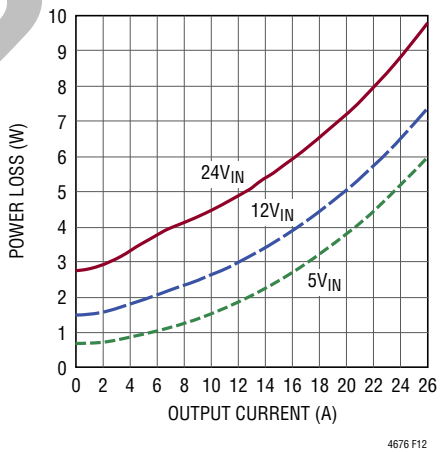


Figure 12. $1.8V_{OUT}$ Power Loss Curve

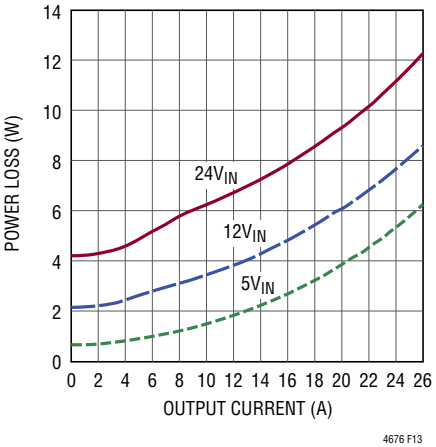


Figure 13. $3.3V_{OUT}$ Power Loss Curve

APPLICATIONS INFORMATION—DERATING CURVES

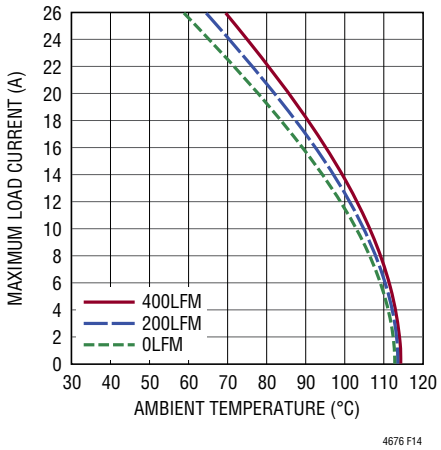


Figure 14. 5V to 1V Derating Curve, No Heat Sink

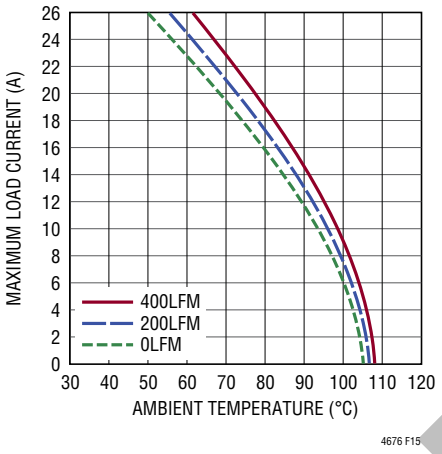


Figure 15. 12V to 1V Derating Curve, No Heat Sink

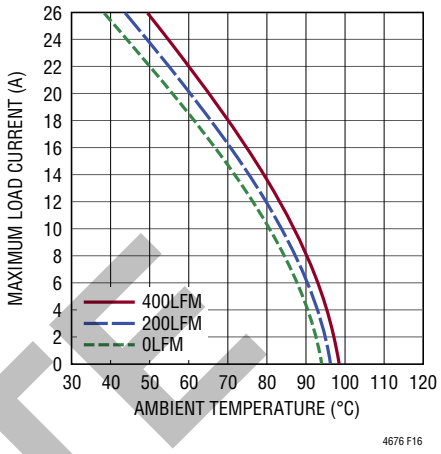


Figure 16. 24V to 1V Derating Curve, No Heat Sink

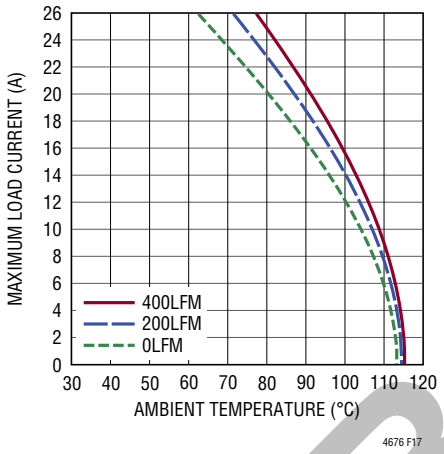


Figure 17. 5V to 1V Derating Curve, with Heat Sink

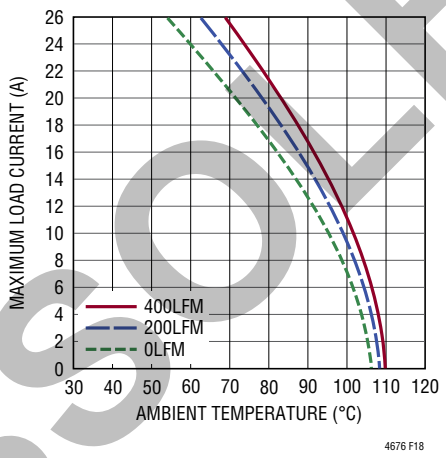


Figure 18. 12V to 1V Derating Curve, with Heat Sink

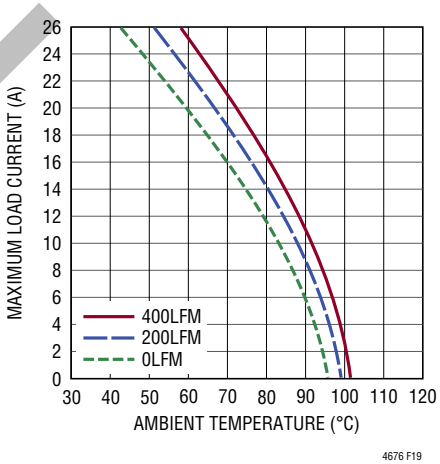


Figure 19. 24V to 1V Derating Curve, with Heat Sink

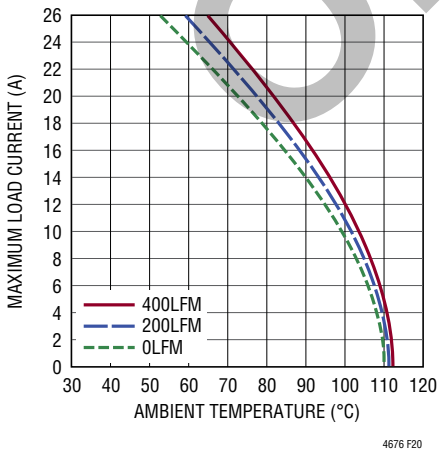


Figure 20. 5V to 1.8V Derating Curve, No Heat Sink

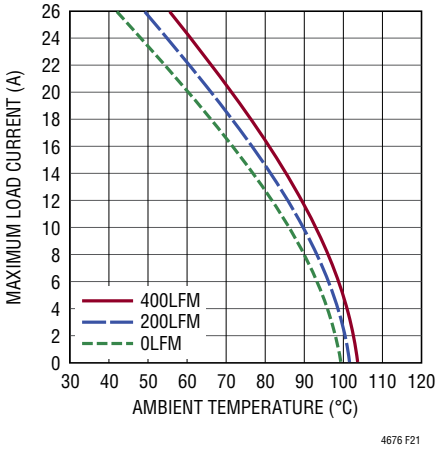


Figure 21. 12V to 1.8V Derating Curve, No Heat Sink

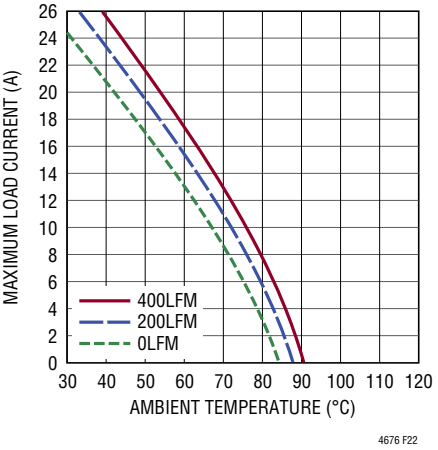


Figure 22. 24V to 1.8V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION—DERATING CURVES

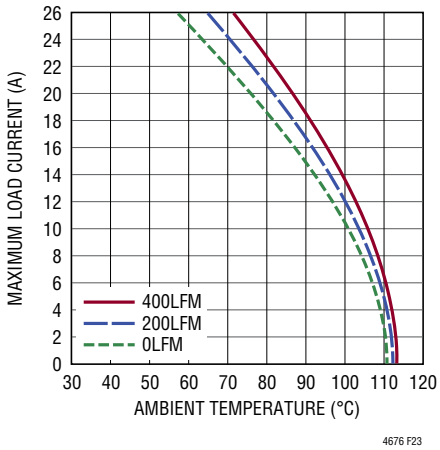


Figure 23. 5V to 1.8V Derating Curve, with Heat Sink

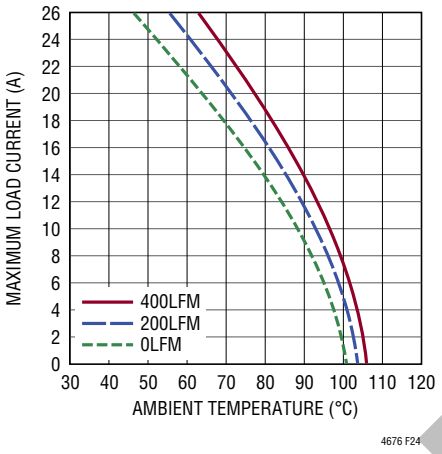


Figure 24. 12V to 1.8V Derating Curve, with Heat Sink

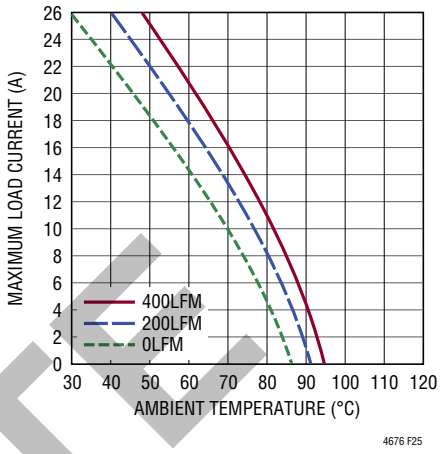


Figure 25. 24V to 1.8V Derating Curve, with Heat Sink

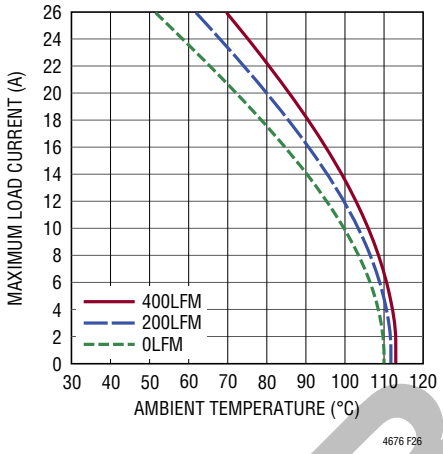


Figure 26. 5V to 3.3V Derating Curve, No Heat Sink

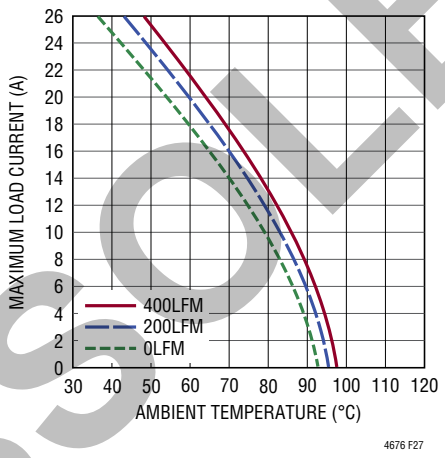


Figure 27. 12V to 3.3V Derating Curve, No Heat Sink

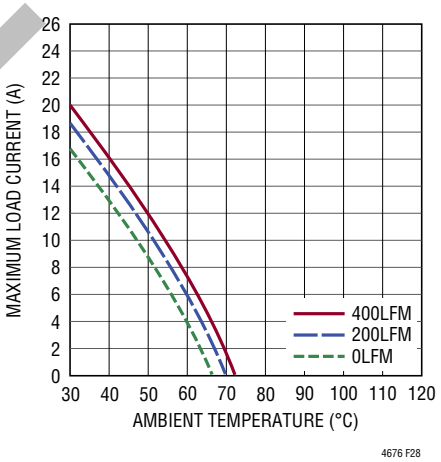


Figure 28. 24V to 3.3V Derating Curve, No Heat Sink

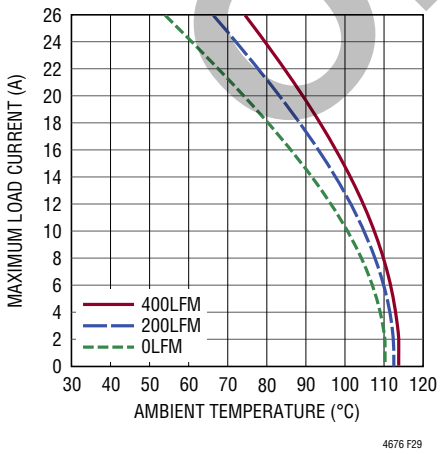


Figure 29. 5V to 3.3V Derating Curve, with Heat Sink

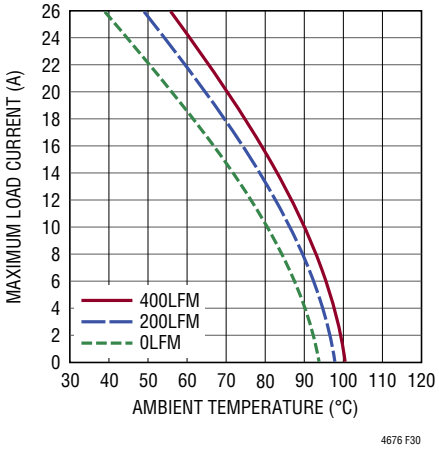


Figure 30. 12V to 3.3V Derating Curve, with Heat Sink

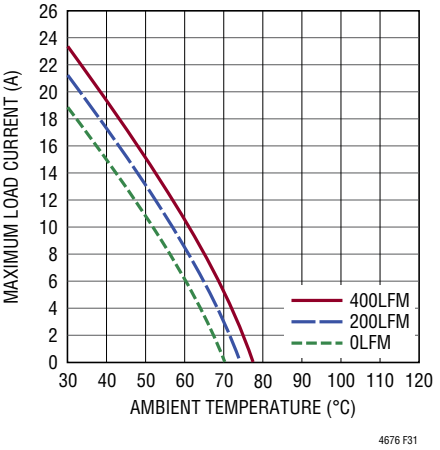


Figure 31. 24V to 3.3V Derating Curve, with Heat Sink

APPLICATIONS INFORMATION

EMI PERFORMANCE

The SW_n pin provides access to the midpoint of the power MOSFETs in LTM4676's power stages.

Connecting an optional series RC network from SW_n to GND can dampen high frequency (~30MHz+) switch node ringing caused by parasitic inductances and capacitances in the switched-current paths. The RC network is called a snubber circuit because it dampens (or "snubs") the resonance of the parasitics, at the expense of higher power loss.

To use a snubber, choose first how much power to allocate to the task and how much PCB real estate is available to implement the snubber. For example, if PCB space allows a low inductance 1W resistor to be used—derated conservatively to 600mW (P_{SNUB})—then the capacitor in the snubber network (C_{SW}) is computed by:

$$C_{SW} = \frac{P_{SNUB}}{V_{INn(MAX)}^2 \bullet f_{SW}}$$

where $V_{INn(MAX)}$ is the maximum input voltage that the input to the power stage (V_{INn}) will see in the application, and f_{SW} is the DC/DC converter's switching frequency of operation. C_{SW} should be NPO, C0G or X7R-type (or better) material.

The snubber resistor (R_{SW}) value is then given by:

$$R_{SW} = \sqrt{\frac{5nH}{C_{SW}}}$$

The snubber resistor should be low ESL and capable of withstanding the pulsed currents present in snubber circuits. A value between 0.7Ω and 4.2Ω is normal.

For ease of snubber implementation, integrated 2.2nF snubber capacitors connect to each of the LTM4676's channel switch nodes via a low inductance path. The electrically floating ends of these snubber capacitors are made available on the $SNUB_n$ pins of the LTM4676. Using the aforementioned guidance on snubber selection, a properly sized snubber resistor can be conveniently connected directly between $SNUB_n$ and GND.

EMI performance of LTM4676 (on DC1811A) with and without a snubber is compared and contrasted in Figures 32 and 33. The snubber resistors applied to the $SNUB_n$ pins reduce EMI signal amplitude by several dBμV/m.

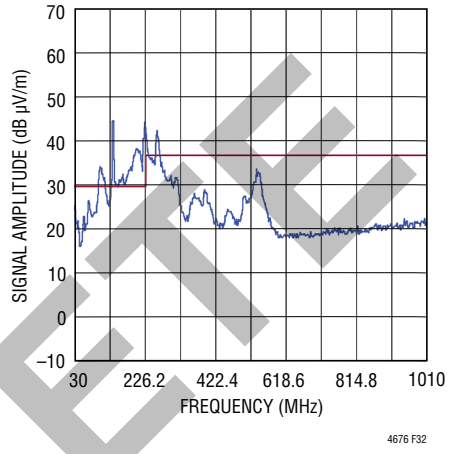


Figure 32. Radiated Emissions Scan of LTM4676 Producing $1V_{OUT}$ at 26A, from $12V_{IN}$. DC1811A Hardware with Outputs Paralleled. No Snubbers Applied. f_{SW} = 350kHz. Measured in a 10m Chamber. Peak Detect Method

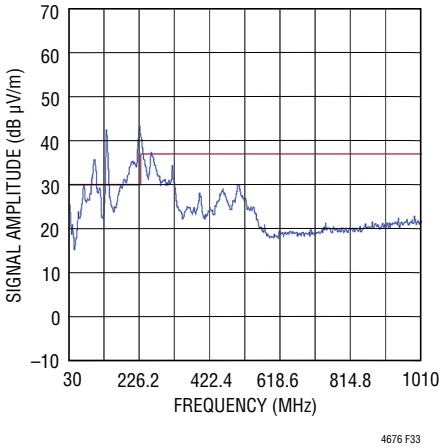


Figure 33. Radiated Emissions Scan of LTM4676 Producing $1V_{OUT}$ at 26A, from $12V_{IN}$. DC1811A Hardware with Outputs Paralleled. 1Ω (1/4W rated) Snubber Resistors Applied from $SNUB_n$ to GND. f_{SW} = 350kHz. Measured in a 10m Chamber. Peak Detect Method

APPLICATIONS INFORMATION

SAFETY CONSIDERATIONS

The LTM4676 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

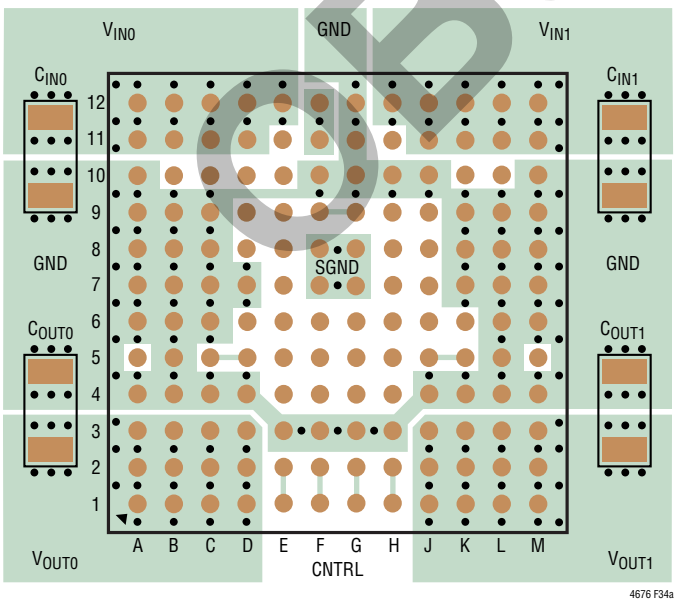
The fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage, thus the internal bottom MOSFET will turn on indefinitely trying to protect the load. Under this fault condition, the input voltage will source very large currents to ground through the failed internal top MOSFET and enabled internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation. The device does support over current and overtemperature protection.

LAYOUT CHECKLIST/EXAMPLE

The high integration of LTM4676 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{INn}, GND and V_{OUTn}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{INn}, GND and V_{OUTn} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the module.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate SGND copper plane for components connected to signal pins. Connect SGND to GND local to the LTM4676.
- For parallel modules, tie the V_{OUTn}, V_{OSNS0}^+/V_{OSNS}^- and/or V_{OSNS1}/SGND voltage-sense differential pair lines, RUN_n, $\overline{GPIO_n}$, $COMP_{na}$, SYNC and SHARE_CLK pins together—as shown in Figure 39.
- Bring out test points on the signal pins for monitoring.

Figure 34 gives a good example of the recommended layout.



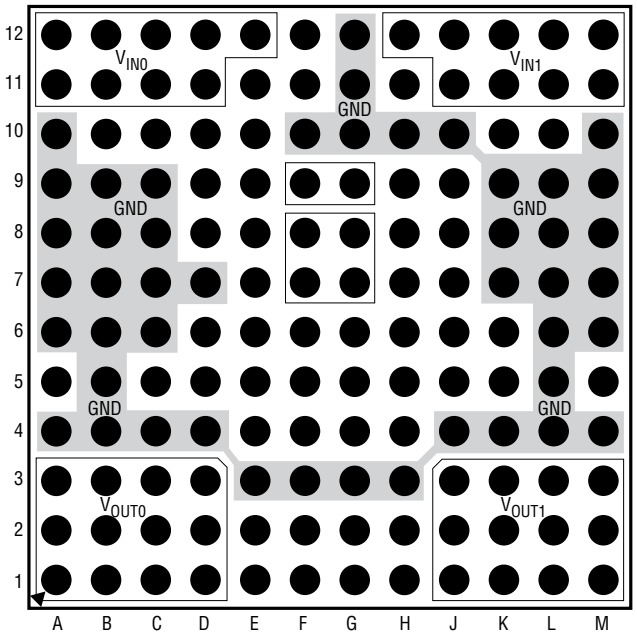
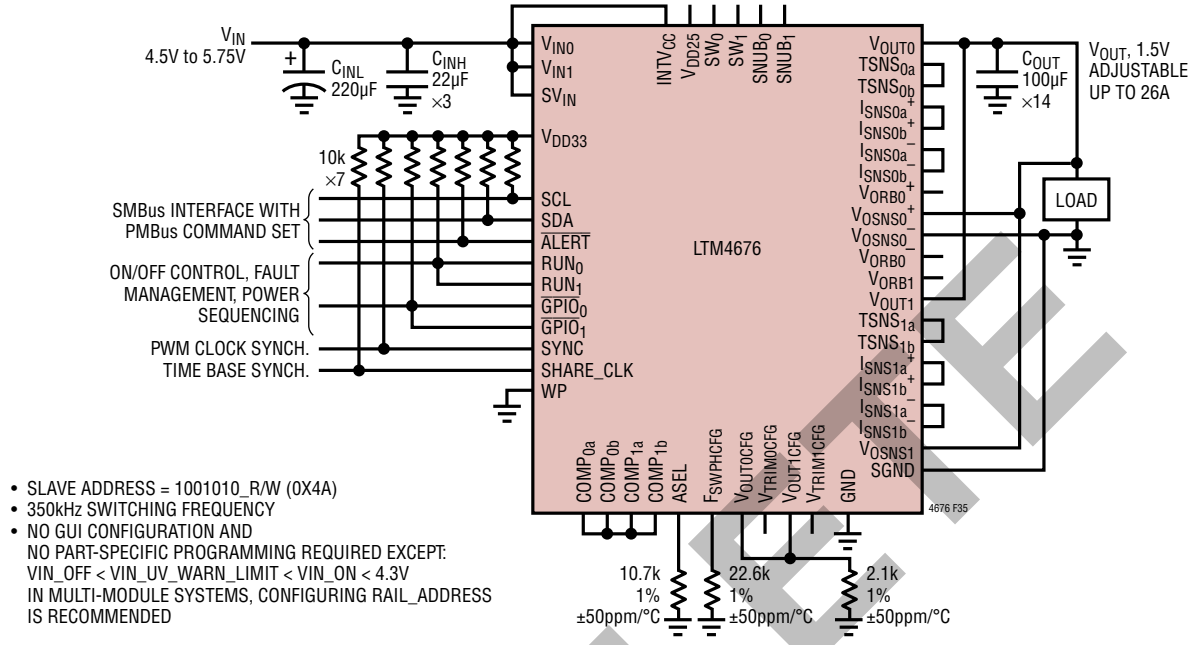


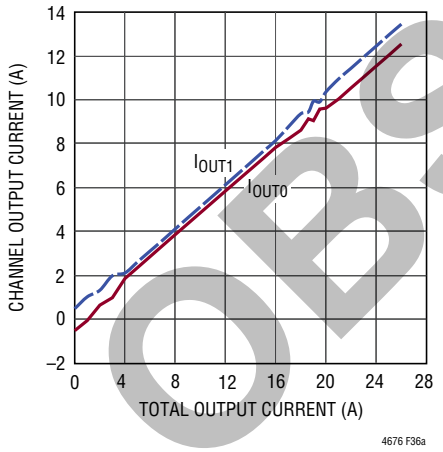
Figure 34. Recommended PCB Layout Package Top View

TYPICAL APPLICATIONS

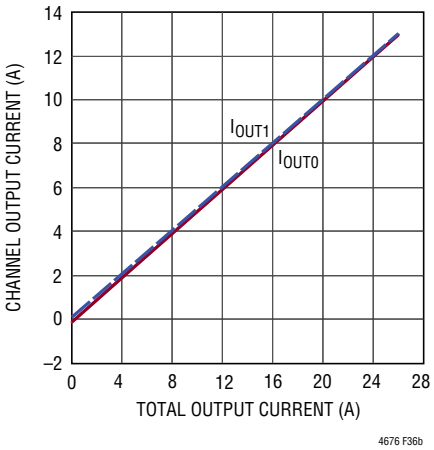


- SLAVE ADDRESS = 1001010_R/W (0X4A)
- 350kHz SWITCHING FREQUENCY
- NO GUI CONFIGURATION AND NO PART-SPECIFIC PROGRAMMING REQUIRED EXCEPT:
  VIN_OFF < VIN_UV_WARN_LIMIT < VIN_ON < 4.3V
  IN MULTI-MODULE SYSTEMS, CONFIGURING RAIL_ADDRESS IS RECOMMENDED

Figure 35. 26A, 1.5V Output DC/DC µModule Regulator with I²C/SMBus/PMBus Serial Interface



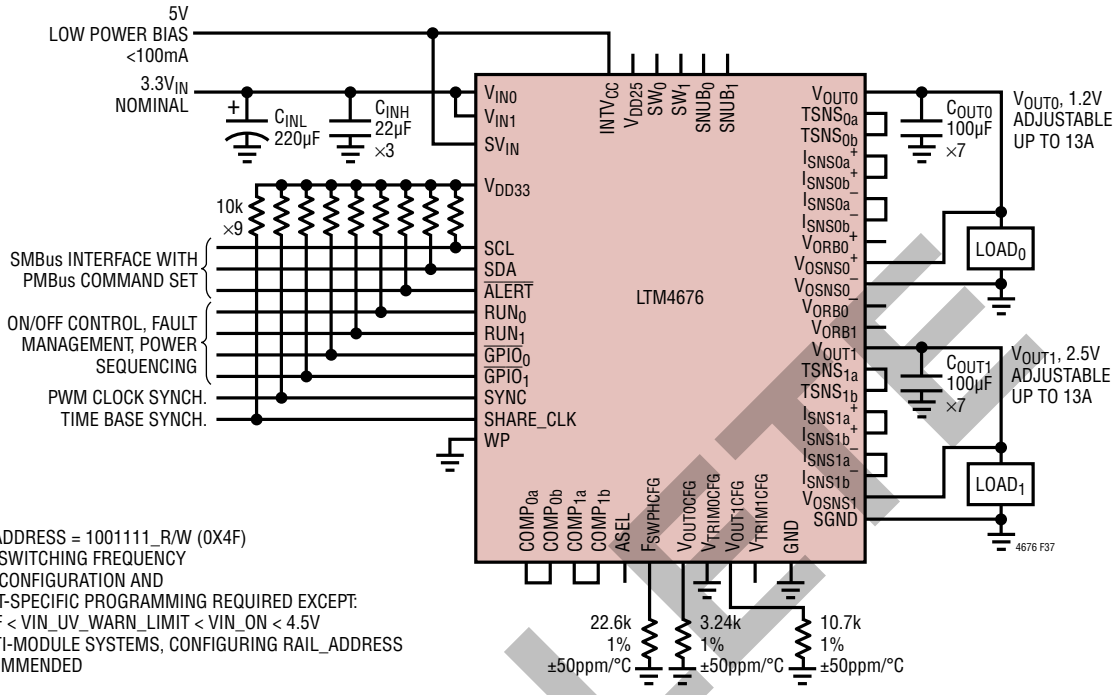
(a) $5V_{IN}$, Figure 35 Circuit



(b) $12V_{IN}$, Figure 35 Circuit with $INTV_{CC}$ Open and V_{OUT} Commanded to 1V

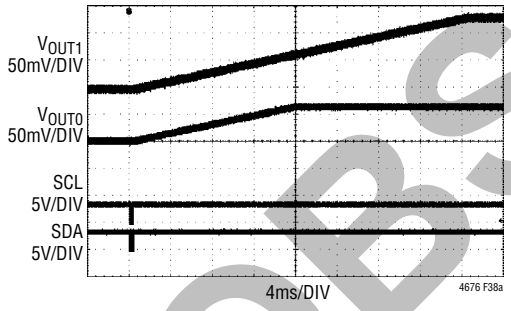
Figure 36. Current Sharing Performance of the LTM4676's Channels

TYPICAL APPLICATIONS

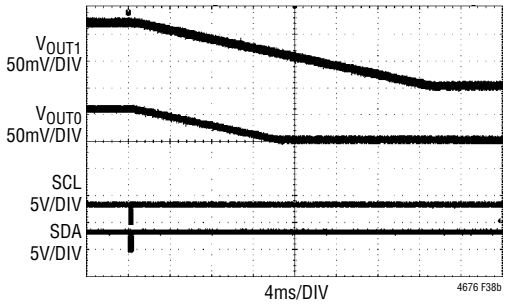


- SLAVE ADDRESS = 1001111_R/W (0X4F)
- 350kHz SWITCHING FREQUENCY
- NO GUI CONFIGURATION AND
  NO PART-SPECIFIC PROGRAMMING REQUIRED EXCEPT:
  VIN_OFF < VIN_UV_WARN_LIMIT < VIN_ON < 4.5V
  IN MULTI-MODULE SYSTEMS, CONFIGURING RAIL_ADDRESS
  IS RECOMMENDED

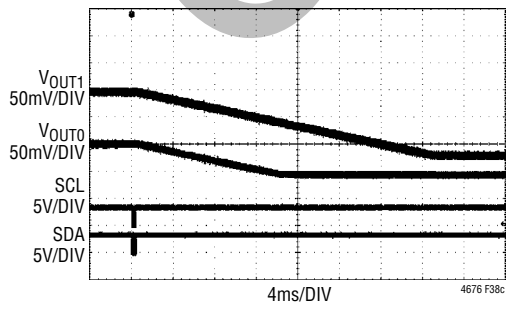
Figure 37. 13A, 1.2V and 2.5V Outputs Generated from 3.3V Power Input and Providing I²C/SMBus/PMBus Serial Interface



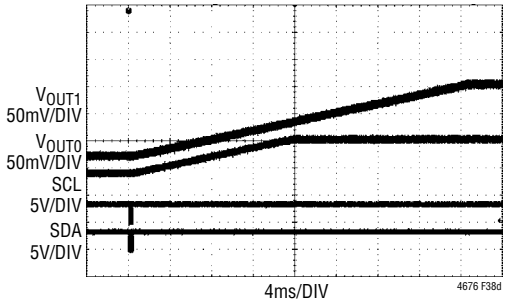
(a) PMBus Operation (Reg. 0x01): 0x80 → 0xA8 (Margin High)



(b) PMBus Operation (Reg. 0x01): 0xA8 → 0x80 (Margin Off)



(c) PMBus Operation (Reg. 0x01): 0x80 → 0x98 (Margin Low)



(d) PMBus Operation (Reg. 0x01): 0x98 → 0x80 (Margin Off)

Figure 38. Output Voltage Margining, Figure 37 Circuit

TYPICAL APPLICATIONS

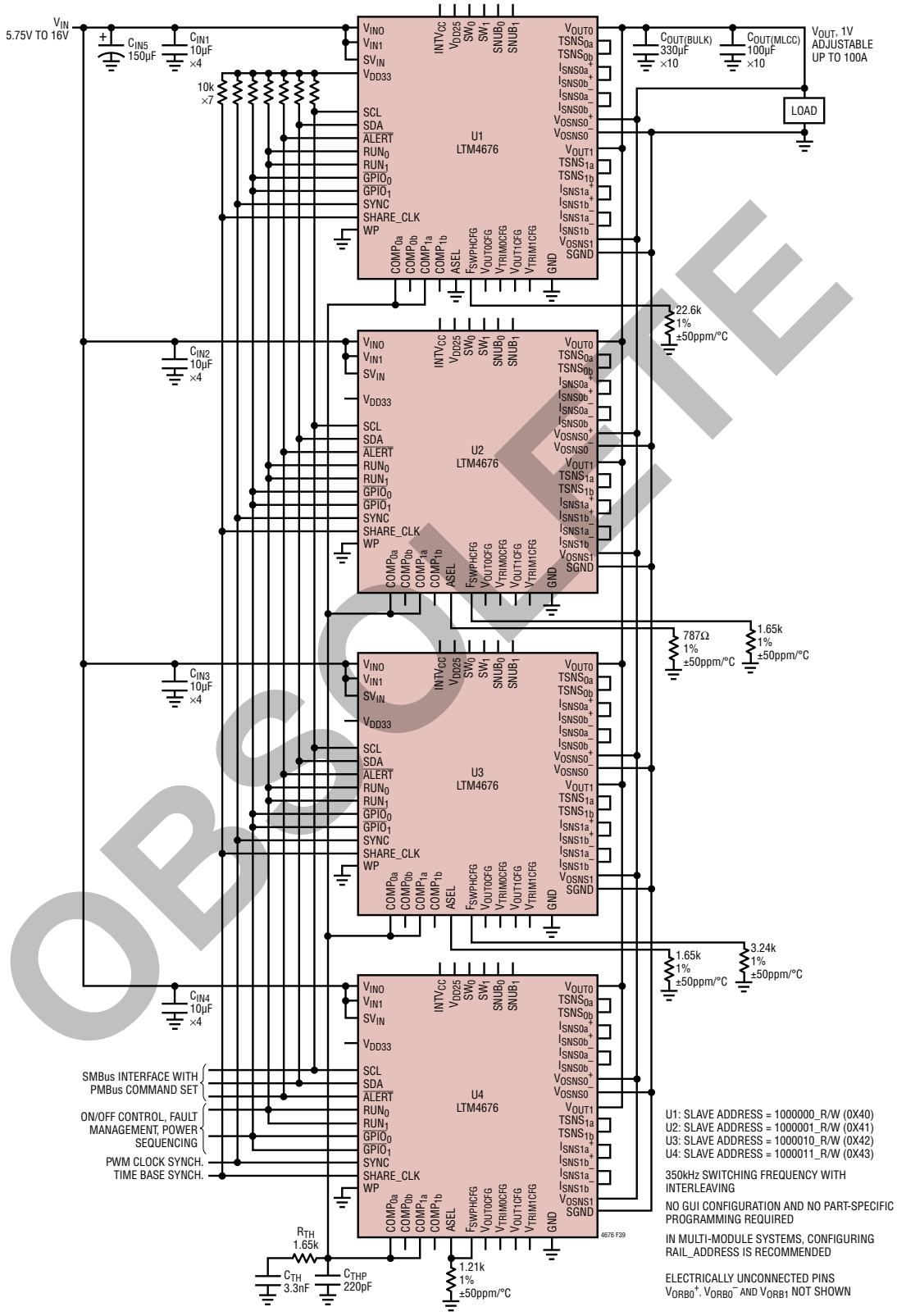
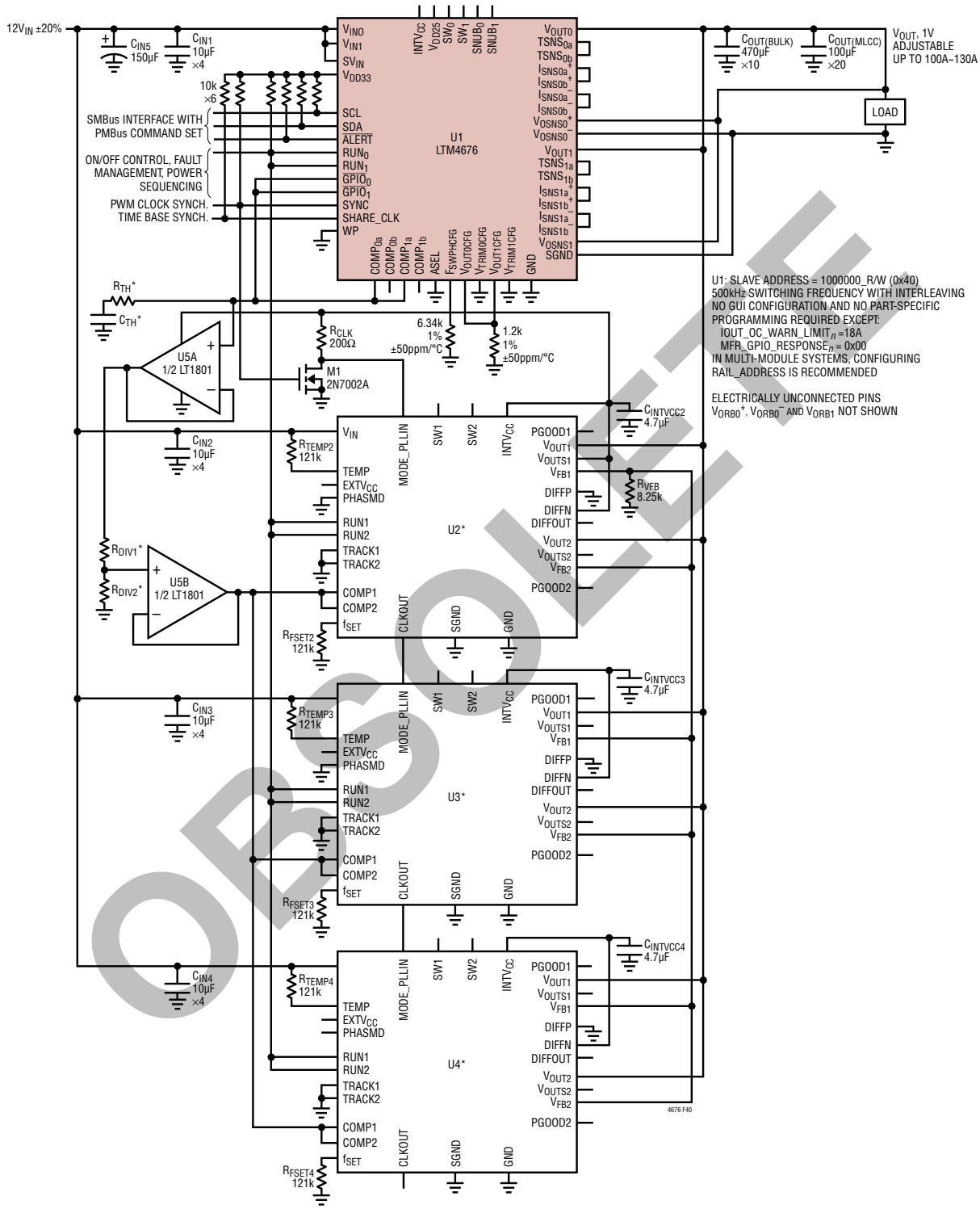


Figure 39. Four Paralleled LTM4676 Producing 1V$_{OUT}$ at Up to 100A. Integrated Power System Management Features Accessible Over 2-Wire I^{2}C/SMBus/PMBus Serial Interface. For Evaluation and More Information, See Demo Boards DC1989, DC1989A-C

TYPICAL APPLICATIONS

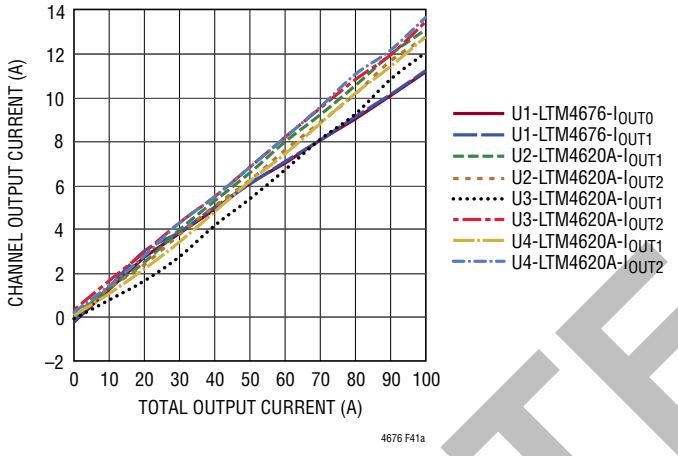


*STUFFING OPTIONS

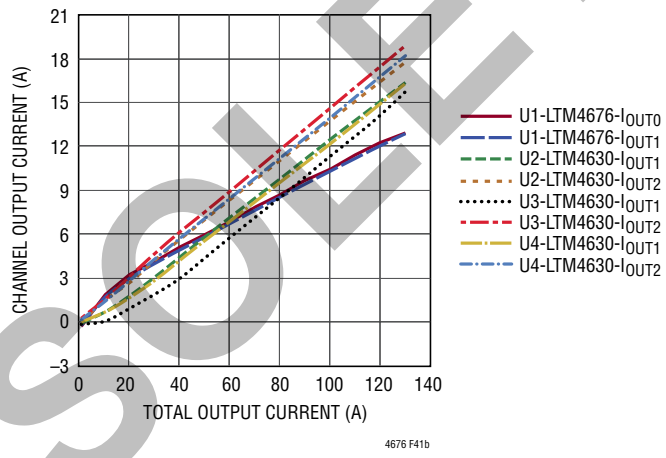
DEMO BOARD	OUTPUT CURRENT	U2, U3, U4	R_{DIV1}	R_{DIV2}	R_{TH}	C_{TH}
DC2106A-A	UP TO 100A	LTM4620A	23.2k	76.8k	6.98k	4.7nF
DC2106A-B	UP TO 130A	LTM4630	20k	80.6k	7.15k	2.2nF

Figure 40. One LTM4676 Operating In Parallel with 3xLTM4620A or 3xLTM4630 (See Demo Boards DC2106A-A, DC2106A-B) Producing 1V_{OUT} at up to 100A ~ 130A. Power System Management Features Accessible Through LTM4676. See Figure 41

TYPICAL APPLICATIONS



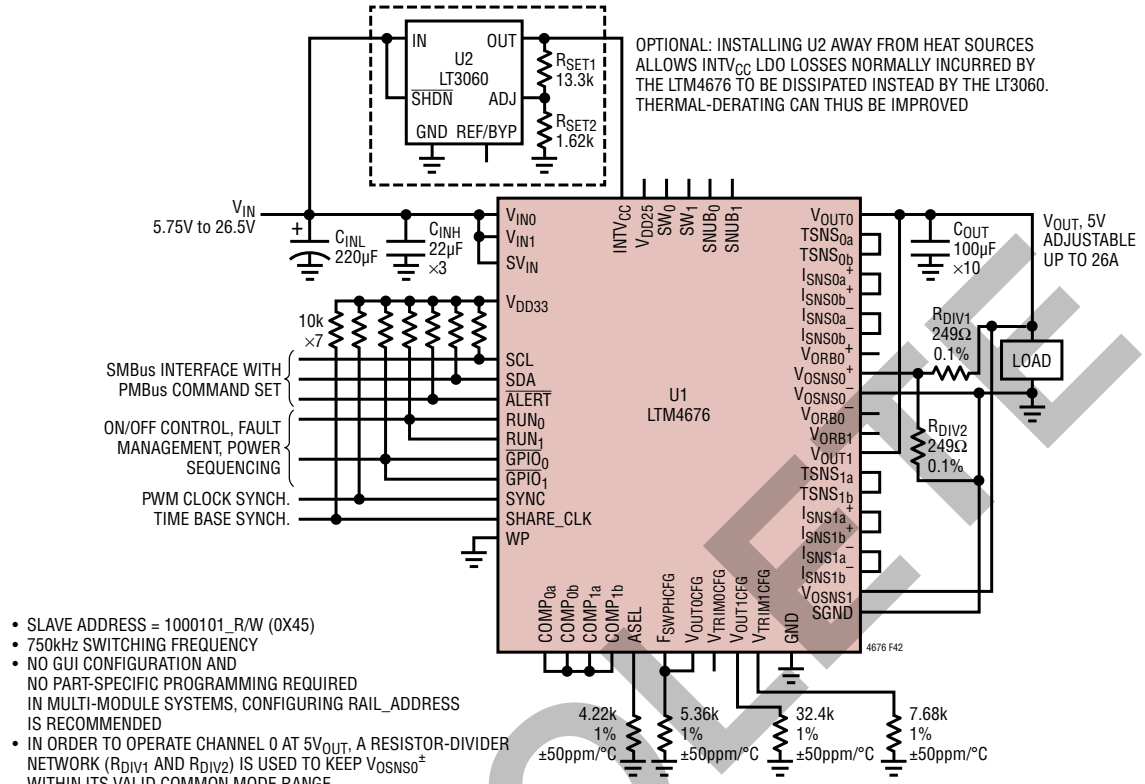
(a) LTM4676 Paralleled with 3x LTM4620A (Up to 100A Output)



(b) LTM4676 Paralleled with 3x LTM4630 (Up to 130A Output)

Figure 41. Current Sharing Performance of Figure 40 Circuit at $12V_{IN}$

TYPICAL APPLICATIONS



- SLAVE ADDRESS = 1000101_R/W (0X45)
- 750kHz SWITCHING FREQUENCY
- NO GUI CONFIGURATION AND NO PART-SPECIFIC PROGRAMMING REQUIRED IN MULTI-MODULE SYSTEMS, CONFIGURING RAIL_ADDRESS IS RECOMMENDED
- IN ORDER TO OPERATE CHANNEL 0 AT 5V_{OUT}, A RESISTOR-DIVIDER NETWORK (R_{DIV1} AND R_{DIV2}) IS USED TO KEEP $V_{OSNS0}^{\pm}$ WITHIN ITS VALID COMMON MODE RANGE
- AS A RESULT OF THE 2:1 FEEDBACK RESISTOR-DIVIDER NETWORK (R_{DIV1} AND R_{DIV2}), ALL LTM4676 CHANNEL 0 V_{OUT}-RELATED PARAMETERS, THRESHOLDS, AND V_{OUT} TELEMETRY ARE COMMANDED AND READBACK AS ONE-HALF OF WHAT IS DESIRED OR PRESENT AT THE LOAD (EXPLICITLY: 5V_{OUT} AT THE LOAD CORRESPONDS TO A $VOUT\_COMMAND_0$ SETTING OF 2.5V AND A $READ\_VOUT_0$ RESULT OF 2.5V)
- IN THIS CONFIGURATION, THE OUTPUT CURRENT READING OF CHANNEL 0 READS LOWER THAN NORMAL AND IS INVALID (AND SIMILARLY, FOR RELATED TELEMETRY: CHANNEL 0 OUTPUT POWER AND INPUT CURRENT READBACK). ALL CHANNEL 1 TELEMETRY, HOWEVER, REMAINS VALID

Figure 42. 26A, 5V Output DC/DC µModule Regulator with Serial Interface

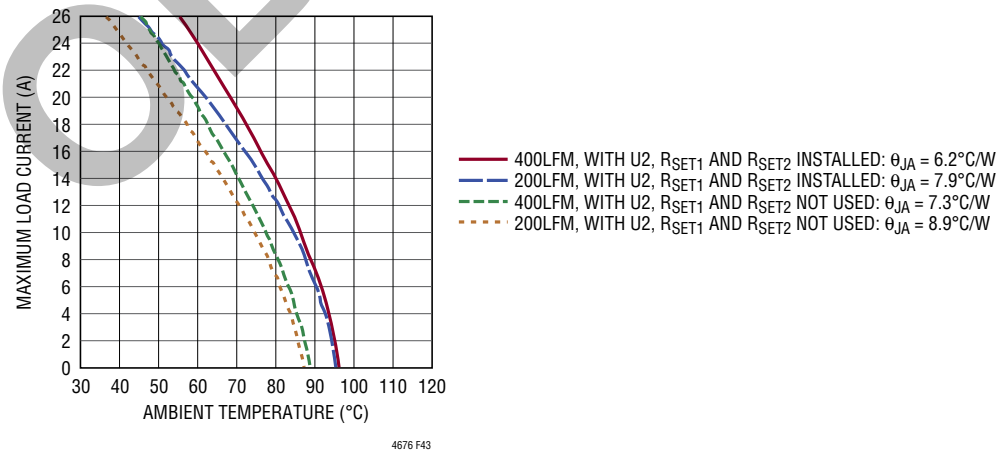


Figure 43. Output Derating Curve of Figure 42 Circuit Tested on DC1811A, 12V_{IN}, No Heat Sink

PACKAGE DESCRIPTION

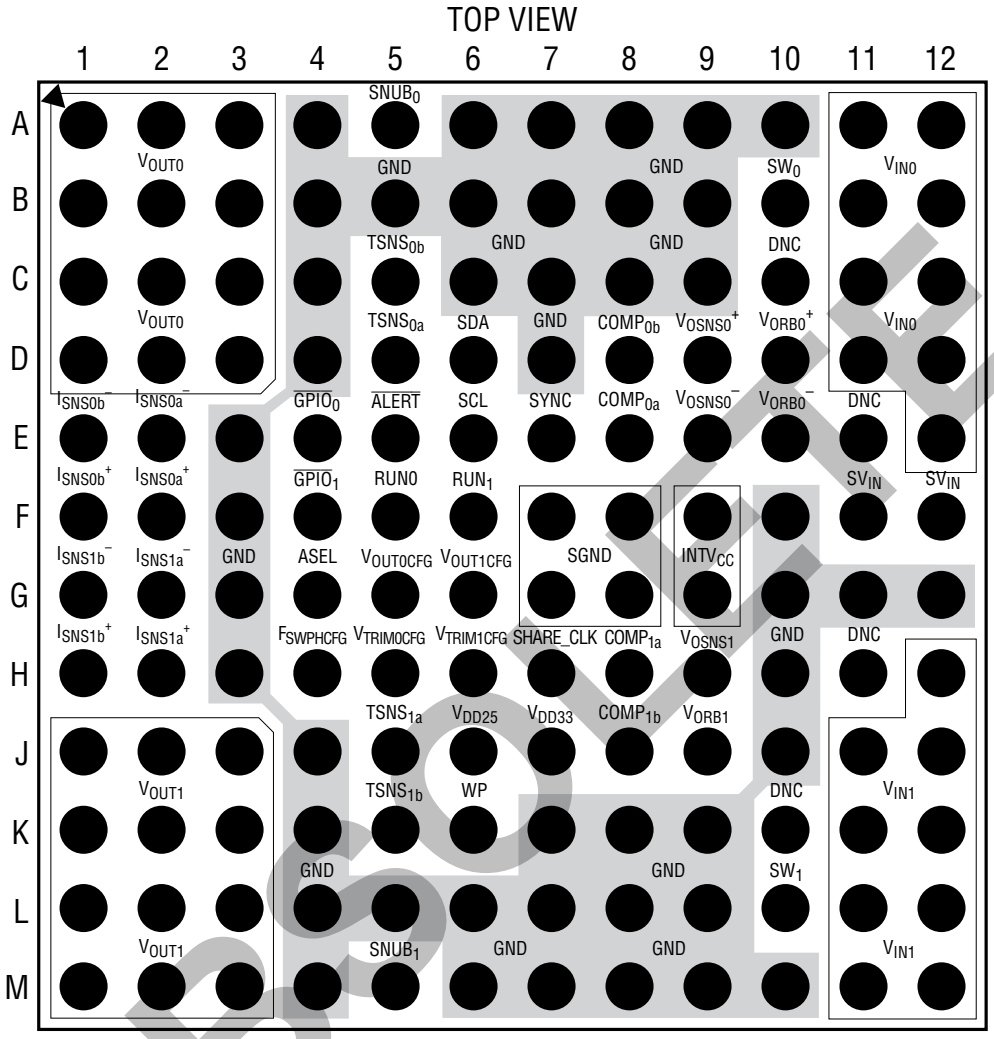
PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Table 21. LTM4676 BGA Pinout

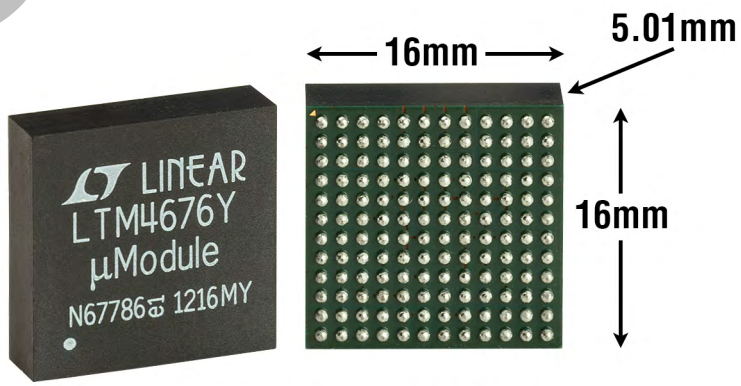
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT0}	B1	V_{OUT0}	C1	V_{OUT0}	D1	V_{OUT0}	E1	I_{SNS0b}^-	F1	I_{SNS0b}^+
A2	V_{OUT0}	B2	V_{OUT0}	C2	V_{OUT0}	D2	V_{OUT0}	E2	I_{SNS0a}^-	F2	I_{SNS0a}^+
A3	V_{OUT0}	B3	V_{OUT0}	C3	V_{OUT0}	D3	V_{OUT0}	E3	GND	F3	GND
A4	GND	B4	GND	C4	GND	D4	GND	E4	$\overline{GPIO_0}$	F4	$\overline{GPIO_1}$
A5	$SNUB_0$	B5	GND	C5	$TSNS_{0b}$	D5	$TSNS_{0a}$	E5	$\overline{ALERT}$	F5	RUN_0
A6	GND	B6	GND	C6	GND	D6	SDA	E6	SCL	F6	RUN_1
A7	GND	B7	GND	C7	GND	D7	GND	E7	SYNC	F7	SGND
A8	GND	B8	GND	C8	GND	D8	$COMP_{0b}$	E8	$COMP_{0a}$	F8	SGND
A9	GND	B9	GND	C9	GND	D9	V_{OSNS0}^+	E9	V_{OSNS0}^-	F9	$INTV_{CC}$
A10	GND	B10	SW_0	C10	DNC	D10	V_{ORB0}^+	E10	V_{ORB0}^-	F10	GND
A11	V_{IN0}	B11	V_{IN0}	C11	V_{IN0}	D11	V_{IN0}	E11	DNC	F11	SV_{IN}
A12	V_{IN0}	B12	V_{IN0}	C12	V_{IN0}	D12	V_{IN0}	E12	V_{IN0}	F12	SV_{IN}

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	I_{SNS1b}^-	H1	I_{SNS1b}^+	J1	V_{OUT1}	K1	V_{OUT1}	L1	V_{OUT1}	M1	V_{OUT1}
G2	I_{SNS1a}^-	H2	I_{SNS1a}^+	J2	V_{OUT1}	K2	V_{OUT1}	L2	V_{OUT1}	M2	V_{OUT1}
G3	GND	H3	GND	J3	V_{OUT1}	K3	V_{OUT1}	L3	V_{OUT1}	M3	V_{OUT1}
G4	ASEL	H4	$F_{SWPHCFG}$	J4	GND	K4	GND	L4	GND	M4	GND
G5	$V_{OUT0CFG}$	H5	$V_{TRIM0CFG}$	J5	$TSNS_{1a}$	K5	$TSNS_{1b}$	L5	GND	M5	$SNUB_1$
G6	$V_{OUT1CFG}$	H6	$V_{TRIM1CFG}$	J6	V_{DD25}	K6	WP	L6	GND	M6	GND
G7	SGND	H7	SHARE_CLK	J7	V_{DD33}	K7	GND	L7	GND	M7	GND
G8	SGND	H8	$COMP_{1a}$	J8	$COMP_{1b}$	K8	GND	L8	GND	M8	GND
G9	$INTV_{CC}$	H9	V_{OSNS1}	J9	V_{ORB1}	K9	GND	L9	GND	M9	GND
G10	GND	H10	GND	J10	GND	K10	DNC	L10	SW1	M10	GND
G11	GND	H11	DNC	J11	V_{IN1}	K11	V_{IN1}	L11	V_{IN1}	M11	V_{IN1}
G12	GND	H12	V_{IN1}	J12	V_{IN1}	K12	V_{IN1}	L12	V_{IN1}	M12	V_{IN1}

PACKAGE DESCRIPTION

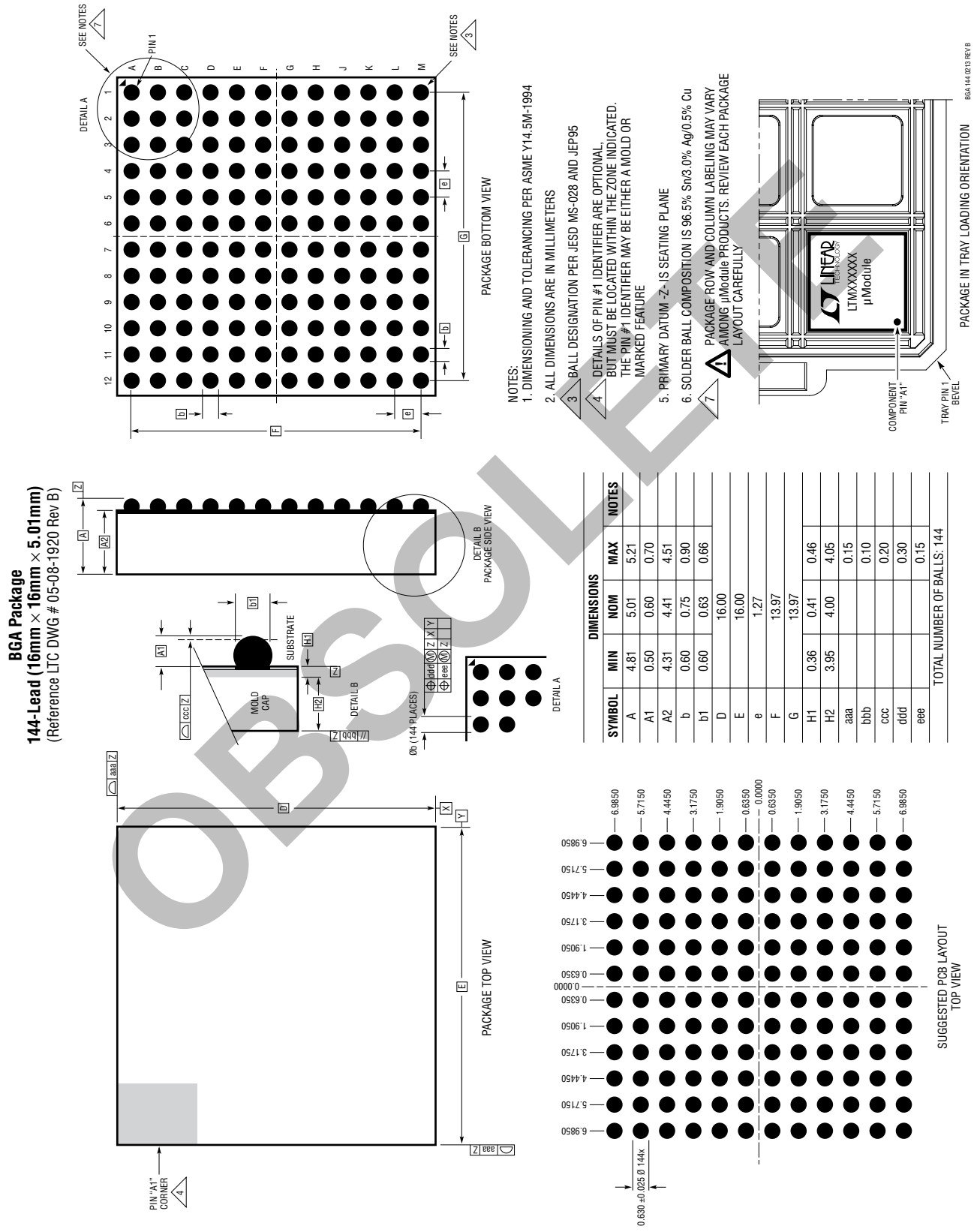


PACKAGE PHOTOGRAPH



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/13	Added Video Tech Clip link	1
		Corrected figure numbers in Tables 15, 16 and 17	61
B	2/14	Added SnPb BGA option	1, 3
		Updated part number in Figure 40	71
C	8/14	Update Note 13	10
		Update Block Diagram	19
		Update Functional Diagram	20
		Update Test Circuits	21
		Update I^2C Commands	27
		Update Manufacturer Product ID Code	28, 40
		Update "RESTORE_USER_ALL" Attributes	35
		Correct Phase Information in Table 4	43
		Update Figures 35, 37, 44	68, 69, 78
D	09/15	Clarified pin function descriptions	18

TYPICAL APPLICATION

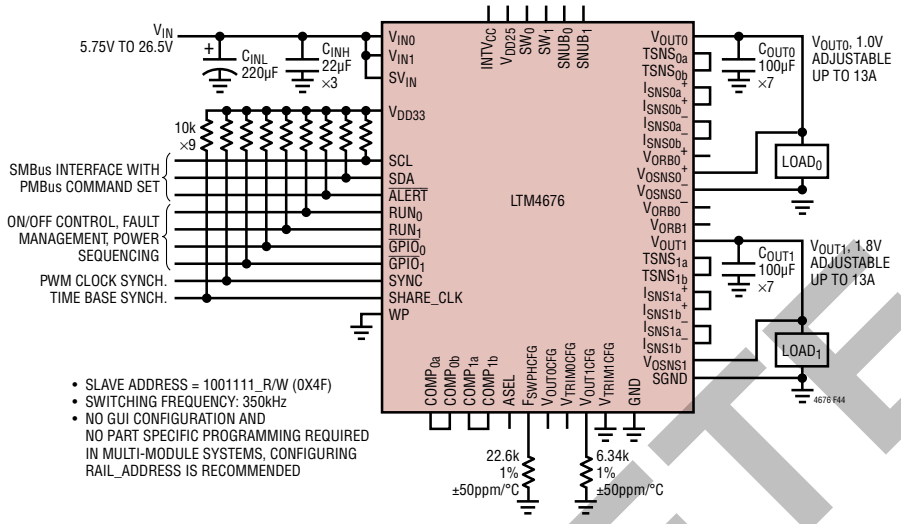


Figure 44. 13A, 1V and 13A, 1.8V Output DC/DC µModule Regulator with Serial Interface

DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search Input V_{in} (Min) V V_{in} (Max) V Output V_{out} V I_{out} A Search	
TechClip Videos	Quick videos detailing how to bench test electrical and thermal performance of µModule products.	
Digital Power System Management	Linear Technology's family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4675	Smaller, Lower Power than LTM4676	Dual 9A, Single 18A; 11.9mm x 16mm BGA; Fits in the Larger Foot Print Layout of the LTM4676 Dual 13A
LTM4676A	Faster Turn-On Time than LTM4676	70ms vs. 170ms; Pin-Compatible with the LTM4676; up to 5.5V_{OUT}
LTM2987	16-Channnel PMBus Power System Manager	Provides Digital Telemetry Control of Several POL Regulators: Fault Log, Margin, Trip, etc.
LTpowerPlay	Free Evaluation and Development Software for Linear Technology's Digital Power System Manager Products (I^2C/PMBus/SMBus Interface)	Program and Adjust Power Management Schemes; Includes Diagnostics and Debugging; Automatic Software Update and Device Drivers