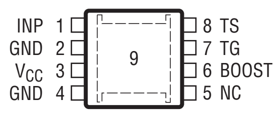
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
V_{CC} .... –0.3V to 15V
BOOST – TS.. –0.3V to 15V
INP Voltage .... –0.3V to 15V
BOOST Voltage (Continuous) .... –0.3V to 95V
BOOST Voltage (100ms) ....–0.3V to 115V
TS Voltage (Continuous) .... –5V to 80V
TS Voltage (100ms) .... –5V to 100V
Peak Output Current < 1µs (TG)................................ 4A
Driver Output TG (with Respect to TS)....... –0.3V to 15V
Operating Temperature Range (Note 2)
LTC4440E ....–40°C to 85°C
LTC4440I ....–40°C to 125°C
Junction Temperature (Note 3) .... 125°C
Storage Temperature Range ....–65°C to 150°C
Lead Temperature (Soldering, 10 sec)...................300°C

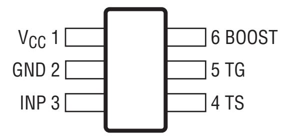
PIN CONFIGURATION

TOP VIEW



MS8E PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 40°C/W (NOTE 4)
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

TOP VIEW



S6 PACKAGE
6-LEAD PLASTIC SOT-23
T_{JMAX} = 125°C, θ_{JA} = 230°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4440EMS8E#PBF	LTC4440EMS8E#TRPBF	LTF9	8-Lead Plastic MSOP	–40°C to 85°C
LTC4440IMS8E#PBF	LTC4440IMS8E#TRPBF	LTF9	8-Lead Plastic MSOP	–40°C to 125°C
LTC4440ES6#PBF	LTC4440ES6#TRPBF	LTZY	6-Lead Plastic SOT-23	–40°C to 85°C
LTC4440IS6#PBF	LTC4440IS6#TRPBF	LTZY	6-Lead Plastic SOT-23	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{BOOST} = 12V, V_{TS} = GND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Supply (V_{CC})							
I_{VCC}	DC Supply Current Normal Operation UVLO	 INP = 0V V_{CC} < UVLO Threshold (Falling) – 0.1V			 250 25	 400 80	 µA µA
UVLO	Undervoltage Lockout Threshold	V_{CC} Rising V_{CC} Falling Hysteresis	● ●	5.7 5.4	6.5 6.2 300	7.3 7.0	V V mV
Bootstrapped Supply (BOOST – TS)							
I_{BOOST}	DC Supply Current Normal Operation UVLO	 INP = 0V V_{BOOST} – V_{TS} < $UVLO_{HS(FALLING)}$ – 0.1V, V_{CC} = INP = 5V			 110 86	 180 170	 µA µA
$UVLO_{HS}$	Undervoltage Lockout Threshold	V_{BOOST} – V_{TS} Rising V_{BOOST} – V_{TS} Falling Hysteresis	● ●	6.75 6.25	7.4 6.9 500	7.95 7.60	V V mV
Input Signal (INP)							
V_{IH}	High Input Threshold	INP Ramping High	●	1.3	1.6	2	V
V_{IL}	Low Input Threshold	INP Ramping Low	●	0.85	1.25	1.6	V
V_{IH} – V_{IL}	Input Voltage Hysteresis				0.350		V
I_{INP}	Input Pin Bias Current				±0.01	±2	µA
Output Gate Driver (TG)							
V_{OH}	High Output Voltage	I_{TG} = –10mA, V_{OH} = V_{BOOST} – V_{TG}			0.7		V
V_{OL}	Low Output Voltage	I_{TG} = 100mA: 0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ 125°C	 ● ●		 150 150	 220 300	 mV mV
I_{PU}	Peak Pull-Up Current	0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ 125°C	● ●	1.7 1.5	2.4 2.4		A A
R_{DS}	Output Pull-Down Resistance	0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ 125°C	● ●		1.5 1.5	2.2 3	Ω Ω
Switching Timing							
t_r	Output Rise Time	10% – 90%, C_L = 1nF 10% – 90%, C_L = 10nF			10 100		ns ns
t_f	Output Fall Time	10% – 90%, C_L = 1nF 10% – 90%, C_L = 10nF			7 70		ns ns
t_{PLH}	Output Low-High Propagation Delay	0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ 125°C	● ●		30 30	65 75	ns ns
t_{PHL}	Output High-Low Propagation Delay	0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ 125°C	● ●		28 28	65 75	ns ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC4440E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4440I is guaranteed and tested over the –40°C to 125°C operating temperature range.

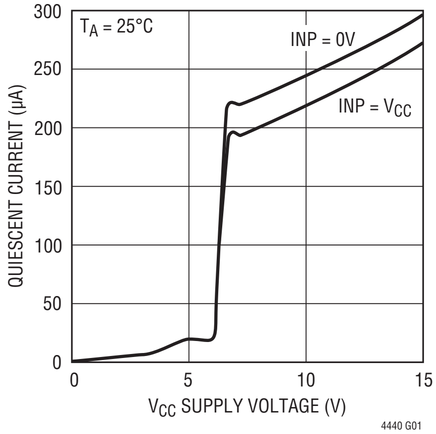
Note 3: T_J is calculated from the ambient temperature T_A and power dissipation PD according to the following formula:

$T_J = T_A + (PD \bullet \theta_{JA}°C/W)$

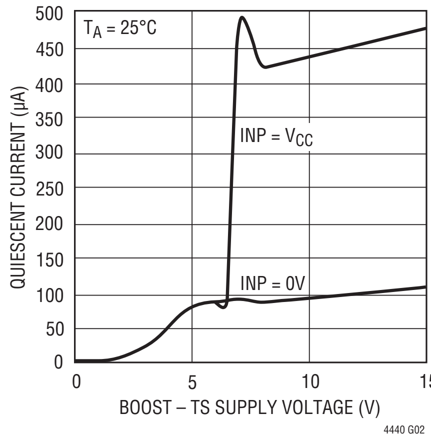
Note 4: Failure to solder the exposed back side of the MS8E package to the PC board will result in a thermal resistance much higher than 40°C/W.

TYPICAL PERFORMANCE CHARACTERISTICS

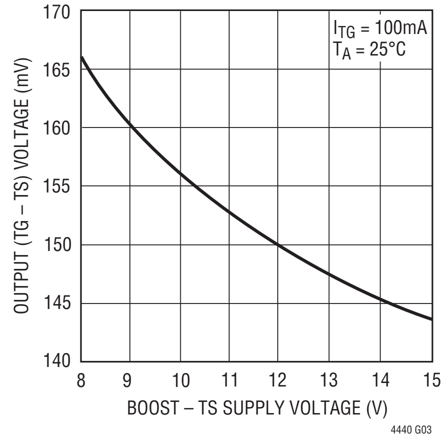
V_{CC} Supply Quiescent Current vs Voltage



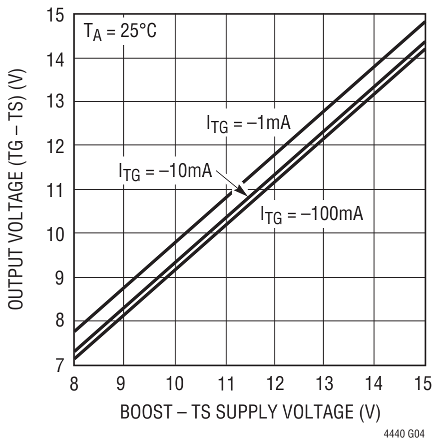
BOOST – TS Supply Quiescent Current vs Voltage



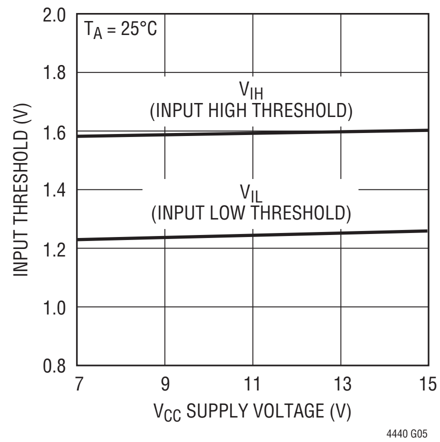
Output Low Voltage (V_{OL}) vs Supply Voltage



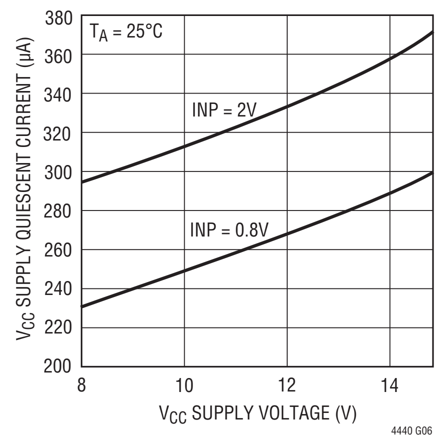
Output High Voltage (V_{OH}) vs Supply Voltage



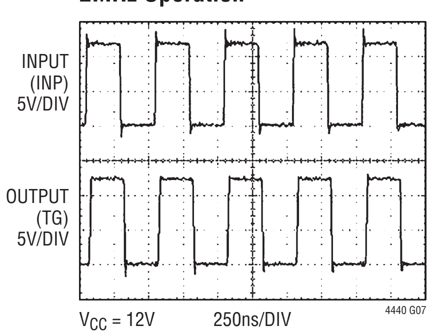
Input Thresholds (INP) vs Supply Voltage



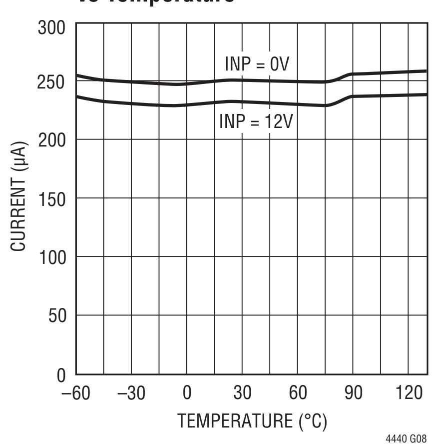
V_{CC} Supply Current at TTL Input Levels



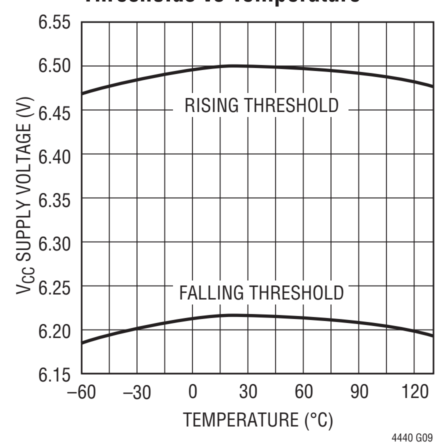
2MHz Operation



V_{CC} Supply Current (V_{CC} = 12V) vs Temperature

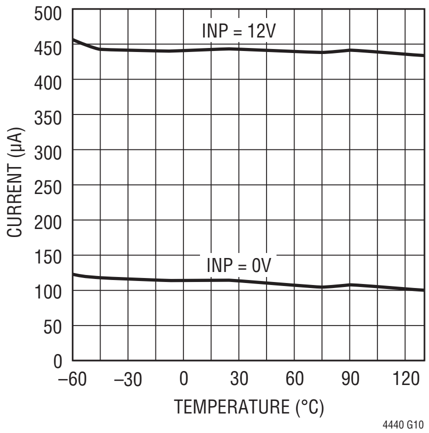


V_{CC} Undervoltage Lockout Thresholds vs Temperature

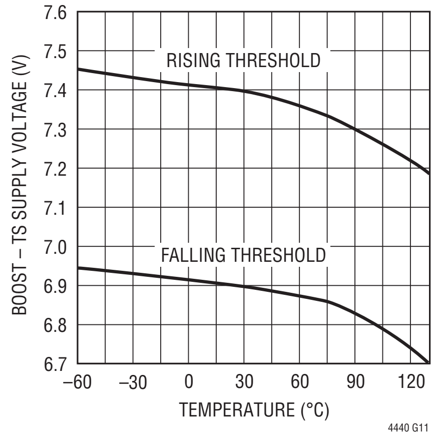


TYPICAL PERFORMANCE CHARACTERISTICS

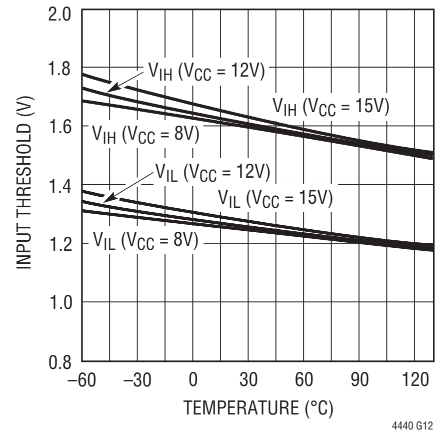
Boost Supply Current vs Temperature



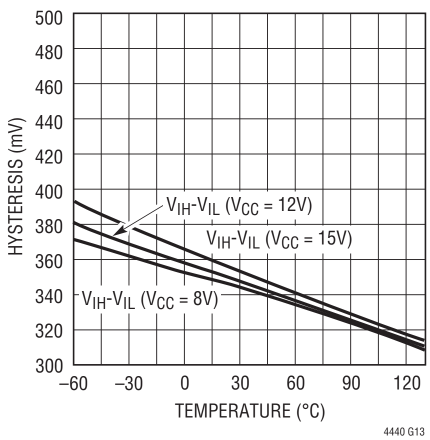
Boost Supply (BOOST – TS) Undervoltage Lockout Thresholds vs Temperature



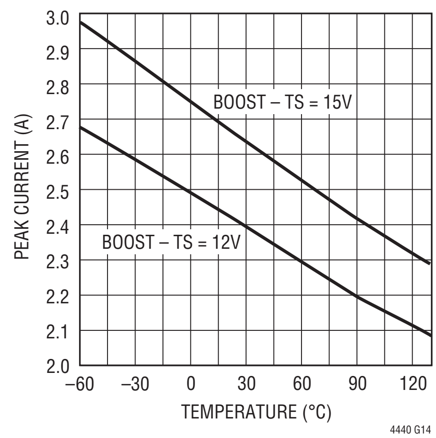
Input Threshold vs Temperature



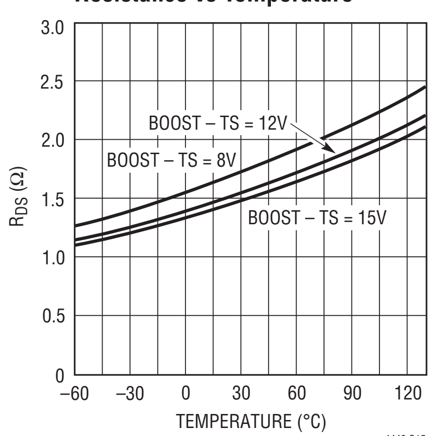
Input Threshold Hysteresis vs Temperature



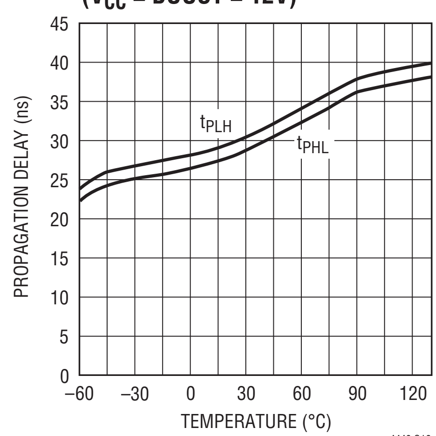
Peak Driver (TG) Pull-Up Current vs Temperature



Output Driver Pull-Down Resistance vs Temperature



Propagation Delay vs Temperature (V_{CC} = BOOST = 12V)



PIN FUNCTIONS

SOT-23 Package

V_{CC} (Pin 1): Chip Supply. This pin powers the internal low side circuitry. A low ESR ceramic bypass capacitor should be tied between this pin and the GND pin (Pin 2).

GND (Pin 2): Chip Ground.

INP (Pin 3): Input Signal. TTL/CMOS compatible input referenced to GND (Pin 2).

TS (Pin 4): Top (High Side) Source Connection.

TG (Pin 5): High Current Gate Driver Output (Top Gate). This pin swings between TS and BOOST.

BOOST (Pin 6): High Side Bootstrapped Supply. An external capacitor should be tied between this pin and TS (Pin 4). Normally, a bootstrap diode is connected between V_{CC} (Pin 1) and this pin. Voltage swing at this pin is from $V_{CC} – V_D$ to $V_{IN} + V_{CC} – V_D$, where V_D is the forward voltage drop of the bootstrap diode.

Exposed Pad MS8E Package

INP (Pin 1): Input Signal. TTL/CMOS compatible input referenced to GND (Pin 2).

GND (Pins 2, 4): Chip Ground.

V_{CC} (Pin 3): Chip Supply. This pin powers the internal low side circuitry. A low ESR ceramic bypass capacitor should be tied between this pin and the GND pin (Pin 2).

NC (Pin 5): No Connect. No connection required. For convenience, this pin may be tied to Pin 6 (BOOST) on the application board.

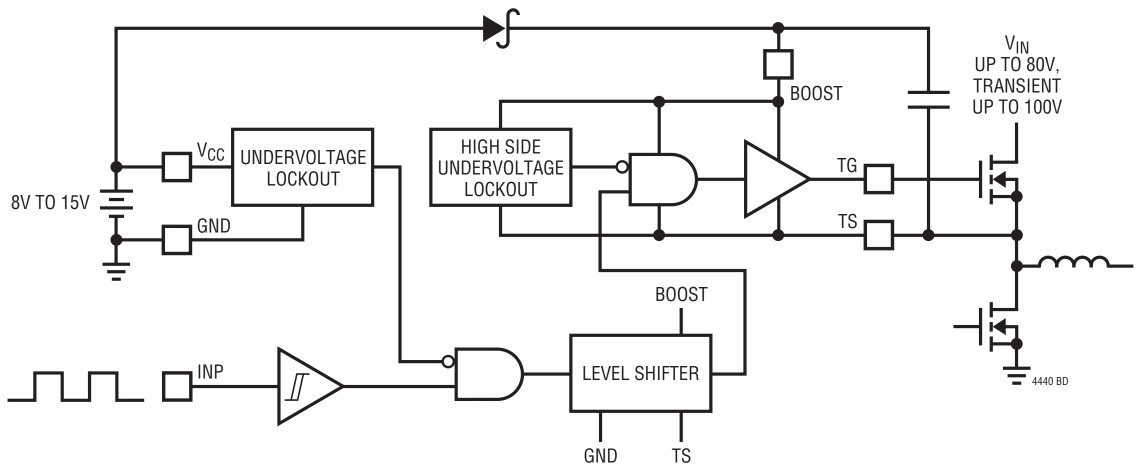
BOOST (Pin 6): High Side Bootstrapped Supply. An external capacitor should be tied between this pin and TS (Pin 8). Normally, a bootstrap diode is connected between V_{CC} (Pin 3) and this pin. Voltage swing at this pin is from $V_{CC} – V_D$ to $V_{IN} + V_{CC} – V_D$, where V_D is the forward voltage drop of the bootstrap diode.

TG (Pin 7): High Current Gate Driver Output (Top Gate). This pin swings between TS and BOOST.

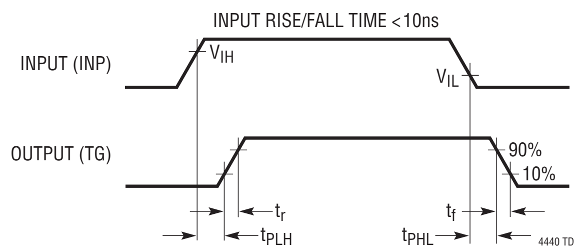
TS (Pin 8): Top (High Side) Source Connection.

Exposed Pad (Pin 9): Ground. Must be electrically connected to Pins 2 and 4 and soldered to PCB ground for optimum thermal performance.

BLOCK DIAGRAM



TIMING DIAGRAM



APPLICATIONS INFORMATION

Overview

The LTC4440 receives a ground-referenced, low voltage digital input signal to drive a high side N-channel power MOSFET whose drain can float up to 100V above ground, eliminating the need for a transformer between the low voltage control signal and the high side gate driver. The LTC4440 normally operates in applications with input supply voltages (V_{IN}) up to 80V, but is able to withstand and continue to function during 100V, 100ms transients on the input supply.

The powerful output driver of the LTC4440 reduces the switching losses of the power MOSFET, which increase with transition time. The LTC4440 is capable of driving a 1nF load with 10ns rise and 7ns fall times using a bootstrapped supply voltage $V_{BOOST-TS}$ of 12V.

Input Stage

The LTC4440 employs TTL/CMOS compatible input thresholds that allow a low voltage digital signal to drive standard power MOSFETs. The LTC4440 contains an internal voltage regulator that biases the input buffer, allowing the input thresholds (V_{IH} = 1.6V, V_{IL} = 1.25V) to be independent of variations in V_{CC}. The 350mV hysteresis between V_{IH} and V_{IL} eliminates false triggering due to noise during switching transitions. However, care should be taken to keep this pin from any noise pickup, especially in high frequency, high voltage applications. The LTC4440 input buffer has a high input impedance and draws negligible input current, simplifying the drive circuitry required for the input.

Output Stage

A simplified version of the LTC4440's output stage is shown in Figure 3 . The pull-down device is an N-channel MOSFET (N1) and the pull-up device is an NPN bipolar junction transistor (Q1). The output swings from the lower rail (TS) to within an NPN V_{BE} (~0.7V) of the positive rail (BOOST). This large voltage swing is important in driving external power MOSFETs, whose $R_{DS(ON)}$ is inversely proportional to its gate overdrive voltage ($V_{GS} - V_{TH}$).

The LTC4440's peak pull-up (Q1) current is 2.4A while the pull-down (N1) resistance is 1.5Ω. The low impedance of N1 is required to discharge the power MOSFET's gate capacitance during high-to-low signal transitions. When the power MOSFET's gate is pulled low (gate shorted to source through N1) by the LTC4440, its source (TS) is pulled low by its load (e.g., an inductor or resistor). The slew rate of the source/gate voltage causes current to flow back to the MOSFET's gate through the gate-to-drain capacitance (C_{GD}). If the MOSFET driver does not have sufficient sink current capability (low output impedance), the current through the power MOSFET's C_{GD} can momentarily pull the gate high, turning the MOSFET back on.

A similar scenario exists when the LTC4440 is used to drive a low side MOSFET. When the low side power MOSFET's gate is pulled low by the LTC4440, its drain voltage is pulled high by its load (e.g., inductor or resistor). The slew rate of the drain voltage causes current to flow back to the MOSFET's gate through its gate-to-drain capacitance. If

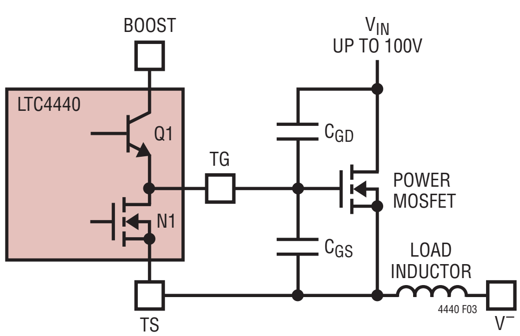


Figure 3. Capacitance Seen by TG During Switching

APPLICATIONS INFORMATION

the MOSFET driver does not have sufficient sink current capability (low output impedance), the current through the power MOSFET's C_{GD} can momentarily pull the gate high, turning the MOSFET back on.

Rise/Fall Time

Since the power MOSFET generally accounts for the majority of the power loss in a converter, it is important to quickly turn it on or off, thereby minimizing the transition time in its linear region. The LTC4440 can drive a 1nF load with a 10ns rise time and 7ns fall time.

The LTC4440's rise and fall times are determined by the peak current capabilities of Q1 and N1. The predriver that drives Q1 and N1 uses a nonoverlapping transition scheme to minimize cross-conduction currents. N1 is fully turned off before Q1 is turned on and vice versa.

Power Dissipation

To ensure proper operation and long-term reliability, the LTC4440 must not operate beyond its maximum temperature rating. Package junction temperature can be calculated by:

$$T_J = T_A + PD\,(\theta_{JA})$$

where:

T_J = Junction Temperature

T_A = Ambient Temperature

PD = Power Dissipation

θ_{JA} = Junction-to-Ambient Thermal Resistance

Power dissipation consists of standby and switching power losses:

$$PD = P_{STDBY} + P_{AC}$$

where:

P_{STDBY} = Standby Power Losses

P_{AC} = AC Switching Losses

The LTC4440 consumes very little current during standby. The DC power loss at V_{CC} = 12V and $V_{BOOST–TS}$ = 12V is only (250µA + 110µA)(12V) = 4.32mW.

AC switching losses are made up of the output capacitive load losses and the transition state losses. The capacitive load losses are primarily due to the large AC currents needed to charge and discharge the load capacitance during switching. Load losses for the output driver driving a pure capacitive load C_{OUT} would be:

$$\text{Load Capacitive Power} = (C_{OUT})(f)(V_{BOOST-TS})^2$$

The power MOSFET's gate capacitance seen by the driver output varies with its V_{GS} voltage level during switching. A power MOSFET's capacitive load power dissipation can be calculated using its gate charge, Q_G. The Q_G value corresponding to the MOSFET's V_{GS} value (V_{CC} in this case) can be readily obtained from the manufacturer's Q_G vs V_{GS} curves:

$$\text{Load Capacitive Power (MOS)} = (V_{BOOST-TS})(Q_G)(f)$$

Transition state power losses are due to both AC currents required to charge and discharge the driver's internal nodal capacitances and cross-conduction currents in the internal gates.

APPLICATIONS INFORMATION

Undervoltage Lockout (UVLO)

The LTC4440 contains both low side and high side undervoltage lockout detectors that monitor V_{CC} and the bootstrapped supply $V_{BOOST–TS}$. When V_{CC} falls below 6.2V, the internal buffer is disabled and the output pin OUT is pulled down to TS. When $V_{BOOST – TS}$ falls below 6.9V, OUT is pulled down to TS. When both supplies are undervoltage, OUT is pulled low to TS and the chip enters a low current mode, drawing approximately 25µA from V_{CC} and 86µA from BOOST.

Bypassing and Grounding

The LTC4440 requires proper bypassing on the V_{CC} and $V_{BOOST–TS}$ supplies due to its high speed switching (nanoseconds) and large AC currents (Amperes). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot.

To obtain the optimum performance from the LTC4440:

A. Mount the bypass capacitors as close as possible between the V_{CC} and GND pins and the BOOST and TS pins. The leads should be shortened as much as possible to reduce lead inductance.

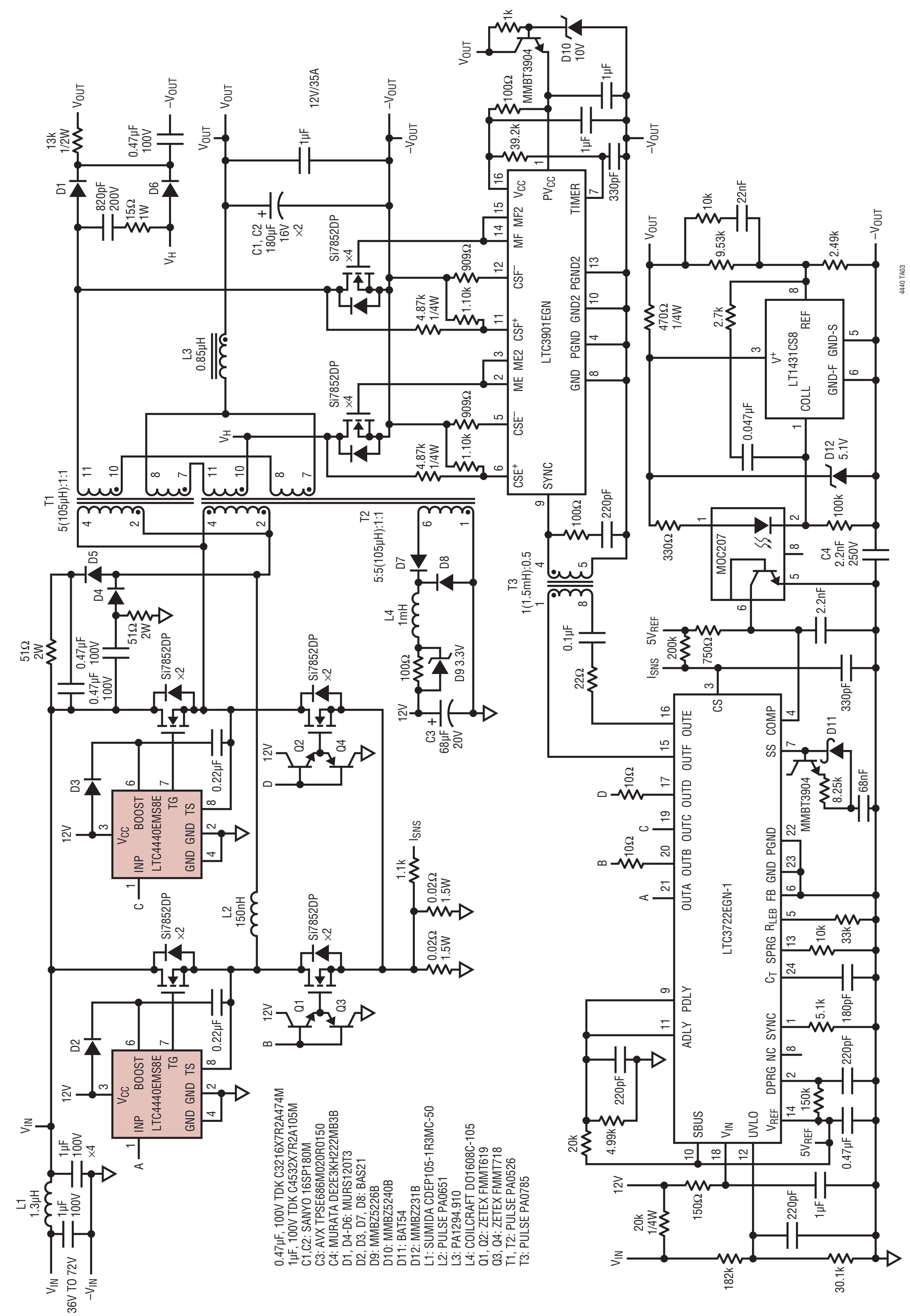
B. Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LTC4440 switches >2A peak currents and any significant ground drop will degrade signal integrity.

C. Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.

D. Keep the copper trace between the driver output pin and the load short and wide.

E. When using the MS8E package, be sure to solder the exposed pad on the back side of the LTC4440 package to the board. Correctly soldered to a 2500mm^2 double-sided 1oz copper board, the LTC4440 has a thermal resistance of approximately 40°C/W. Failure to make good thermal contact between the exposed back side and the copper board will result in thermal resistances far greater than 40°C/W.

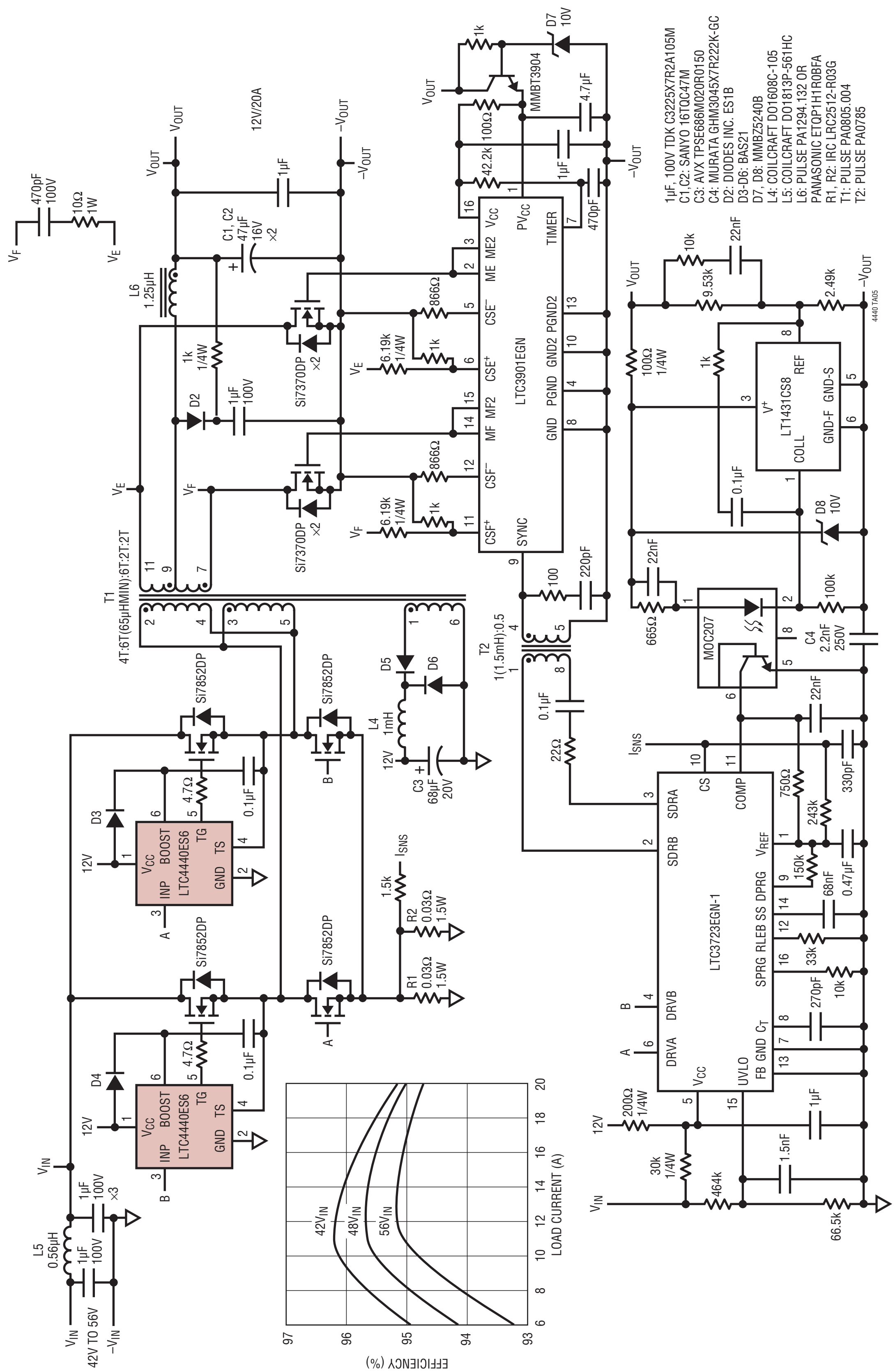
TYPICAL APPLICATIONS



LTC3722/LTC4440 420W 36V-72V$_{IN}$ to 12V/35A Isolated Full-Bridge Supply

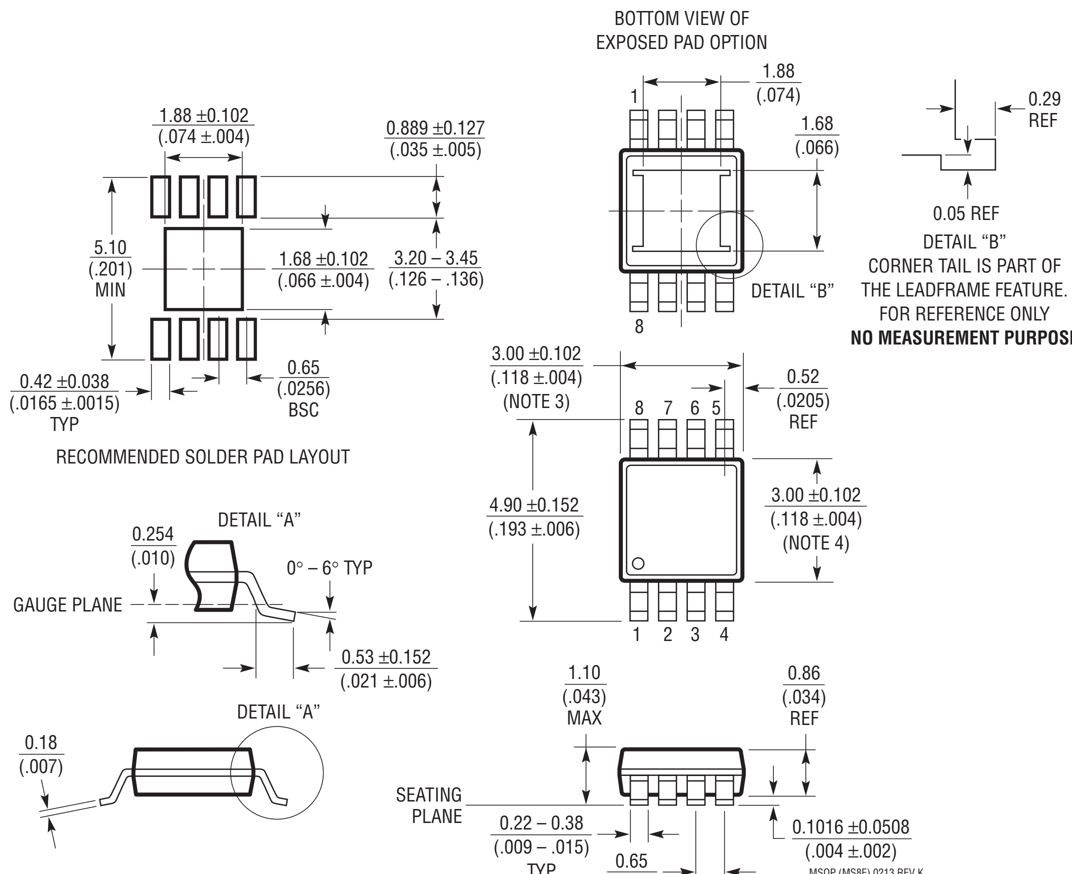
TYPICAL APPLICATIONS

LTC3723-1 240W 42-56V_{IN} to 12V/20A Isolated 1/4Brick (2.3" × 1.45")



PACKAGE DESCRIPTION

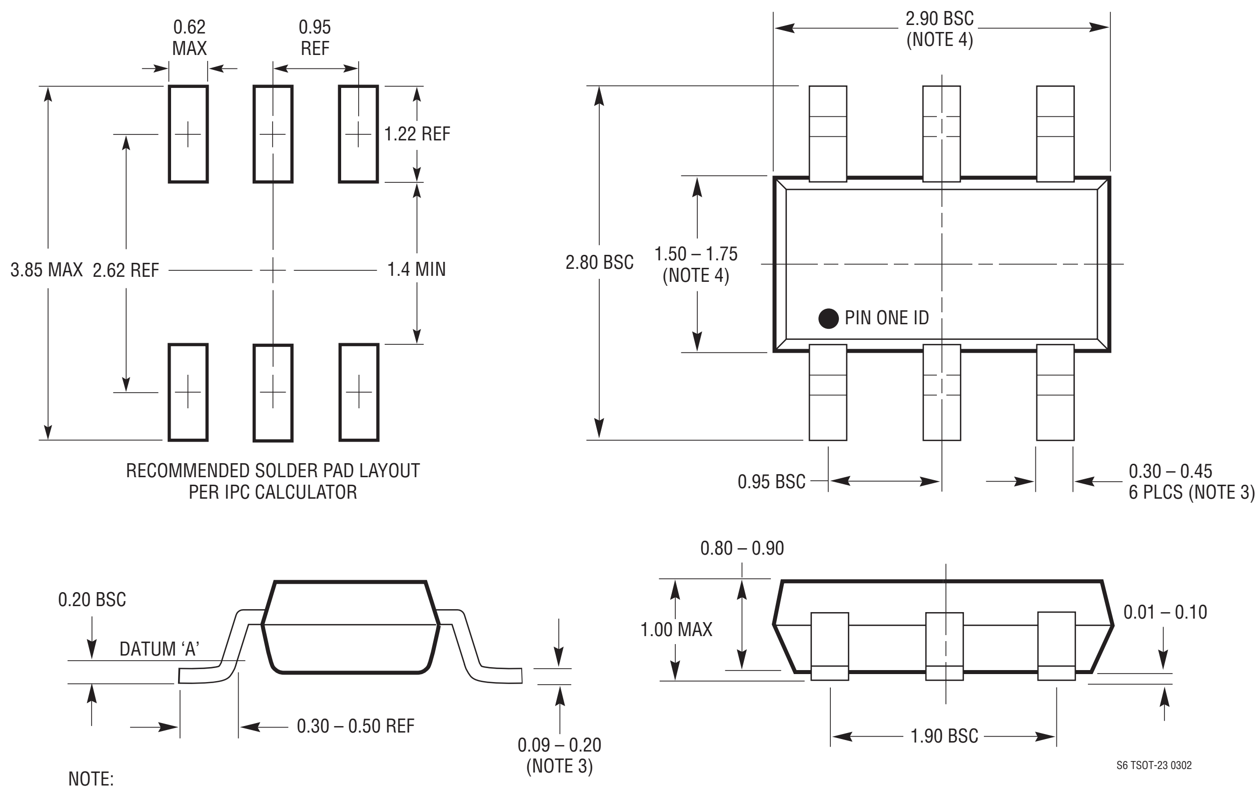
MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev K)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



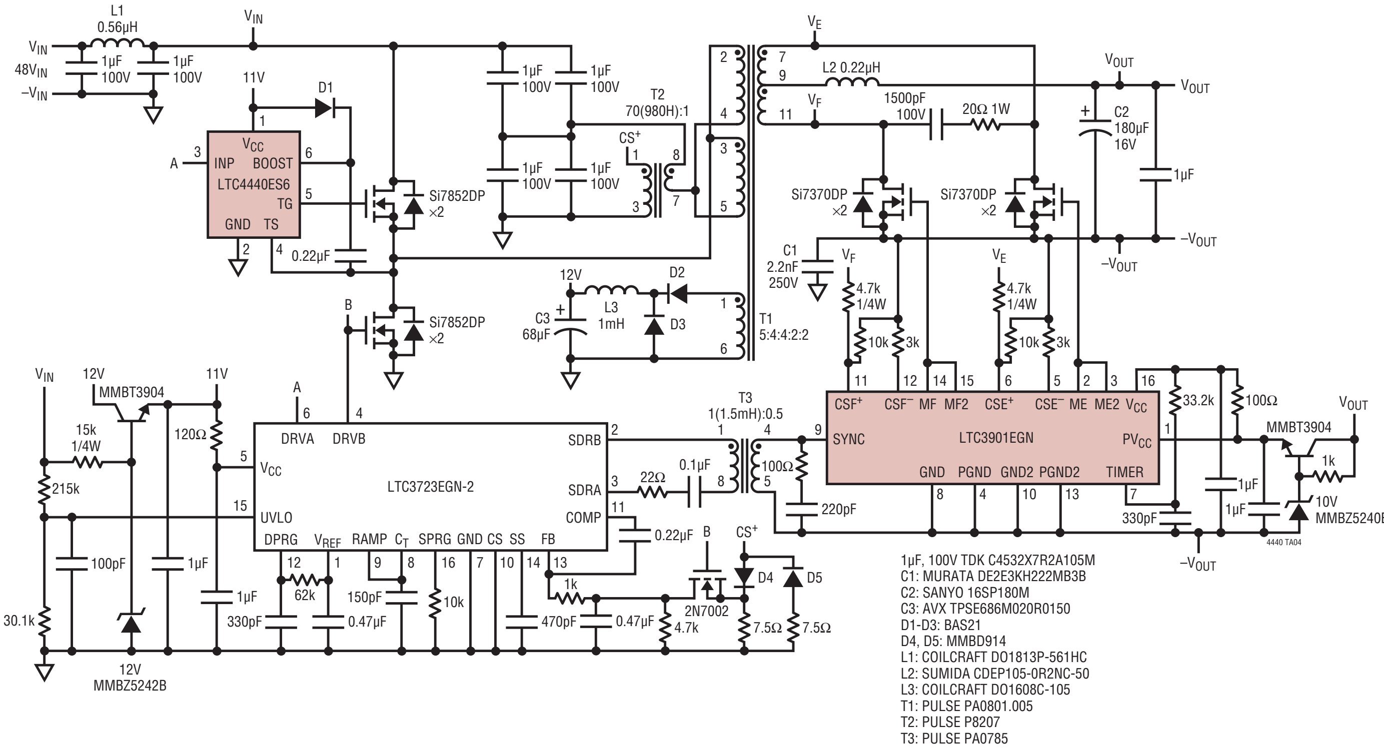
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	1013	Added comparison table	1
B	0215	Released I-Grade Version	2, 3

TYPICAL APPLICATION

LTC3723-2/LTC4440/LTC3901 240W 42V-56V_{IN} to Unregulated 12V Half-Bridge Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4441	6A N-Channel MOSFET Gate Driver	Up to 25V Supply Voltage, Adjustable Gate Drive Voltage from 5V to 8V
LT1910	Protected High Side MOSFET Driver	Up to 48V/60V Surge Supply Voltage, Adjustable Current Limit
LTC4442	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, 6V ≤ V_{CC} ≤ 9.5V
LTC4449	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, 4.5V ≤ V_{CC} ≤ 6.5V
LTC4444/ LTC4444-5	High Voltage Synchronous N-Channel MOSFET Driver with Shoot-Through Protection	Up to 100V Supply Voltage, 4.5V/7.2V ≤ V_{CC} ≤ 13.5V, 3A Peak Pull-Up/0.55Ω Peak Pull-Down
LTC4446	High Voltage Synchronous N-Channel MOSFET Driver without Shoot-Through Protection	Up to 100V Supply Voltage, 7.2V ≤ V_{CC} ≤ 13.5V, 3A Peak Pull-Up/0.55Ω Peak Pull-Down
LTC1154	High Side Micropower MOSFET Driver	Up to 18V Supply Voltage, 85µA Quiescent Current, Internal Charge Pump
LTC1155	Dual High Side Micropower MOSFET Driver	Up to 18V Supply Voltage, 85µA Quiescent Current, Internal Charge Pump
LTC3900	Synchronous Rectifier Driver for Forward Converters	Pulse Transformer Synchronous Input
LTC3901	Synchronous Rectifier Driver for Push-Pull and Full-Bridge Converters	Pulse Transformer Synchronous Input
LTC3722-1/ LTC3722-2	Synchronous Phase Modulated Full-Bridge Controllers	Adjustable Synchronous Rectification Timing for Highest Efficiency
LTC3723-1/ LTC3723-2	Synchronous Push-Pull and Full-Bridge Controllers	High Efficiency with On-Chip MOSFET Drivers

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC4440
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