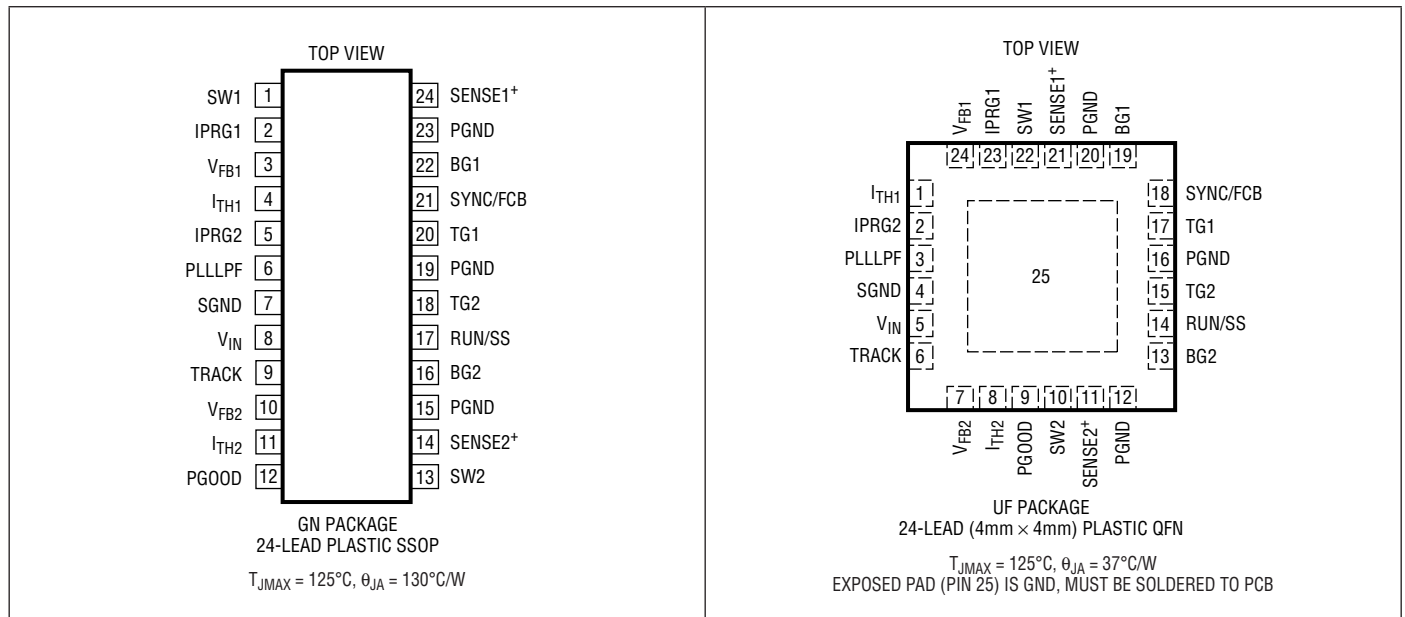


ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN})	-0.3V to 10V	PGOOD	-0.3V to 10V
PLLLPF, RUN/SS, SYNC/FCB, TRACK, SENSE1 ⁺ , SENSE2 ⁺ , IPRG1, IPRG2 Voltages	-0.3V to ($V_{IN} + 0.3V$)	TG1, TG2, BG1, BG2 Peak Output Current (<10 μ s)	1A
V_{FB1} , V_{FB2} , I_{TH1} , I_{TH2} Voltages	-0.3V to 2.4V	Operating Temperature Range (Note 2)	-40°C to 85°C
SW1, SW2 Voltages	-2V to $V_{IN} + 1V$ or 10V Max	Storage Temperature Range	-65°C to 125°C
		Junction Temperature (Note 3)	125°C
		Lead Temperature (Soldering, 10 sec) (LTC3736EGN-2)	300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3736-2EGN#PBF	LTC3736-2EGN#TRPBF		24-Lead Plastic SSOP	-40°C to 85°C
LTC3736-2EUF#PBF	LTC3736-2EUF#TRPBF	37362	24-Lead (4mm x 4mm) Plastic QFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 4.2\text{V}$ unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops						
Input DC Supply Current	(Note 4)					
Normal Mode	$\text{RUN/SS} = V_{IN}$			4.75	750	μA
Shutdown	$\text{RUN/SS} = 0\text{V}$			9	20	μA
UVLO	$V_{IN} = \text{UVLO Threshold} - 200\text{mV}$			3	10	μA
Undervoltage Lockout Threshold	V_{IN} Falling	●	1.95	2.25	2.55	V
	V_{IN} Rising	●	2.15	2.45	2.75	V
Shutdown Threshold at RUN/SS			0.45	0.65	0.85	V
Start-Up Current Source	$\text{RUN/SS} = 0\text{V}$		0.4	0.7	1	μA
Regulated Feedback Voltage	0°C to 85°C (Note 5)		0.594	0.6	0.606	V
	-40°C to 85°C	●	0.591	0.6	0.609	V
Output Voltage Line Regulation	$2.75\text{V} < V_{IN} < 9.8\text{V}$ (Note 5)			0.05	0.2	mV/V
Output Voltage Load Regulation	$I_{TH} = 0.9\text{V}$ (Note 5)			0.12	0.5	%
	$I_{TH} = 1.7\text{V}$			-0.12	-0.5	%
$V_{FB1,2}$ Input Current	(Note 5)			10	50	nA
TRACK Input Current	TRACK = 0.6V			10	50	nA
Overvoltage Protect Threshold	Measured at V_{FB}		0.66	0.68	0.7	V
Overvoltage Protect Hysteresis				20		mV
Auxiliary Feedback Threshold	SYNC/FCB Ramping Positive		0.525	0.6	0.675	V
Top Gate (TG) Drive 1, 2 Rise Time	$C_L = 3000\text{pF}$			40		ns
Top Gate (TG) Drive 1, 2 Fall Time	$C_L = 3000\text{pF}$			40		ns
Bottom Gate (BG) Drive 1, 2 Rise Time	$C_L = 3000\text{pF}$			50		ns
Bottom Gate (BG) Drive 1, 2 Fall Time	$C_L = 3000\text{pF}$			40		ns
Maximum Current Sense Voltage ($\Delta V_{\text{SENSE}(\text{MAX})}$)	IPRG = Floating	●	220	240	260	mV
(SENSE+ – SW)	IPRG = 0V	●	150	167	185	mV
	IPRG = V_{IN}	●	320	345	370	mV
Soft-Start Time	Time for V_{FB1} to Ramp from 0.05V to 0.55V		0.667	0.833	1	ms
Oscillator and Phase-Locked Loop						
Oscillator Frequency	Unsynchronized (SYNC/FCB Not Clocked)					
	PLLLPF = Floating		480	550	600	kHz
	PLLLPF = 0V		260	300	340	kHz
	PLLLPF = V_{IN}		650	750	825	kHz
Phase-Locked Loop Lock Range	SYNC/FCB Clocked					
	Minimum Synchronizable Frequency	●		200	250	kHz
	Maximum Synchronizable Frequency	●	850	1150		kHz
Phase Detector Output Current						
Sinking	$f_{\text{OSC}} > f_{\text{SYNC/FCB}}$			-4		μA
Sourcing	$f_{\text{OSC}} < f_{\text{SYNC/FCB}}$			4		μA
PGOOD Output						
PGOOD Voltage Low	I_{PGOOD} Sinking 1mA			125		mV
PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage					
	$V_{FB} < 0.6\text{V}$, Ramping Positive		-13	-10	-7	%
	$V_{FB} < 0.6\text{V}$, Ramping Negative		-16	-13.3	-10	%
	$V_{FB} < 0.6\text{V}$, Ramping Negative		7	10	13	%
	$V_{FB} < 0.6\text{V}$, Ramping Positive		10	13.3	16	%

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3736E-2 is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the -40°C to 85°C operating range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \cdot \theta_{JA}^{\circ\text{C/W}})$$

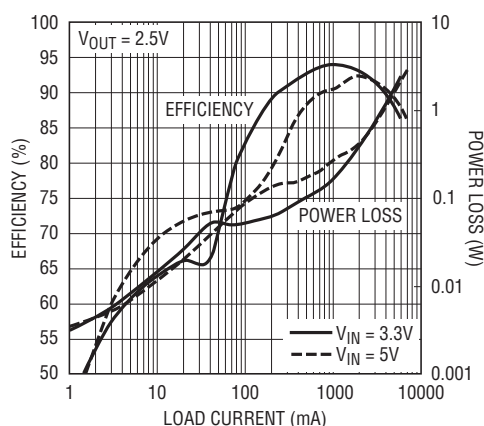
Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

Note 5: The LTC3736-2 is tested in a feedback loop that serves I_{TH} to a specified voltage and measures the resultant V_{FB} voltage.

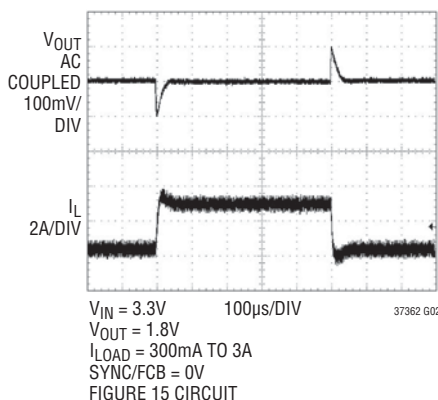
Note 6: Peak current sense voltage is reduced dependent on duty cycle to a percentage of value as shown in Figure 1.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

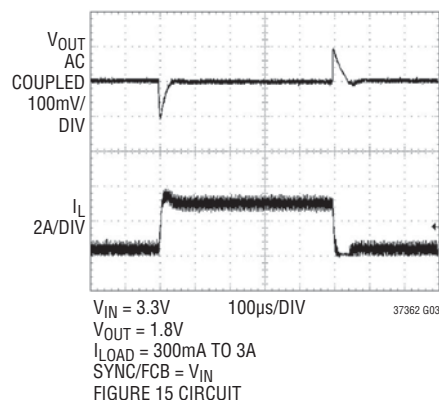
Efficiency and Power Loss vs Load Current



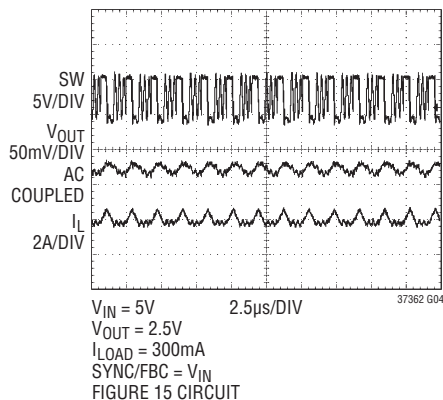
Load Step (Forced Continuous Mode)



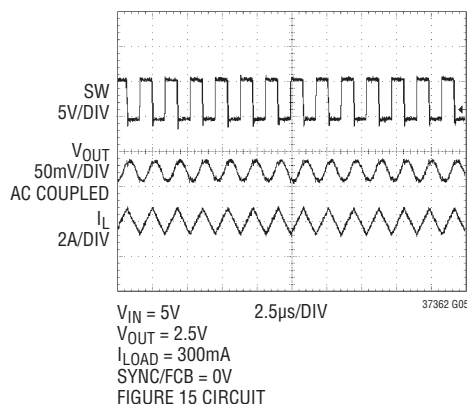
Load Step (Pulse-Skipping Mode)



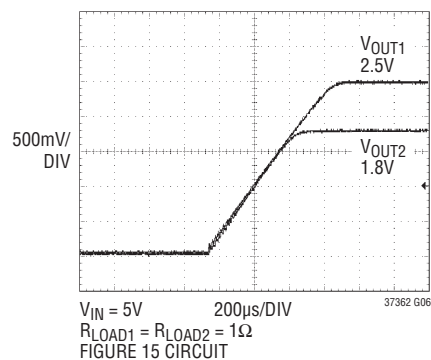
Light Load (Pulse-Skipping Mode)



Light Load (Forced Continuous Mode)

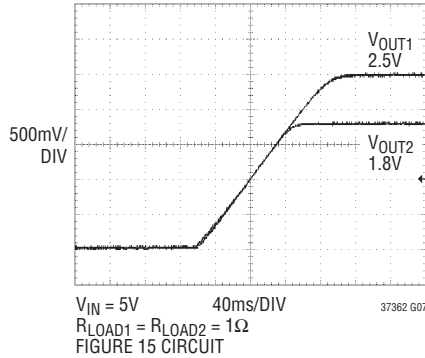


Tracking Start-Up with Internal Soft-Start ($C_{SS} = 0\mu\text{F}$)

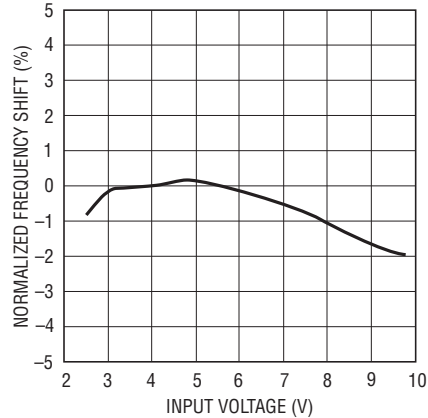


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted.

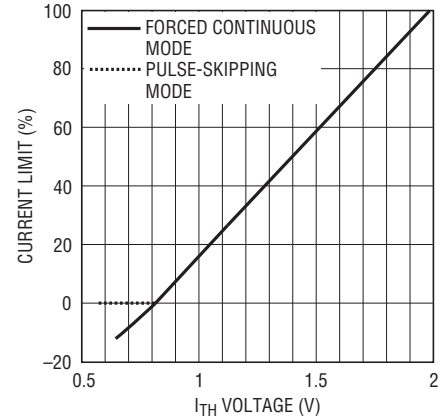
Tracking Start-Up with External Soft-Start ($C_{SS} = 0.10\mu\text{F}$)



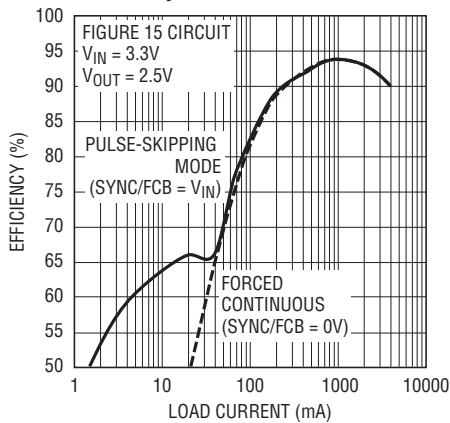
Oscillator Frequency vs Input Voltage



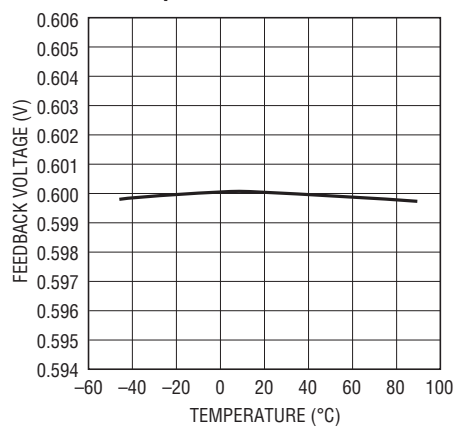
Maximum Current Sense Voltage vs I_{TH} Pin Voltage



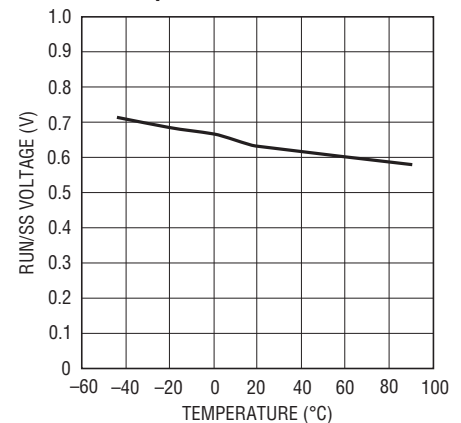
Efficiency vs Load Current



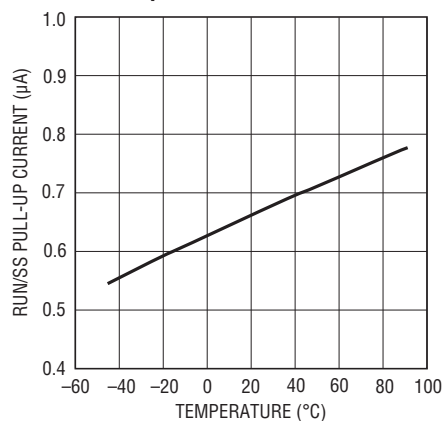
Regulated Feedback Voltage vs Temperature



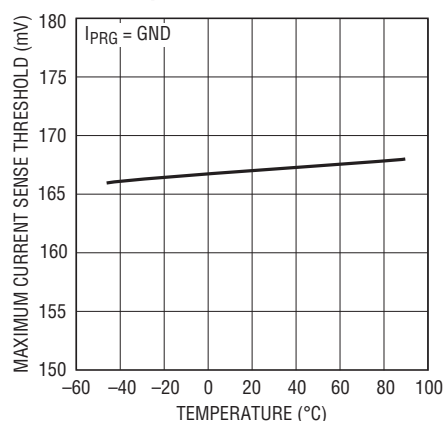
Shutdown (RUN) Threshold vs Temperature



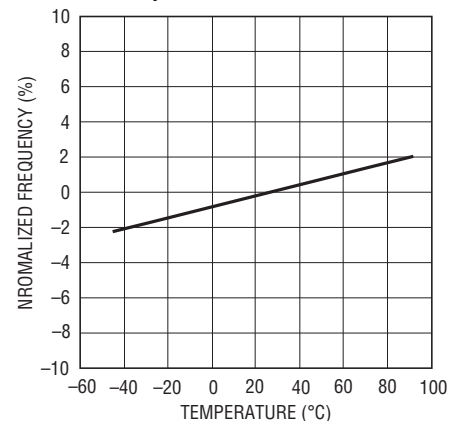
RUN/SS Pull-Up Current vs Temperature



Maximum Current Sense Threshold vs Temperature

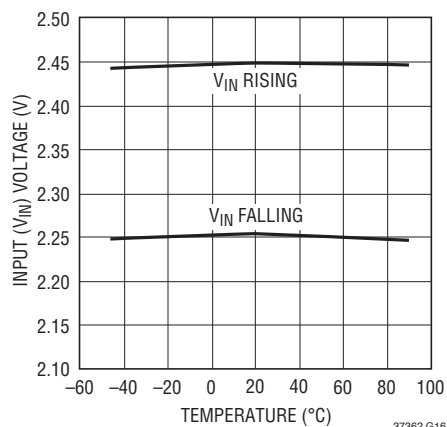


Oscillator Frequency vs Temperature



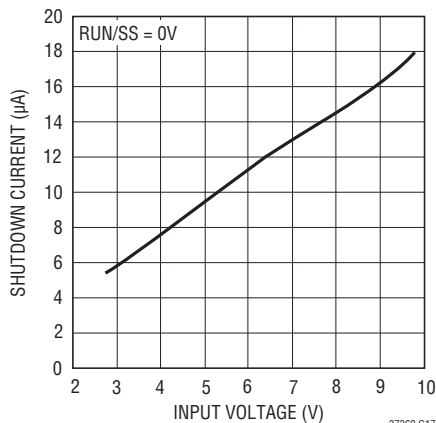
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Undervoltage Lockout Threshold
vs Temperature



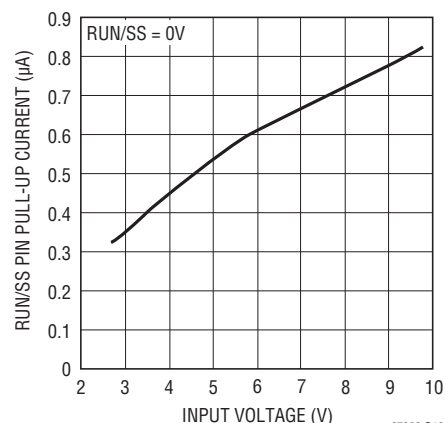
37362 G16

Shutdown Quiescent Current
vs Input Voltage



37362 G17

RUN/SS Start-Up Current
vs Input Voltage



37362 G18

PIN FUNCTIONS (QFN/SSOP Package)

I_{TH1}/I_{TH2} (Pins 1, 8/Pins 4, 11): Current Threshold and Error Amplifier Compensation Point. Nominal operating range on these pins is from 0.7V to 2V. The voltage on these pins determines the threshold of the main current comparator.

PLLLPF (Pin 3/Pin 6): Frequency Set/PLL Lowpass Filter. When synchronizing to an external clock, this pin serves as the lowpass filter point for the phase-locked loop. Normally a series RC is connected between this pin and ground.

When not synchronizing to an external clock, this pin serves as the frequency select input. Tying this pin to GND selects 300kHz operation; tying this pin to V_{IN} selects 750kHz operation. Floating this pin selects 550kHz operation.

SGND (Pin 4/Pin 7): Small-Signal Ground. This pin serves as the ground connection for most internal circuits.

V_{IN} (Pin 5/Pin 8): Chip Signal Power Supply. This pin powers the entire chip except for the gate drivers. Externally filtering this pin with a lowpass RC network (e.g., R = 10Ω, C = 1µF) is suggested to minimize noise pickup, especially in high load current applications.

TRACK (Pin 6/Pin 9): Tracking Input for Second Controller. Allows the start-up of V_{OUT2} to track that of V_{OUT1} according to a ratio established by a resistor divider on V_{OUT1} connected to the TRACK pin. For one-to-one tracking of V_{OUT1} and V_{OUT2} during start-up, a resistor divider with

values equal to those connected to V_{FB2} from V_{OUT2} should be used to connect to TRACK from V_{OUT1}.

PGOOD (Pin 9/Pin 12): Power Good Output Voltage Monitor Open-Drain Logic Output. This pin is pulled to ground when the voltage on either feedback pin (V_{FB1}, V_{FB2}) is not within ±13.3% of its nominal set point.

PGND (Pins 12, 16, 20, 25/Pins 15, 19, 23): Power Ground. These pins serve as the ground connection for the gate drivers and the negative input to the reverse current comparators. The Exposed Pad must be soldered to PCB ground.

RUN/SS (Pin 14/Pin 17): Run Control Input and Optional External Soft-Start Input. Forcing this pin below 0.65V shuts down the chip (both channels). Driving this pin to V_{IN} or releasing this pin enables the chip, using the chip's internal soft-start. An external soft-start can be programmed by connecting a capacitor between this pin and ground.

TG1/TG2 (Pins 17, 15/Pins 18, 20): Top (PMOS) Gate Drive Output. These pins drive the gates of the external P-channel MOSFETs. These pins have an output swing from PGND to SENSE⁺.

SYNC/FCB (Pin 18/Pin 21): This pin performs three functions: 1) auxiliary winding feedback input, 2) external clock synchronization input for phase-locked loop, and 3) pulse-skipping operation or forced continuous mode

37362fb

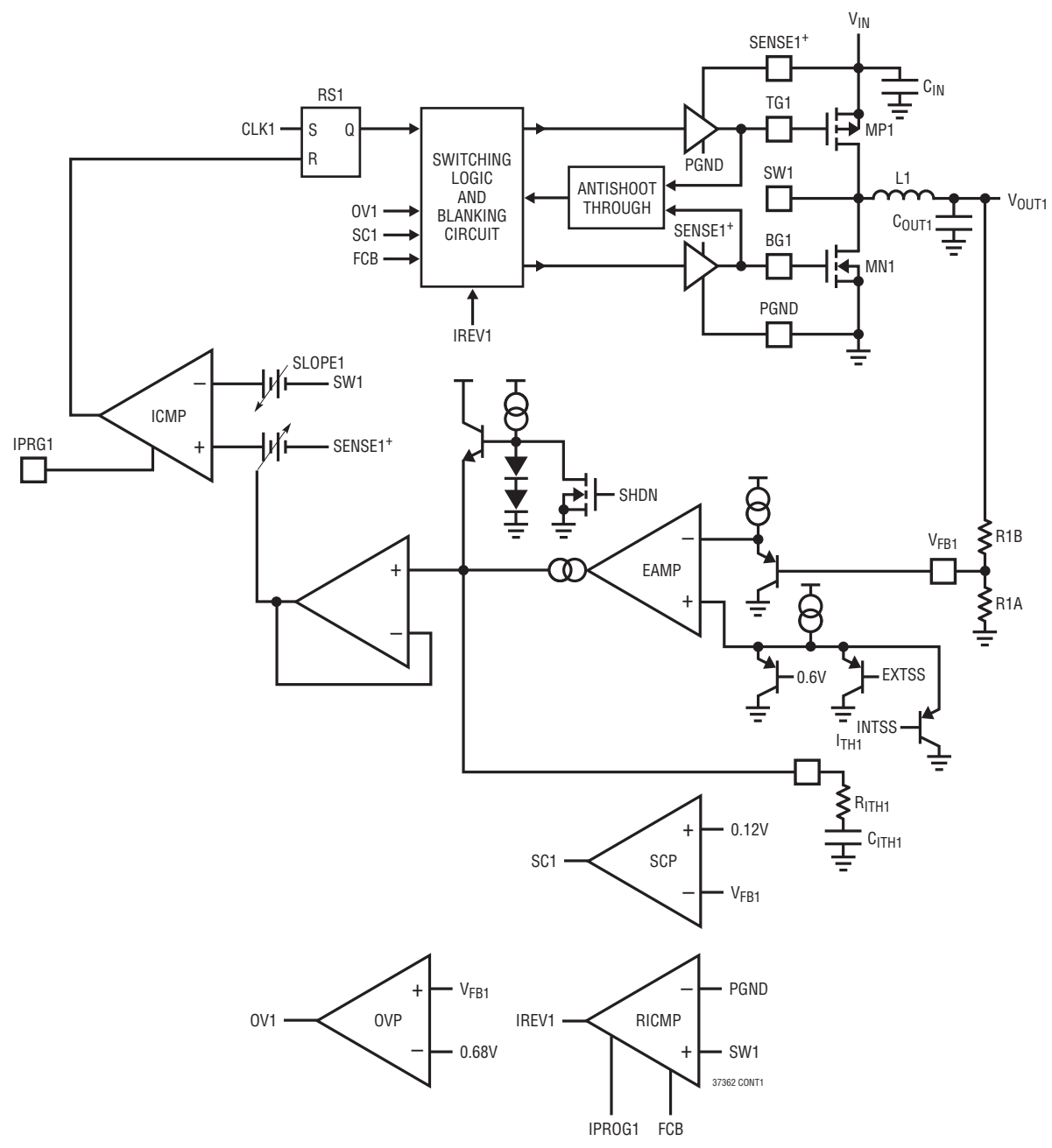
SENSE1+/SENSE2+ (Pins 21, 11/Pins 24, 14): Positive Input to Differential Current Comparator. Also powers the gate drivers. Normally connected to the source of the external P-channel MOSFET.

V_{FB1}/V_{FB2} (Pins 24, 7/Pins 3, 10): Feedback Pins. Receives the remotely sensed feedback voltage for its controller from an external resistor divider across the output.

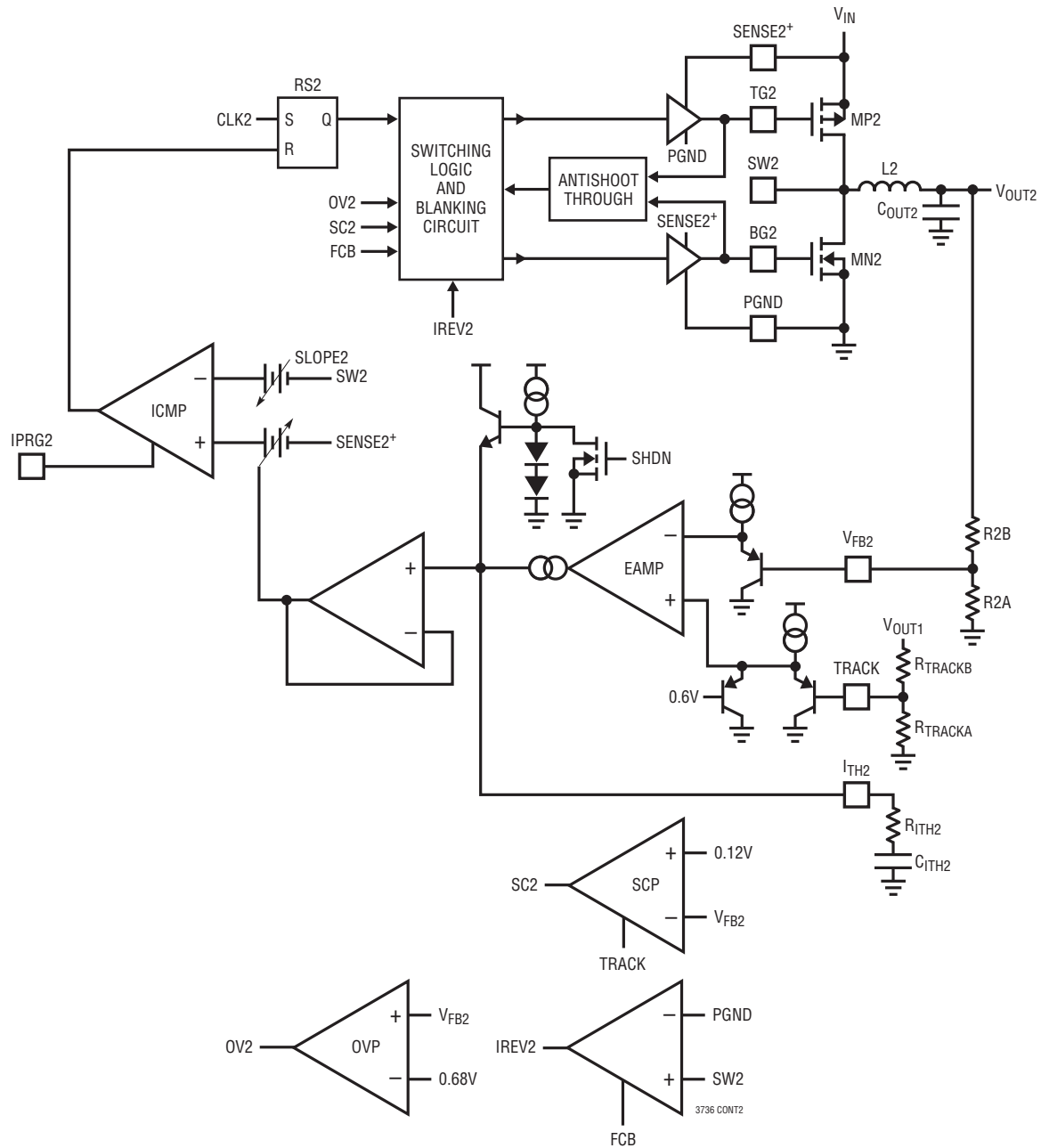
FUNCTIONAL DIAGRAM (Common Circuitry)



FUNCTIONAL DIAGRAM (Controller 1)



FUNCTIONAL DIAGRAM (Controller 2)



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3736-2 uses a constant-frequency, current mode architecture with the two controllers operating 180 degrees out-of-phase. During normal operation, the top external P-channel power MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the current comparator (I_{CMP}) resets the latch. The peak inductor current at which I_{CMP} resets the RS latch is determined by the voltage on the I_{TH} pin, which is driven by the output of the error amplifier (EAMP). The V_{FB} pin receives the output voltage feedback signal from an external resistor divider. This feedback signal is compared to the internal 0.6V reference voltage by the EAMP. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top P-channel MOSFET is off, the bottom N-channel MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator, I_{RCMP} , or the beginning of the next cycle.

Shutdown, Soft-Start and Tracking Start-Up (RUN/SS and TRACK Pins)

The LTC3736-2 is shut down by pulling the RUN/SS pin low. In shutdown, all controller functions are disabled and the chip draws only 9 μ A. The TG outputs are held high (off) and the BG outputs low (off) in shutdown. Releasing RUN/SS allows an internal 0.7 μ A current source to charge up the RUN/SS pin. When the RUN/SS pin reaches 0.65V, the LTC3736-2's two controllers are enabled.

The start-up of V_{OUT1} is controlled by the LTC3736-2's internal soft-start. During soft-start, the error amplifier EAMP compares the feedback signal V_{FB1} to the internal soft-start ramp (instead of the 0.6V reference), which rises linearly from 0V to 0.6V in about 1ms. This allows the output voltage to rise smoothly from 0V to its final value, while maintaining control of the inductor current.

The 1ms soft-start time can be increased by connecting the optional external soft-start capacitor C_{SS} between the RUN/SS and SGND pins. As the RUN/SS pin continues to rise linearly from approximately 0.65V to 1.3V (being charged by the internal 0.7 μ A current source), the EAMP regulates the V_{FB1} proportionally linearly from 0V to 0.6V.

The start-up of V_{OUT2} is controlled by the voltage on the TRACK pin. When the voltage on the TRACK pin is less than the 0.6V internal reference, the LTC3736-2 regulates the V_{FB2} voltage to the TRACK pin instead of the 0.6V reference. Typically, a resistor divider on V_{OUT1} is connected to the TRACK pin to allow the start-up of V_{OUT2} to track that of V_{OUT1} . For one-to-one tracking during start-up, the resistor divider would have the same values as the divider on V_{OUT2} that is connected to V_{FB2} .

Light Load Operation (Pulse-Skipping or Continuous Conduction) (SYNC/FCB Pin)

The LTC3736-2 can be enabled to enter high efficiency pulse-skipping operation or forced continuous conduction mode at low load currents. To select pulse-skipping operation, tie the SYNC/FCB pin to a DC voltage above 0.6V (e.g., V_{IN}). To select forced continuous operation, tie the SYNC/FCB to a DC voltage below 0.6V (e.g., SGND). This 0.6V threshold between pulse-skipping operation and forced continuous mode can be used in secondary winding regulation as described in the Auxiliary Winding Control Using SYNC/FCB Pin discussion in the Applications Information section.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin. The P-channel MOSFET is turned on every cycle (constant frequency) regardless of the I_{TH} pin voltage. In this mode, the efficiency at light loads is lower than in pulse-skipping operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry.

When the SYNC/FCB pin is tied to a DC voltage above 0.6V or when it is clocked by an external clock source to use the phase-locked loop (see Frequency Selection and Phase-Locked Loop), the LTC3736-2 operates in PWM pulse-skipping mode at light loads. In this mode, the current comparator I_{CMP} may remain tripped for several cycles and force the external P-channel MOSFET to stay off for the same number of cycles. The inductor current is not allowed to reverse, though (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference. However, it provides low current efficiency

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OPERATION (Refer to Functional Diagram)

higher than forced continuous mode. During start-up or a short-circuit condition (V_{FB1} or $V_{FB2} \leq 0.54V$), the LTC3736-2 operates in pulse-skipping mode (no current reversal allowed), regardless of the state of the SYNC/FCB pin.

Short-Circuit Protection

When an output is shorted to ground ($V_{FB} < 0.12V$), the switching frequency of that controller is reduced to one fifth of the normal operating frequency. The other controller is unaffected and maintains normal operation.

The short-circuit threshold on V_{FB2} is based on the smaller of 0.12V and a fraction of the voltage on the TRACK pin. This also allows V_{OUT2} to start up and track V_{OUT1} more easily. Note that if V_{OUT1} is truly short-circuited ($V_{OUT1} = V_{FB1} = 0V$), then the LTC3736-2 will try to regulate V_{OUT2} to 0V if a resistor divider on V_{OUT1} is connected to the TRACK pin.

Output Overvoltage Protection

As a further protection, the overvoltage comparator (OV) guards against transient overshoots, as well as other more serious conditions that may overvoltage the output. When the feedback voltage on the V_{FB} pin has risen 13.33% above the reference voltage of 0.6V, the external P-channel MOSFET is turned off and the N-channel MOSFET is turned on until the overvoltage is cleared.

Frequency Selection and Phase-Locked Loop (PLLLPF and SYNC/FCB Pins)

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3736-2's controllers can be selected using the PLLLPF pin.

If the SYNC/FCB is not being driven by an external clock source, the PLLLPF can be floated, tied to V_{IN} or tied to SGND to select 550kHz, 750kHz or 300kHz, respectively.

A phase-locked loop (PLL) is available on the LTC3736-2 to synchronize the internal oscillator to an external clock source that is connected to the SYNC/FCB pin. In this case, a series RC should be connected between the PLLLPF pin and SGND to serve as the PLL's loop filter. The LTC3736-2 phase detector adjusts the voltage on the PLLLPF pin to align the turn-on of controller 1's external P-channel MOSFET to the rising edge of the synchronizing signal. Thus, the turn-on of controller 2's external P-channel MOSFET is 180 degrees out-of-phase with the rising edge of the external clock source.

The typical capture range of the LTC3736-2's phase-locked loop is from approximately 200kHz to 1MHz, and is guaranteed over temperature to be between 250kHz and 850kHz. In other words, the LTC3736-2's PLL is guaranteed to lock to an external clock source whose frequency is between 250kHz and 850kHz.

Dropout Operation

When the input supply voltage (V_{IN}) decreases towards the output voltage, the rate of change of the inductor current while the external P-channel MOSFET is on (ON cycle) decreases. This reduction means that the P-channel MOSFET will remain on for more than one oscillator cycle if the inductor current has not ramped up to the threshold set by the EAMP on the I_{TH} pin. Further reduction in the input supply voltage will eventually cause the P-channel MOSFET to be turned on 100%, i.e., DC. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor.

Undervoltage Lockout

To prevent operation of the external MOSFETs below safe input voltage levels, an undervoltage lockout is incorporated in the LTC3736-2. When the input supply voltage (V_{IN}) drops below 2.3V, the external P- and N-channel MOSFETs and all internal circuitry are turned off except for the undervoltage block, which draws only a few microamperes.

OPERATION (Refer to Functional Diagram)

Peak Current Sense Voltage Selection and Slope Compensation (IPRG1 and IPRG2 Pins)

When a controller is operating below 20% duty cycle, the peak current sense voltage (between the SENSE⁺ and SW pins) allowed across the external P-channel MOSFET is determined by:

$$\Delta V_{\text{SENSE(MAX)}} = \frac{A(V_{\text{ITH}} - 0.7\text{V})}{10}$$

where A is a constant determined by the state of the IPRG pins. Floating the IPRG pin selects A = 1.875; tying IPRG to V_{IN} selects A = 2.7; tying IPRG to SGND selects A = 1.3. The maximum value of V_{ITH} is typically about 1.98V, so the maximum sense voltage allowed across the external P-channel MOSFET is 240mV, 345mV, or 167mV for the three respective states of the IPRG pin. The peak sense voltages for the two controllers can be independently selected by the IPRG1 and IPRG2 pins.

However, once the controller's duty cycle exceeds 20%, slope compensation begins and effectively reduces the peak sense voltage by a scale factor given by the curve in Figure 1.

The peak inductor current is determined by the peak sense voltage and the on-resistance of the external P-channel MOSFET:

$$I_{\text{PK}} = \frac{\Delta V_{\text{SENSE(MAX)}}}{R_{\text{DS(ON)}}$$

Power Good (PGOOD) Pin

A window comparator monitors both feedback voltages and the open-drain PGOOD output pin is pulled low when either or both feedback voltages are not within $\pm 10\%$ of the 0.6V reference voltage. PGOOD is low when the LTC3736-2 is shut down or in undervoltage lockout.

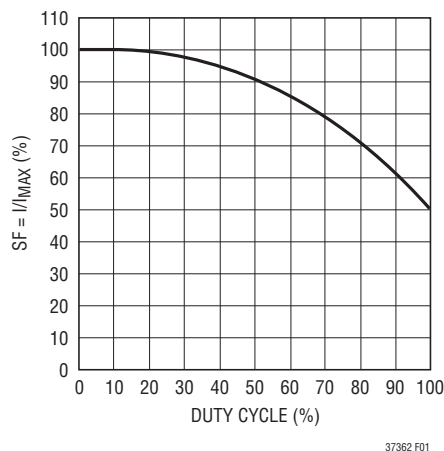


Figure 1. Maximum Peak Current vs Duty Cycle

2-Phase Operation

Why the need for 2-phase operation? Until recently, constant-frequency dual switching regulators operated both controllers in phase (i.e., single-phase operation). This means that both topside MOSFETs (P-channel) are turned on at the same time, causing current pulses of up to twice the amplitude of those from a single regulator to be drawn from the input capacitor. These large amplitude pulses increase the total RMS current flowing in the input capacitor, requiring the use of larger and more expensive input capacitors, and increase both EMI and power losses in the input capacitor and input power supply.

With 2-phase operation, the two controllers of the LTC3736-2 are operated 180 degrees out-of-phase. This effectively interleaves the current pulses coming from the topside MOSFET switches, greatly reducing the time where they overlap and add together. The result is a significant reduction in the total RMS current, which in turn allows the use of smaller, less expensive input capacitors, reduces shielding requirements for EMI and improves real world operating efficiency.

OPERATION (Refer to Functional Diagram)

Figure 2 shows example waveforms for a single-phase dual controller versus a 2-phase LTC3736-2 system. In this case, 2.5V and 1.8V outputs, each drawing a load current of 2A, are derived from a 7V (e.g., a 2-cell Li-Ion battery) input supply. In this example, 2-phase operation would reduce the RMS input capacitor current from $1.79\text{A}_{\text{RMS}}$ to $0.91\text{A}_{\text{RMS}}$. While this is an impressive reduction by itself, remember that power losses are proportional to I_{RMS}^2 , meaning that actual power wasted is reduced by a factor of 3.86.

The reduced input ripple current also means that less power is lost in the input power path, which could include batteries, switches, trace/connector resistances, and

protection circuitry. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage. Significant cost and board footprint savings are also realized by being able to use smaller, less expensive, lower RMS current-rated input capacitors.

Of course, the improvement afforded by 2-phase operation is a function of the relative duty cycles of the two controllers, which in turn are dependent upon the input supply voltage. Figure 3 depicts how the RMS input current varies for single-phase and 2-phase dual controllers with 2.5V and 1.8V outputs over a wide input voltage range.

It can be readily seen that the advantages of 2-phase operation are not limited to a narrow operating range, but in fact extend over a wide region. A good rule of thumb for most applications is that 2-phase operation will reduce the input capacitor requirement to that for just one channel operating at maximum current and 50% duty cycle.

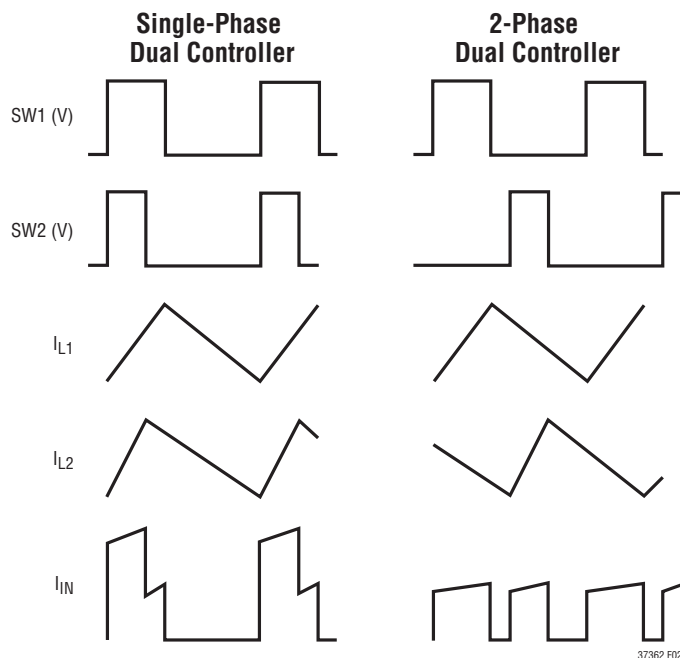


Figure 2. Example Waveforms for a Single-Phase Dual Controller vs the 2-Phase LTC3736-2

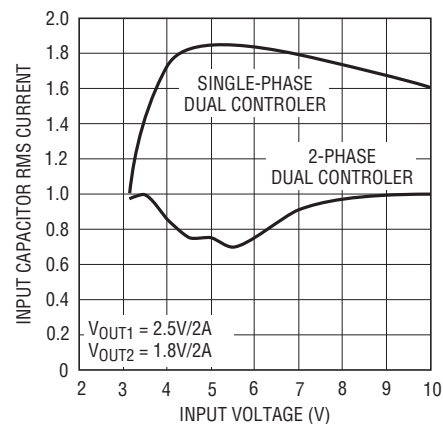


Figure 3. RMS Input Current Comparison

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The typical LTC3736-2 application circuit is shown in Figure 13. External component selection for each of the LTC3736-2's controllers is driven by the load requirement and begins with the selection of the inductor (L) and the power MOSFETs (MP and MN).

Power MOSFET Selection

Each of the LTC3736-2's two controllers requires two external power MOSFETs: a P-channel MOSFET for the topside (main) switch and an N-channel MOSFET for the bottom (synchronous) switch. Important parameters for the power MOSFETs are the breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} , turn-off delay $t_{D(OFF)}$ and the total gate charge Q_G .

The gate drive voltage is the input supply voltage. Since the LTC3736-2 is designed for operation down to low input voltages, a sublogic level MOSFET ($R_{DS(ON)}$ guaranteed at $V_{GS} = 2.5V$) is required for applications that work close to this voltage. When these MOSFETs are used, make sure that the input supply to the LTC3736-2 is less than the absolute maximum MOSFET V_{GS} rating, which is typically 8V.

The P-channel MOSFET's on-resistance is chosen based on the required load current. The maximum average output load current $I_{OUT(MAX)}$ is equal to the peak inductor current minus half the peak-to-peak ripple current I_{RIPPLE} . The LTC3736-2's current comparator monitors the drain-to-source voltage V_{DS} of the P-channel MOSFET, which is sensed between the SENSE⁺ and SW pins. The peak inductor current is limited by the current threshold, set by the voltage on the I_{TH} pin of the current comparator. The voltage on the I_{TH} pin is internally clamped, which limits the maximum current sense threshold $\Delta V_{SENSE(MAX)}$ to approximately 240mV when IPRG is floating (167mV when IPRG is tied low; 345mV when IPRG is tied high).

The output current that the LTC3736-2 can provide is given by:

$$I_{OUT(MAX)} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}} - \frac{I_{RIPPLE}}{2}$$

A reasonable starting point is setting ripple current I_{RIPPLE} to be 40% of $I_{OUT(MAX)}$. Rearranging the above equation yields:

$$R_{DS(ON)(MAX)} = \frac{5}{6} \cdot \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

or Duty Cycle < 20%.

However, for operation above 20% duty cycle, slope compensation has to be taken into consideration to select the appropriate value of $R_{DS(ON)}$ to provide the required amount of load current:

$$R_{DS(ON)(MAX)} = \frac{5}{6} \cdot SF \cdot \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

where SF is a scale factor whose value is obtained from the curve in Figure 1.

These must be further derated to take into account the significant variation in on-resistance with temperature. The following equation is a good guide for determining the required $R_{DS(ON)MAX}$ at 25°C (manufacturer's specification), allowing some margin for variations in the LTC3736-2 and external component values:

$$R_{DS(ON)(MAX)} = \frac{5}{6} \cdot 0.9 \cdot SF \cdot \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)} \cdot \rho_T}$$

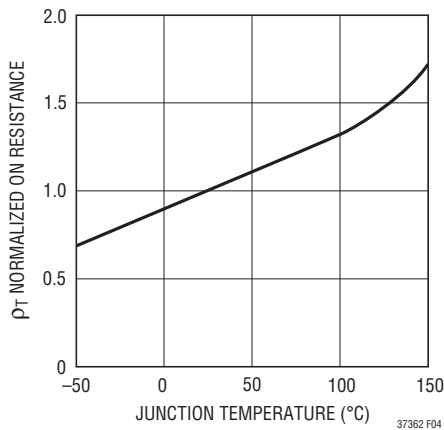
The ρ_T is a normalizing term accounting for the temperature variation in on-resistance, which is typically about 0.4%/°C, as shown in Figure 4. Junction-to-case temperature T_{JC} is about 10°C in most applications. For a maximum ambient temperature of 70°C, using $\rho_{80^\circ C} \sim 1.3$ in the above equation is a reasonable choice.

The power dissipated in the top and bottom MOSFETs strongly depends on their respective duty cycles and load current. When the LTC3736-2 is operating in continuous mode, the duty cycles for the MOSFETs are:

$$\text{Top P-Channel Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Bottom N-Channel Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

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Figure 4. $R_{DS(ON)}$ vs Temperature

The MOSFET power dissipations at maximum output current are:

$$P_{TOP} = \frac{V_{OUT}}{V_{IN}} \cdot I_{OUT(MAX)}^2 \cdot \rho_T \cdot R_{DS(ON)} + 2 \cdot V_{IN}^2 \cdot I_{OUT(MAX)} \cdot C_{RSS} \cdot f_{OSC}$$

$$P_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \cdot I_{OUT(MAX)}^2 \cdot \rho_T \cdot R_{DS(ON)}$$

Both MOSFETs have I^2R losses and the P_{TOP} equation includes an additional term for transition losses, which are largest at high input voltages. The bottom MOSFET losses are greatest at high input voltage or during a short-circuit when the bottom duty cycle is nearly 100%.

The LTC3736-2 utilizes a nonoverlapping, antishoot-through gate drive control scheme to ensure that the P- and N-channel MOSFETs are not turned on at the same time. To function properly, the control scheme requires that the MOSFETs used are intended for DC/DC switching applications. Many power MOSFETs, particularly P-channel MOSFETs, are intended to be used as static switches and therefore are slow to turn on or off.

Reasonable starting criteria for selecting the P-channel MOSFET are that it must typically have a gate charge (Q_G)

less than 25nC to 30nC (at 4.5V_{GS}) and a turn-off delay ($t_{D(OFF)}$) of less than approximately 140ns. However, due to differences in test and specification methods of various MOSFET manufacturers, and in the variations in Q_G and $t_{D(OFF)}$ with gate drive (V_{IN}) voltage, the P-channel MOSFET ultimately should be evaluated in the actual LTC3736-2 application circuit to ensure proper operation.

Shoot-through between the P-channel and N-channel MOSFETs can most easily be spotted by monitoring the input supply current. As the input supply voltage increases, if the input supply current increases dramatically, then the likely cause is shoot-through. Note that some MOSFETs that do not work well at high input voltages (e.g., $V_{IN} > 5V$) may work fine at lower voltages (e.g., 3.3V). Table 1 shows a selection of P-channel MOSFETs from different manufacturers that are known to work well in LTC3736-2 applications.

Selecting the N-channel MOSFET is typically easier, since for a given $R_{DS(ON)}$, the gate charge and turn-on and turn-off delays are much smaller than for a P-channel MOSFET.

Table 1. Selected P-Channel MOSFETs Suitable for LTC3736-2 Applications

PART NUMBER	MANUFACTURER	TYPE	PACKAGE
Si7540DP	Siliconix	Complementary P/N	PowerPak SO-8
Si9801DY	Siliconix	Complementary P/N	SO-8
FDW2520C	Fairchild	Complementary P/N	TSSOP-8
FDW2521C	Fairchild	Complementary P/N	TSSOP-8
Si3447BDV	Siliconix	Single P	TSOP-6
Si9433BDY	Siliconix	Single P	SO-8
FDC602P	Fairchild	Single P	TSOP-6
FDC606P	Fairchild	Single P	TSOP-6
FDC638P	Fairchild	Single P	TSOP-6
FDW2502P	Fairchild	Dual P	TSSOP-8
FDS6875	Fairchild	Dual P	SO-8
HAT1054R	Hitachi	Dual P	SO-8
NTMD6P02R2-D	On Semiconductor	Dual P	SO-8

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Operating Frequency and Synchronization

The choice of operating frequency, f_{OSC} , is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, both gate charge loss and transition loss. However, lower frequency operation requires more inductance for a given amount of ripple current.

The internal oscillator for each of the LTC3736-2's controllers runs at a nominal 550kHz frequency when the PLLLPF pin is left floating and the SYNC/FCB pin is a DC low or high. Pulling the PLLLPF to V_{IN} selects 750kHz operation; pulling the PLLLPF to GND selects 300kHz operation.

Alternatively, the LTC3736-2 will phase-lock to a clock signal applied to the SYNC/FCB pin with a frequency between 250kHz and 850kHz (see Phase-Locked Loop and Frequency Synchronization).

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency f_{OSC} directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN} - V_{OUT}}{f_{OSC} \cdot L} \right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \cdot I_{RIPPLE}} \cdot \frac{V_{OUT}}{V_{IN}}$$

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Schottky Diode Selection (Optional)

The Schottky diodes D1 and D2 in Figure 16 conduct current during the dead time between the conduction of the power MOSFETs. This prevents the body diode of the bottom N-channel MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency. A 1A Schottky diode is generally a good size for most LTC3736-2 applications, since it conducts a relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance. This diode may be omitted if the efficiency loss can be tolerated.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula below to determine the maximum RMS capacitor

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current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single-phase power supply solution.

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx \frac{I_{MAX}}{V_{IN}} \left[(V_{OUT})(V_{IN} - V_{OUT}) \right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3736-2, ceramic capacitors can also be used for C_{IN} . Always consult the manufacturer if there is any question.

The benefit of the LTC3736-2 2-phase operation can be calculated by using the equation above for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a

2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The sources of the P-channel MOSFETs should be placed within 1cm of each other and share a common $C_{IN}(s)$. Separating the sources and C_{IN} may produce undesirable voltage and current resonances at V_{IN} .

A small (0.1 μ F to 1 μ F) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3736-2, is also suggested. A 10 Ω resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation between the two channels.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE} \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage.

Setting Output Voltage

The LTC3736-2 output voltages are each set by an external feedback resistor divider carefully placed across the output, as shown in Figure 5. The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \cdot \left(1 + \frac{R_B}{R_A} \right)$$

To improve the frequency response, a feedforward capacitor, C_{FF} , may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

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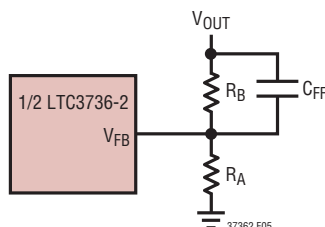


Figure 5. Setting Output Voltage

Run/Soft-Start Function

The RUN/SS pin is a dual purpose pin that provides the optional external soft-start function and a means to shut down the LTC3736-2.

Pulling the RUN/SS pin below 0.65V puts the LTC3736-2 into a low quiescent current shutdown mode ($I_Q = 9\mu A$). If RUN/SS has been pulled all the way to ground, there will be a delay before the LTC3736-2 comes out of shutdown and is given by:

$$t_{\text{DELAY}} = 0.65V \cdot \frac{C_{\text{SS}}}{0.7\mu A} = 0.93s/\mu F \cdot C_{\text{SS}}$$

This pin can be driven directly from logic as shown in Figure 6. Diode D1 in Figure 6 reduces the start delay but allows C_{SS} to ramp up slowly providing the soft-start function. This diode (and capacitor) can be deleted if the external soft-start is not needed.

During soft-start, the start-up of V_{OUT1} is controlled by slowly ramping the positive reference to the error amplifier from 0V to 0.6V, allowing V_{OUT1} to rise smoothly from 0V to its final value. The default internal soft-start time is 1ms.

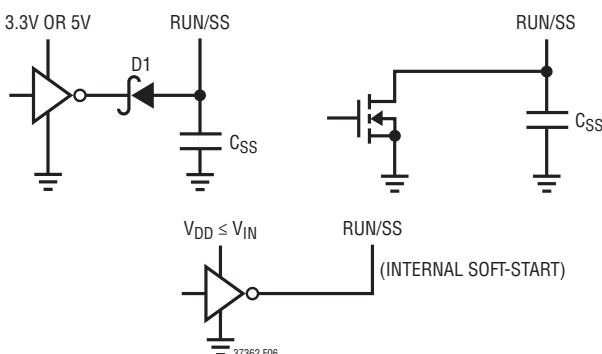


Figure 6. RUN/SS Pin Interfacing

This can be increased by placing a capacitor between the RUN/SS pin and SGND. In this case, the soft-start time will be approximately:

$$t_{\text{SS1}} = C_{\text{SS}} \cdot \frac{600mV}{0.7\mu A}$$

Tracking

The start-up of V_{OUT2} is controlled by the voltage on the TRACK pin. Normally this pin is used to allow the start-up of V_{OUT2} to track that of V_{OUT1} as shown qualitatively in Figures 7a and 7b. When the voltage on the TRACK pin is less than the internal 0.6V reference, the LTC3736-2 regulates the V_{FB2} voltage to the TRACK pin voltage instead of 0.6V. The start-up of V_{OUT2} may ratiometrically track that of V_{OUT1} , according to a ratio set by a resistor divider (Figure 7c):

$$\frac{V_{\text{OUT1}}}{V_{\text{OUT2}}} = \frac{R_{2A}}{R_{\text{TRACKA}}} \cdot \frac{R_{\text{TRACKA}} + R_{\text{TRACKB}}}{R_{2B} + R_{2A}}$$

For coincident tracking ($V_{\text{OUT1}} = V_{\text{OUT2}}$ during start-up),

$$R_{2A} = R_{\text{TRACKA}}$$

$$R_{2B} = R_{\text{TRACKB}}$$

The ramp time for V_{OUT2} to rise from 0V to its final value is:

$$t_{\text{SS2}} = t_{\text{SS1}} \cdot \frac{R_{\text{TRACKA}}}{R_{1A}} \cdot \frac{R_{1A} + R_{1B}}{R_{\text{TRACKA}} + R_{\text{TRACKB}}}$$

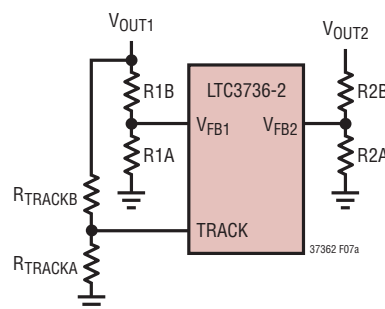
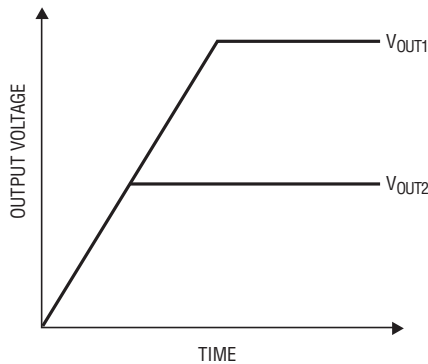
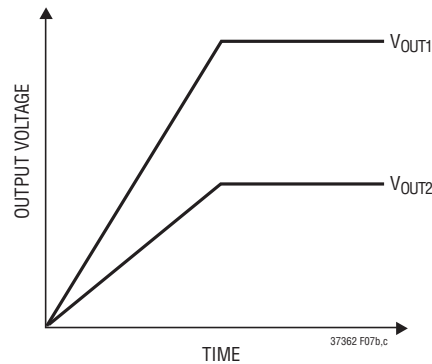


Figure 7a. Using the TRACK Pin

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(7b) Coincident Tracking



(7c) Ratiometric Tracking

Figures 7b and 7c. Two Different Modes of Output Voltage Tracking

For coincident tracking,

$$t_{SS2} = t_{SS1} \cdot \frac{V_{OUT2F}}{V_{OUT1F}}$$

where V_{OUT1F} and V_{OUT2F} are the final, regulated values of V_{OUT1} and V_{OUT2} . V_{OUT1} should always be greater than V_{OUT2} when using the TRACK pin. If no tracking function is desired, then the TRACK pin may be tied to V_{IN} . However, in this situation there would be no (internal nor external) soft-start on V_{OUT2} .

Phase-Locked Loop and Frequency Synchronization

The LTC3736-2 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the external P-channel MOSFET of controller 1 to be locked to the rising edge of an external clock signal applied to the SYNC/FCB pin. The turn-on of controller 2's external P-channel MOSFET is thus 180 degrees out-of-phase with the external clock. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the PLLPF pin. The relationship between the voltage on the PLLPF pin and operating

frequency, when there is a clock signal applied to SYNC/FCB, is shown in Figure 8 and specified in the Electrical Characteristics table. Note that the LTC3736-2 can only be synchronized to an external clock whose frequency is within range of the LTC3736-2's internal VCO, which is nominally 200kHz to 1MHz. This is guaranteed, over temperature and variations, to be between 300kHz and 750kHz. A simplified block diagram is shown in Figure 9.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC} , then current is sourced continuously from the phase detector output, pulling up the PLLPF pin. When the external clock frequency is less

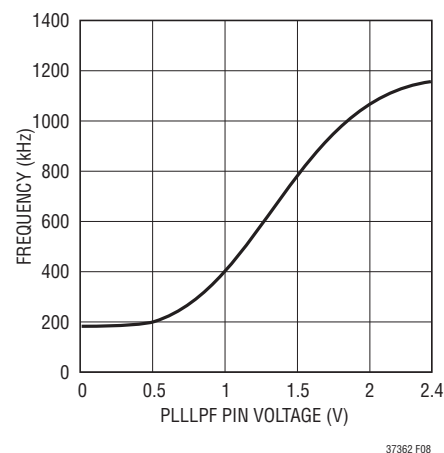


Figure 8. Relationship Between Oscillator Frequency and Voltage at the PLLPF Pin When Synchronizing to an External Clock

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continuous applications with low ripple current at light loads. If forced continuous mode is selected and the duty cycle falls below the minimum on-time requirement, the output will be regulated by overvoltage protection.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting efficiency and which change would produce the most improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + \dots)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, five main sources usually account for most of the losses in LTC3736-2 circuits: 1) LTC3736-2 DC bias current, 2) MOSFET gate charge current, 3) I^2R losses, and 4) transition losses.

1. The V_{IN} (pin) current is the DC supply current, given in the electrical characteristics, excluding MOSFET driver currents. V_{IN} current results in a small loss that increases with V_{IN} .
2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from SENSE+ to ground. The resulting dQ/dt is a current out of SENSE+, which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f \cdot Q_P$.
3. I^2R losses are calculated from the DC resistances of the MOSFETs and inductor. In continuous mode, the average output current flows through L but is "chopped" between the top P-channel MOSFET and the bottom N-channel MOSFET. The MOSFET $R_{DS(ON)}$ s multiplied by duty cycle can be summed with the resistance of L to obtain I^2R losses.

4. Transition losses apply to the top external P-channel MOSFET and increase with higher operating frequencies and input voltages. Transition losses can be estimated from:

$$\text{Transition Loss} = 2 (V_{IN})^2 I_{O(MAX)} C_{RSS}(f)$$

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, where ESR is the effective series resistance of C_{OUT} . ΔI_{LOAD} also begins to charge or discharge C_{OUT} , which generates a feedback error signal. The regulator loop then returns V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

The I_{TH} series R_C - C_C filter (see Functional Diagram) sets the dominant pole-zero loop compensation. The I_{TH} external components shown in the Typical Application on the front page of this data sheet will provide an adequate starting point for most applications. The values can be modified slightly (from 0.2 to 5 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of $1\mu s$ to $10\mu s$ will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability. The gain of the loop will be increased by increasing R_C , and the bandwidth of the loop will be increased by decreasing C_C . The output voltage settling behavior is

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related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

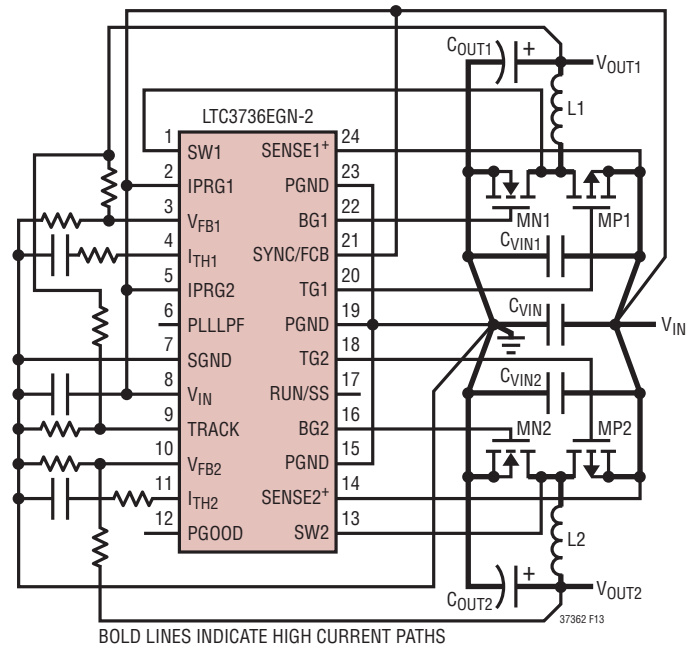
A second, more severe transient is caused by switching in loads with large ($>1\mu\text{F}$) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT} , causing a rapid drop in V_{OUT} . No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $(25)(C_{LOAD})$. Thus a $10\mu\text{F}$ capacitor would require a $250\mu\text{s}$ rise time, limiting the charging current to about 200mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3736-2. These items are illustrated in the layout diagram of Figure 13. Figure 14 depicts the current waveforms present in the various branches of the 2-phase dual regulator.

1. The power loop (input capacitor, MOSFETs, inductor, output capacitor) of each channel should be as small as possible and isolated as much as possible from the power loop of the other channel. Ideally, the drains of the P- and N-channel FETs should be connected close to one another with an input capacitor placed across the FET sources (from the P-channel source to the N-channel source) right at the FETs. It is better to have two separate, smaller valued input capacitors (e.g., two $10\mu\text{F}$ —one for each channel) than it is to have a single larger valued capacitor (e.g., $22\mu\text{F}$) that the channels share with a common connection.
2. The signal and power grounds should be kept separate. The signal ground consists of the feedback resistor dividers, I_{TH} compensation networks and the SGND pin.

The power grounds consist of the (–) terminal of the input and output capacitors and the source of the N-channel MOSFET. Each channel should have its own



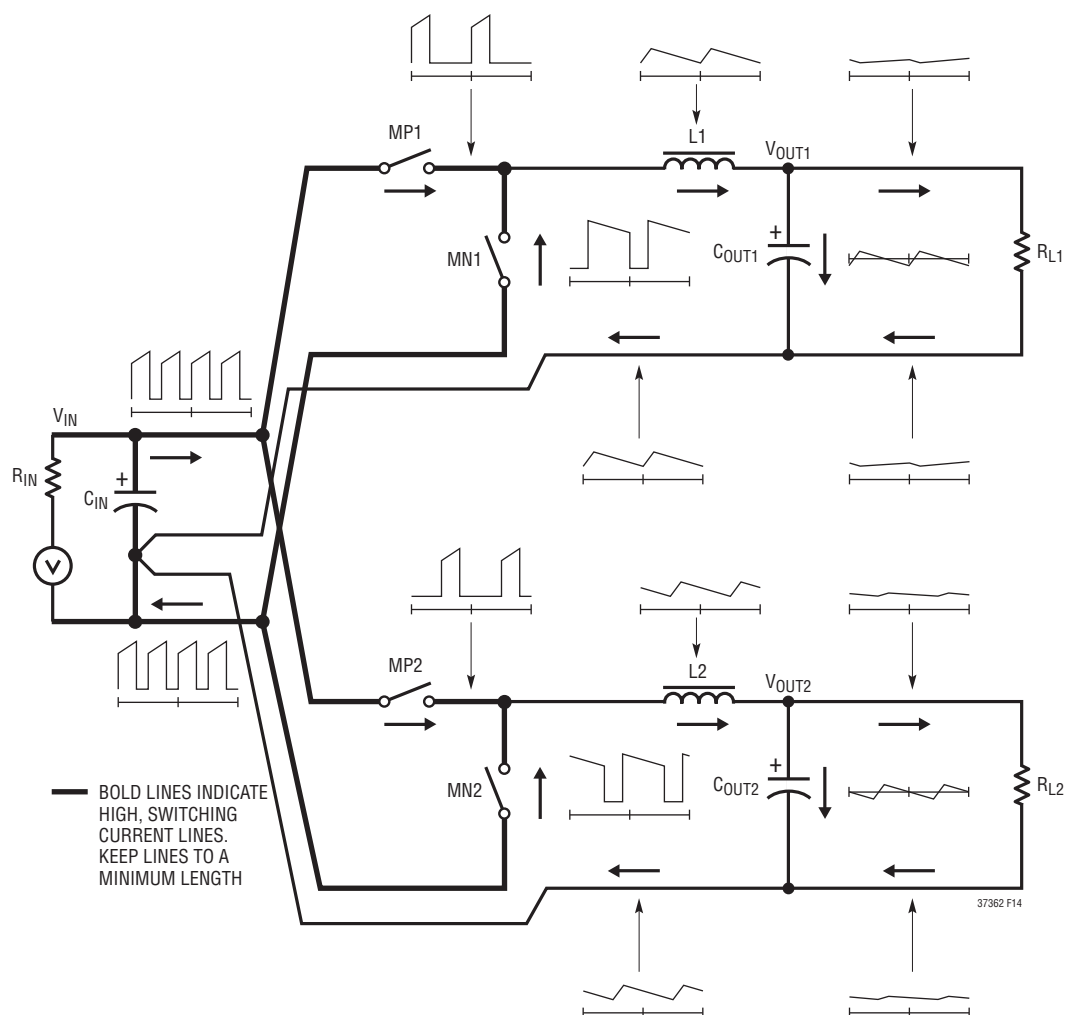
Figures 13. LTC3736-2 Layout Diagram

power ground for its power loop (as described above in item 1). The power grounds for the two channels should connect together at a common point. It is most important to keep the ground paths with high switching currents away from each other.

The PGND pins on the LTC3736-2 IC should be shorted together and connected to the common power ground connection (away from the switching currents).

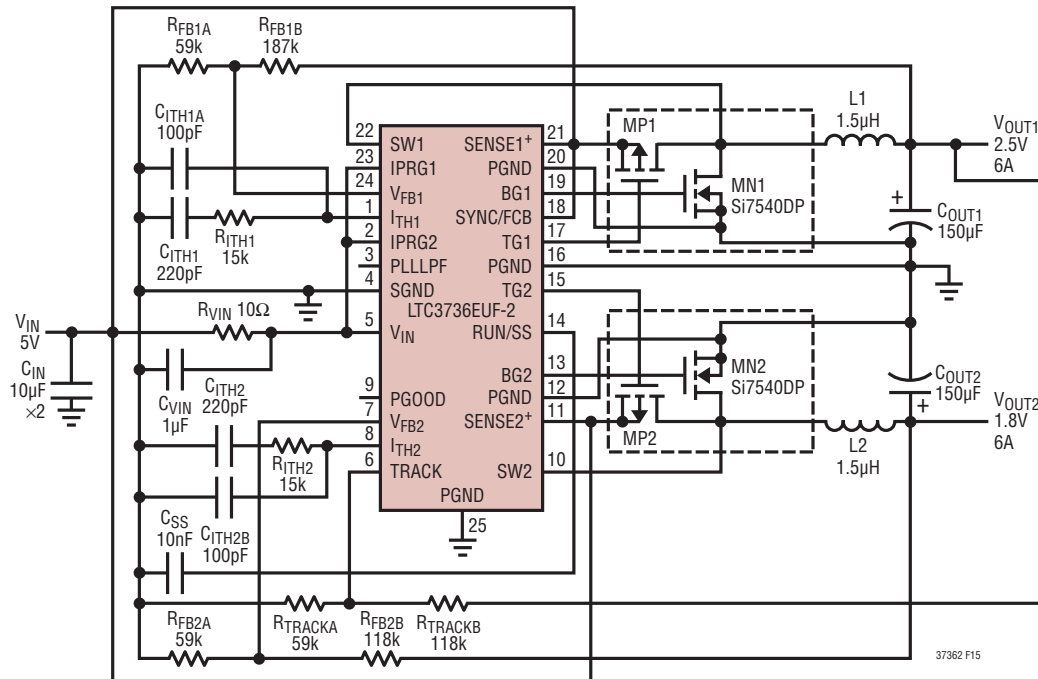
3. Put the feedback resistors close to the V_{FB} pins. The trace connecting the top feedback resistor (R_B) to the output capacitor should be a Kelvin trace. The I_{TH} compensation components should also be very close to the LTC3736-2.
4. The current sense traces (SENSE⁺ and SW) should be Kelvin connections right at the P-channel MOSFET source and drain.
5. Keep the switch nodes (SW1, SW2) and the gate driver nodes (TG1, TG2, BG1, BG2) away from the small-signal components, especially the opposite channel's feedback resistors, I_{TH} compensation components, and the current sense pins (SENSE⁺ and SW).

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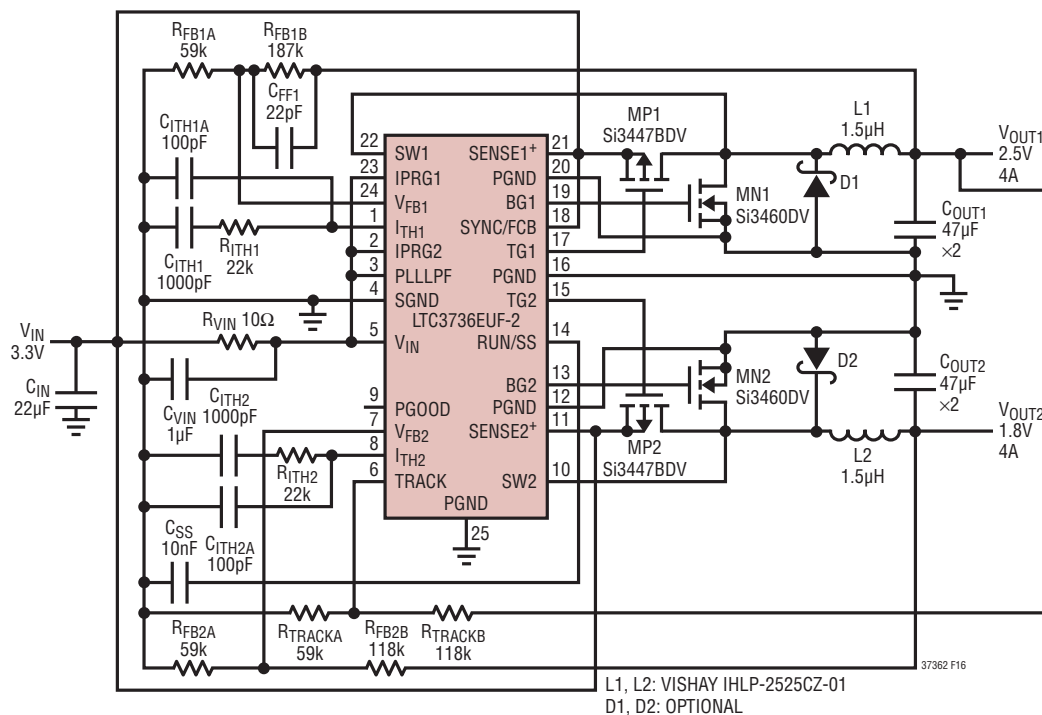


Figures 14. Branch Current Waveforms

TYPICAL APPLICATIONS



Figures 15. 2-Phase, 550kHz, Dual Output Synchronous DC/DC Converter

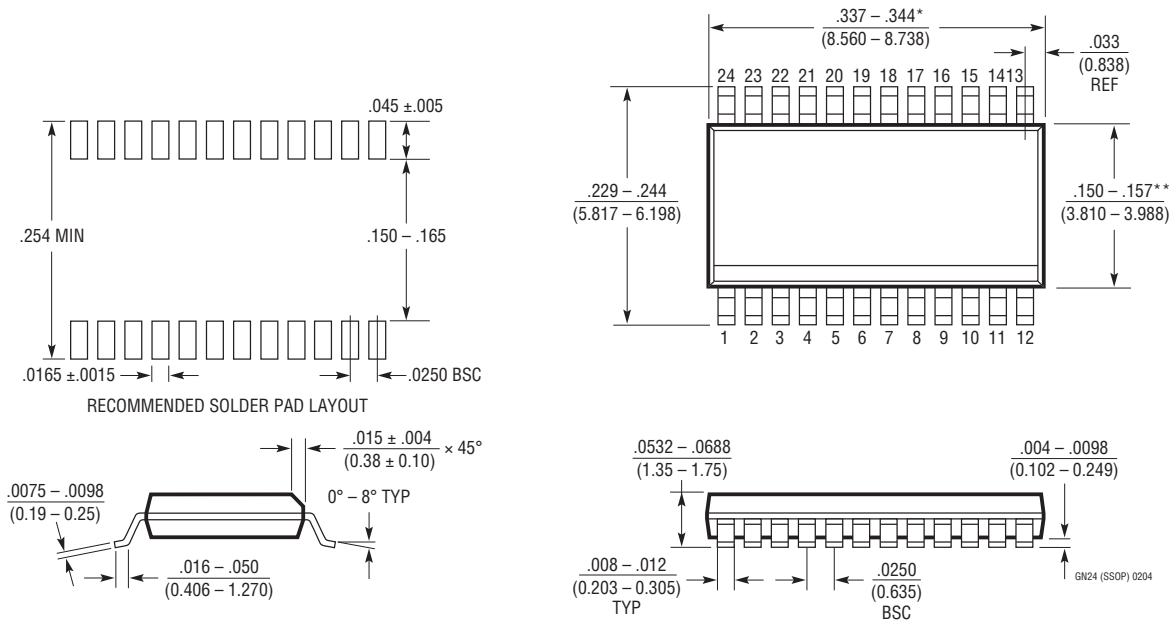


Figures 16. 2-Phase, 750kHz, Dual Output Synchronous DC/DC Converter

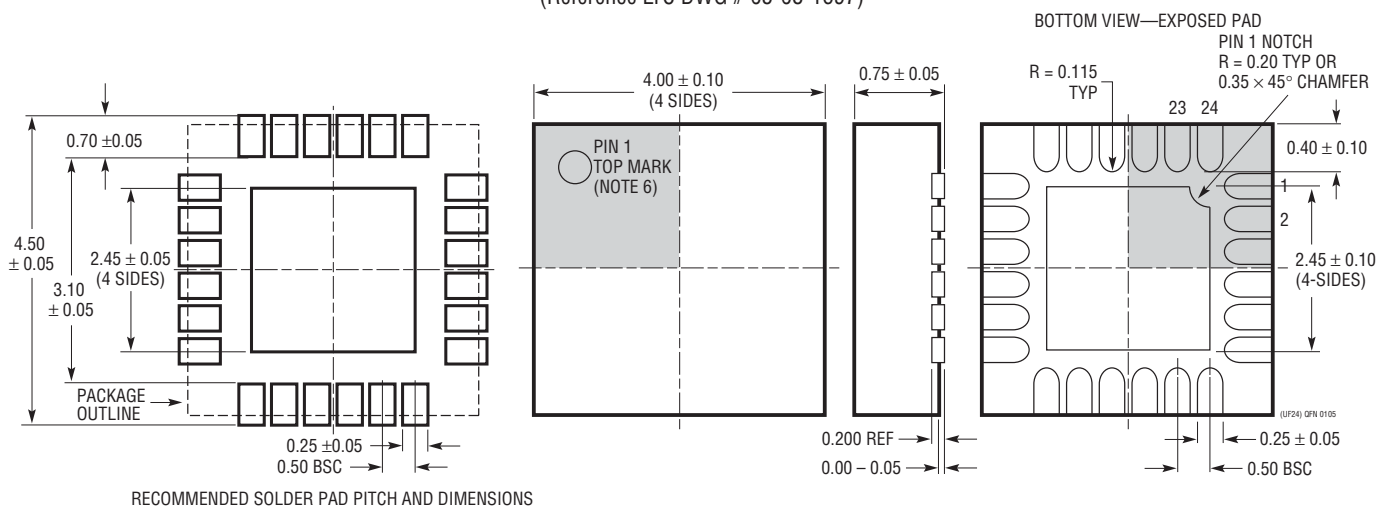


PACKAGE DESCRIPTION

GN Package 24-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)

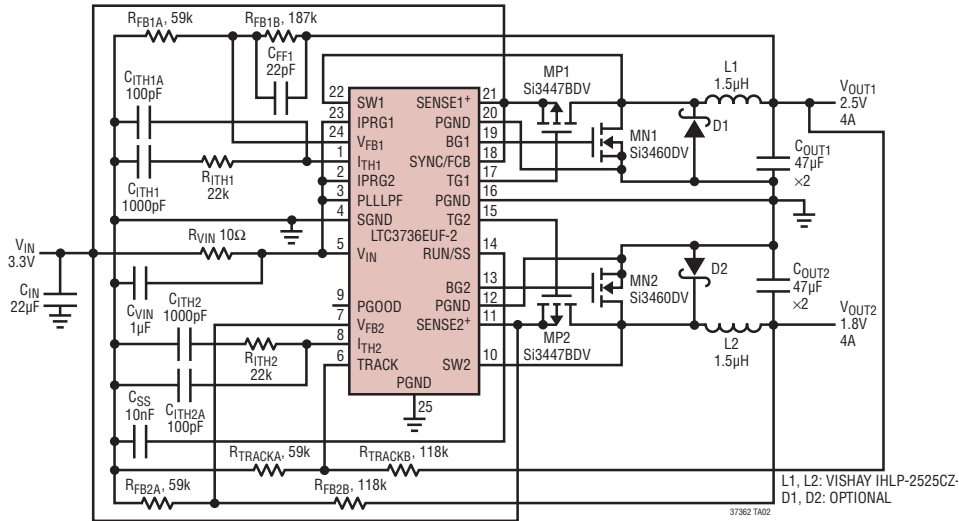


UF Package 24-Lead Plastic QFN (4mm × 4mm) (Reference LTC DWG # 05-08-1697)



TYPICAL APPLICATION

2-Phase, 750kHz, Dual Output Synchronous DC/DC Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1735	High Efficiency Synchronous Step-Down Controller	Burst Mode Operation, 16-Pin Narrow SSOP, $3.5V \leq V_{IN} \leq 36V$
LTC1778	No R_{SENSE}^{TM} Synchronous Step-Down Controller	Current Mode Operation Without Sense Resistor, Fast Transient Response, $4V \leq V_{IN} \leq 36V$
LTC2923	Power Supply Tracking Controller	Controls Up to Three Supplies, 10-Lead MSOP
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 2.5V to 5.5V, $I_Q = 60\mu A$, $I_{SD} < 1\mu A$, MS Package
LTC3416	4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter with Output Tracking	95% Efficiency, V_{IN} : 2.25V to 5.5V, $I_{SD} < 1\mu A$, TSSOP-20E Package
LTC3418	8A, 4MHz Synchronous Step-Down Regulator	V_{IN} : 2.25V to 5.5V, 5mm \times 7mm QFN Package
LTC3701	2-Phase, Low Input Voltage Dual Step-Down DC/DC Controller	$2.5V \leq V_{IN} \leq 9.8V$, 550kHz, PGOOD, PLL, 16-Lead SSOP
LTC3708	Fast 2-Phase, No R_{SENSE} Buck Controller with Output Tracking	Constant On-Time Dual Controller, V_{IN} Up to 36V, Very Low Duty Cycle Operation, 5mm \times 5mm QFN Package
LTC3728/LTC3728L	Dual, 550kHz, 2-Phase Synchronous Step-Down Switching Regulator	Constant Frequency, V_{IN} to 36V, 5V and 3.3V LDOs, 5mm \times 5mm QFN or 28-Lead SSOP
LTC3736	Dual, 2-Phase, No R_{SENSE} Synchronous Controller	$2.75V \leq V_{IN} \leq 9.8V$, Output Tracking
LTC3736-1	Dual, 2-Phase, No R_{SENSE} Synchronous Controller with Spread Spectrum	V_{IN} : 2.75V to 9.8V, 4mm \times 4mm QFN Package Spread Spectrum Operation; Output Tracking
LTC3737	Dual, 2-Phase, No R_{SENSE} Controller with Output Tracking	Nonsynchronous Constant Frequency with PLL, 4mm \times 4mm QFN and 24-Lead SSOP Packages
LTC3772	No R_{SENSE} Step-Down DC/DC Controller	$2.75V \leq V_{IN} \leq 9.8V$, SOT-23 or 3mm \times 2mm DFN Packages
LTC3776	Dual, 2-Phase, No R_{SENSE} Synchronous Controller for DDR/QDR Memory Termination	Provides V_{DDQ} and V_{TT} with One IC, $2.75V \leq V_{IN} \leq 9.8V$, 4mm \times 4mm QFN and 24-Lead SSOP Packages
LTC3808	No R_{SENSE} , Low EMI, Synchronous Step-Down Controller with Output Tracking	$2.75V \leq V_{IN} \leq 9.8V$; Spread Spectrum Operation; 3mm \times 4mm DFN and 16-Lead SSOP Packages
LTC3809/LTC3809-1	No R_{SENSE} Synchronous Step-Down Controllers	2.75V to 9.8V, 3mm \times 3mm DFN and 10-Lead MSOPE Packages

No R_{SENSE} is a trademark of Linear Technology Corporation.

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