

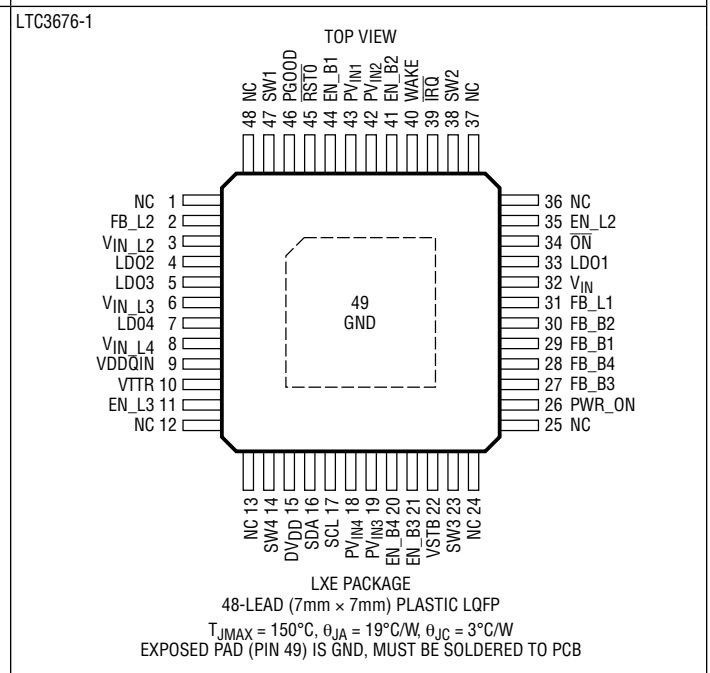
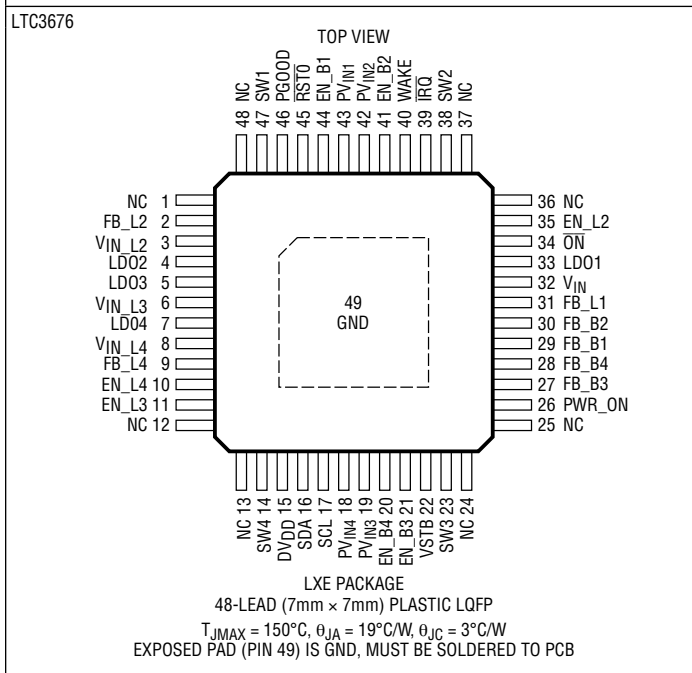
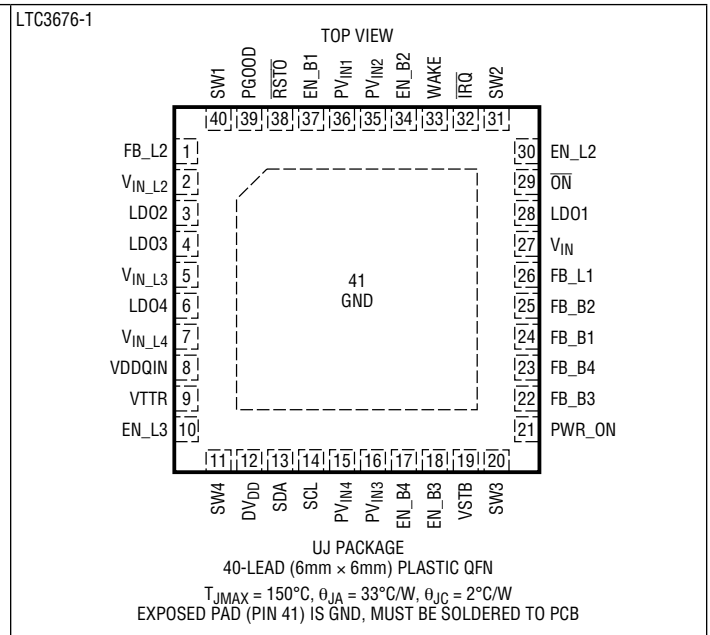
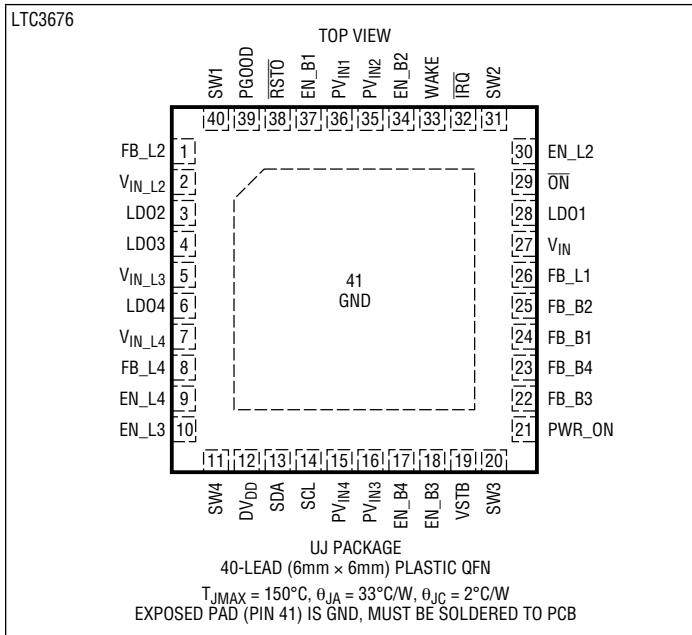
LTC3676/LTC3676-1

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} , DV_{DD} -0.3V to 6V
 PV_{IN1} , PV_{IN2} , PV_{IN3} , PV_{IN4} , V_{IN_L2} ,
 V_{IN_L3} , V_{IN_L4} -0.3V to $V_{IN} + 0.3V$
 $LDO1$, FB_L1 , $LDO2$, FB_L2 , $LDO3$, $LDO4$, FB_L4 ,
 FB_B1 , FB_B2 , FB_B3 , FB_B4 , $PGOOD$, $VSTB$, EN_B1 ,
 EN_B2 , EN_B3 , EN_B4 , EN_L2 , EN_L3 , EN_L4 , \overline{ON} ,

$WAKE$, \overline{RSTO} , PWR_ON , \overline{IRQ} , V_{TTR} ,
 $VDDQIN$ -0.3V to 6V
 SDA , SCL -0.3V to $DV_{DD} + 0.3V$
 Operating Junction Temperature Range
 (Notes 2, 3) -40°C to 150°C
 Storage Temperature Range -65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|------------------|--------------------|---------------|---------------------------------|-------------------|
| LTC3676EUJ#PBF | LTC3676EUJ#TRPBF | LTC3676UJ | 40-Lead (6mm × 6mm) Plastic QFN | -40°C to 125°C |
| LTC3676IUJ#PBF | LTC3676IUJ#TRPBF | LTC3676UJ | 40-Lead (6mm × 6mm) Plastic QFN | -40°C to 125°C |
| LTC3676HUJ#PBF | LTC3676HUJ#TRPBF | LTC3676UJ | 40-Lead (6mm × 6mm) Plastic QFN | -40°C to 150°C |
| LTC3676EUJ-1#PBF | LTC3676EUJ-1#TRPBF | LTC3676UJ-1 | 40-Lead (6mm × 6mm) Plastic QFN | -40°C to 125°C |
| LTC3676IUJ-1#PBF | LTC3676IUJ-1#TRPBF | LTC3676UJ-1 | 40-Lead (6mm × 6mm) Plastic QFN | -40°C to 125°C |
| LTC3676HUJ-1#PBF | LTC3676HUJ-1#TRPBF | LTC3676UJ-1 | 40-Lead (6mm × 6mm) Plastic QFN | -40°C to 150°C |

AUTOMOTIVE PRODUCTS**

| | | | | |
|-----------------|-------------------|-----------|---------------------------------|----------------|
| LTC3676EUJ#WPBF | LTC3676EUJ#WTRPBF | LTC3676UJ | 40-Lead (6mm × 6mm) Plastic QFN | -40°C to 125°C |
| LTC3676IUJ#WPBF | LTC3676IUJ#WTRPBF | LTC3676UJ | 40-Lead (6mm × 6mm) Plastic QFN | -40°C to 125°C |
| LTC3676HUJ#WPBF | LTC3676HUJ#WTRPBF | LTC3676UJ | 40-Lead (6mm × 6mm) Plastic QFN | -40°C to 150°C |

| LEAD FREE FINISH | TRAY | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|-------------------|-------------------|---------------|-----------------------------------|-------------------|
| LTC3676ELXE#PBF | LTC3676ELXE#PBF | LTC3676LXE | 48-Lead (7mm × 7mm) Plastic eLQFP | -40°C to 125°C |
| LTC3676ILXE#PBF | LTC3676ILXE#PBF | LTC3676LXE | 48-Lead (7mm × 7mm) Plastic eLQFP | -40°C to 125°C |
| LTC3676HLXE#PBF | LTC3676HLXE#PBF | LTC3676LXE | 48-Lead (7mm × 7mm) Plastic eLQFP | -40°C to 150°C |
| LTC3676ELXE-1#PBF | LTC3676ELXE-1#PBF | LTC3676LXE-1 | 48-Lead (7mm × 7mm) Plastic eLQFP | -40°C to 125°C |
| LTC3676ILXE-1#PBF | LTC3676ILXE-1#PBF | LTC3676LXE-1 | 48-Lead (7mm × 7mm) Plastic eLQFP | -40°C to 125°C |
| LTC3676HLXE-1#PBF | LTC3676HLXE-1#PBF | LTC3676LXE-1 | 48-Lead (7mm × 7mm) Plastic eLQFP | -40°C to 150°C |

AUTOMOTIVE PRODUCTS**

| | | | | |
|------------------|------------------|------------|-----------------------------------|----------------|
| LTC3676ELXE#WPBF | LTC3676ELXE#WPBF | LTC3676LXE | 48-Lead (7mm × 7mm) Plastic eLQFP | -40°C to 125°C |
| LTC3676ILXE#WPBF | LTC3676ILXE#WPBF | LTC3676LXE | 48-Lead (7mm × 7mm) Plastic eLQFP | -40°C to 125°C |
| LTC3676HLXE#WPBF | LTC3676HLXE#WPBF | LTC3676LXE | 48-Lead (7mm × 7mm) Plastic eLQFP | -40°C to 150°C |

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

[Tape and reel specifications](#). Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

LTC3676/LTC3676-1

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Note 2). $V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_L2} = V_{IN_L3} = V_{IN_L4} = DV_{DD} = 3.8\text{V}$. All regulators disabled unless otherwise noted.

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|--------------------------------|---|------|------|------|---------------|
| Operating Input Supply Voltage, V_{IN} | | ● | 2.7 | | 5.5 | V |
| V_{IN} Standby Current | PWR_ON = 0V | ● | | 12 | 21 | μA |
| Undervoltage Fault Rising (Note 7) | | ● | | 2.55 | 2.65 | V |
| Undervoltage Fault Falling | | ● | 2.35 | 2.45 | | V |
| Undervoltage Warning | CNTRL[4:2] = 000 (POR Default) | | | 2.7 | | V |
| | CNTRL[4:2] = 001 | | | 2.8 | | V |
| | CNTRL[4:2] = 010 | | | 2.9 | | V |
| | CNTRL[4:2] = 011 | | | 3.0 | | V |
| | CNTRL[4:2] = 100 | | | 3.1 | | V |
| | CNTRL[4:2] = 101 | | | 3.2 | | V |
| | CNTRL[4:2] = 110 | | | 3.3 | | V |
| | CNTRL[4:2] = 111 | | | 3.4 | | V |

Step-Down Switching Regulators 1, 2, 3 and 4

| | | | | | | |
|--|---|---|----------|-------|-----------|---------------|
| Output Voltage Range | | ● | V_{FB} | | PV_{IN} | V |
| Burst Mode [®] V_{IN} Quiescent Current | $V_{FB_BX} = 850\text{mV}$ (Note 5) | ● | | 23 | 50 | μA |
| Pulse-Skipping Mode V_{IN} Quiescent Current | $V_{FB_BX} = 850\text{mV}$ (Note 5) | ● | | 120 | 200 | μA |
| Forced Continuous V_{IN} Quiescent Current | $V_{FB_BX} = 0\text{V}$ (Note 5) | ● | | 170 | 300 | μA |
| Feedback Pin Input Current | $V_{FB_BX} = 850\text{mV}$ | | -0.05 | | 0.05 | μA |
| Maximum Duty Cycle | $V_{FB} = 0\text{V}$ | ● | 100 | | | % |
| SW Pull-Down Resistance | Regulator Disabled | | | 625 | | Ω |
| Feedback Reference Soft-Start Rate | (Note 6) | | | 0.8 | | V/ms |
| High Feedback Regulation Voltage (V_{FB}) | DVBxA[4:0] = DVBxB[4:0] = 11111, $V_{IN} = 2.7\text{V}$ to 5.5V | ● | 788 | 800 | 812 | mV |
| Default Feedback Regulation Voltage (V_{FB}) | DVBxA[4:0] = DVBxB[4:0] = 11001, $V_{IN} = 2.7\text{V}$ to 5.5V | ● | 714 | 725 | 736 | mV |
| Low Feedback Regulation Voltage (V_{FB}) | DVBxA[4:0] = DVBxB[4:0] = 00000, $V_{IN} = 2.7\text{V}$ to 5.5V | ● | 404 | 412.5 | 421 | mV |
| Feedback LSB Step Size | | | | 12.5 | | mV |
| Switching Frequency | BUCKx[2] = 0 | ● | 1.7 | 2.25 | 2.7 | MHz |
| | BUCKx[2] = 1 | ● | 0.85 | 1.125 | 1.35 | MHz |

1.5A Step-Down Switching Regulators 1 and 2

| | | | | | | |
|--------------------|--|---|-----|-----|--|------------------|
| PMOS Current Limit | | ● | 2.0 | | | A |
| PMOS On-Resistance | | | | 160 | | $\text{m}\Omega$ |
| NMOS On-Resistance | | | | 80 | | $\text{m}\Omega$ |

2.5A Step-Down Switching Regulators 3 and 4

| | | | | | | |
|--------------------|--|---|-----|-----|--|------------------|
| PMOS Current Limit | | ● | 3.0 | | | A |
| PMOS On-Resistance | | | | 120 | | $\text{m}\Omega$ |
| NMOS On-Resistance | | | | 70 | | $\text{m}\Omega$ |

Step-Down Switching Regulator 1 and VTTR (LTC3676-1)

| | | | | | | |
|------------------------------------|---------------------------|---|------------------------|-----------------------|------------------------|----|
| Buck 1 Feedback Regulation Voltage | $V_{DDQIN} = 1.5\text{V}$ | ● | $VTTR - 10$ | $VTTR$ | $VTTR + 10$ | mV |
| VTTR Output Voltage | $V_{DDQIN} = 1.5\text{V}$ | ● | $0.49 \cdot V_{DDQIN}$ | $0.5 \cdot V_{DDQIN}$ | $0.51 \cdot V_{DDQIN}$ | mV |
| VTTR Maximum Output Current | | ● | -10 | | 10 | mA |
| I_{VIN} VTTR Enabled | | | | 1 | | mA |

LDO Regulators 2, 3 and 4

| | | | | | | |
|------------------------------------|--------------------|--|--|-----|--|----------|
| Feedback Reference Soft-Start Rate | | | | 10 | | V/ms |
| Output Pull-Down Resistance | Regulator Disabled | | | 625 | | Ω |

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| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|--|---|--------------|------------|--------------|---------------|
| LDO Regulator 1 | | | | | | |
| Output Voltage Range | | | V_{FB_L1} | | V_{IN} | |
| Feedback Regulation Voltage (V_{FB_L1}) | | ● | 689 | 725 | 761 | mV |
| Line Regulation | $I_{LD01} = 1\text{mA}$, $V_{LD01} = 1.2\text{V}$, $V_{IN} = 2.7\text{V to } 5.5\text{V}$ | | | 0.15 | | %/V |
| Load Regulation | $I_{LD01} = 0.1\text{mA to } 25\text{mA}$, $V_{LD01} = 3.3\text{V}$ | | | 0.1 | | % |
| Available Output Current | | ● | 25 | | | mA |
| Short-Circuit Output Current Limit | | | | 65 | 100 | mA |
| Dropout Voltage (Note 4) | $I_{LD01} = 25\text{mA}$, $V_{LD01} = 3.3\text{V}$ | | | 200 | 280 | mV |
| Feedback Pin Input Current | $V_{FB_L1} = 850\text{mV}$ | | -0.05 | | 0.05 | μA |
| LDO Regulator 2 | | | | | | |
| V_{IN_L2} Input Voltage | | ● | 1.7 | | V_{IN} | V |
| LDO2 Output Voltage Range | $I_{LD02} = 0\text{mA}$ | | V_{FB_L2} | | V_{IN_L2} | V |
| Available Output Current | | ● | 300 | | | mA |
| V_{IN_L2} Quiescent Current | Regulator Enabled, $I_{LD02} = 0\text{A}$ | ● | | 12 | 25 | μA |
| V_{IN_L2} Shutdown Current | Regulator Disabled | ● | | 0 | 1 | μA |
| V_{IN} Quiescent Current | Regulator Enabled | ● | | 50 | 85 | μA |
| Feedback Regulation Voltage (V_{FB_L2}) | | ● | 0.707 | 0.725 | 0.743 | V |
| Line Regulation | $I_{LD02} = 1\text{mA}$, $V_{IN} = 2.7\text{V to } 5.5\text{V}$ | | | 0.01 | | %/V |
| Load Regulation | $I_{LD02} = 1\text{mA to } 300\text{mA}$ | | | 0.01 | | % |
| Short-Circuit Current Limit | | | | | 770 | mA |
| Dropout Voltage (Note 4) | $I_{LD02} = 300\text{mA}$, $V_{LD02} = 2.5\text{V}$ $I_{LD02} = 300\text{mA}$, $V_{LD02} = 1.2\text{V}$ | | | 210 450 | 260 615 | mV mV |
| Feedback Pin Input Current | $V_{FB_L2} = 725\text{mV}$ | | -0.05 | | 0.05 | μA |
| LDO Regulator 3 | | | | | | |
| V_{IN_L3} Input Voltage | | ● | 2.35 | | V_{IN} | V |
| Output Voltage | $I_{LD03} = 0\text{mA}$ | ● | 1.746 | 1.8 | 1.854 | V |
| Available Output Current | | ● | 300 | | | mA |
| V_{IN_L3} Quiescent Current | Regulator Enabled, $I_{LD03} = 0\text{A}$ | ● | | 14 | 25 | μA |
| V_{IN_L3} Shutdown Current | Regulator Disabled | ● | | 0 | 1 | μA |
| V_{IN} Quiescent Current | Regulator Enabled | ● | | 50 | 85 | μA |
| Line Regulation | $I_{LD03} = 1\text{mA}$, $V_{IN} = 2.7\text{V to } 5.5\text{V}$ | | | 0.01 | | %/V |
| Load Regulation | $I_{LD03} = 1\text{mA to } 300\text{mA}$ | | | 0.05 | | % |
| Short-Circuit Current Limit | | | | | 770 | mA |
| Dropout Voltage (Note 4) | $I_{LD03} = 300\text{mA}$, $V_{LD03} = 1.8\text{V}$ | | | 280 | 350 | mV |
| LDO Regulator 4 | | | | | | |
| V_{IN_L4} Input Voltage | | ● | 1.7 | | V_{IN} | V |
| LDO4 Output Voltage Range (LTC3676) | $I_{LD04} = 0\text{mA}$ | | V_{FB_L4} | | V_{IN_L4} | V |
| Feedback Regulation Voltage (LTC3676) (V_{FB_L4}) | | ● | 0.707 | 0.725 | 0.743 | V |
| Output Voltage (LTC3676-1) | $I_{LD04} = 1\text{mA}$, $LDOB[4:3] = 00$ | ● | 1.164 | 1.2 | 1.236 | V |
| | $LDOB[4:3] = 01$ | ● | 2.425 | 2.5 | 2.575 | V |
| | $LDOB[4:3] = 10$ | ● | 2.716 | 2.8 | 2.884 | V |
| | $LDOB[4:3] = 11$ | ● | 2.91 | 3.0 | 3.09 | V |

LTC3676/LTC3676-1

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| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|--|---|-------|------------|------------|--------------------------------|
| Available Output Current | | ● | 300 | | | mA |
| V_{IN_L4} Quiescent Current | Regulator Enabled, $I_{LD04} = 0\text{A}$ | ● | | 12 | 25 | μA |
| V_{IN_L4} Shutdown Current | Regulator Disabled | ● | | 0 | 1 | μA |
| V_{IN} Quiescent Current | Regulator Enabled | ● | | 50 | 85 | μA |
| Line Regulation | $I_{LD04} = 1\text{mA}$, $V_{IN} = 2.7\text{V}$ to 5.5V | | | 0.01 | | %/V |
| Load Regulation (LTC3676) | $I_{LD04} = 1\text{mA}$ to 300mA | | | 0.01 | | % |
| Load Regulation (LTC3676-1) | | | | 0.05 | | % |
| Short-Circuit Current Limit | | | | | 770 | mA |
| Dropout Voltage (Note 4) | $I_{LD04} = 300\text{mA}$, $V_{LD04} = 2.5\text{V}$ $I_{LD04} = 300\text{mA}$, $V_{LD04} = 1.2\text{V}$ | | | 210 450 | 260 615 | mV mV |
| Feedback Pin Input Current (LTC3676) | $V_{FB_L4} = 725\text{mV}$ | | -0.05 | | 0.05 | μA |
| Enable Inputs | | | | | | |
| Threshold Rising | All Enables Low | ● | | 0.75 | 1.2 | V |
| Threshold Falling | One Enable High | ● | 0.4 | 0.7 | | V |
| Precision Threshold | One or More Regulators Previously Enabled | ● | 0.370 | 0.400 | 0.430 | V |
| Input Pull-Down Resistance | | | | 4.5 | | $\text{M}\Omega$ |
| VSTB, PWR_ON Inputs | | | | | | |
| Threshold | | ● | 0.370 | 0.400 | 0.430 | V |
| Pull-Down Resistance | | | | 4.5 | | $\text{M}\Omega$ |
| Pushbutton Interface | | | | | | |
| $\overline{\text{ON}}$ Threshold Rising | | ● | | 0.75 | 1.2 | V |
| $\overline{\text{ON}}$ Threshold Falling | | ● | 0.4 | 0.7 | | V |
| $\overline{\text{ON}}$ Input Current | $\overline{\text{ON}} = V_{IN}$ $\overline{\text{ON}} = 0\text{V}$ | | -1 | -40 | 1 | μA μA |
| $\overline{\text{ON}}$ Low Time to $\overline{\text{IRQ}}$ Low | | | | 50 | | ms |
| $\overline{\text{ON}}$ High Time to $\overline{\text{IRQ}}$ High | | | | 0.2 | | μs |
| $\overline{\text{ON}}$ Low Time to WAKE High | | | | 400 | | ms |
| $\overline{\text{ON}}$ Low Time to Hard Reset | CNTRL[6] = 0 | | | 10 | | s |
| $\overline{\text{IRQ}}$ Minimum Pulse Width | | | | 50 | | ms |
| $\overline{\text{IRQ}}$ Blanking from WAKE Low | | | | 1 | | s |
| Minimum WAKE Low Time | | | | 1 | | s |
| WAKE High Time with PWR_ON = 0V | | | | 5 | | s |
| PWR_ON High to WAKE High | | | | 3 | | ms |
| PWR_ON Low to WAKE Low | | | | 3 | | ms |
| Status Output Pins (WAKE, PGOOD, RSTO, IRQ) | | | | | | |
| WAKE Output Low Voltage | $I_{WAKE} = 3\text{mA}$ | | | 0.1 | 0.4 | V |
| WAKE Output High Leakage Current | $V_{WAKE} = 3.8\text{V}$ | | -0.1 | | 0.1 | μA |
| PGOOD Output Low Voltage | $I_{PGOOD} = 3\text{mA}$ | | | 0.1 | 0.4 | V |
| PGOOD Output High Leakage Current | $V_{PGOOD} = 3.8\text{V}$ | | -0.1 | | 0.1 | μA |
| PGOOD Threshold Rising | | | | -6 | | % |
| PGOOD Threshold Falling | | | | -8 | | % |
| RSTO Output Low Voltage | $I_{RSTO} = 3\text{mA}$ | | | 0.1 | 0.4 | V |
| RSTO Output High Leakage Current | $V_{RSTO} = 3.8\text{V}$ | | -0.1 | | 0.1 | μA |

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| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------------|-------------------------|------|------|-----|---------------|
| LDO1 Power Good Threshold Rising | | | -7.5 | | % |
| LDO1 Power Good Threshold Falling | | | -10 | | % |
| IRQ Output Low Voltage | $I_{IRQ} = 3\text{mA}$ | | 0.1 | 0.4 | V |
| IRQ Output High Leakage Current | $V_{IRQ} = 3.8\text{V}$ | -0.1 | | 0.1 | μA |

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|----------------------------|--|---|---------------|------------------------------|-----|--------------------|
| I²C Port | | | | | | |
| DV _{VDD} | DV _{VDD} Input Supply Voltage | | ● 1.6 | | 5.5 | V |
| I _{DVDD} | DV _{VDD} Quiescent Current | SCL/SDA = 0kHz | | 0.3 | 1 | μA |
| DV _{VDD_UVLO} | DV _{VDD} UVLO Level | | | 1 | | V |
| ADDRESS | LTC3676 Device Address LTC3676-1 Device Address | | | 0111100[R/W] 0111101[R/W] | | |
| V _{IH} | SDA/SCL Input Threshold Rising | | | 70 | | %DV _{VDD} |
| V _{IL} | SDA/SCL Input Threshold Falling | | | 30 | | %DV _{VDD} |
| I _{IH} | SDA/SCL High Input Current | SDA = SCL = 5.5V | -1 | 0 | 1 | μA |
| I _{IL} | SDA/SCL Low Input Current | SDA = SCL = 0V | -1 | 0 | 1 | μA |
| V _{OL_SDA} | SDA Output Low Voltage | $I_{SDA} = 3\text{mA}$ | | | 0.4 | V |
| f _{SCL} | Clock Operating Frequency | | | | 400 | kHz |
| t _{BUF} | Bus Free Time Between Stop and Start Condition | | 1.3 | | | μs |
| t _{HD_STA} | Hold Time After Repeated Start Condition | | 0.6 | | | μs |
| t _{SU_STA} | Repeated Start Condition Setup Time | | 0.6 | | | μs |
| t _{SU_STO} | Stop Condition Setup Time | | 0.6 | | | μs |
| t _{HD_DAT(O)} | Data Hold Time Output | | 0 | | 900 | ns |
| t _{HD_DAT(I)} | Data Hold Time Input | | 0 | | | ns |
| t _{SU_DAT} | Data Setup Time | | 100 | | | ns |
| t _{LOW} | SCL Clock Low Period | | 1.3 | | | μs |
| t _{HIGH} | SCL Clock High Period | | 0.6 | | | μs |
| t _f | Clock/Data Fall Time | $C_B = \text{Capacitance of BUS Line (pF)}$ | $20 + 0.1C_B$ | | 300 | ns |
| t _r | Clock/Data Rise Time | $C_B = \text{Capacitance of BUS Line (pF)}$ | $20 + 0.1C_B$ | | 300 | ns |
| t _{SP} | Input Spike Suppression Pulse Width | | | | 50 | ns |

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3676 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3676E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the -40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3676I is guaranteed over the -40°C to 125°C operating junction temperature range and the LTC3676H is guaranteed over the full -40°C to

150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C . The junction temperature (T_J in $^\circ\text{C}$) is calculated from the ambient temperature (T_A in $^\circ\text{C}$) and power dissipation (P_D , in Watts), and package to junction ambient thermal impedance (θ_{JA} in $\text{Watts}/^\circ\text{C}$) according to the formula:

$$T_J = T_A + (P_D \cdot \theta_{JA}).$$

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and

ELECTRICAL CHARACTERISTICS

other environmental factors.

Note 3: The LTC3676 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

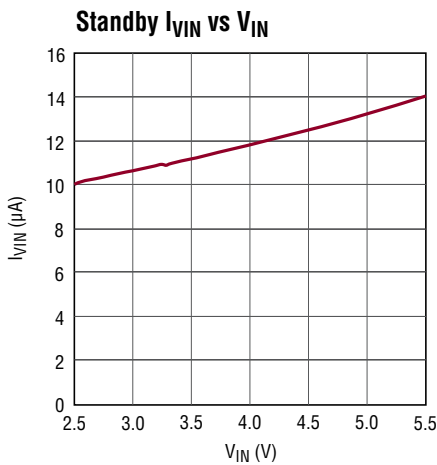
Note 4: Dropout voltage is defined as $(V_{IN} - V_{LDO1})$ for LDO1 or $(V_{IN_LX} - V_{LDOx})$ for other LDOs when V_{LDOx} is 3% lower than V_{LDOx} measured with $V_{IN} = V_{IN_LX} = 4.3V$.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

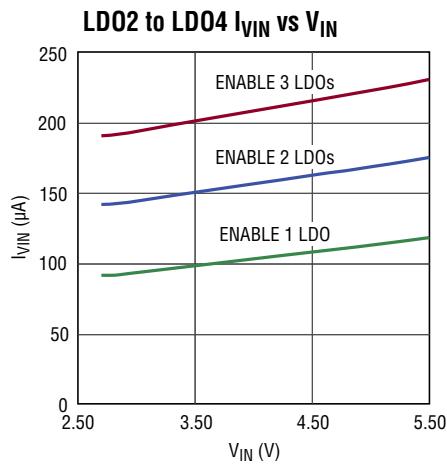
Note 6: Soft-Start measured in test mode with regulator error amplifier in unity-gain mode.

Note 7: The LTC3676 and LTC3676-1 will operate before V_{IN} has risen higher than V_{IN} undervoltage fault rising (2.65V rising), but will shutdown if V_{IN} does not cross the rising threshold in less than 5 seconds. Please refer to the Operation section.

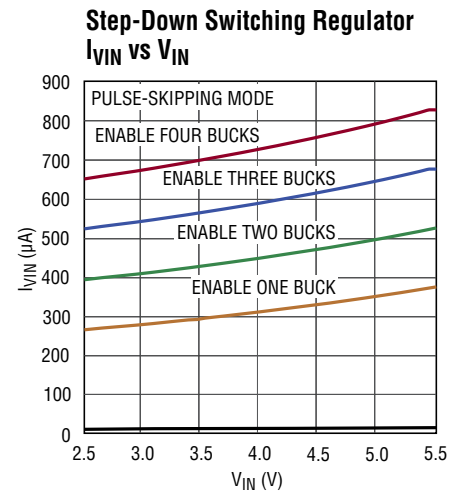
TYPICAL PERFORMANCE CHARACTERISTICS $V_{IN} = 3.8V$, $T_A = 25^\circ C$ unless otherwise noted



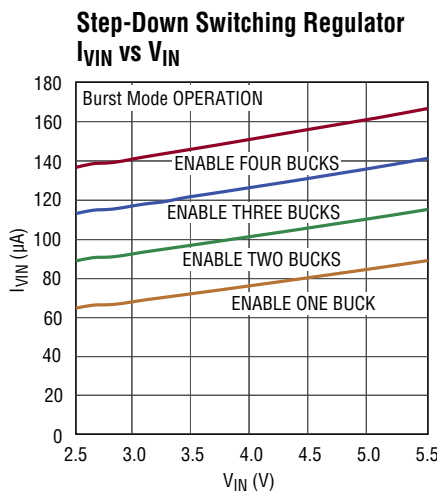
3676 G01



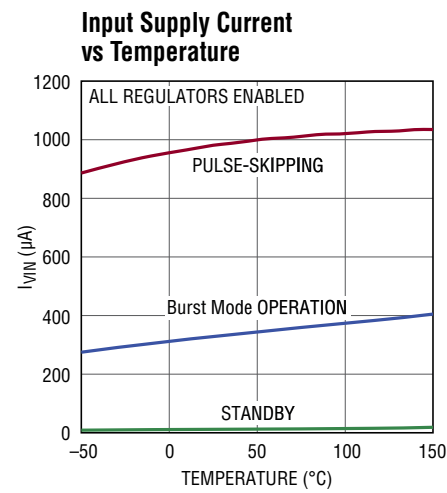
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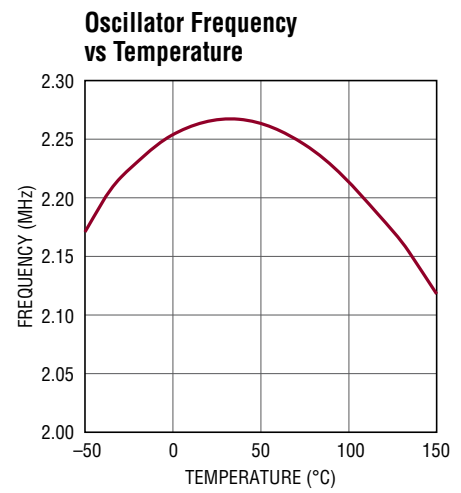
3676 G03



3676 G04



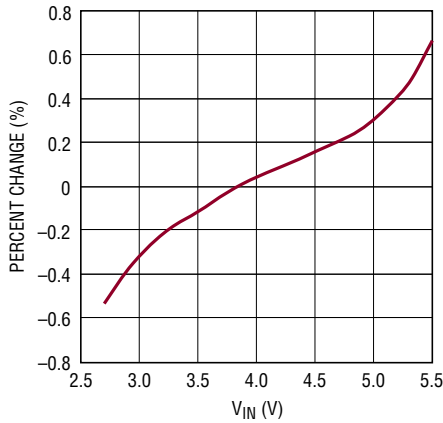
3676 G05



3676 G06

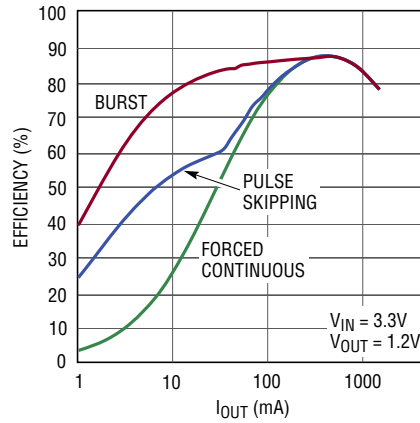
TYPICAL PERFORMANCE CHARACTERISTICS

Oscillator Frequency Change vs V_{IN}



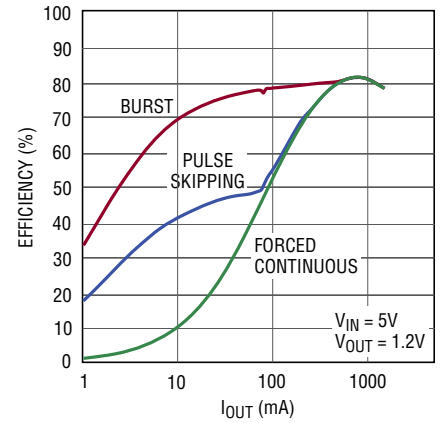
3676 G07

Step-Down Switching Regulators 1 and 2 Efficiency vs I_{OUT}



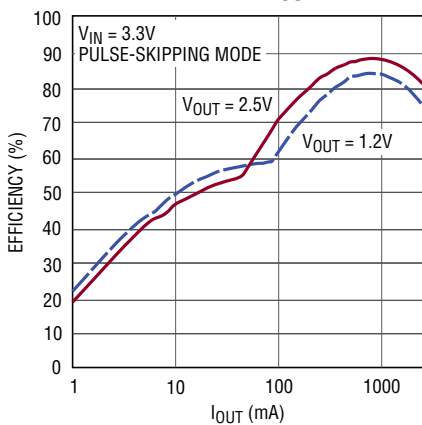
3676 G08

Step-Down Switching Regulators 1 and 2 Efficiency vs I_{OUT}



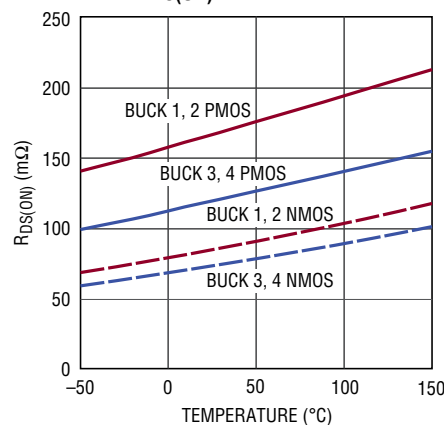
3676 G09

Step-Down Switching Regulators 3 and 4 Efficiency vs I_{OUT}



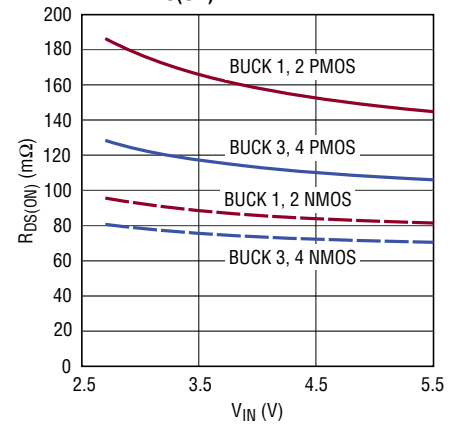
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Buck $R_{DS(ON)}$ vs Temperature



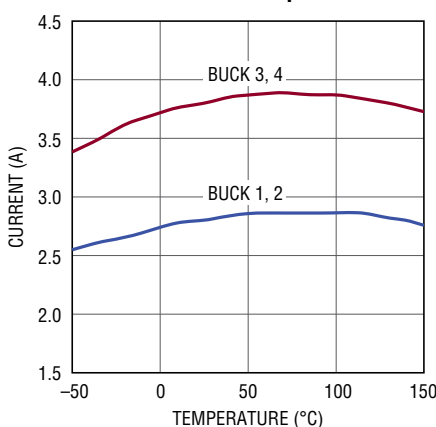
3676 G11

Buck $R_{DS(ON)}$ vs V_{IN}



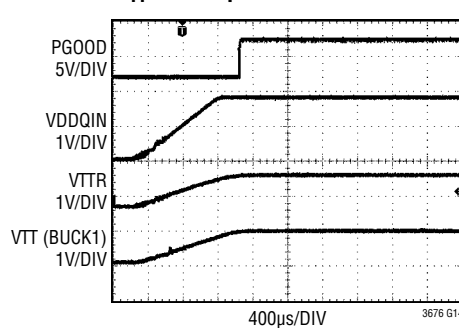
3676 G12

Step-Down Switching Regulator Current Limit vs Temperature

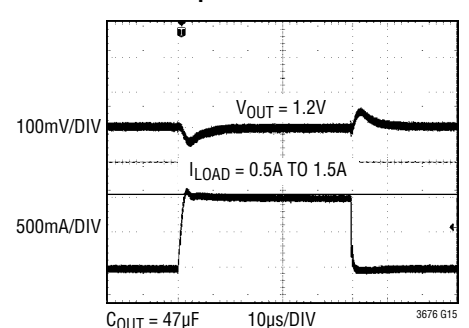


3676 G13

LTC3676-1 VDDQIN, VTTR and V_{TT} Start-Up

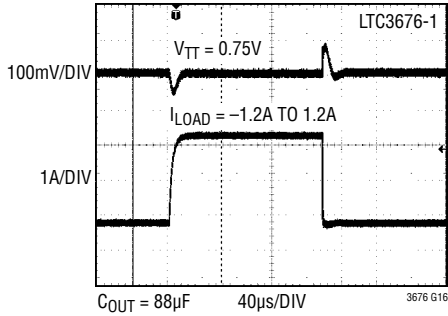


Step-Down Switching Regulator Load Step

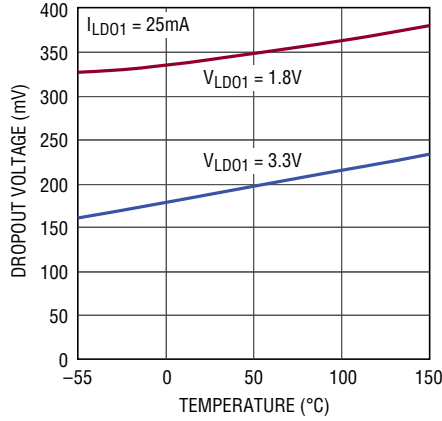


TYPICAL PERFORMANCE CHARACTERISTICS

LTC3676-1 V_{TT} Load Step

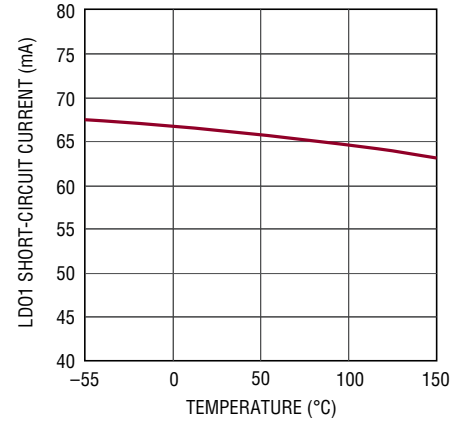


LD01 Dropout Voltage vs Temperature



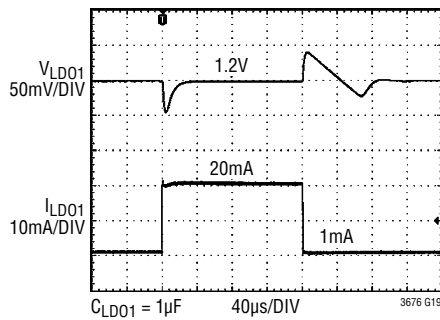
3676 G17

LD01 Short-Circuit Current vs Temperature

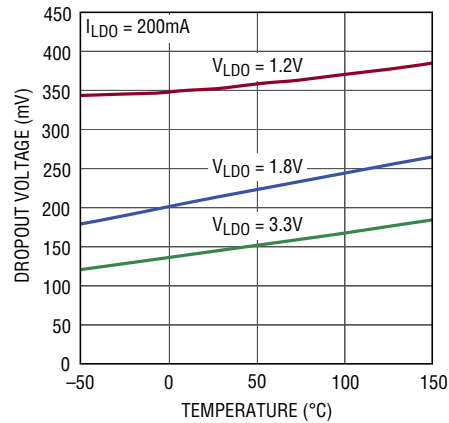


3676 G18

LD01 Load Step Response

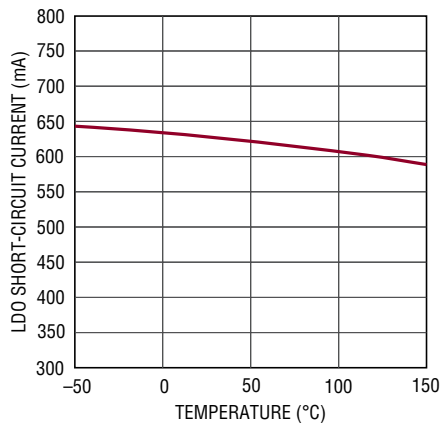


LD02 to LD04 Dropout Voltage vs Temperature



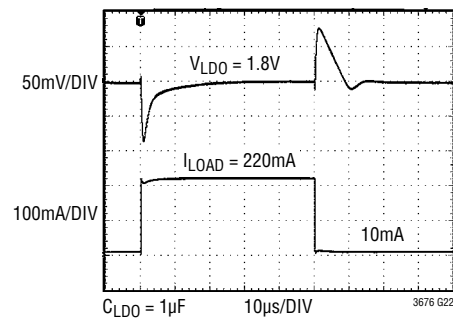
3676 G20

LD02 to LD04 Short-Circuit Current vs Temperature



3676 G21

LD02 to LD04 Load Step Response



PIN FUNCTIONS (QFN/LQFP)

FB_L2 (Pin 1/Pin 2): Feedback Input for LDO2. Set output voltage using a resistor divider connected from LDO2 to this pin to ground.

V_{IN_L2} (Pin 2/Pin 3): Power Input for LDO2. This pin should be bypassed to ground with a 1 μ F or greater ceramic capacitor. Voltage on V_{IN_L2} should not exceed voltage on V_{IN} pin.

LDO2 (Pin 3/Pin 4): Output Voltage of LDO2. Nominal output voltage is set with a resistor feedback divider that serves to a fixed 725mV reference. This pin must be bypassed to ground with a 1 μ F or greater ceramic capacitor.

LDO3 (Pin 4/Pin 5): Output Voltage of LDO3. Nominal output voltage is a fixed 1.8V. This pin must be bypassed to ground with a 1 μ F or greater ceramic capacitor.

V_{IN_L3} (Pin 5/Pin 6): Power Input for LDO3. This pin should be bypassed to ground with a 1 μ F or greater ceramic capacitor. Voltage on V_{IN_L3} should not exceed voltage on V_{IN} pin.

LDO4 (Pin 6/Pin 7): Output Voltage of LDO4. Nominal output voltage is set with a resistor feedback divider that serves to a fixed 725mV reference. This pin must be bypassed to ground with a 1 μ F or greater ceramic capacitor.

V_{IN_L4} (Pin 7/Pin 8): Power Input for LDO4. This pin should be bypassed to ground with a 1 μ F or greater ceramic capacitor. Voltage on V_{IN_L4} should not exceed voltage on V_{IN} pin.

FB_L4 (Pin 8/Pin 9): Feedback Input for LTC3676 LDO4. Set output voltage using a resistor divider connected from LDO4 to this pin to ground.

VDDQIN (Pin 8/Pin 9): V_{DD} Sense Input for LTC3676-1. Tie DDR memory V_{DD} supply to this pin.

EN_L4 (Pin 9/Pin 10): Enable LDO4 Input for LTC3676. Active high enables LDO4. A weak pull-down pulls EN_L4 low when left floating.

VTTR (Pin 9/Pin 10): DDR V_{REF} Output Pin for LTC3676-1. Buffered reference equal to one-half VDDQIN voltage on Pin 8.

EN_L3 (Pin 10/Pin 11): Enable LDO3 Input. Active high enables LDO3. A weak pull-down pulls EN_L3 low when left floating.

SW4 (Pin 11/Pin 14): Switch Pin for Step-Down Switching Regulator 4. Connect one side of step-down switching regulator 4 inductor to this pin.

DV_{DD} (Pin 12/Pin 15): Supply Voltage for I²C Serial Port. This pin sets the logic reference level of SCL and SDA I²C pins. DV_{DD} resets I²C registers to power-on state when driven to <1V. SCL and SDA logic levels are scaled to DV_{DD}. Connect a 0.1 μ F decoupling capacitor from this pin to ground.

SDA (Pin 13/Pin 16): Data Pin for the I²C Serial Port. The I²C logic levels are scaled with respect to DV_{DD}.

SCL (Pin 14/Pin 17): Clock Pin for the I²C Serial Port. The I²C logic levels are scaled with respect to DV_{DD}.

PV_{IN4} (Pin 15/Pin 18): Power Input for Step-Down Switching Regulator 4. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 10 μ F or greater ceramic capacitor.

PV_{IN3} (Pin 16/Pin 19): Power Input for Step-Down Switching Regulator 3. Tie this pin to the V_{IN} supply. This pin should be bypassed to ground with a 10 μ F or greater ceramic capacitor.

EN_B4 (Pin 17/Pin 20): Enable Step-Down Switching Regulator 4. Active high input enables step-down switching regulator 4. A weak pull-down pulls EN_B4 low when left floating.

EN_B3 (Pin 18/Pin 21): Enable Step-Down Switching Regulator 3. Active high input enables step-down switching regulator 3. A weak pull-down pulls EN_B3 low when left floating.

VSTB (Pin 19/Pin 22): Voltage Standby. When VSTB is low, the DAC registers are selected by command register bit DVbxA[5]. When VSTB is high, the DAC registers are forced to DVbxB registers. Tie VSTB to ground if unused.

SW3 (Pin 20/Pin 23): Switch Pin for Step-Down Switching Regulator 3. Connect one side of step-down switching regulator 3 inductor to this pin.

PWR_ON (Pin 21/Pin 26): External Power On. Handshaking pin to acknowledge successful power-on sequence. PWR_ON must be driven high within five seconds of WAKE going high to keep power on. PWR_ON can be

PIN FUNCTIONS

used to activate the WAKE output by driving high. Drive low to shut down WAKE.

FB_B3 (Pin 22/Pin 27): Feedback Input for Step-Down Switching Regulator 3. Set output voltage using resistor divider connected from the output of step-down switching regulator 3 to this pin to ground.

FB_B4 (Pin 23/Pin 28): Feedback Input for Step-Down Switching Regulator 4. Set output voltage using resistor divider connected from the output of step-down switching regulator 4 to this pin to ground.

FB_B1 (Pin 24/Pin 29): Feedback Input for Step-Down Switching Regulator 1. Set output voltage using resistor divider connected from the output of step-down switching regulator 1 to this pin to ground.

FB_B2 (Pin 25/Pin 30): Feedback Input for Step-Down Switching Regulator 2. Set output voltage using resistor divider connected from the output of step-down switching regulator 2 to this pin to ground.

FB_L1 (Pin 26/Pin 31): Feedback Input for LDO1. Set output voltage using a resistor divider connected from LDO1 to this pin to ground.

V_{IN} (Pin 27/Pin 32): Supply Voltage Input. This pin should be bypassed to ground with a 1 μ F or greater ceramic capacitor. All switching regulator PV_{IN} supplies should be tied to V_{IN}.

LDO1 (Pin 28/Pin 33): Always On LDO1 Output. This pin provides an always-on supply voltage useful for light loads such as a watchdog microprocessor or a real time clock. Connect a 1 μ F capacitor from LDO1 to ground.

$\overline{\text{ON}}$ (Pin 29/Pin 34): Pushbutton Input. A weak internal pull-up forces $\overline{\text{ON}}$ high when left floating. A normally open pushbutton is connected from $\overline{\text{ON}}$ to ground forcing a low state when pushed.

EN_L2 (Pin 30/Pin 35): Enable LDO2 Input. Active high enables LDO2. A weak pull-down pulls EN_L2 low when left floating.

SW2 (Pin 31/Pin 38): Switch Pin for Step-Down Switching Regulator 2. Connect one side of step-down switching regulator 2 inductor to this pin.

$\overline{\text{IRQ}}$ (Pin 32/Pin 39): Interrupt Request Output. Open-drain driver is pulled low for power good, undervoltage, and overtemperature warning and fault conditions. Clear $\overline{\text{IRQ}}$ by writing to the I²C CLIRQ command register.

WAKE (Pin 33/Pin 40): System Wake Up. Open-drain driver output releases high when signaled by pushbutton activation or PWR_ON input. It may be used to initiate a pin-strapped power-up sequence by connecting to a regulator enable pin.

EN_B2 (Pin 34/Pin 41): Enable Step-Down Switching Regulator 2. Active high input enables step-down switching regulator 2. A weak pull-down pulls EN_B2 low when left floating.

PV_{IN2} (Pin 35/Pin 42): Power Input for Step-Down Switching Regulator 2. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 10 μ F or greater ceramic capacitor.

PV_{IN1} (Pin 36/Pin 43): Power Input for Step-Down Switching Regulator 1. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 10 μ F or greater ceramic capacitor.

EN_B1 (Pin 37/Pin 44): Enable Step-Down Switching Regulator 1. Active high enables step-down switching regulator 1. The LTC3676-1 EN_B1 pin enables both VTTR output and switching regulator 1. A weak pull-down pulls EN_B1 low when left floating.

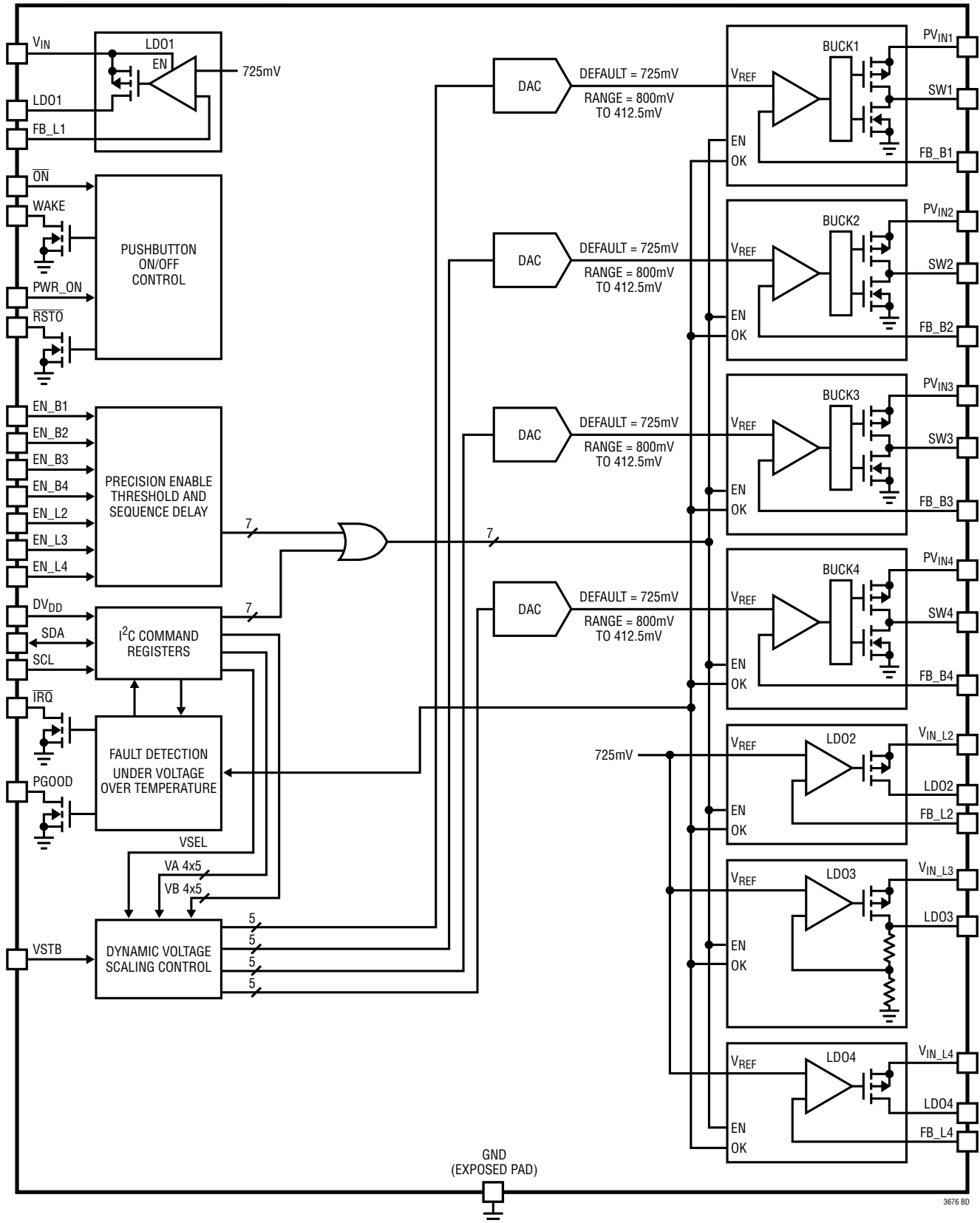
$\overline{\text{RSTO}}$ (Pin 38/Pin 45): Reset Output. Open-drain output pulls low when the always-on regulator LDO1 is below regulation or during a hard reset initiated by a pushbutton input or command registers.

PGOOD (Pin 39/Pin 46): Power Good Output. Open-drain output pulls low when any enabled regulator falls below power good threshold or during dynamic voltage slew unless disabled in command register. Pulls low when all regulators are disabled.

SW1 (Pin 40/Pin 47): Switch Pin for Step-Down Switching Regulator 1. Connect one side of step-down switching regulator 1 inductor to this pin.

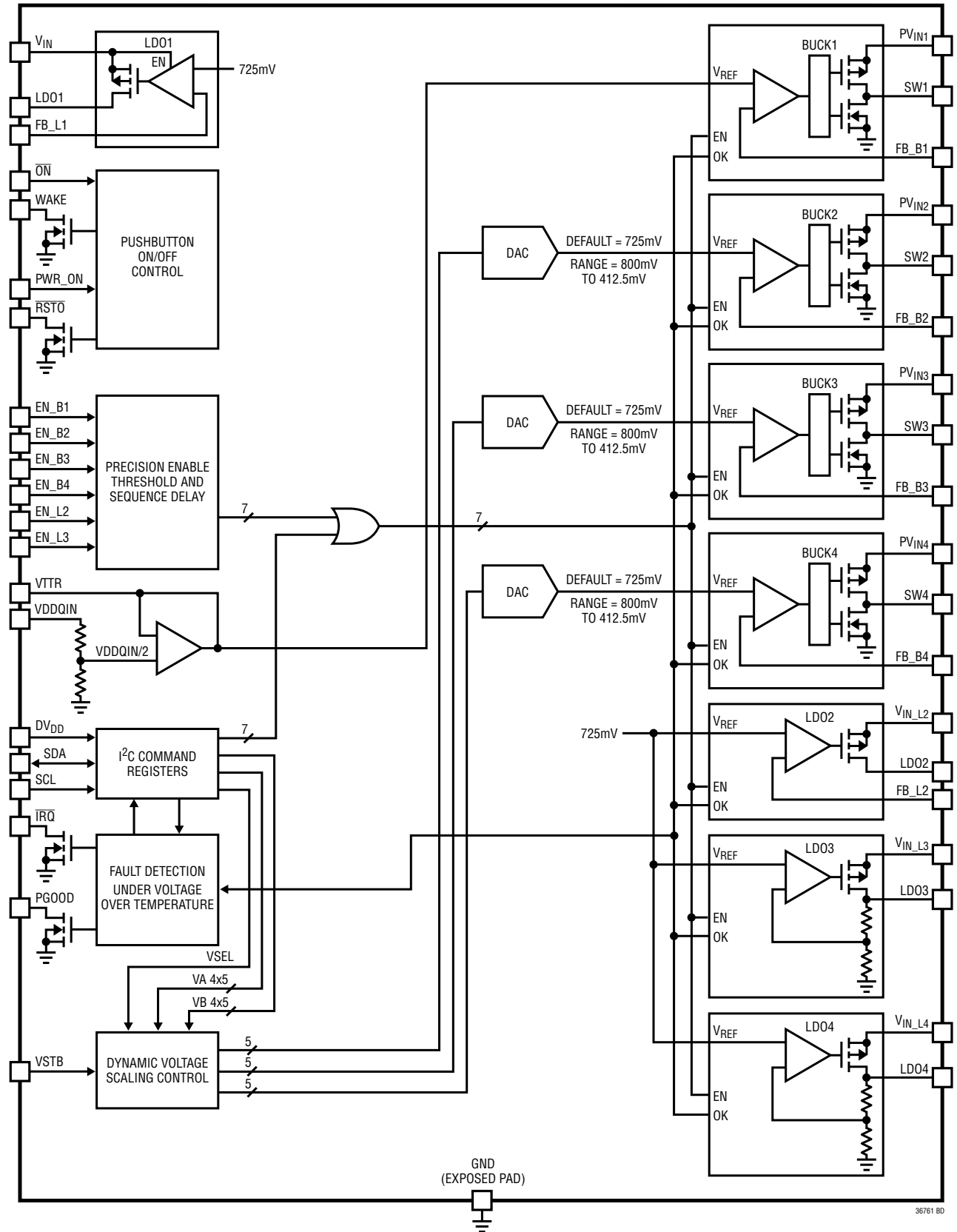
GND (Exposed Pad Pin 41/Pin 49): Ground. The exposed pad must be connected to a continuous ground plane of the printed circuit board by multiple interconnect vias directly under the LTC3676 to maximize electrical and thermal conduction.

BLOCK DIAGRAM—LTC3676



3676 BD

BLOCK DIAGRAM—LTC3676-1



36761 BD

OPERATION

INTRODUCTION

The LTC3676 is a complete power management solution for portable microprocessors and peripheral devices. It generates a total of eight voltage rails for supplying power to the processor core, DDR memory, I/O, always-on real-time clock and HDD functions. Supplying the voltage rails are an always-on low quiescent current 25mA LDO, two 2.5A step-down regulators, two 1.5A step-down regulators, and three 300mA low dropout regulators. Supporting the multiple regulators is a highly configurable power-on sequencing capability, dynamic voltage scaling DAC output voltage control, a pushbutton interface controller, control via an I²C interface, and extensive status and interrupt outputs.

The LTC3676-1 supports DDR memory applications by replacing the LTC3676 LDO4 feedback and enable pins with VDDQIN and VTTR pins. The DDR V_{DD} supply is connected to the LTC3676-1 VDDQIN pin. A buffered DDR termination voltage equal to one half the voltage on VDDQIN is output on VTTR. The VTTR voltage is connected internally on the LTC3676-1 to the reference side of the Buck1 error amplifier. When Buck1 is configured with a gain of one, its output can be used as at DDR termination supply. Table 1 shows the functional differences between the LTC3676 and LTC3676-1.

Table 1. Functional Differences LTC3676 vs LTC3676-1

| | LTC3676 | LTC3676-1 |
|---------------------------------|--|--|
| Buck1 Default Frequency | 2.25MHz | 1.125MHz |
| Buck1 Default Mode | Pulse-Skipping | Forced Continuous |
| Buck1 Output | External Resistor Divider. Slewing DAC Reference | External Unity Gain. VTTR Reference |
| LDO4 Enable | EN_L4 Pin or I ² C | I ² C |
| LDO4 Output | External Resistor Divider. 725mV Reference | I ² C Select 1 of 4 Fixed Outputs |
| FB_L4 Pin | External Resistor Divider | — |
| EN_L4 Pin | Enable LDO4. | — |
| VDDQIN Pin | — | Connect to DDR Memory Supply |
| VTTR Pin | — | Buffered Output Equals One-Half VDDQIN |
| I ² C Device Address | Write = 0x78 Read = 0x79 | Write = 0x7A Read = 0x7B |

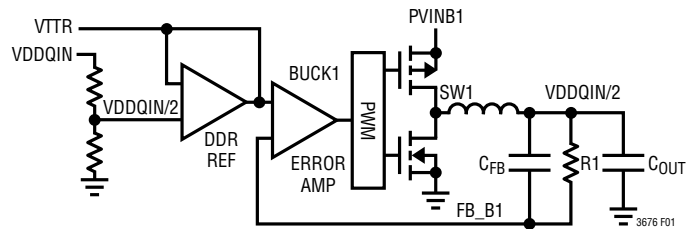


Figure 1. V_{TT} Buck Regulator and VTTR Reference Block Diagram

Always-On 25mA Low Dropout Regulator

The LTC3676 includes a low quiescent current low dropout regulator that remains powered whenever a valid supply is present on V_{IN}. The always-on LDO1 remains active until V_{IN} drops below 2.0V (typical). This is below the 2.5V undervoltage threshold in effect for the rest of the LTC3676 circuits. The always-on LDO is used to provide power to a standby microcontroller, real-time clock, or other keep-alive circuits. The LDO is guaranteed to support a 25mA load. A 1μF low impedance ceramic bypass capacitor from LDO1 to GND is required for compensation. A power good monitor pulls \overline{RSTO} low whenever LDO1 is 8% below its regulation target. LDO1 has current limit circuitry to protect from short circuit and overloading. The output voltage of LDO1 is set with a resistor divider connected from LDO1 output pin to the feedback pin FB_L1, as shown in Figure 2. The output voltage is calculated using the following formula:

$$V_{LDO1} = 725 \cdot \left(1 + \frac{R1}{R2} \right) \text{ (mV)}$$

300mA Low Dropout Regulators

Three LDO regulators on the LTC3676 will each deliver up to 300mA output. Each LDO regulator has a separate input supply to help manage power loss in the LDO output devices. The LDO regulators are enabled by pin input or I²C command register. When disabled, the regulator outputs are pulled to ground through a 625Ω resistor. A low ESR 1μF ceramic capacitor should be tied from the LDO output to ground. The 300mA LDO regulators have current limit control circuits. The LDO input voltages, V_{IN_L2}, V_{IN_L3}, and V_{IN_L4} must be at a potential of V_{IN} or less.

The LDO regulator I²C command register controls are shown in Table 2 and Table 3.

OPERATION

LTC3676 Resistor Programmable LDO2 and LDO4

LDO2 and LDO4 output voltages are programmed by resistor dividers tied from the LDO output pin to the feedback pin as shown in Figure 2. The output voltage is calculated using the following formula:

$$V_{LDO} = 725 \cdot \left(1 + \frac{R1}{R2} \right) \text{ (mV)}$$

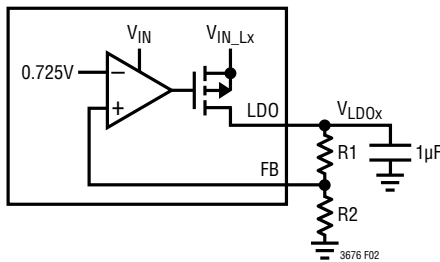


Figure 2. LDO1, LDO2 and LDO4 Application Circuit

Fixed Output LDO3

Regulator LDO3 has a fixed voltage output of 1.8V.

Table 2. LDO2 and LDO3 Control Command Register Settings

| COMMAND REGISTER[BIT] | VALUE | SETTING |
|-----------------------|---------|---|
| LDOA[0] | 0* 1 | Do Not Keep Alive LDO2 in Standby Keep Alive LDO2 in Standby |
| LDOA[1] | 0* 1 | Enable LDO2 at Any Output Voltage Enable LDO2 Only if Output Voltage is <300mV |
| LDOA[2] | 0* 1 | LDO2 Disabled if EN_L2 is Low LDO2 Enable |
| LDOA[3] | 0* 1 | Do Not Keep Alive LDO3 in Standby Keep Alive LDO3 in Standby |
| LDOA[4] | 0* 1 | Enable LDO3 at Any Output Voltage Enable LDO3 Only if Output Voltage is <300mV |
| LDOA[5] | 0* 1 | LDO3 Disabled if EN_L3 is Low LDO3 Enabled |

*denotes default power-on value.

LDO4 Operation LTC3676-1

LDO4 on the LTC3676-1 has neither enable nor feedback pins. There are four LDO4 output voltages selectable by command register bits LDOB[4:3]. The power-on default

output is 1.2V with selectable outputs of 2.5V, 2.8V, and 3.0V. LDO4 is enabled only through the command register bit LDOB[2].

LDO4 Command Register Controls

Table 3. LDO4 Control Command Register Settings

| COMMAND REGISTER[BIT] | VALUE | SETTING |
|-----------------------|---------|---|
| LDOB[0] | 0* 1 | Do Not Keep Alive LDO4 in Standby Keep Alive LDO4 in Standby |
| LDOB[1] | 0* 1 | Enable LDO4 at Any Output Voltage Enable LDO4 Only if Output Voltage is <300mV |
| LDOB[2] (LTC3676) | 0* 1 | LDO4 Disabled if EN_L4 is Low LDO4 Enabled |
| LDOB[2] (LTC3676-1) | 0* 1 | LDO4 Disabled LDO4 Enabled |
| LDOB[4:3] (LTC3676-1) | 00* | LDO4 Output = 1.2V |
| LDOB[4:3] (LTC3676-1) | 01 | LDO4 Output = 2.5V |
| LDOB[4:3] (LTC3676-1) | 10 | LDO4 Output = 2.8V |
| LDOB[4:3] (LTC3676-1) | 11 | LDO4 Output = 3V |

*denotes default power-on value.

STEP-DOWN SWITCHING REGULATORS

The LTC3676 contains four buck regulators. Two of the buck regulators are capable of delivering up to 2.5A load current and the other two can deliver up to 1.5A each. The regulators have forward and reverse current limiting, soft-start, and switch slew rate control for lower radiated EMI.

The LTC3676 buck regulators are capable of 100% duty cycle, or dropout, regulation. When in dropout the regulator output voltage is equal to PV_{IN} minus the load current times $R_{DS(ON)}$ of the converters PMOS device and inductor DCR.

Each buck regulator is enabled using its enable pin or I²C command register control. Operating modes, start-up option, reference voltage, and switch slew rate are controlled using the I²C port.

The buck converter I²C command register controls are shown in Table 4, Table 5, Table 6, and Table 7.

OPERATION

Operating Modes

The buck regulators operate in either pulse-skipping, Burst Mode operation, or forced continuous mode. In pulse-skipping the regulator will skip pulses at light loads but operate at constant frequency at higher load. In Burst Mode the regulator operates in Burst Mode at light loads and in constant frequency PWM mode at higher load. In forced continuous setting the inductor current is allowed to be less than zero over the full range of duty cycles. In forced continuous operation the buck regulator has the ability to sink output current. Because the regulator is switching every cycle regardless of output load, forced continuous mode results in the least output voltage ripple at light load.

Output Voltage Programming

Each of the step-down converters uses a dynamically slewing DAC for its reference. The output voltage of the DAC reference is selectable using a 5-bit I²C command register. The output voltage is set by using a resistor divider connected from the step-down switching regulator output to its feedback pin as shown in Figure 3. The output voltage is calculated using the following formula:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \cdot (DVBx \cdot 12.5 + 412.5) \text{ (mV)}$$

DVBx is the decimal value of the 5-bit binary number in the I²C command registers. The default DAC input code is 11001 (25 in decimal) which corresponds to a reference

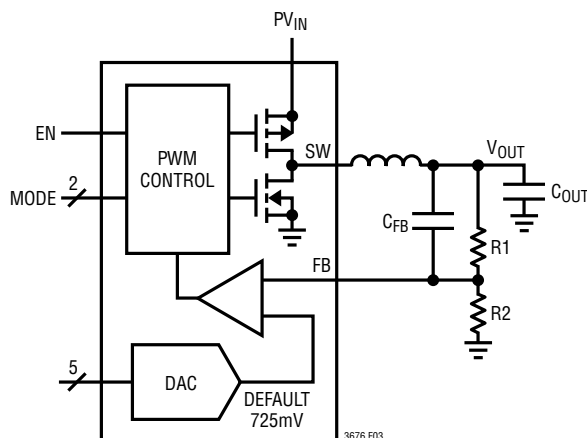


Figure 3. Step-Down Switching Regulator Application Circuit

voltage of 725mV. Typical values for R1 are in the range of 40k to 1M. Capacitor C_{FB} cancels the pole created by the feedback resistors and the input capacitance on the FB pin and helps to improve load step transient response. A value of 10pF is recommended.

Inductor Selection

The choice of step-down switching regulator inductor influences the efficiency and output voltage ripple of the converter. A larger inductor improves efficiency since the peak current is closer to the average output current. Larger inductors generally have higher series resistance that counters the efficiency advantage of reduced peak current.

Inductor ripple current is a function of switching frequency, inductance, V_{IN}, and V_{OUT} as shown in this equation:

$$\Delta I_L = \frac{1}{f \cdot L} \cdot V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A good starting design point is to use an inductor that gives ripple equal to 30% of the maximum output current. Select an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure the inductor does not saturate.

Input and Output Capacitor Selection

Low ESR ceramic capacitors should be used at both the output and input supply of the switching regulators. Only X5R or X7R ceramic capacitors should be used since they have better temperature and voltage stability than other ceramic types.

Operating Frequency

The switching frequency of each of the LTC3676 switching regulators may be set using the I²C command registers. The default switching frequency is 2.25MHz and the selectable frequency is 1.125MHz. Operation at lower frequency improves efficiency by reducing internal gate charge and switching losses at the expense of a larger inductor.

The lowest duty cycle of the step-down converter is determined by minimum on-time. Minimum on-time is the shortest time duration that the converter can turn its top PMOS on and off again. The time is the sum of gate charge

OPERATION

time plus internal delays of the peak current sense and PWM control. If the converters duty cycle will be 20% or less at 2.25MHz it is recommended to use the 1.125MHz setting to avoid minimum duty cycle. If the duty cycle falls below the minimum on-time of the converter, the output voltage ripple will increase as the converter skips cycles.

The default setting for the LTC3676-1 Buck1 switching frequency is 1.125MHz to ensure minimum on time effects are avoided at DDR termination reference voltages.

Phase Selection

To reduce the cycle by cycle peak current drawn by the switching regulators, the clock phase at which each of the LTC3676 buck's PMOS switch turns on can be set using I²C command register settings.

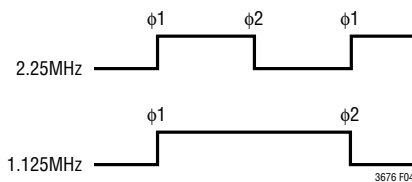


Figure 4. Phase Settings Full- and Half-Speed Buck Clock

Switch Slew Rate Control

To help reduce EMI the switch rise time of each buck regulator is slew limited by default. A faster setting is selectable using the I²C buck command registers. The faster setting will improve efficiency if limited edge rate is not required.

Soft-Start

To reduce inrush current at start-up each buck regulator soft starts when enabled. When enabled the internal reference voltage is ramped from ground to the level of the slewing DAC output at a rate of 0.8V/ms. During soft-start the converter is forced to pulse-skipping mode regardless of command register mode settings.

Table 4. Buck1 Control Command Register

| COMMAND REGISTER[BIT] | VALUE | SETTING |
|-----------------------|-------|---|
| BUCK1[0] | 0* | Switch Slew Rate Normal |
| | 1 | Switch Slew Rate Fast |
| BUCK1[1] | 0* | Do Not Keep Enabled in Device Standby |
| | 1 | Keep Enabled in Device Standby |
| BUCK1[2] (LTC3676) | 0* | Switching Frequency 2.25MHz |
| | 1 | Switching Frequency 1.125MHz |
| BUCK1[2] (LTC3676-1) | 0* | Switching Frequency 1.125MHz |
| | 1 | Switching Frequency 2.25MHz |
| BUCK1[3] | 0* | Clock Phase 1 |
| | 1 | Clock Phase 2 |
| BUCK1[4] | 0* | Enable at Any Output Voltage |
| | 1 | Enable Only if Output Voltage Is <300mV |
| BUCK1[6:5] | 00* | Pulse-Skipping Mode |
| | 01 | Burst Mode Operation |
| | 10 | Forced Continuous Mode |
| BUCK1[7] | 0* | Buck1 Disabled if EN_B1 Pin Is Low |
| | 1 | Buck1 Enabled |

*denotes default power on-value.

Table 5. Buck2 Control Command Register

| COMMAND REGISTER[BIT] | VALUE | SETTING |
|-----------------------|-------|---|
| BUCK2[0] | 0* | Switch Slew Rate Normal |
| | 1 | Switch Slew Rate Fast |
| BUCK2[1] | 0* | Do Not Keep Enabled in Device Standby |
| | 1 | Keep Enabled in Device Standby |
| BUCK2[2] | 0* | Switching Frequency 2.25MHz |
| | 1 | Switching Frequency 1.125MHz |
| BUCK2[3] | 0* | Clock Phase 1 |
| | 1 | Clock Phase 2 |
| BUCK2[4] | 0* | Enable at Any Output Voltage |
| | 1 | Enable Only if Output Voltage Is <300mV |
| BUCK2[6:5] | 00* | Pulse-Skipping Mode |
| | 01 | Burst Mode Operation |
| | 10 | Forced Continuous Mode |
| BUCK2[7] | 0* | Buck2 Disabled if EN_B2 Pin Is Low |
| | 1 | Buck2 Enabled |

*denotes default power-on value.

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Table 6. Buck3 Control Command Register

| COMMAND REGISTER[BIT] | VALUE | SETTING |
|-----------------------|-----------------|---|
| BUCK3[0] | 0* 1 | Switch Slew Rate Normal Switch Slew Rate Fast |
| BUCK3[1] | 0* 1 | Do Not Keep Enabled in Device Standby Keep Enabled in Device Standby |
| BUCK3[2] | 0* 1 | Switching Frequency 2.25MHz Switching Frequency 1.125MHz |
| BUCK3[3] | 0* 1 | Clock Phase 1 Clock Phase 2 |
| BUCK3[4] | 0* 1 | Enable at Any Output Voltage Enable Only if Output Voltage Is <300mV |
| BUCK3[6:5] | 00* 01 10 | Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode |
| BUCK3[7] | 0* 1 | Buck3 Disabled if EN_B3 Pin Is Low Buck3 Enabled |

*denotes default power-on value.

Table 7. Buck4 Control Command Register

| COMMAND REGISTER[BIT] | VALUE | SETTING |
|-----------------------|-----------------|---|
| BUCK4[0] | 0* 1 | Switch Slew Rate Normal Switch Slew Rate Fast |
| BUCK4[1] | 0* 1 | Do Not Keep Enabled in Device Standby Keep Enabled in Device Standby |
| BUCK4[2] | 0* 1 | Switching Frequency 2.25MHz Switching Frequency 1.125MHz |
| BUCK4[3] | 0* 1 | Clock Phase 1 Clock Phase 2 |
| BUCK4[4] | 0* 1 | Enable at Any Output Voltage Enable Only if Output Voltage Is <300mV |
| BUCK4[6:5] | 00* 01 10 | Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode |
| BUCK4[7] | 0* 1 | Buck4 Disabled if EN_B4 Pin Is Low Buck4 Enabled |

*denotes default power-on value.

SLEWING DAC REFERENCE OPERATION

Each LTC3676 step-down switching regulators error amplifier reference voltage is supplied by a 5-bit DAC with an output voltage range of 412.5mV to 800mV in 12.5mV steps. One of two 5-bit codes stored in I²C command registers is selected for input to the DAC. When a change in code is detected by the DAC control circuits, the output of the DAC is slewed at 3.5mV/μs to the new value.

Dynamic Voltage Scaling

Table 8 shows the command registers used to control dynamic voltage scaling (DVS) of the step-down switching regulators input reference DAC. The command register bits DVB1A[4:0] and DVB1B[4:0] store two 5-bit inputs to the DAC reference for Buck1. The bit stored in command register DVB1A[5] selects either the 5 bits stored in DVB1A[4:0] or DVB1B[4:0] DAC as input to the DAC reference. Buck2, Buck3, and Buck4 operate the same way using their assigned “A” and “B” command registers shown in Table 8. When the DAC detects a change in its input code it automatically slews to the new value at a rate of 3.5mV/μs. A DVS can be initiated using the I²C select bit or using the VSTB pin.

The LTC3676 VSTB pin HIGH selects the 5 bits stored in all four DVbX “B” registers. This facilitates a simultaneous DAC slew between the values in the “A” registers and the values in the “B” registers. The VSTB pin is logically ORed with the I²C command register bit. If the I²C select bit is already set high, the “B” registers are already selected and VSTB will have no effect. If no change in output is desired using the VSTB pin, set the value in the “A” register equal to the value in the “B”.

Command register bits DVB1B[5], DVB2B[5], DVB3B[5], and DVB4B[5] control whether the PGOOD status pin is pulled low while the DAC output is slewing. The default command register setting is to pull the PGOOD pin low during DAC slew. As shown in Figure 5, during the DVS, PGOOD will be held low for just the duration of the DVS and the PGSTAT register is not affected.

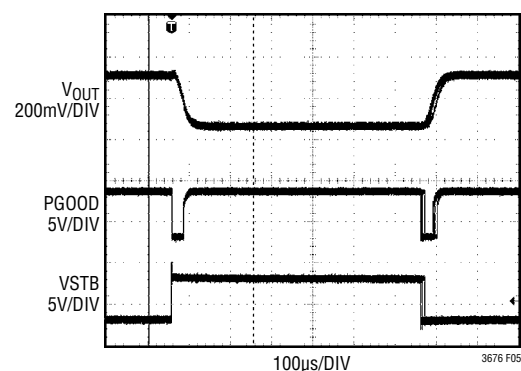


Figure 5. Dynamic Voltage Scaling

OPERATION

Table 8. Buck1, Buck2, Buck3, and Buck4 Slewing DAC Control Command Registers

| COMMAND REGISTER[BIT] | VALUE | SETTING |
|-----------------------|-------|---------------------------------|
| DVB1A[4:0] | bbbb | Buck1 Reference DAC Input A |
| DVB1A[5] | 0* | Select DVB1A[4:0] |
| | 1 | Select DVB1B[4:0] |
| DVB1B[4:0] | bbbb | Buck1 Reference DAC Input B |
| DVB1B[5] | 0* | Pull PGOOD Low Slewing Buck1 |
| | 1 | Do Not Pull PGOOD Slewing Buck1 |
| DVB2A[4:0] | bbbb | Buck2 Reference DAC Input A |
| DVB2A[5] | 0* | Select DVB2A[4:0] |
| | 1 | Select DVB2B[4:0] |
| DVB2B[4:0] | bbbb | Buck2 Reference DAC Input B |
| DVB2B[5] | 0* | Pull PGOOD Low Slewing Buck2 |
| | 1 | Do Not Pull PGOOD Slewing Buck2 |
| DVB3A[4:0] | bbbb | Buck3 Reference DAC Input A |
| DVB3A[5] | 0* | Select DVB3A[4:0] |
| | 1 | Select DVB3B[4:0] |
| DVB3B[4:0] | bbbb | Buck3 Reference DAC Input B |
| DVB3B[5] | 0* | Pull PGOOD Low Slewing Buck3 |
| | 1 | Do Not Pull PGOOD Slewing Buck3 |
| DVB4A[4:0] | bbbb | Buck4 Reference DAC Input A |
| DVB4A[5] | 0* | Select DVB4A[4:0] |
| | 1 | Select DVB4B[4:0] |
| DVB4B[4:0] | bbbb | Buck4 Reference DAC Input B |
| DVB4B[5] | 0* | Pull PGOOD Low Slewing Buck4 |
| | 1 | Do Not Pull PGOOD Slewing Buck4 |

*denotes default power-on value.

PUSHBUTTON OPERATION

Operating Mode State Diagram

Figure 6 shows the state diagram of the LTC3676 enable and sequence controller. First application of power to the V_{IN} pin brings the controller to the power-on reset/hard reset (POR/HRST) state. In this state the I^2C command registers have been set to their default values, only LDO1 is operating, and the device is waiting for pushbutton or PWR_ON inputs. Regulator enable pins and command register enable bits are ignored in the POR/HRST state. In the POR/HRST state V_{IN} draws typically 12 μ A.

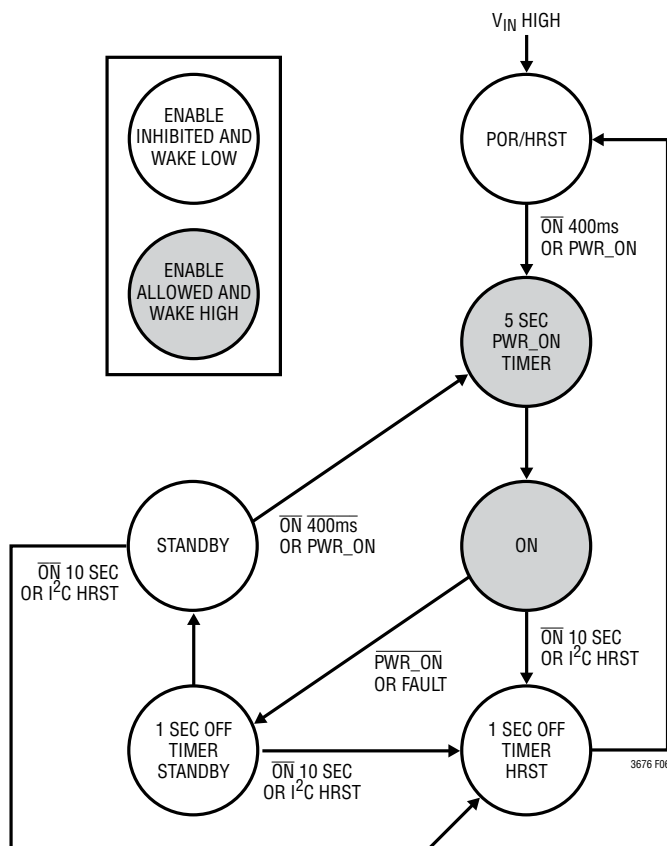


Figure 6. LTC3676 Operating Mode State Diagram

Power Up Using Pushbutton

When the \overline{ON} pin is held low for 400ms the WAKE pin is pulled high, enable pins are recognized, and the five second PWR_ON timer is started. If in the ON state and PWR_ON is low or a fault is detected, then WAKE is brought low and after a 1 second power-down time, the STANDBY state is entered. In STANDBY, the enable bits in the command registers are cleared and enable pins are ignored. Table 9 shows the control of command registers, enables, and WAKE at each state.

The 5 second power-on state is intended for the system to detect that power rails are correct and either drive PWR_ON pin high or set command register bit CNTRL[7] high to keep the rails active. If there were a system level problem

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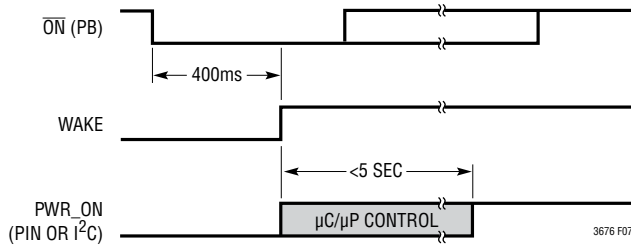


Figure 7. Power Up Using Pushbutton

keeping the processor from driving PWR_ON, then the LTC3676 will pull WAKE low, shut off all regulators, and enter the STANDBY state. The STANDBY state is also a low power, 12 μ A (typical) state.

Table 9. Register, Enable, WAKE Control During Operating Mode State Control

| STATE | REGISTERS | ENABLES | WAKE |
|-------------------------|--|---------------|------|
| POR/HRST DEFAULT | R/W | Inhibited | LOW |
| 5 SEC PWR_ON TIMER | R/W | Allowed | HIGH |
| ON | R/W | Allowed | HIGH |
| 1 SEC OFF TIMER HRST | Set to POR Defaults | Sequence Down | LOW |
| 1 SEC OFF TIMER STANDBY | I ² C Enable and SW Mode Bits Cleared | Sequence Down | LOW |
| STANDBY | R/W | Inhibited | LOW |

Power Down Using Pushbutton

When in the ON state, the system controller is responsible for deciding what action to take when a pushbutton event occurs. By monitoring the $\overline{\text{IRQ}}$ status pin and IRQSTAT[0]

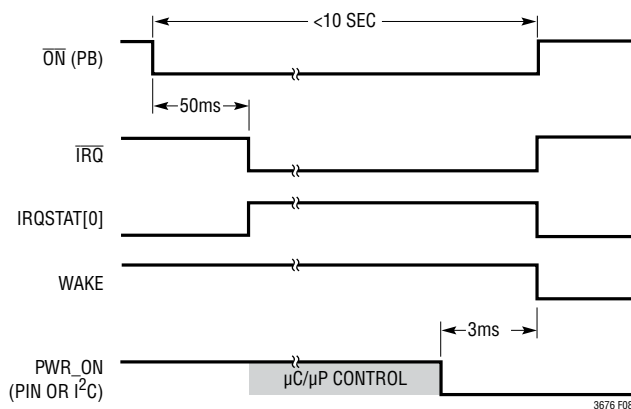


Figure 8. Power-Down Using Pushbutton

status register bit, the controller can detect a pushbutton request. If a power-down into standby state is desired then the controller should drive PWR_ON low and set command register bit CNTRL[7] low.

Button Status Indication

When a pushbutton pulls $\overline{\text{ON}}$ low for 50ms in the ON state, $\overline{\text{IRQ}}$ is pulled low and the PB status bit in the IRQSTAT[0] status register is set. $\overline{\text{IRQ}}$ and the IRQSTAT status bit are active while $\overline{\text{ON}}$ is low or for a minimum of 50ms.

Power Up and Down with PWR_ON

The PWR_ON pin is an alternative way to power up the LTC3676 instead of using the $\overline{\text{ON}}$ pin. When PWR_ON is driven high or command register CNTRL[7] is set high, WAKE is pulled HIGH and the LTC3676 passes through the 5 second PWR_ON timer to the ON state. Figure 9 shows PWR_ON and WAKE timing. WAKE stays high for a minimum of 5 seconds.

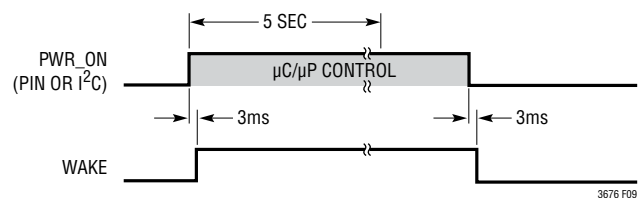


Figure 9. Power Up and Down with PWR_ON

POWER ON SEQUENCING

Enable Pin Operation

The LTC3676 enable pins facilitate pin-strapping output rails to enable pins to up-sequence the LTC3676 regulators in any order. Figure 10 shows an example of pin-strapped sequence connections.

The enable pins normally have a 0.75V (typical) input voltage threshold. If any enable is driven high, the remaining enable input thresholds switches to an accurate 400mV threshold. To ensure separation of the sequenced rails, there is a built-in 450 μ s delay from the enable pin threshold crossing to the internal enable of the regulator. Figure 11 shows the start-up timing of the example shown in Figure 10.

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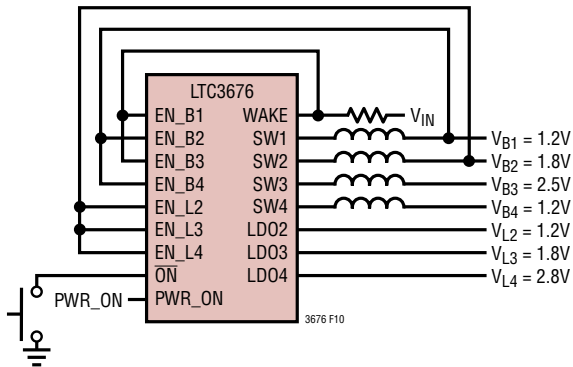


Figure 10. Pin-Strapped Power-On Sequence Application

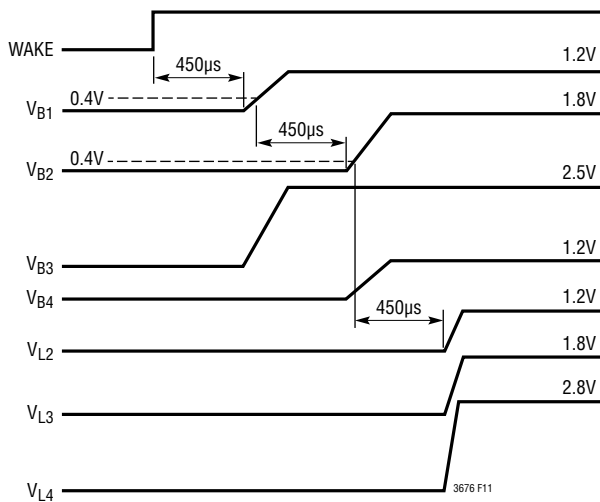


Figure 11. Pin-Strapped Power-On Sequence

Software Control Mode

Once a power-up sequence is completed, each regulator may be enabled and disabled individually by the system as needed for power management requirements by using the command register bit CNTRL[5]. When CNTRL[5] is set high the regulators ignore the state of their enable pins and respond only to I²C command register bit settings. The software control mode bit is reset in the one second standby and hard reset timer states so a pin strapped sequence begins at the next LTC3676 power on.

Keep Alive Operation

Each regulator has a dedicated command register keep alive bit that, when set, forces a regulator to be enabled regardless of the enable pins, command register enable

bits, or the operating state of the LTC3676. A hard reset or fault shutdown resets the keep alive bits.

POWER OFF SEQUENCING

Sequence down command registers SQD1 and SQD2 are used to set the time, relative to WAKE falling, that a regulator is disabled either by lowering PWR_ON, or a fault induced shutdown. Table 10 shows register settings for SQD1 and SQD2.

Table 10. Sequence Down Control Command Register Settings

| COMMAND REGISTER[BIT] | VALUE | SETTING |
|-----------------------|-------|---------------------------------------|
| SQD1[1:0] | 00* | Disable Buck1 at Falling WAKE |
| | 01 | Disable Buck1 at Falling WAKE + 100ms |
| | 10 | Disable Buck1 at Falling WAKE + 200ms |
| | 11 | Disable Buck1 at Falling WAKE + 300ms |
| SQD1[3:2] | 00* | Disable Buck2 at Falling WAKE |
| | 01 | Disable Buck2 at Falling WAKE + 100ms |
| | 10 | Disable Buck2 at Falling WAKE + 200ms |
| | 11 | Disable Buck2 at Falling WAKE + 300ms |
| SQD1[5:4] | 00* | Disable Buck3 at Falling WAKE |
| | 01 | Disable Buck3 at Falling WAKE + 100ms |
| | 10 | Disable Buck3 at Falling WAKE + 200ms |
| | 11 | Disable Buck3 at Falling WAKE + 300ms |
| SQD1[7:6] | 00* | Disable Buck4 at Falling WAKE |
| | 01 | Disable Buck4 at Falling WAKE + 100ms |
| | 10 | Disable Buck4 at Falling WAKE + 200ms |
| | 11 | Disable Buck4 at Falling WAKE + 300ms |
| SQD2[1:0] | 00* | Disable LDO2 at Falling WAKE |
| | 01 | Disable LDO2 at Falling WAKE + 100ms |
| | 10 | Disable LDO2 at Falling WAKE + 200ms |
| | 11 | Disable LDO2 at Falling WAKE + 300ms |
| SQD2[3:2] | 00* | Disable LDO3 at Falling WAKE |
| | 01 | Disable LDO3 at Falling WAKE + 100ms |
| | 10 | Disable LDO3 at Falling WAKE + 200ms |
| | 11 | Disable LDO3 at Falling WAKE + 300ms |
| SQD2[5:4] | 00* | Disable LDO4 at Falling WAKE |
| | 01 | Disable LDO4 at Falling WAKE + 100ms |
| | 10 | Disable LDO4 at Falling WAKE + 200ms |
| | 11 | Disable LDO3 at Falling WAKE + 300ms |

*denotes default power-on value.

Figure 12 shows an example of a shutdown sequence. In this example, the bits in command registers SQD1 and SQD2 are set so that LDO2, LDO3, and LDO4 shut off at the same time as WAKE. Buck2 and Buck4 shut off 100ms after WAKE. Buck3 shuts off 200ms after wake and Buck1 shuts off 300ms after WAKE.

OPERATION

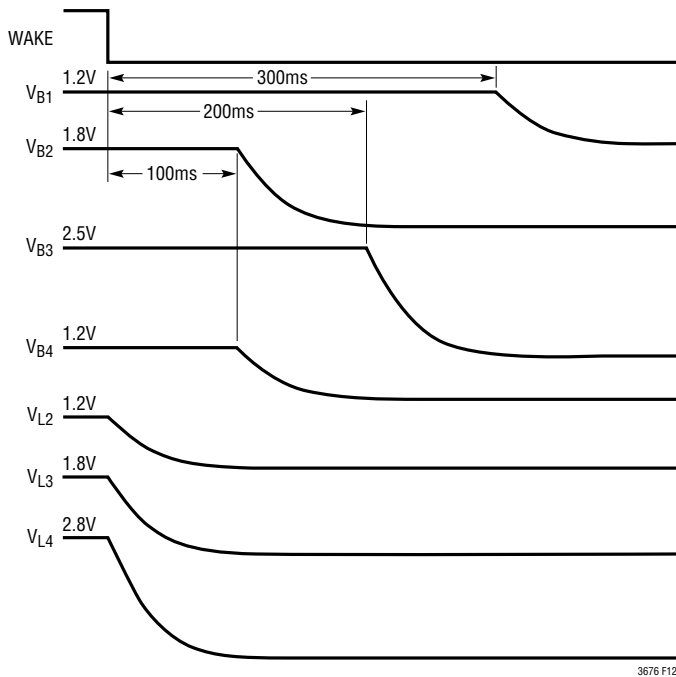


Figure 12. Power-Down Sequence

FAULT DETECTION AND REPORTING

The LTC3676 has fault detection circuits that monitor for V_{IN} undervoltage, die overtemperature, and regulator output undervoltage. Status of the fault detect circuits is indicated by the \overline{IRQ} and PGOOD pins and the IRQSTAT and PGSTAT status registers.

V_{IN} Undervoltage

The undervoltage (UV) circuit monitors the input supply voltage, V_{IN} , and when the voltage falls below 2.45V creates a FAULT condition that forces the LTC3676 into the standby state. The LTC3676 also provides a (UV) warning that is triggered at user programmable V_{IN} voltages as shown in Table 11.

The V_{IN} undervoltage (2.65V Max) defines the voltage at which V_{IN} rising undervoltage fault is detected. The LTC3676 will respond to PWR_ON and regulator enable pins when V_{IN} is less the V_{IN} undervoltage fault rising threshold at initial application of V_{IN} . An internal timer will inhibit all enables if V_{IN} does not cross the rising fault threshold within 5 seconds. PWR_ON and enables should be asserted only when the application has applied V_{IN} greater than the minimum V_{IN} input of 2.7V. A power

good signal from a V_{IN} pre regulator or voltage divider from V_{IN} to the 400mV (typ) PWR_ON input threshold may be used to ensure V_{IN} is above 2.7V.

Table 11. Undervoltage Warning Threshold Command Register Settings

| COMMAND REGISTER[BIT] | VALUE | FALLING V_{IN} THRESHOLD |
|-----------------------|-------|----------------------------|
| CNTRL[4:2] | 000* | 2.7V |
| | 001 | 2.8V |
| | 010 | 2.9V |
| | 011 | 3.0V |
| | 100 | 3.1V |
| | 101 | 3.2V |
| | 110 | 3.3V |
| | 111 | 3.4V |

*denotes default power-on value.

Overtemperature

To prevent thermal damage the LTC3676 incorporates an overtemperature (OT) circuit. When the die temperature reaches 155°C the OT circuits create a FAULT condition that forces the LTC3676 into standby. When the OT circuit detects the temperature falls below 140°C the FAULT condition is cleared. The LTC3676 also has an OT warning circuit that indicates the die temperature is approaching the OT fault threshold. The OT warning threshold is user programmable as shown in Table 12.

Table 12. Overtemperature Warning Threshold Command Register Settings

| COMMAND REGISTER[BIT] | VALUE | OT WARNING THRESHOLD |
|-----------------------|-------|----------------------|
| CNTRL[1:0] | 00* | 10°C Below OT Fault |
| | 01 | 20°C Below OT Fault |
| | 10 | 30°C Below OT Fault |
| | 11 | 40°C Below OT Fault |

*denotes default power-on value.

PGOOD Status Pin

The PGOOD open-drain status pin is pulled low when all regulators are disabled. PGOOD is released when all enabled regulator outputs are above 94% of programmed value. When any enabled regulator output falls below 92% of its programmed value for longer than 50 μ s the PGOOD pin is pulled low. The 50 μ s transient filter on PGOOD prevents PGOOD glitches due to transients. If the error condition persists for longer than 20ms, the \overline{IRQ} pin is pulled low and status register IRQSTAT bit 2 is set to indicate a persistent

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PGOOD fault. The PGOOD pin is held low for the duration of the low output condition plus 1ms. Figure 13 shows the timing of PGOOD during enable and fault events.

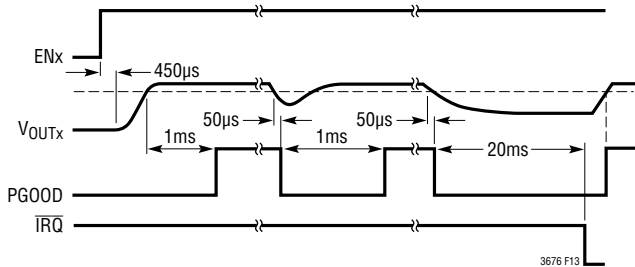


Figure 13. Output Low Voltage PGOOD and $\overline{\text{IRQ}}$ Timing

PGSTAT and MSKPG Registers

The power good status of each regulator is accessible through the LTC3676 I²C interface by reading the contents of the PGOOD status registers. Table 13 shows the PGSTATL and PGSTATRT register contents. The data in the PGSTATL register is held for a minimum of 1ms. The data in the PGSTATRT register is held only for the duration of the low voltage condition.

Table 13. Power Good Status Register

| STATUS REGISTER[BIT] | VALUE | REGULATOR OUTPUT LOW STATUS |
|----------------------|-------|-----------------------------|
| PGSTAT[0] | 0 | Buck1 Output Low |
| | 1 | Buck1 Output OK |
| PGSTAT[1] | 0 | Buck2 Output Low |
| | 1 | Buck2 Output OK |
| PGSTAT[2] | 0 | Buck3 Output Low |
| | 1 | Buck3 Output OK |
| PGSTAT[3] | 0 | Buck4 Output Low |
| | 1 | Buck4 Output OK |
| PGSTAT[4] | 0 | LD01 Output Low |
| | 1 | LD01 Output OK |
| PGSTAT[5] | 0 | LD02 Output Low |
| | 1 | LD02 Output OK |
| PGSTAT[6] | 0 | LD03 Output Low |
| | 1 | LD03 Output OK |
| PGSTAT[7] | 0 | LD04 Output Low |
| | 1 | LD04 Output OK |

Each regulator has a corresponding bit in the MSKPG status register as shown in Table 14. When set, a bit blocks the

PGOOD pin from being pulled low in the event of a low output voltage fault from its matching regulator. Setting a bit in the MSKPG command register does not mask the status in the PGOOD status registers.

Table 14. Power Good Status Masking Command Register

| COMMAND REGISTER[BIT] | VALUE | |
|-----------------------|-------|-------------------------|
| MSKPG [0] | 0 | Mask Buck1 PGOOD Status |
| | 1* | Pass Buck1 PGOOD Status |
| MSKPG [1] | 0 | Mask Buck2 PGOOD Status |
| | 1* | Pass Buck2 PGOOD Status |
| MSKPG [2] | 0 | Mask Buck3 PGOOD Status |
| | 1* | Pass Buck3 PGOOD Status |
| MSKPG [3] | 0 | Mask Buck4 PGOOD Status |
| | 1* | Pass Buck4 PGOOD Status |
| MSKPG [5] | 0 | Mask LD02 PGOOD Status |
| | 1* | Pass LD02 PGOOD Status |
| MSKPG [6] | 0 | Mask LD03 PGOOD Status |
| | 1* | Pass LD03 PGOOD Status |
| MSKPG [7] | 0 | Mask LD04 PGOOD Status |
| | 1* | Pass LD04 PGOOD Status |

*denotes default power-on value.

$\overline{\text{IRQ}}$ Status Pin

The $\overline{\text{IRQ}}$ pin is pulled and latched low when undervoltage, overtemperature or persistent PGOOD events occur. The $\overline{\text{IRQ}}$ pin is cleared by addressing the CLRIRQ command register or by holding $\overline{\text{ON}}$ low for 50ms.

Table 15. Interrupt Request Status Register

| STATUS REGISTER[BIT] | VALUE | IRQSTAT REGISTER BIT MEANING |
|----------------------|-------|--------------------------------------|
| IRQSTAT [0] | 0 | |
| | 1 | Pushbutton Status Active (Real Time) |
| IRQSTAT [1] | 0 | |
| | 1 | Hard Reset Occurred |
| IRQSTAT [2] | 0 | |
| | 1 | PGOOD Timeout Occurred |
| IRQSTAT [3] | 0 | |
| | 1 | Undervoltage Warning |
| IRQSTAT [4] | 0 | |
| | 1 | Undervoltage Standby Occurred |
| IRQSTAT [5] | 0 | |
| | 1 | Overtemperature Warning |
| IRQSTAT [6] | 0 | |
| | 1 | Overtemperature Standby Occurred |

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IRQSTAT and MSKIRQ Registers

The bits in the MSKIRQ command register (see Table 16) are set to mask warning, fault, and pushbutton status reporting to the $\overline{\text{IRQ}}$ pin. When set to mask, the $\overline{\text{IRQ}}$ pin is not pulled low as a result of a fault or warning. Even though the $\overline{\text{IRQ}}$ pin is not pulled low the masked bit is set in the IRQSTAT (see Table 15) register. When undervoltage, overtemperature faults, and hard reset signals are masked, the $\overline{\text{IRQ}}$ pin is not pulled low but the LTC3676 state controller is pushed into the STANDBY or POR/HRST state. Accessing the CLRIRQ status register clears the latched bits in the IRQSTAT status register and releases the $\overline{\text{IRQ}}$ pin.

Table 16. Interrupt Request Mask Command Register

| COMMAND REGISTER[BIT] | VALUE | |
|-----------------------|---------|--|
| MSKIRQ [0] | 0* 1 | Pass Pushbutton Status Mask Pushbutton Status |
| MSKIRQ [2] | 0* 1 | Pass PGOOD Timeout Mask PGOOD Timeout |
| MSKIRQ [3] | 0* 1 | Pass Undervoltage Warning Mask Undervoltage Warning |
| MSKIRQ [4] | 0* 1 | Pass Undervoltage Shutdown Mask Undervoltage Shutdown |
| MSKIRQ [5] | 0* 1 | Pass Overtemperature Warning Mask Overtemperature Warning |
| MSKIRQ [6] | 0* 1 | Pass Overtemperature Shutdown Mask Overtemperature Shutdown |

*denotes default power-on value.

The IRQ pin and IRQSTAT register are not cleared by hard reset or fault shutdown. If V_{IN} remains applied while the LTC3676 is in STANDBY or POR/HRST then IRQSTAT may be read on the subsequent power up to determine if a fault or hard reset occurred.

$\overline{\text{RSTO}}$ Status Pin

The LTC3676 $\overline{\text{RSTO}}$ status pin is pulled low when always-on LDO1 is 8% below its programmed value or when the LTC3676 is in the one second HRST timer state.

Hard Reset

A hard reset can be initiated by holding the $\overline{\text{ON}}$ pin low or writing to the HRST command register. Bit six of the CNTRL command register determines how long $\overline{\text{ON}}$ must remain low to initiate the hard reset. A hard reset sets

all I²C command register bits to their default power-on state. Table 17 shows the command register control of hard reset function.

Table 17. Hard Reset Time Control Command Register

| COMMAND REGISTER[BIT] | VALUE | SETTING |
|-----------------------|---------|-------------------------|
| CNTRL[6] | 0* 1 | 10 seconds 5 seconds |

*denotes default power-on value.

A hard reset command will push the LTC3676 state controller through the 1 second HRST timer state and into the POR/HRST state.

Fault Shutdown

An undervoltage or overtemperature fault will push the LTC3676 state controller through the 1 second standby timer state and into standby state. If a down sequence is selected in the command registers, it will be executed during the 1 second power down interval.

LTC3676-1 Operation

The LTC3676-1 option supports DDR memory operation by generating a DDR termination reference and supply rail equal to one-half the voltage applied to VDDQIN Pin 8.

An internal resistive divider creates a reference voltage of one-half the voltage on VDDQIN. This reference is used by the V_{TT} reference buffer to output one-half of VDDQIN on VTTR Pin 9. The VTTR voltage is used as the reference for 1.5A switching regulator 1 which is used as the DDR termination supply. The LTC3676-1 EN_B1 pin and command register bit Buck1[7] enable both VTTR output and switching regulator 1. The LTC3676-1 switching regulator 1 settings are fixed to one-half frequency and forced continuous operation.

Figure 1 shows typical application connections for the LTC3676-1 DDR termination reference and termination supply.

LDO4 has I²C command register selectable output voltages of 1.2V (default), 2.5V, 2.8V and 3V and is enabled only using the I²C command register. Table 18 shows the LDO4 command register controls for the LTC3676-1.

OPERATION

Table 18. LDO4 Control Command Register Setting (LTC3676-1)

| COMMAND REGISTER[BIT] | VALUE | SETTING |
|-----------------------|-----------------------|---|
| LDOB[0] | 0* 1 | Do Not Keep Alive LDO4 in Standby Keep Alive LDO4 in Standby |
| LDOB[1] | 0* 1 | Enable LDO4 at Any Output Voltage Enable LDO4 Only if Output Voltage Is <300mV |
| LDOB[2] | 0* 1 | LDO4 Disabled LDO4 Enable |
| LDOB[4:3] | 00* 01 10 11 | 1.2V 2.5V 2.8V 3.0V |

*denotes default power-on value.

I²C OPERATION

The LTC3676 communicates with a bus master using the standard I²C 2-wire interface. The timing diagram in Figure 14 shows the relationship of the signals on the bus. The two bus lines, SDA and SCL must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on SDA and SCL. The LTC3676 is both a slave receiver and slave transmitter. The I²C control signals, SDA and SCL are scaled internally to the DV_{DD} supply. DV_{DD} must be connected to the same power supply as the bus pull-up resistors.

The I²C port has an undervoltage lockout on the DV_{DD} pin. When DV_{DD} is below approximately 1V, the I²C serial port is cleared and the command registers are set to default POR values.

The complete I²C command register table is shown in Table 20 and Table 21.

I²C Bus Speed

The I²C port operates at speeds up to 400kHz. It has built in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

I²C START and STOP Conditions

A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The master may transmit either the slave write or the slave read address. Once data is written to the LTC3676, the master may transmit a STOP condition which commands the LTC3676 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for communication with another I²C device.

I²C Byte Format

Each byte sent to or received from the LTC3676 must be 8 bits long followed by an extra clock cycle for the acknowledge bit. The data should be sent to the LTC3676 most significant bit (MSB) first.

I²C Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. When the LTC3676 is written to, it acknowledges its write address and subsequent data bytes. When it is read from, the LTC3676 acknowledges its read address only. The bus master should acknowledge data returned from the LTC3676.

An acknowledge generated by the LTC3676 lets the master know that the latest byte of information was received. The master generates the acknowledge related clock and releases the SDA line during the acknowledge clock cycle. The LTC3676 pulls down the SDA line during the write acknowledge clock pulse so that it is a stable LOW during the HIGH period of this clock pulse.

At the end of a byte of data transferred from the LTC3676 during a READ operation, the LTC3676 releases the SDA line to allow the master to acknowledge receipt of the data. Failure of the master to acknowledge data from the LTC3676 has no effect on the operation of the I²C port.

OPERATION

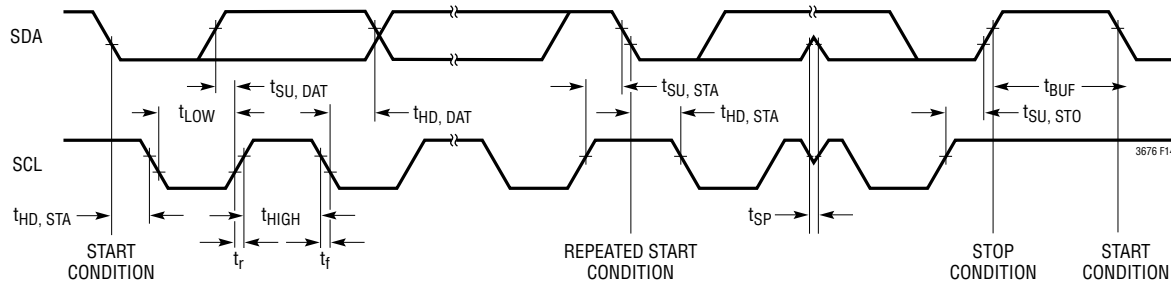


Figure 14. LTC3676 I²C Serial Port Timing

I²C Slave Address

The LTC3676 responds to factory programmed read and write addresses. The least significant bit of the address byte is 0 when writing data and 1 when reading data. Table 19 shows read and write addresses for the LTC3676 options.

Table 19. LTC3676 and LTC3676-1 I²C Read and Write Addresses

| LTC PART NUMBER | R/W | ADDRESS |
|-----------------|-----------|-----------------|
| LTC3676 | \bar{W} | 0111 1000, 0x78 |
| LTC3676 | R | 0111 1001, 0x79 |
| LTC3676-1 | \bar{W} | 0111 1010, 0x7A |
| LTC3676-1 | R | 0111 1011, 0x7B |

I²C Write Operation

The LTC3676 has twenty-two command registers for control input. They are accessed by the I²C port via a sub-addressed writing system.

A single write cycle of the LTC3676 consists of exactly three bytes except when a clear interrupt or hard reset command is written. The first byte is always the LTC3676 write address. The second byte represents the LTC3676 sub-address. The sub-address is a pointer which directs the subsequent data byte within the LTC3676. The third byte consists of the data to be written to the location pointed to by the sub-address.

As shown in Figure 15, the LTC3676 supports multiple sub-addressed write operations. Data pairs sent following the chip write address are interpreted as sub-address and data. Any number of sub-address and data pairs may be sent. The data in the command registers is not acted on by the LTC3676 until a STOP signal is issued.

The LTC3676 will keep interim writes to the registers when a repeat START condition occurs. A repeat start may be used to set up other devices on the I²C bus prior to sending a STOP condition. The LTC3676 will act on the data written prior to the repeat start when a STOP condition is detected.

I²C Read Operation

Figure 16 shows the LTC3676 command register read sequence. The bus master reads a byte of data from a LTC3676 command or status register by first writing the LTC3676 write address followed by the sub-address to be read from. The LTC3676 acknowledges each of the two bytes. Next, the bus master initiates a new START condition and sends the LTC3676 read address. Following the acknowledge of the read address by the LTC3676, the LTC3676 pushes data onto the I²C bus for the 8 clock cycles. The bus master then acknowledges the data on its ninth clock.

The last read sub-address that is written to the LTC3676 is stored. This allows repeated polling of a command or status register without the need to re-write its sub-address. Additionally, the last register written may be immediately read by issuing a START condition followed by read address and clocking out the data.

OPERATION

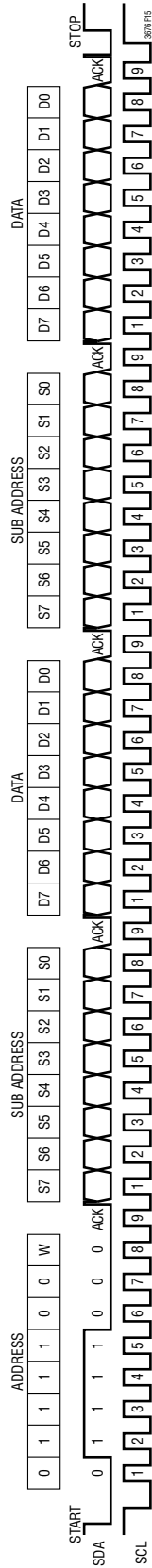


Figure 15. LTC3676 I²C Serial Port Multiple Write Pattern

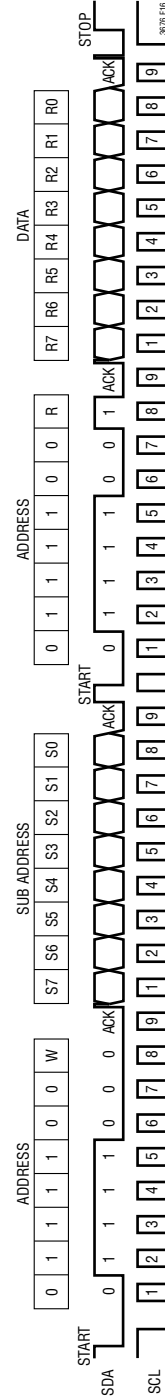


Figure 16. LTC3676 I²C Serial Port Read Pattern

OPERATION

Table 20. LTC3676 Command Registers

| REG | NAME | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | DEFAULT |
|------|-------|---|--|---|--|---|--|---|---|-----------|
| 0x01 | BUCK1 | Enable: 0 = Disabled if EN_B1 Low 1 = Enabled | Mode: 00 = Pulse-Skipping 01 = Burst 10 = Forced Continuous | | Start-Up: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV | Phase Select: 0 = Clock Phase 1 1 = Clock Phase 2 | Clock Rate: 0 = 2.25MHz 1 = 1.125MHz | Keep Alive Buck1: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown. | Switch DV/DT Control: 0 = Slow 1 = Fast | 0000 0000 |
| 0x02 | BUCK2 | Enable: 0 = Disabled if EN_B2 Low 1 = Enabled | Mode: 00 = Pulse-Skipping 01 = Burst 10 = Forced Continuous | | Start-Up: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV | Phase Select: 0 = Clock Phase 1 1 = Clock Phase 2 | Clock Rate: 0 = 2.25MHz 1 = 1.125MHz | Keep Alive Buck2: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown | Switch DV/DT Control: 0 = Slow 1 = Fast | 0000 0000 |
| 0x03 | BUCK3 | Enable: 0 = Disabled if EN_B3 Low 1 = Enabled | Mode: 00 = Pulse-Skipping 01 = Burst 10 = Forced Continuous | | Start-Up: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV | Phase Select: 0 = Clock Phase 1 1 = Clock Phase 2 | Clock Rate: 0 = 2.25MHz 1 = 1.125MHz | Keep Alive Buck3: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown | Switch DV/DT Control: 0 = Slow 1 = Fast | 0000 0000 |
| 0x04 | BUCK4 | Enable: 0 = Disabled if EN_B4 Low 1 = Enabled | Mode: 00 = Pulse-Skipping 01 = Burst 10 = Forced Continuous | | Start-Up: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV | Phase Select: 0 = Clock Phase 1 1 = Clock Phase 2 | Clock Rate: 0 = 2.25MHz 1 = 1.125MHz | Keep Alive Buck4: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown | Switch DV/DT Control: 0 = Slow 1 = Fast | 0000 0000 |
| 0x05 | LDOA | Reserved | Reserved | Enable LDO3: 0 = Disabled if EN_L3 Low 1 = Enabled | Start-Up LDO3: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV | Keep Alive LDO3: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown. | Enable LDO2: 0 = Disabled if EN_L2 Low 1 = Enabled | Start-Up LDO2: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV | Keep Alive LDO2: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown | XX00 0000 |
| 0x06 | LDOB | Reserved | Reserved | Reserved | LTC3676-1 LDO4 Output Voltage: 00 = 1.2V 01 = 2.5V 10 = 2.8V 11 = 3.0V | | Enable LDO4: 0 = Disabled if EN_L4 Low 1 = Enabled | Start-Up LDO4: 0 = Enable at Any Output Voltage 1 = Enable Only if Output <300mV | Keep Alive LDO4: 0 = Do Not Keep Alive 1 = Keep Alive in Shutdown | XXX0 0000 |
| 0x07 | SQD1 | Sequence Down Buck4: 00 = With WAKE 01 = WAKE + 100ms 10 = WAKE + 200ms 11 = WAKE + 300ms | | Sequence Down Buck3: 00 = With WAKE 01 = WAKE + 100ms 10 = WAKE + 200ms 11 = WAKE + 300ms | | Sequence Down Buck2: 00 = With WAKE 01 = WAKE + 100ms 10 = WAKE + 200ms 11 = WAKE + 300ms | | Sequence Down Buck1: 00 = With WAKE 01 = WAKE + 100ms 10 = WAKE + 200ms 11 = WAKE + 300ms | | 0000 0000 |

OPERATION

| REG | NAME | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | DEFAULT |
|------|-------|---|---|--|---|--|------|--|------|-----------|
| 0x08 | SQD2 | Reserved | Reserved | Sequence Down LD04: 00 = With WAKE 01 = WAKE + 100ms 10 = WAKE + 200ms 11 = WAKE + 300ms | | Sequence Down LD03: 00 = With WAKE 01 = WAKE + 100ms 10 = WAKE + 200ms 11 = WAKE + 300ms | | Sequence Down LD02: 00 = With WAKE 01 = WAKE + 100ms 10 = WAKE + 200ms 11 = WAKE + 300ms | | XX00 0000 |
| 0x09 | CNTRL | PWR_ON: 0 = Not PWR_ON 1 = PWR_ON "ORed" with PWR_ON PIN | Pushbutton Hard Reset Timer: 0 = 10 sec 1 = 5 sec | Software Control Mode: 0 = Pin or Register Control 1 = Inhibit Pin Control | UV Warning Threshold: 000 = 2.7V 001 = 2.8V 010 = 2.9V 011 = 3.0V 100 = 3.1V 101 = 3.2V 110 = 3.3V 111 = 3.4V | | | Over temperature Warning Levels: 00 = 10°C Below Overtemperature 01 = 20°C Below Overtemperature 10 = 30°C Below Overtemperature 11 = 40°C Below Overtemperature | | 0000 0000 |
| 0x0A | DVB1A | Reserved | Reserved | Buck1 Reference Select: 0 = DVB1A[4-0] 1 = DVB1B[4-0] | Buck1 Feedback Reference Input (VA): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size | | | | | XX01 1001 |
| 0x0B | DVB1B | Reserved | Reserved | PGOOD Mask: 0 = PGOOD Low When Slewing 1 = PGOOD Not Forced Low When Slewing | Buck1 Feedback Reference Input (VB): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size | | | | | XX01 1001 |
| 0x0C | DVB2A | Reserved | Reserved | Buck2 Reference Select: 0 = DVB2A[4-0] 1 = DVB2B[4-0] | Buck2 Feedback Reference Input (VA): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size | | | | | XX01 1001 |
| 0x0D | DVB2B | Reserved | Reserved | PGOOD Mask: 0 = PGOOD Low When Slewing 1 = PGOOD Not Forced Low When Slewing | Buck2 Feedback Reference Input (VB): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size | | | | | XX01 1001 |
| 0x0E | DVB3A | Reserved | Reserved | Buck3 Reference Select: 0 = DVB3A[4-0] 1 = DVB3B[4-0] | Buck3 Feedback Reference Input (VA): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size | | | | | XX01 1001 |

OPERATION

| REG | NAME | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] | DEFAULT | |
|------|--------|------------------------------|---------------------------------------|---|---|---------------------------------|----------------------------|----------------------------|----------------------------|-----------|-----------|
| 0x0F | DVB3B | Reserved | Reserved | PGOOD Mask: 0 = PGOOD Low When Slewing 1 = PGOOD Not Forced Low When Slewing | Buck3 Feedback Reference Input (VB): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size | | | | | | XX01 1001 |
| 0x10 | DVB4A | Reserved | Reserved | Buck4 Reference. Select: 0 = DVB4A[4-0] 1 = DVB4B[4-0] | Buck4 Feedback Reference Input (VA): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size | | | | | | XX01 1001 |
| 0x11 | DVB4B | Reserved | Reserved | PGOOD Mask: 0 = PGOOD Low When Slewing 1 = PGOOD Not Forced Low When Slewing | Buck4 Feedback Reference Input (VB): 00000 = 412.5mV 11001 = 725mV 11111 = 800mV 12.5mV Step Size | | | | | | XX01 1001 |
| 0x12 | MSKIRQ | Reserved | Mask Over- temperature Shutdown | Mask Over- temperature Warning | Mask Undervoltage Shutdown | Mask Undervoltage Warning | Mask PGOOD Timeout | Reserved | Mask Push Button Status | X000 00X0 | |
| 0x13 | MSKPG | Allow LDO4 PGOOD Fault | Allow LDO3 PGOOD Fault | Allow LDO2 PGOOD Fault | Reserved | Allow Buck4 PGOOD Fault | Allow Buck3 PGOOD Fault | Allow Buck2 PGOOD Fault | Allow Buck1 PGOOD Fault | 1111 1111 | |
| 0x14 | USER | User Bit 7 | User Bit 6 | User Bit 5 | User Bit 4 | User Bit 3 | User Bit 2 | User Bit 1 | User Bit 0 | 0000 0000 | |
| 0x1E | HRST | Hard Reset Command. No Data. | | | | | | | | | |
| 0x1F | CLRIRQ | Clear IRQ Command. No Data | | | | | | | | | |

Table 21. LTC3676 Status Registers

| REG | NAME | B[7] | B[6] | B[5] | B[4] | B[3] | B[2] | B[1] | B[0] |
|------|----------|------------------------|----------------------------------|---------------------------------|--------------------------|-------------------------|-------------------------|-------------------------|-------------------------------------|
| 0x15 | IRQSTAT | Reserved | Over- temperature Shutdown | Over- temperature Warning | Undervoltage Shutdown | Undervoltage Warning | PGOOD Timeout | Hard Reset | Pushbutton Status (Real Time) |
| 0x16 | PGSTATL | LDO4 PGOOD Hold 1ms | LD03 PGOOD Hold 1ms | LD02 PGOOD Hold 1ms | LD01 PGOOD Hold 1ms | Buck4 PGOOD Hold 1ms | Buck3 PGOOD Hold 1ms | Buck2 PGOOD Hold 1ms | Buck1 PGOOD Hold 1ms |
| 0x17 | PGSTATRT | LDO4 PGOOD | LD03 PGOOD | LD02 PGOOD | LD01 PGOOD | Buck4 PGOOD | Buck3 PGOOD | Buck2 PGOOD | Buck1 PGOOD |

Reserved Bits

The bits marked as reserved in command registers cannot be written to and will return inconsistent data when read. These bits must be considered invalid and masked by software when reading.

APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS AND BOARD LAYOUT

Printed Circuit Board Power Dissipation

In order to ensure optimal performance and the ability to deliver maximum output power to any regulator, it is critical that the exposed ground pad on the backside of the LTC3676 package be soldered to a ground plane on the board. The exposed pad is the only GND connection for the LTC3676. Correctly soldered to a 2500mm² ground plane on a double-sided 1oz copper board, the LTC3676 has a thermal resistance (θ_{JA}) of approximately 33°C/W. Failure to make good thermal contact between the exposed pad on the backside of the package and an adequately sized ground plane will result in thermal resistances far greater than 33°C/W. To ensure the junction temperature of the LTC3676 die does not exceed the maximum rated limit and to prevent overtemperature faults, the power output of the LTC3676 must be managed by the application. The total power dissipation in the LTC3676 is approximated by summing the power dissipation in each of the switching regulators and the LDO regulators. The power dissipation in a switching regulator is estimated by:

$$P_{D(SWx)} = V_{OUTx} \cdot I_{OUTx} \cdot \frac{100 - \text{Eff}\%}{100} \text{ (W)}$$

where V_{OUTx} is the programmed output voltage I_{OUTx} is the load current and Eff is the % efficiency that can be measured or looked up from the efficiency curves for the programmed output voltage.

The power dissipated by an LDO regulator is estimated by:

$$P_{D(LDOx)} = (V_{IN_Lx} - V_{LDOx}) \cdot I_{LDOx} \text{ (W)}$$

where V_{LDOx} is the programmed output voltage, $V_{IN(LDOx)}$ is the LDO supply voltage, and I_{LDOx} is the output load current. If one of the switching regulator outputs is used as an LDO supply voltage, remember to include the LDO supply current in the switching regulator load current for calculating power loss.

An example using the equations above with the parameters in Table 23 shows an application that is at a junction temperature of 118°C at an ambient temperature of 55°C. LDO2, LDO3, and LDO4 are powered by step-down Buck2 and Buck4. The total load on Buck2 and Buck4 is the sum

of the application load and the LDO load. This example is with the LDO regulators at one third rated current and the switching regulators at three quarters rated current.

Table 22. LTC3676 Power Loss Example

| | V _{IN} | V _{OUT} | APPLICATION LOAD (A) | TOTAL LOAD (A) | EFF (%) | P _D (mW) |
|---|-----------------|------------------|----------------------|----------------|---------|---------------------|
| LDO1 | 3.8 | 1.2 | 0.01 | 0.010 | – | 26.00 |
| LDO2 | 1.8 | 1.2 | 0.1 | 0.100 | – | 60.00 |
| LDO3 | 3.3 | 1.8 | 0.1 | 0.100 | – | 150.00 |
| LDO4 | 3.3 | 2.5 | 0.1 | 0.100 | – | 80.00 |
| Buck1 | 3.8 | 1.2 | 1.875 | 1.875 | 80 | 450.00 |
| Buck2 | 3.8 | 1.8 | 1.775 | 1.875 | 85 | 506.25 |
| Buck3 | 3.8 | 1.25 | 1.125 | 1.125 | 80 | 281.25 |
| Buck4 | 3.8 | 3.3 | 0.925 | 1.125 | 90 | 371.25 |
| Total Power = | | | | | | 1925 |
| Internal Junction Temperature at 55°C Ambient | | | | | | 118°C |

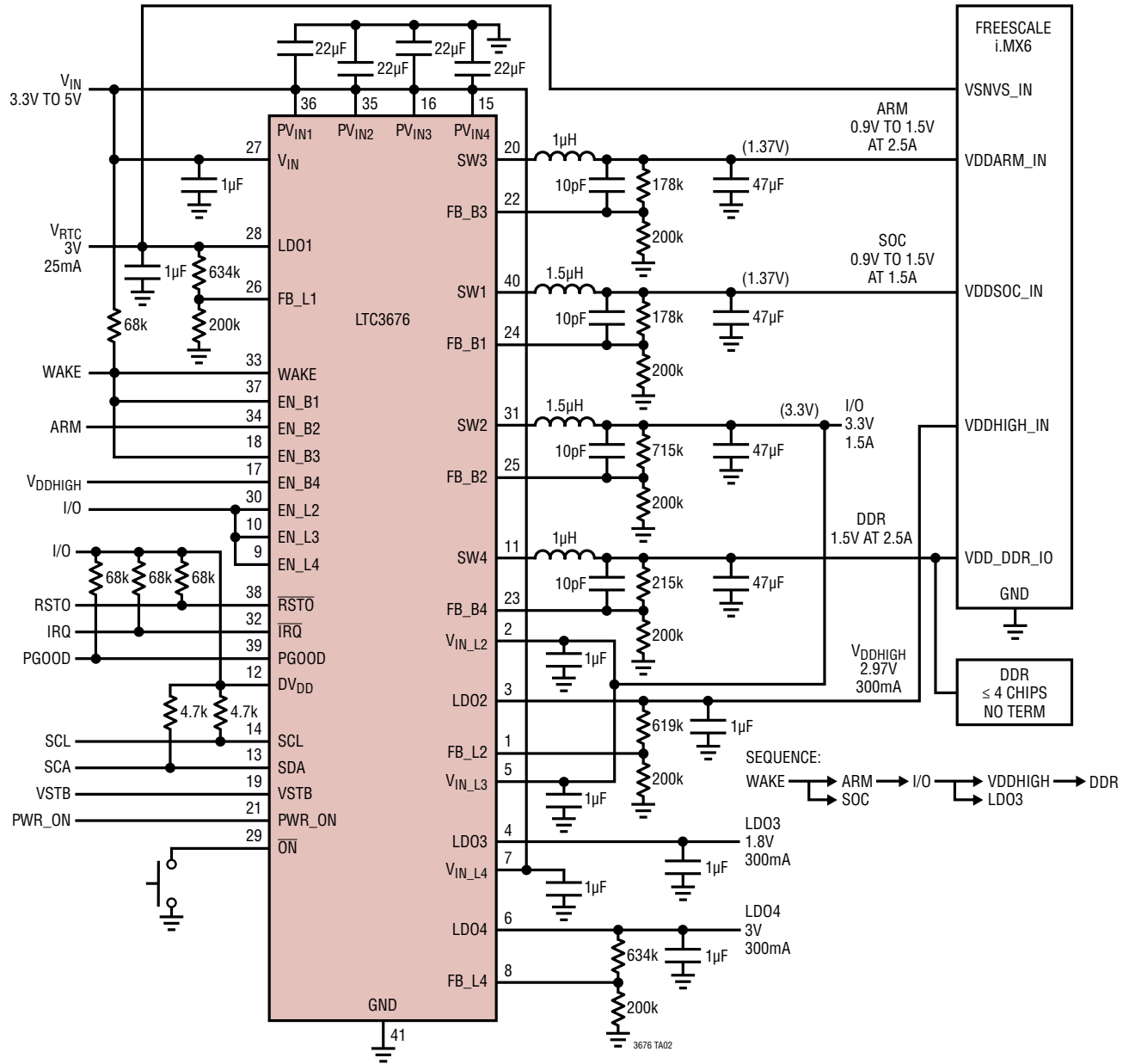
Printed Circuit Board Layout

When laying out the printed circuit board, the following checklist should be followed to ensure proper operation of the LTC3676:

1. Connect the exposed pad of the package (Pin 41) directly to a large ground plane to minimize thermal and electrical impedance.
2. The switching regulator input supply traces to their decoupling capacitors should be as short as possible. Connect the GND side of the capacitors directly to the ground plane of the board. The decoupling capacitors provide the AC current to the internal power MOSFETs and their drivers. It is important to minimize inductance from the capacitors to the LTC3676 pins.
3. Minimize the switching power traces connecting SW1, SW2, SW3, and SW4 to the inductors to reduce radiated EMI and parasitic coupling. Keep sensitive nodes such as the feedback pins away from or shielded from the large voltage swings on the switching nodes.
4. Minimize the length of the connection between the step-down switching regulator inductors and the output capacitors. Connect the GND side of the output capacitors directly to the thermal ground plane of the board.

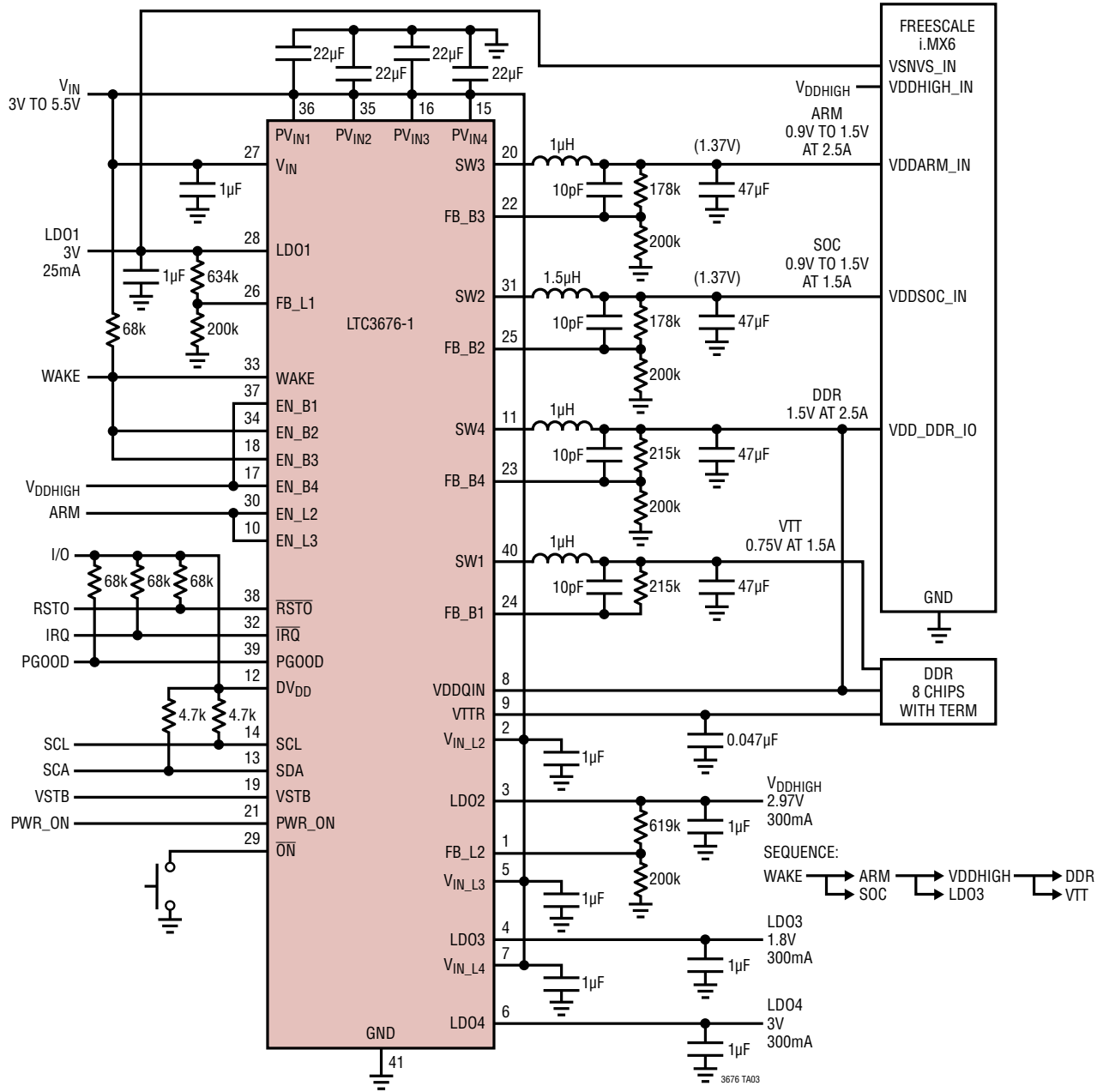
TYPICAL APPLICATIONS

LTC3676 PMIC Configured to Support Freescale i.MX6 Processor



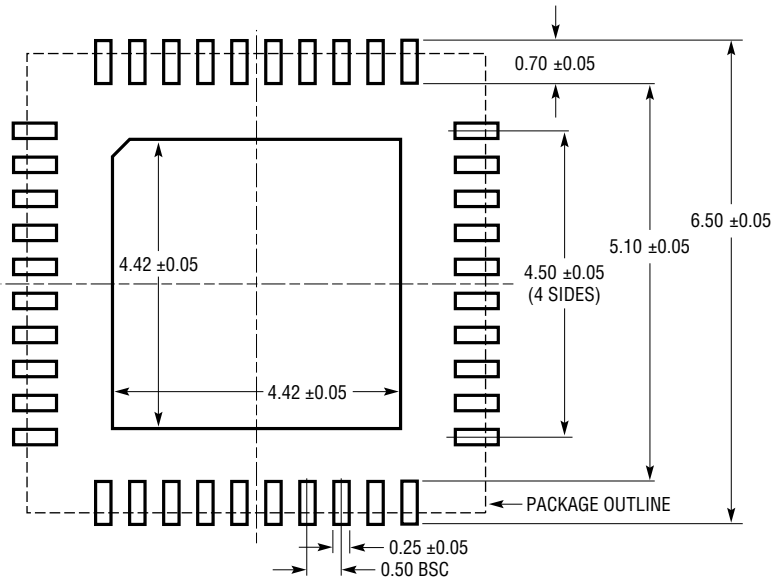
TYPICAL APPLICATIONS

LTC3676-1 PMIC Configured to Support Freescale i.MX6 Processor with DDR V_{TT} and V_{TR}

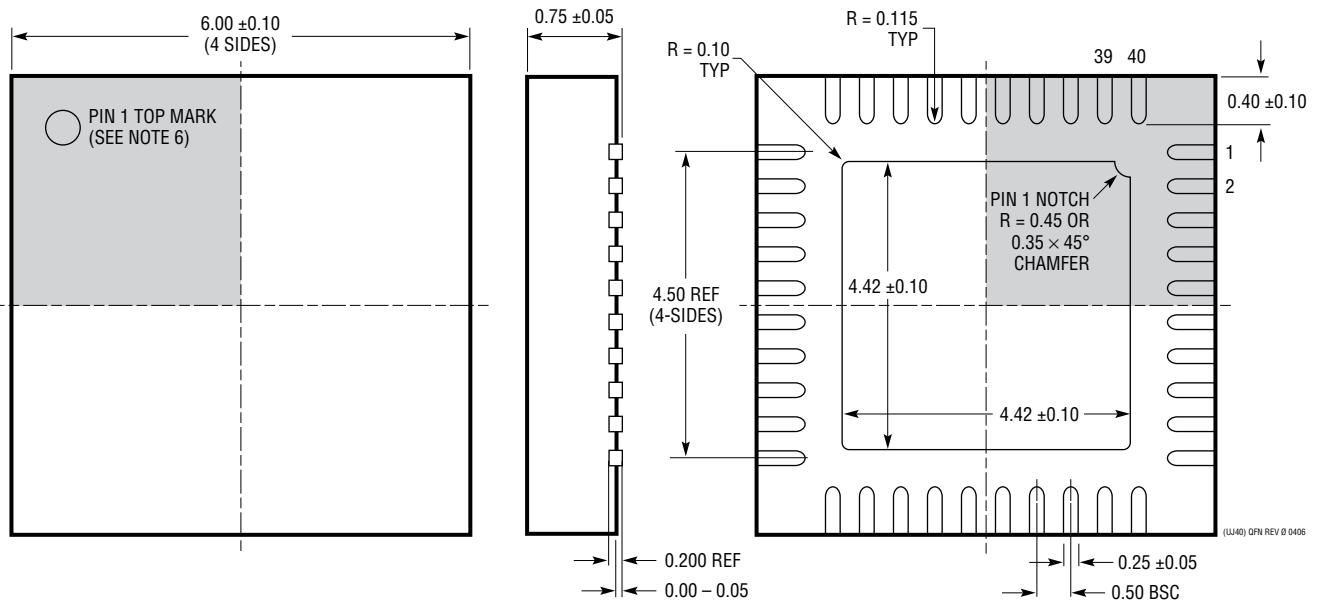


PACKAGE DESCRIPTION

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
 (Reference LTC DWG # 05-08-1728 Rev 0)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

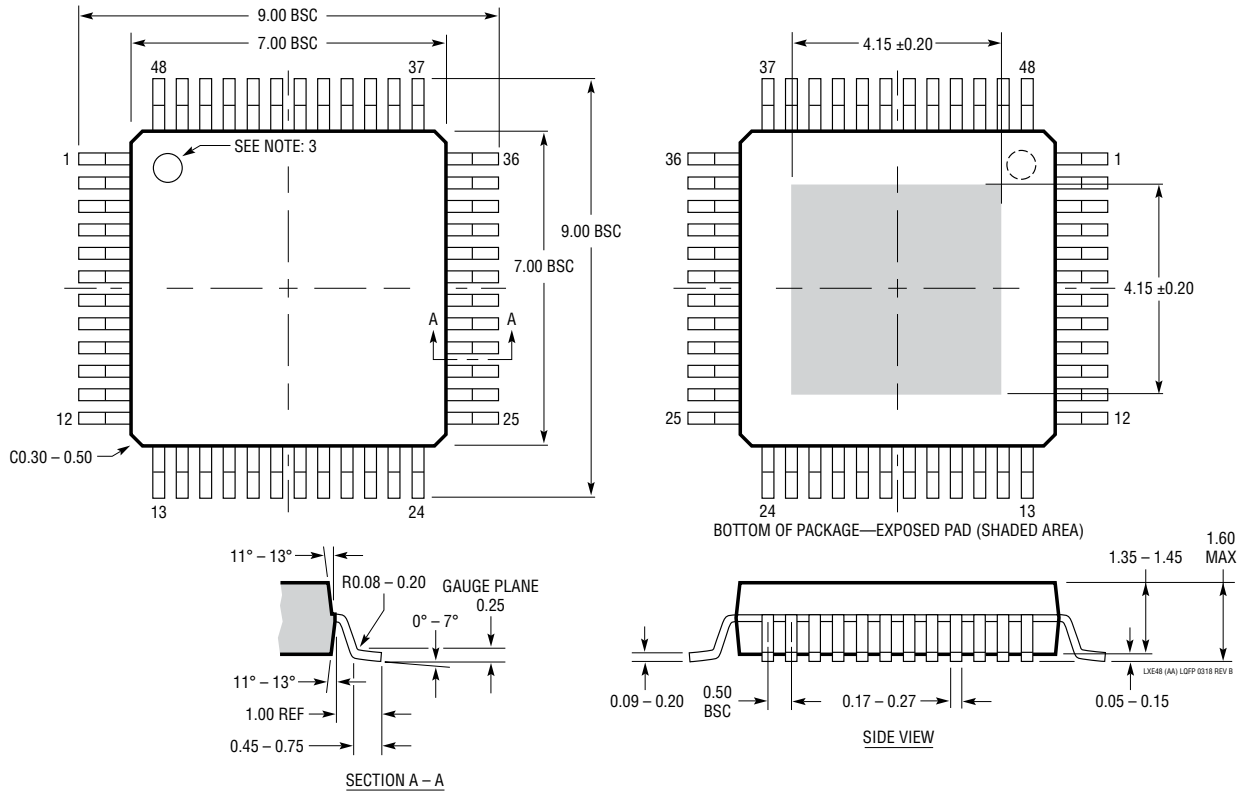


- NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
 2. DRAWING NOT TO SCALE
 3. ALL DIMENSIONS ARE IN MILLIMETERS
 4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
 5. EXPOSED PAD SHALL BE SOLDER PLATED
 6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

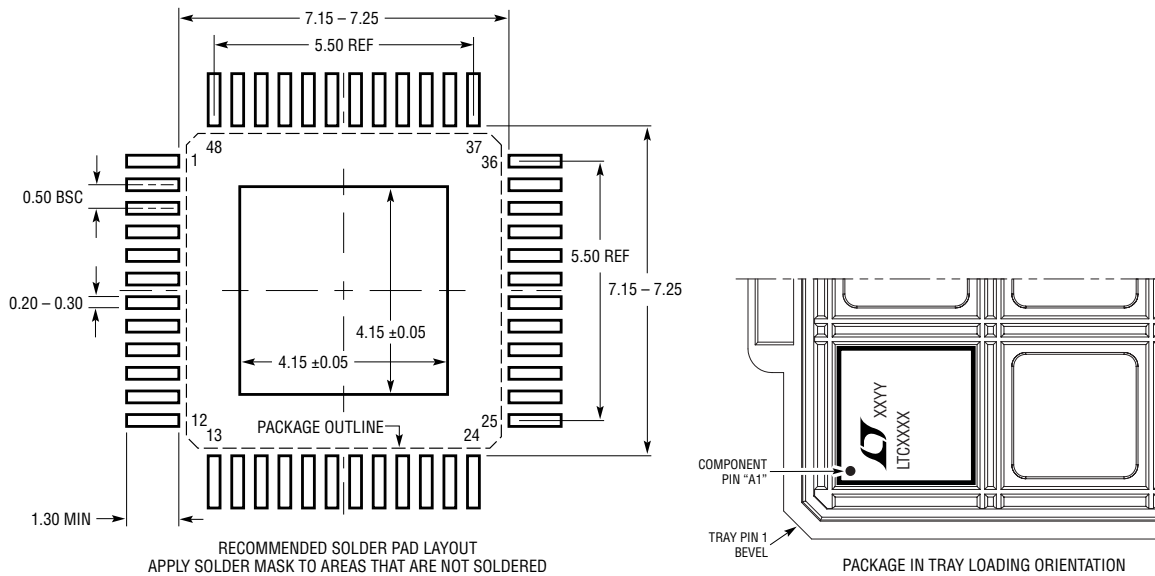
BOTTOM VIEW—EXPOSED PAD

PACKAGE DESCRIPTION

LXE Package 48-Lead Plastic Exposed Pad LQFP (7mm × 7mm) (Reference LTC DWG #05-08-1927 Rev B) Exposed Pad Variation AA



- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
 2. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm (10 MILS) BETWEEN THE LEADS AND ON ANY SIDE OF EXPOSED PAD, MAX 0.50mm (20 MILS) AT CORNER OF EXPOSED PAD, IF PRESENT
 3. PIN-1 IDENTIFIER IS A MOLDED INDENTATION
 4. DRAWING IS NOT TO SCALE

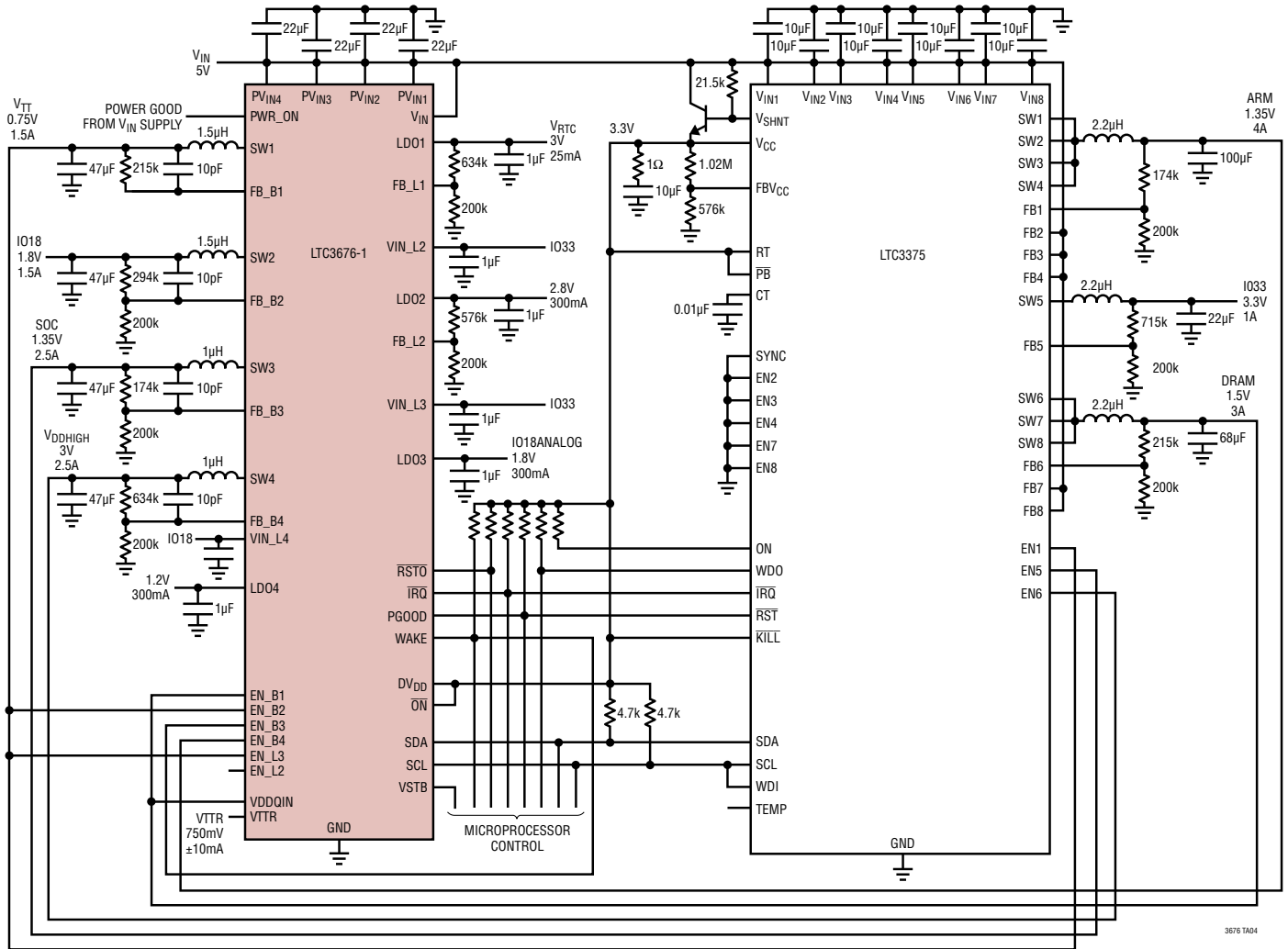


REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|-----|-------|--|--------------------|
| A | 12/13 | Modified the Typical Application Circuit. | 1 |
| | | Modified Start-Up Sequence Path. | 1 |
| | | Changed Conditions on V_{IN} Burst Mode Quiescent Current. | 3 |
| | | Removed Transient Response comment from V_{OUT} Programming. | 16 |
| | | Modified Command Registers table. | 28-30 |
| | | Modified P_D equation in PCB Power Dissipation section Table 22. | 31 |
| | | Changed R and C values in Typical Applications. | 32, 33, 36 |
| B | 09/14 | Changed C values in application circuits. | 1, 32, 33, 36 |
| | | Corrected pin names in Conditions in Electrical Characteristics table. | 3 to 5 |
| | | Corrected units on Current Limit graph. | 8 |
| | | Corrected units on LDO1 Dropout and LDO1 Load Response graphs. | 9 |
| | | Corrected Operation Introduction section. | 14 |
| | | Modified LTC3676-1 Operation section. | 24 |
| | | Changed table reference in I^2C Operation section. | 25 |
| | | Changed table number for Command Registers section. | 28 |
| C | 09/14 | Clarified Command Registers table. | 30 |
| | | Added LQFP Package (LXE). | 1 to 3, 11, 12, 36 |
| D | 05/15 | Modified Thermal Resistance of LXE Package. | 2 |
| | | Modified Pin Description of EN_B1. | 12 |
| | | Modified Figure 1 GND. | 15 |
| | | Clarified LTC3676-1 Operation Section. | 25 |
| | | Amended Package Drawing. | 36 |
| E | 04/17 | Added thermal resistances Θ_{JA} . | 2 |
| F | 09/17 | Modified Buck $R_{DS(ON)}$ curves. | 9 |
| | | Modified LTC3676-1 Operation section. | 25 |
| | | Added Reserved Bits section to Table 21. | 31 |
| G | 07/19 | Add AEC-Q100 Qualification and Orderable Part Numbers. | 1, 3 |
| H | 04/21 | Modified Features section. | 1 |
| | | Modified Absolute Maximum Ratings section. | 2 |
| | | Added Automotive Products to Order Information section. | 3 |
| | | Modified Electrical Characteristics section. | 4 to 8 |
| | | Corrected Block Diagram. | 13, 14 |
| | | Modified Operation section. | 15 to 26 |
| | | Corrected LDO power equation in Applications Information section. | 32 |

TYPICAL APPLICATION

Sequenced Power for High Performance Processor and DDR Memory Using LTC3375 Parallelable Buck Converters



RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|-------------------------------------|---|--|
| LTC3101 | 1.8V to USB, Multioutput DC/DC Converter with Low Loss USB Power Controller | Seamless Transition Between Multiple Input Power Sources, V _{IN} Range: 1.8V to 5.5V, Buck-Boost Converter V _{OUT} Range: 1.5V to 5.25V, 3.3V _{OUT} at 800mA for V _{IN} ≥ 3V, Dual 350mA Buck Regulators, V _{OUT} : 0.6V to V _{IN} , 38μA Quiescent Current in Burst Mode Operation, 24-Lead 4mm × 4mm × 0.75mm QFN Package |
| LTC3375 | 8-Channel Programmable, Parallelable 1A Buck DC/DCs | 8-Channel Independent Step-Down DC/DCs. Master Slave Configurable for Up to 4A per Output Channel with a Single Inductor, Die Temperature Monitor Output, 48-Lead 7mm × 7mm QFN Package |
| LTC3589/ LTC3589-1/ LTC3589-2 | 8-Output Regulator with Sequencing and I ² C | Triple I ² C Adjustable High Efficiency Step-Down DC/DC Converters: 1.6A, 1A, 1A. High Efficiency 1.2A Buck-Boost DC/DC Converter. Triple 250mA LDO Regulators. Pushbutton ON/OFF Control with System Reset. Flexible Pin-Strap Sequencing Operation. I ² C and Independent Enable Control Pins, DVS and Slew Rate Control, 40-Lead 6mm × 6mm × 0.75mm QFN Package |
| LTC3586/ LTC3586-1 | Switching USB Power Manager PMIC with Li-Ion/Polymer Charger | Complete Multifunction PMIC: Switching Power Manager, 1A Buck-Boost + 2 Bucks + Boost + LDO, 4mm × 6mm QFN-38 Package, LTC3586-1 Version Has 4.1V V _{FLOAT} . |

Rev. H