

LTC3588-1

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}		V_{OUT}	-0.3V to Lesser of ($V_{IN2} + 0.3V$) or 6V
Low Impedance Source	-0.3V to 18V*	PGOOD.....	-0.3V to Lesser of ($V_{OUT} + 0.3V$) or 6V
Current Fed, $I_{SW} = 0A$	25mA†	I_{PZ1}, I_{PZ2}	$\pm 50mA$
PZ1, PZ2	0V to V_{IN}	I_{SW}	350mA
D0, D1	-0.3V to [Lesser of ($V_{IN2} + 0.3V$) or 6V]	Operating Junction Temperature Range	
CAP	[Higher of -0.3V or ($V_{IN} - 6V$)] to V_{IN}	(Notes 2, 3)	-40 to 125°C
V_{IN2}	-0.3V to [Lesser of ($V_{IN} + 0.3V$) or 6V]	Storage Temperature Range	-65 to 150°C
		Lead Temperature (Soldering, 10 sec)	
		MSE Only	300°C

* V_{IN} has an internal 20V clamp

† For $t < 1ms$ and Duty Cycle $< 1\%$,
Absolute Maximum Continuous Current = 5mA

PIN CONFIGURATION

<p>TOP VIEW</p> <p>DD PACKAGE 10-LEAD (3mm × 3mm) PLASTIC DFN</p> <p>$T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 43^{\circ}C/W$, $\theta_{JC} = 7.5^{\circ}C/W$ EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB</p>	<p>TOP VIEW</p> <p>MSE PACKAGE 10-LEAD PLASTIC eMSOP</p> <p>$T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 45^{\circ}C/W$, $\theta_{JC} = 10^{\circ}C/W$ EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB</p>
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ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3588EDD-1#PBF	LTC3588EDD-1#TRPBF	LFKY	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC3588IDD-1#PBF	LTC3588IDD-1#TRPBF	LFKY	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC3588EMSE-1#PBF	LTC3588EMSE-1#TRPBF	LTFKX	10-Lead Plastic eMSOP	-40°C to 125°C
LTC3588IMSE-1#PBF	LTC3588IMSE-1#TRPBF	LTFKX	10-Lead Plastic eMSOP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

This product is only offered in trays. For more information go to: <http://www.linear.com/packaging/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are for $T_A = 25^\circ\text{C}$. (Note 2) $V_{IN} = 5.5\text{V}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	Low Impedance Source on V_{IN}	●			18.0	V
I_{VIN}	V_{IN} Quiescent Current UVLO Buck Enabled, Sleeping Buck Enabled, Sleeping Buck Enabled, Not Sleeping	$V_{IN} = 2.5\text{V}$, Not PGOOD $V_{IN} = 4.5\text{V}$ $V_{IN} = 18\text{V}$ $I_{SW} = 0\text{A}$ (Note 4)			450 950 1.7 150	700 1500 2.5 250	nA nA μA μA
V_{UVLO}	V_{IN} Undervoltage Lockout Threshold	V_{IN} Rising 1.8V Output Selected; D1 = 0, D0 = 0 2.5V Output Selected; D1 = 0, D0 = 1 3.3V Output Selected; D1 = 1, D0 = 0 3.6V Output Selected; D1 = 1, D0 = 1 V_{IN} Falling 1.8V Output Selected; D1 = 0, D0 = 0 2.5V Output Selected; D1 = 0, D0 = 1 3.3V Output Selected; D1 = 1, D0 = 0 3.6V Output Selected; D1 = 1, D0 = 1	● ● ● ● ● ● ● ● ● ●	3.77 3.77 4.73 4.73 2.66 2.66 3.42 3.75	4.04 4.04 5.05 5.05 2.87 2.87 3.67 4.02	4.30 4.30 5.37 5.37 3.08 3.08 3.91 4.28	V V V V V V V V V V
V_{SHUNT}	V_{IN} Shunt Regulator Voltage	$I_{VIN} = 1\text{mA}$		19.0	20.0	21.0	V
I_{SHUNT}	Maximum Protective Shunt Current	1ms Duration		25			mA
	Internal Bridge Rectifier Loss ($ V_{PZ1} - V_{PZ2} - V_{IN}$)	$I_{BRIDGE} = 10\mu\text{A}$		350	400	450	mV
	Internal Bridge Rectifier Reverse Leakage Current	$V_{REVERSE} = 18\text{V}$				20	nA
	Internal Bridge Rectifier Reverse Breakdown Voltage	$I_{REVERSE} = 1\mu\text{A}$		V_{SHUNT}	30		V
V_{OUT}	Regulated Output Voltage	1.8V Output Selected Sleep Threshold Wake-Up Threshold 2.5V Output Selected Sleep Threshold Wake-Up Threshold 3.3V Output Selected Sleep Threshold Wake-Up Threshold 3.6V Output Selected Sleep Threshold Wake-Up Threshold	● ● ● ● ● ● ● ● ● ● ● ●	1.710 2.425 3.201 3.492	1.812 1.788 2.512 2.488 3.312 3.288 3.612 3.588	1.890 2.575 3.399 3.708	V V V V V V V V
	PGOOD Falling Threshold	As a Percentage of the Selected V_{OUT}		83	92		%
I_{VOUT}	Output Quiescent Current	$V_{OUT} = 3.6\text{V}$			89	150	nA
I_{PEAK}	Buck Peak Switch Current			200	260	350	mA
I_{BUCK}	Available Buck Output Current			100			mA
R_P	Buck PMOS Switch On-Resistance				1.1		Ω
R_N	Buck NMOS Switch On-Resistance				1.3		Ω
	Max Buck Duty Cycle		●	100			%
$V_{IH(D0, D1)}$	D0/D1 Input High Voltage		●	1.2			V
$V_{IL(D0, D1)}$	D0/D1 Input Low Voltage		●			0.4	V
$I_{IH(D0, D1)}$	D0/D1 Input High Current					10	nA
$I_{IL(D0, D1)}$	D0/D1 Input Low Current					10	nA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

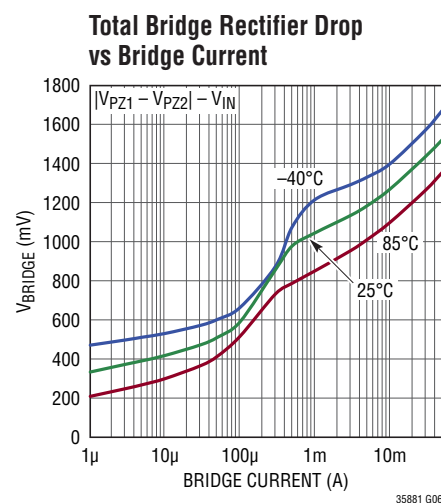
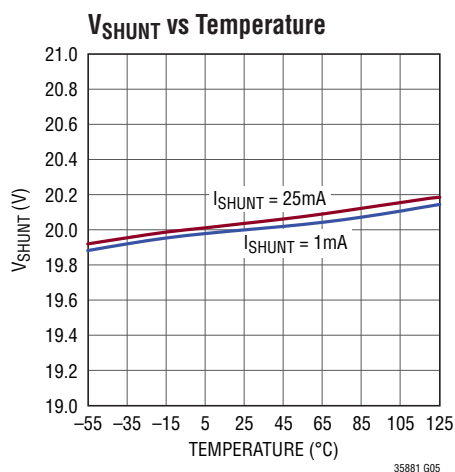
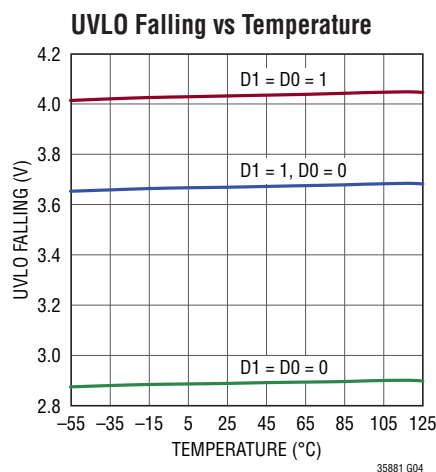
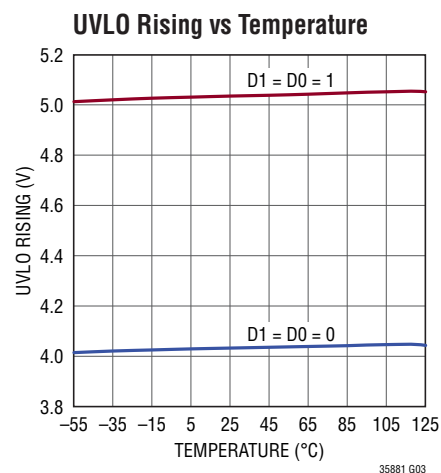
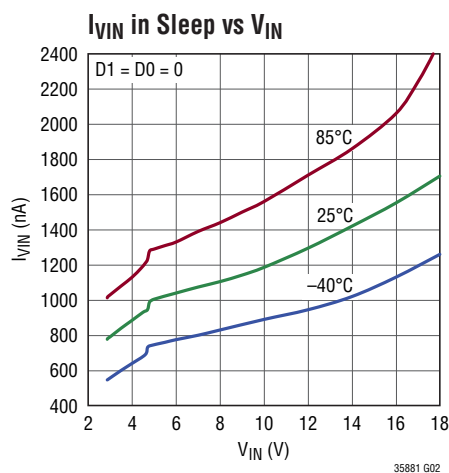
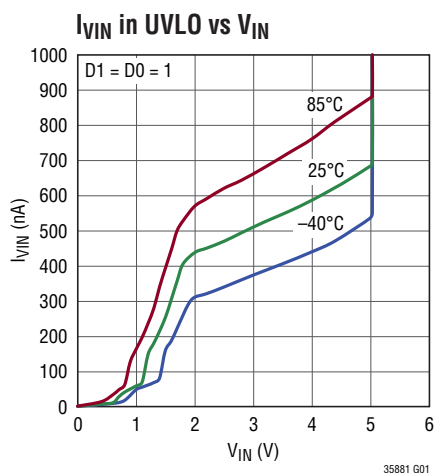
Note 2: The LTC3588-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3588E-1 is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the -40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LTC3588I-1 is guaranteed over the full -40°C to 125°C operating

junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The junction temperature (T_J , in °C) is calculated from the ambient temperature (T_A , in °C) and power dissipation (P_D , in Watts) according to the formula: $T_J = T_A + (P_D \cdot \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

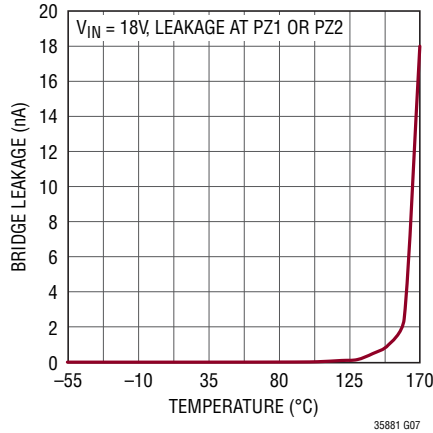
Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

TYPICAL PERFORMANCE CHARACTERISTICS

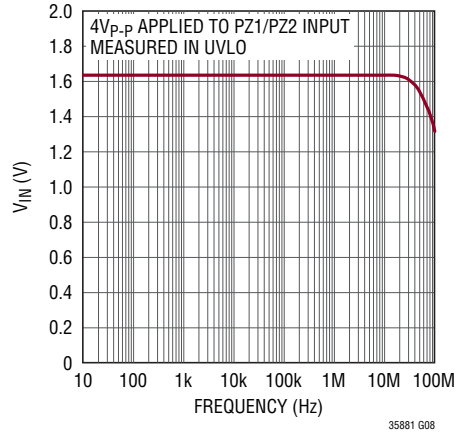


TYPICAL PERFORMANCE CHARACTERISTICS

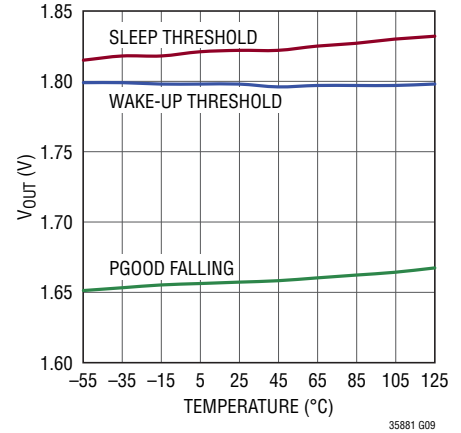
Bridge Leakage vs Temperature



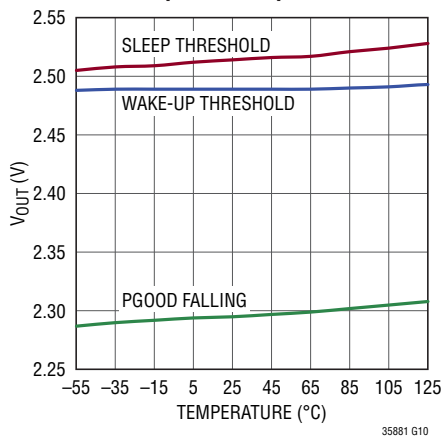
Bridge Frequency Response



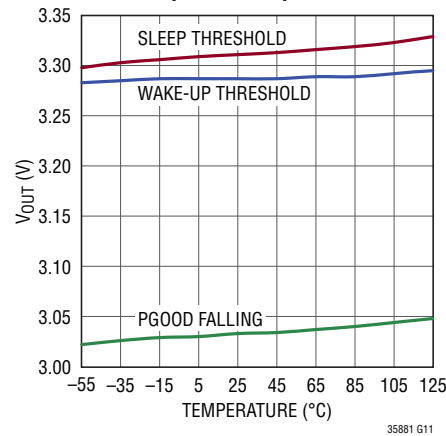
1.8V Output vs Temperature



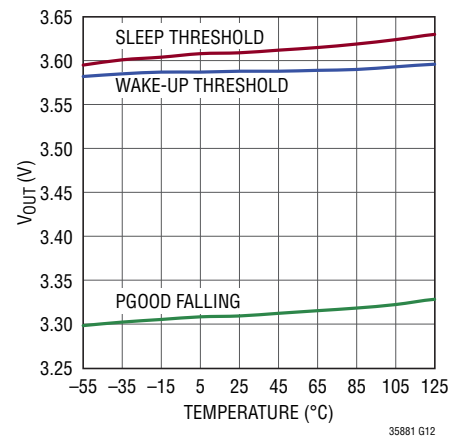
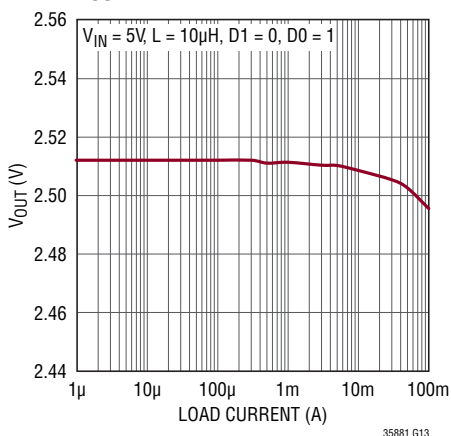
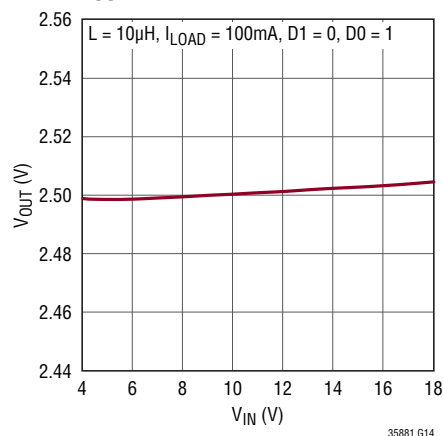
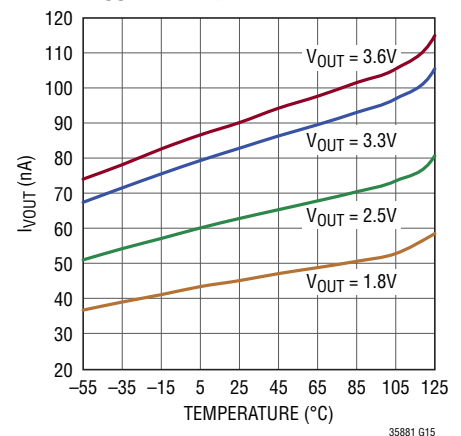
2.5V Output vs Temperature



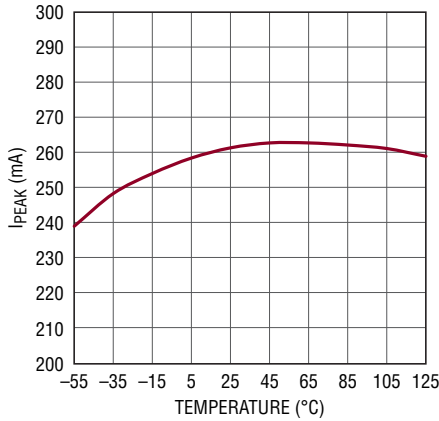
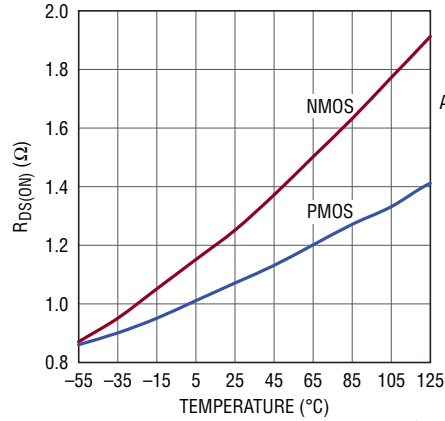
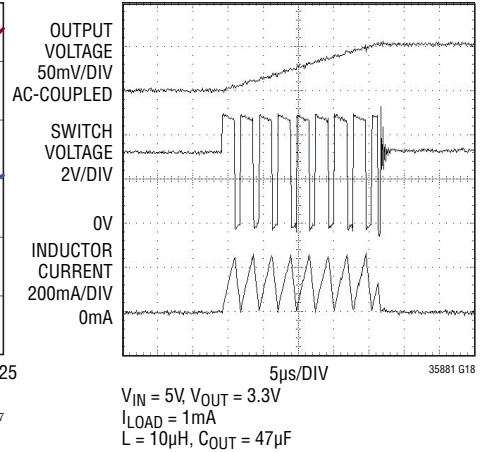
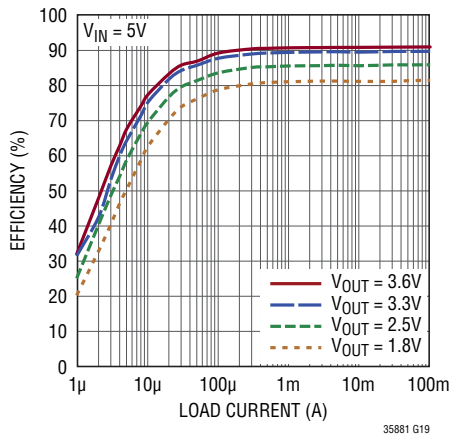
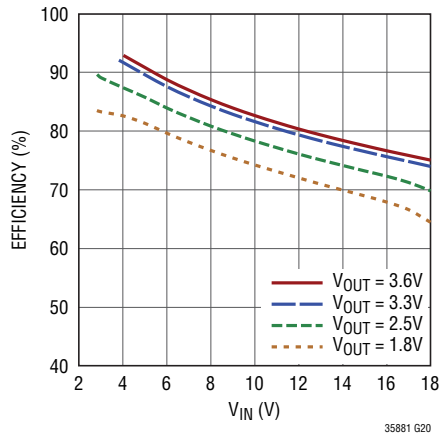
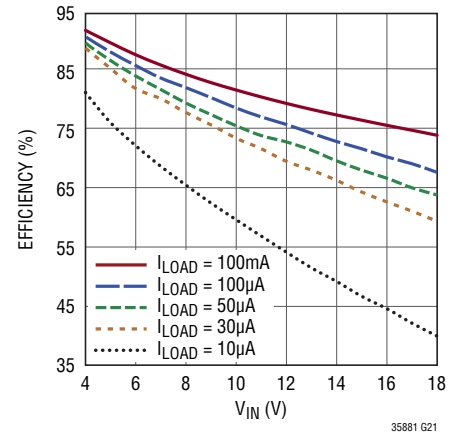
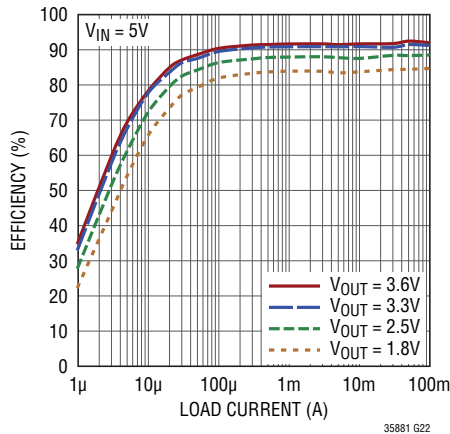
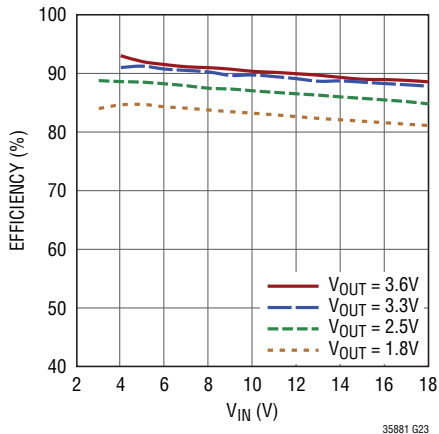
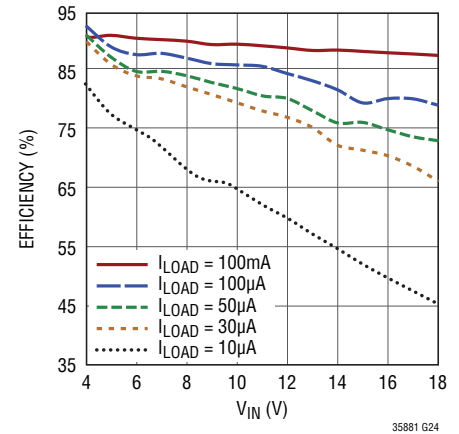
3.3V Output vs Temperature



3.6V Output vs Temperature

 V_{OUT} Load Regulation V_{OUT} Line Regulation I_{OUT} vs Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

 I_{PEAK} vs Temperature **$R_{DS(ON)}$ of PMOS/NMOS vs Temperature****Operating Waveforms****Efficiency vs I_{LOAD} , $L = 10\mu$ H****Efficiency vs V_{IN} for $I_{LOAD} = 100mA$, $L = 10\mu$ H****Efficiency vs V_{IN} for $V_{OUT} = 3.3V$, $L = 10\mu$ H****Efficiency vs I_{LOAD} , $L = 100\mu$ H****Efficiency vs V_{IN} for $I_{LOAD} = 100mA$, $L = 100\mu$ H****Efficiency vs V_{IN} for $V_{OUT} = 3.3V$, $L = 100\mu$ H**

PIN FUNCTIONS

PZ1 (Pin 1): Input connection for piezoelectric element or other AC source (used in conjunction with PZ2).

PZ2 (Pin 2): Input connection for piezoelectric element or other AC source (used in conjunction with PZ1).

CAP (Pin 3): Internal rail referenced to V_{IN} to serve as gate drive for buck PMOS switch. A $1\mu\text{F}$ capacitor should be connected between CAP and V_{IN} . This pin is not intended for use as an external system rail.

V_{IN} (Pin 4): Rectified Input Voltage. A capacitor on this pin serves as an energy reservoir and input supply for the buck regulator. The V_{IN} voltage is internally clamped to a maximum of 20V (typical).

SW (Pin 5): Switch Pin for the Buck Switching Regulator. A $10\mu\text{H}$ or larger inductor should be connected from SW to V_{OUT} .

V_{OUT} (Pin 6): Sense pin used to monitor the output voltage and adjust it through internal feedback.

V_{IN2} (Pin 7): Internal low voltage rail to serve as gate drive for buck NMOS switch. Also serves as a logic high rail for output voltage select bits D0 and D1. A $4.7\mu\text{F}$ capacitor should be connected from V_{IN2} to GND. This pin is not intended for use as an external system rail.

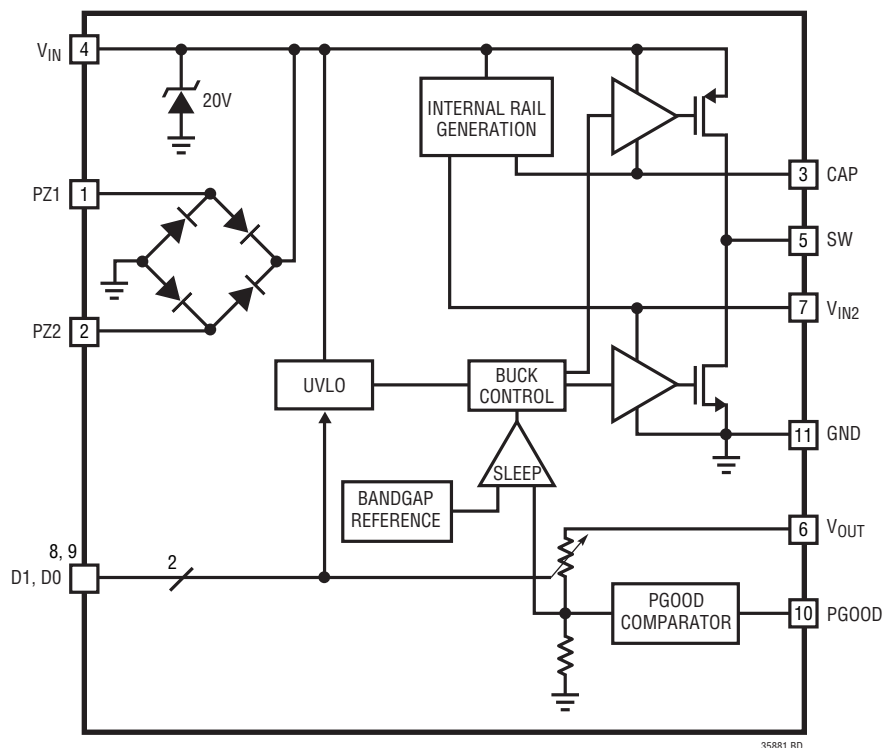
D1 (Pin 8): Output Voltage Select Bit. D1 should be tied high to V_{IN2} or low to GND to select desired V_{OUT} (see Table 1).

D0 (Pin 9): Output Voltage Select Bit. D0 should be tied high to V_{IN2} or low to GND to select desired V_{OUT} (see Table 1).

PGOOD (Pin 10): Power good output is logic high when V_{OUT} is above 92% of the target value. The logic high is referenced to the V_{OUT} rail.

GND (Exposed Pad Pin 11): Ground. The Exposed Pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3588-1.

BLOCK DIAGRAM



OPERATION

The LTC3588-1 is an ultralow quiescent current power supply designed specifically for energy harvesting and/or low current step-down applications. The part is designed to interface directly to a piezoelectric or alternative A/C power source, rectify a voltage waveform and store harvested energy on an external capacitor, bleed off any excess power via an internal shunt regulator, and maintain a regulated output voltage by means of a nanopower high efficiency synchronous buck regulator.

Internal Bridge Rectifier

The LTC3588-1 has an internal full-wave bridge rectifier accessible via the differential PZ1 and PZ2 inputs that rectifies AC inputs such as those from a piezoelectric element. The rectified output is stored on a capacitor at the V_{IN} pin and can be used as an energy reservoir for the buck converter. The low-loss bridge rectifier has a total drop of about 400mV with typical piezo generated currents ($\sim 10\mu A$). The bridge is capable of carrying up to 50mA. One side of the bridge can be operated as a single-ended DC input. PZ1 and PZ2 should never be shorted together when the bridge is in use.

Undervoltage Lockout (UVLO)

When the voltage on V_{IN} rises above the UVLO rising threshold the buck converter is enabled and charge is transferred from the input capacitor to the output capacitor. A wide ($\sim 1V$) UVLO hysteresis window is employed with a lower threshold approximately 300mV above the selected regulated output voltage to prevent short cycling during buck power-up. When the input capacitor voltage is depleted below the UVLO falling threshold the buck converter is disabled. Extremely low quiescent current (450nA typical) in UVLO allows energy to accumulate on the input capacitor in situations where energy must be harvested from low power sources.

Internal Rail Generation

Two internal rails, CAP and V_{IN2} , are generated from V_{IN} and are used to drive the high side PMOS and low side NMOS of the buck converter, respectively. Additionally the V_{IN2} rail serves as logic high for output voltage select bits D0 and D1. The V_{IN2} rail is regulated at 4.8V above GND while the CAP rail is regulated at 4.8V below V_{IN} . These are not intended to be used as external rails. Bypass capacitors are connected to the CAP and V_{IN2} pins to serve as energy reservoirs for driving the buck switches. When V_{IN} is below 4.8V, V_{IN2} is equal to V_{IN} and CAP is held at GND. Figure 1 shows the ideal V_{IN} , V_{IN2} and CAP relationship.

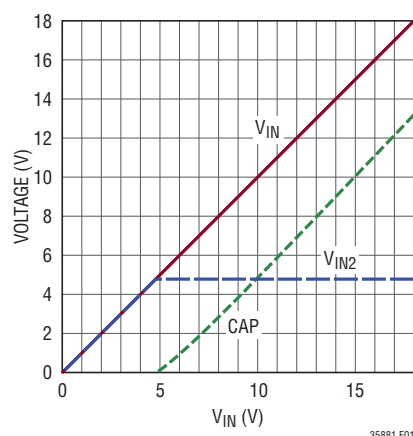


Figure 1. Ideal V_{IN} , V_{IN2} and CAP Relationship

Buck Operation

The buck regulator uses a hysteretic voltage algorithm to control the output through internal feedback from the V_{OUT} sense pin. The buck converter charges an output capacitor through an inductor to a value slightly higher than the regulation point. It does this by ramping the inductor current up to 260mA through an internal PMOS switch and then ramping it down to 0mA through an internal NMOS switch. This efficiently delivers energy to the output capacitor. The ramp rate is determined by V_{IN} , V_{OUT} , and the inductor value. If the input voltage falls below the UVLO falling threshold

OPERATION

before the output voltage reaches regulation, the buck converter will shut off and will not be turned on until the input voltage again rises above the UVLO rising threshold. During this time the output voltage will be loaded by less than 100nA. When the buck brings the output voltage into regulation the converter enters a low quiescent current sleep state that monitors the output voltage with a sleep comparator. During this operating mode load current is provided by the buck output capacitor. When the output voltage falls below the regulation point the buck regulator wakes up and the cycle repeats. This hysteretic method of providing a regulated output reduces losses associated with FET switching and maintains an output at light loads. The buck delivers a minimum of 100mA of average load current when it is switching.

When the sleep comparator signals that the output has reached the sleep threshold the buck converter may be in the middle of a cycle with current still flowing through the inductor. Normally both synchronous switches would turn off and the current in the inductor would freewheel to zero through the NMOS body diode. The LTC3588-1 keeps the NMOS switch on during this time to prevent the conduction loss that would occur in the diode if the NMOS were off. If the PMOS is on when the sleep comparator trips the NMOS will turn on immediately in order to ramp down the current. If the NMOS is on it will be kept on until the current reaches zero.

Though the quiescent current when the buck is switching is much greater than the sleep quiescent current, it is still a small percentage of the average inductor current which results in high efficiency over most load conditions. The buck operates only when sufficient energy has been accumulated in the input capacitor and the length of time the converter needs to transfer energy to the output is much less than the time it takes to accumulate energy. Thus, the buck operating quiescent current is averaged over a long period of time so that the total average quiescent current is low. This feature accommodates sources that harvest small amounts of ambient energy.

Four selectable voltages are available by tying the output select bits, D0 and D1, to GND or V_{IN2} . Table 1 shows the four D0/D1 codes and their corresponding output voltages.

Table 1. Output Voltage Selection

D1	D0	V_{OUT}	V_{OUT} QUIESCENT CURRENT (I_{VOUT})
0	0	1.8V	44nA
0	1	2.5V	62nA
1	0	3.3V	81nA
1	1	3.6V	89nA

The internal feedback network draws a small amount of current from V_{OUT} as listed in Table 1.

Power Good Comparator

A power good comparator produces a logic high referenced to V_{OUT} on the PGOOD pin the first time the converter reaches the sleep threshold of the programmed V_{OUT} , signaling that the output is in regulation. The PGOOD pin will remain high until V_{OUT} falls to 92% of the desired regulation voltage. Several sleep cycles may occur during this time. Additionally, if PGOOD is high and V_{IN} falls below the UVLO falling threshold, PGOOD will remain high until V_{OUT} falls to 92% of the desired regulation point. This allows output energy to be used even if the input is lost. Figure 2 shows the behavior for $V_{OUT} = 3.6V$ and no load. At $t = 75s$ V_{IN} becomes high impedance and is discharged by the quiescent current of the LTC3588-1 and through servicing V_{OUT} which is discharged by its own leakage current. V_{IN} crosses UVLO falling but PGOOD remains high until V_{OUT} decreases to 92% of the desired regulation point. The PGOOD pin is designed to drive a microprocessor or other chip I/O and is not intended to drive higher current loads such as an LED.

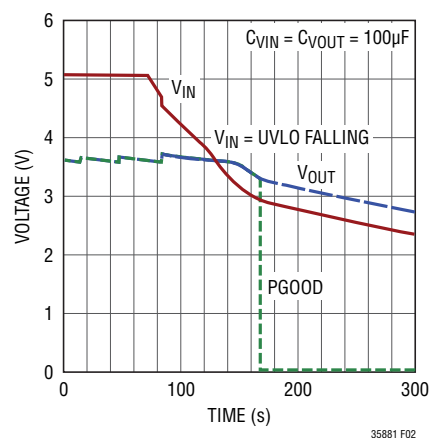


Figure 2. PGOOD Operation During Transition to UVLO

OPERATION

The D0/D1 inputs can be switched while in regulation as shown in Figure 3. If V_{OUT} is programmed to a voltage with a PGOOD falling threshold above the old V_{OUT} , PGOOD will transition low until the new regulation point is reached. When V_{OUT} is programmed to a lower voltage, PGOOD will remain high through the transition.

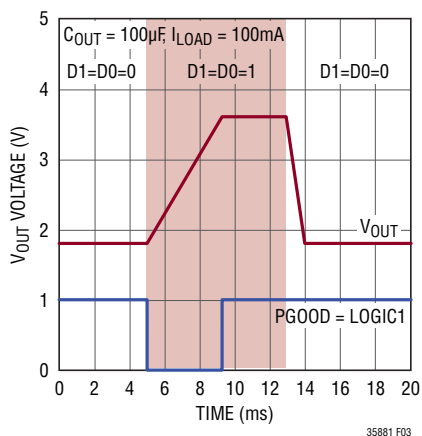


Figure 3. PGOOD Operation During D0/D1 Transition

Energy Storage

Harvested energy can be stored on the input capacitor or the output capacitor. The wide input range takes advantage of the fact that energy storage on a capacitor is proportional to the square of the capacitor voltage. After the output voltage is brought into regulation any excess energy is stored on the input capacitor and its voltage increases. When a load exists at the output the buck can efficiently transfer energy stored at a high voltage to the regulated output. While energy storage at the input utilizes the high voltage at the input, the load current is limited to what the buck converter can supply. If larger loads need to be serviced the output capacitor can be sized to support a larger current for some duration. For example, a current burst could begin when PGOOD goes high and would continuously deplete the output capacitor until PGOOD went low.

APPLICATIONS INFORMATION

Introduction

The LTC3588-1 harvests ambient vibrational energy through a piezoelectric element in its primary application. Common piezoelectric elements are PZT (lead zirconate titanate) ceramics, PVDF (polyvinylidene fluoride) polymers, or other composites. Ceramic piezoelectric elements exhibit a piezoelectric effect when the crystal structure of the ceramic is compressed and internal dipole movement produces a voltage. Polymer elements comprised of long-chain molecules produce a voltage when flexed as molecules repel each other. Ceramics are often used under direct pressure while a polymer can be flexed more readily. A wide range of piezoelectric elements are available and produce a variety of open-circuit voltages and short-circuit currents. Typically the open-circuit voltage and short-circuit currents increase with available vibrational energy as shown in Figure 4. Piezoelectric elements can be placed in series or in parallel to achieve desired open-circuit voltages.

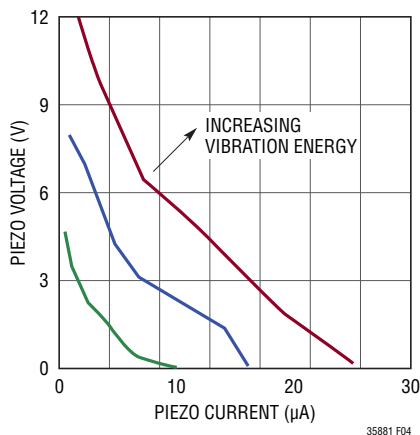


Figure 4. Typical Piezoelectric Load Lines for Piezo Systems T220-A4-503X

The LTC3588-1 is well-suited to a piezoelectric energy harvesting application. The 20V input protective shunt can accommodate a variety of piezoelectric elements. The low quiescent current of the LTC3588-1 enables efficient energy accumulation from piezoelectric elements which can have short-circuit currents on the order of tens of microamps. Piezoelectric elements can be obtained from manufacturers listed in Table 2.

Table 2. Piezoelectric Element Manufacturers

Advanced Cerametrics	www.advancedcerametrics.com
Piezo Systems	www.piezo.com
Measurement Specialties	www.meas-spec.com
PI (Physik Instrumente)	www.pi-usa.us
MIDE Technology Corporation	www.mide.com
Morgan Technical Ceramics	www.morganelectroceramics.com

The LTC3588-1 will gather energy and convert it to a useable output voltage to power microprocessors, wireless sensors, and wireless transmission components. Such a wireless sensor application may require much more peak power than a piezoelectric element can produce. However, the LTC3588-1 accumulates energy over a long period of time to enable efficient use for short power bursts. For continuous operation, these bursts must occur with a low duty cycle such that the total output energy during the burst does not exceed the average source power integrated over an energy accumulation cycle. For piezoelectric inputs the time between cycles could be minutes, hours, or longer depending on the selected capacitor values and the nature of the vibration source.

APPLICATIONS INFORMATION

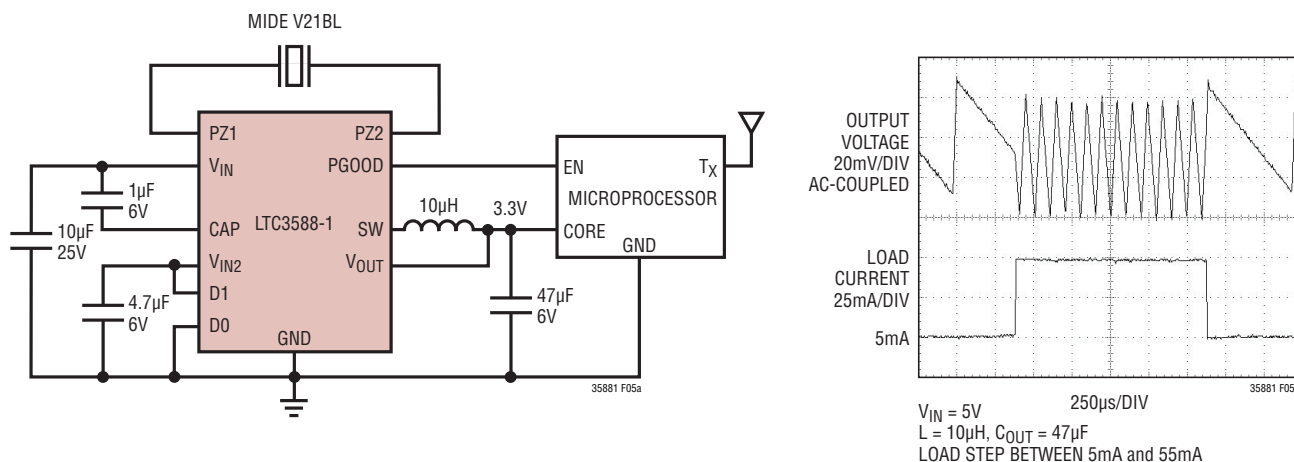


Figure 5. 3.3V Piezoelectric Energy Harvester Powering a Microprocessor with a Wireless Transmitter and 50mA Load Step Response

PGOOD Signal

The PGOOD signal can be used to enable a sleeping microprocessor or other circuitry when V_{OUT} reaches regulation, as shown in Figure 5. Typically V_{IN} will be somewhere between the UVLO thresholds at this time and a load could only be supported by the output capacitor. Alternatively, waiting a period of time after PGOOD goes high would let the input capacitor accumulate more energy allowing load current to be maintained longer as the buck efficiently transfers that energy to the output. While active, a microprocessor may draw a small load when operating sensors, and then draw a large load to transmit data. Figure 5 shows the LTC3588-1 responding smoothly to such a load step.

Input and Output Capacitor Selection

The input and output capacitors should be selected based on the energy needs and load requirements of the application. In every case the V_{IN} capacitor should be rated to withstand the highest voltage ever present at V_{IN} . For 100mA or smaller loads, storing energy at the input takes advantage of the high voltage input since the buck can deliver 100mA average load current efficiently to the output. The input capacitor should then be sized to store enough energy to provide output power for the length of time required. This may involve using a large capacitor, letting V_{IN} charge to a high voltage, or both. Enough energy

should be stored on the input so that the buck does not reach the UVLO falling threshold which would halt energy transfer to the output. In general:

$$P_{LOAD} t_{LOAD} = \frac{1}{2} \eta C_{IN} (V_{IN}^2 - V_{UVLOFALLING}^2)$$

$$V_{UVLOFALLING} \leq V_{IN} \leq V_{SHUNT}$$

The above equation can be used to size the input capacitor to meet the power requirements of the output for the desired duration. Here η is the average efficiency of the buck converter over the input range and V_{IN} is the input voltage when the buck begins to switch. This equation may overestimate the input capacitor necessary since load current can deplete the output capacitor all the way to the lower PGOOD threshold. It also assumes that the input source charging has a negligible effect during this time.

The duration for which the regulator sleeps depends on the load current and the size of the output capacitor. The sleep time decreases as the load current increases and/or as the output capacitor decreases. The DC sleep hysteresis window is $\pm 12mV$ around the programmed output voltage. Ideally this means that the sleep time is determined by the following equation:

$$t_{SLEEP} = C_{OUT} \frac{24mV}{I_{LOAD}}$$

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This is true for output capacitors on the order of 100 μ F or larger, but as the output capacitor decreases towards 10 μ F delays in the internal sleep comparator along with the load current may result in the V_{OUT} voltage slewing past the ± 12 mV thresholds. This will lengthen the sleep time and increase V_{OUT} ripple. A capacitor less than 10 μ F is not recommended as V_{OUT} ripple could increase to an undesirable level.

If transient load currents above 100mA are required then a larger capacitor can be used at the output. This capacitor will be continuously discharged during a load condition and the capacitor can be sized for an acceptable drop in V_{OUT} :

$$C_{OUT} = (I_{LOAD} - I_{BUCK}) \frac{t_{LOAD}}{V_{OUT+} - V_{OUT-}}$$

Here V_{OUT+} is the value of V_{OUT} when PGOOD goes high and V_{OUT-} is the desired lower limit of V_{OUT} . I_{BUCK} is the average current being delivered from the buck converter, typically $I_{PEAK}/2$.

A standard surface mount ceramic capacitor can be used for C_{OUT} , though some applications may be better suited to a low leakage aluminum electrolytic capacitor or a supercapacitor. These capacitors can be obtained from manufacturers such as Vishay, Illinois Capacitor, AVX, or CAP-XX.

Inductor

The buck is optimized to work with an inductor in the range of 10 μ H to 22 μ H, although inductor values outside this range may yield benefits in some applications. For typical applications, a value of 10 μ H is recommended. A larger inductor will benefit high voltage applications by increasing the on-time of the PMOS switch and improving efficiency by reducing gate charge loss. Choose an inductor with a DC current rating greater than 350mA. The DCR of the inductor can have an impact on efficiency as it is a source of loss. Trade-offs between price, size, and

DCR should be evaluated. Table 3 lists several inductors that work well with the LTC3588-1.

Table 3. Recommended Inductors for LTC3588-1

INDUCTOR TYPE	L (μ H)	MAX I_{DC} (mA)	MAX DCR (Ω)	SIZE in mm (L x W x H)	MANUFACTURER
CDRH2D18/LDNP	10	430	0.180	3 x 3 x 2	Sumida
107AS-100M	10	650	0.145	2.8 x 3 x 1.8	Toko
EPL3015-103ML	10	350	0.301	2.8 x 3 x 1.5	Coilcraft
MLP3225s100L	10	1000	0.130	3.2 x 2.5 x 1.0	TDK
XLP2010-163ML	10	490	0.611	2.0 x 1.9 x 1.0	Coilcraft
SLF7045T	100	500	0.250	7.0 x 7.0 x 4.5	TDK

V_{IN2} and CAP Capacitors

A 1 μ F capacitor should be connected between V_{IN} and CAP and a 4.7 μ F capacitor should be connected between V_{IN2} and GND. These capacitors hold up the internal rails during buck switching and compensate the internal rail generation circuits. In applications where the input source is limited to less than 6V, the CAP pin can be tied to GND and the V_{IN2} pin can be tied to V_{IN} as shown in Figure 6. An optional 5.6V Zener diode can be connected to V_{IN} to clamp V_{IN} in this scenario. The leakage of the Zener diode below its Zener voltage should be considered as it may be comparable to the quiescent current of the LTC3588-1. This circuit does not require the capacitors on V_{IN2} and CAP, saving components and allowing a lower voltage rating for the single V_{IN} capacitor.

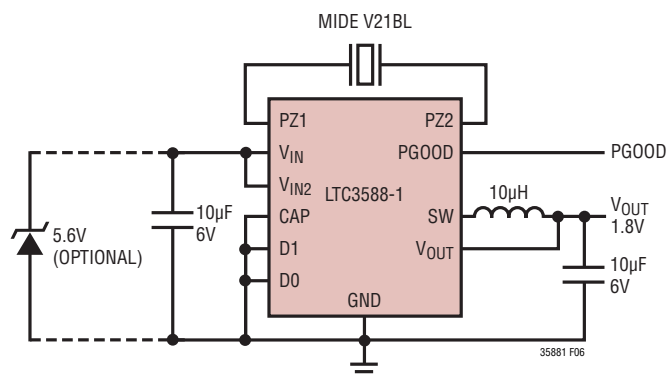


Figure 6. Smallest Solution Size 1.8V Low Voltage Input Piezoelectric Power Supply

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Additional Applications with Piezo Inputs

The versatile LTC3588-1 can be used in a variety of configurations. Figure 7 shows a single piezo source powering two LTC3588-1s simultaneously, providing capability for multiple rail systems. This setup features automatic supply sequencing as the LTC3588-1 with the lower voltage output (i.e. lower UVLO rising threshold) will come up first. As the piezo provides input power both V_{IN} rails will initially come up together, but when one output starts drawing power, only its corresponding V_{IN} will fall as the bridges of each LTC3588-1 provide isolation. Input piezo energy will then be directed to this lower voltage capacitor until both V_{IN} rails are again equal. This configuration is expandable to any number of LTC3588-1s powered by a single piezo as long as the piezo can support the sum total of the quiescent currents from each LTC3588-1.

A piezo powered LTC3588-1 can also be used in concert with a battery connected to V_{IN} to supplement the system if ambient vibrational energy ceases as shown in Figure 8. A blocking diode placed in series with the battery to V_{IN} prevents reverse current in the battery if the piezo source charges V_{IN} past the battery voltage. A 9V battery is shown, but any stack of batteries of a given chemistry can be used as long as the battery stack voltage does not exceed 18V. In this setup the presence of the piezo energy harvester can greatly increase the life of the battery. If the piezo source is removed the LTC3588-1 can serve as a standalone nanopower buck converter. In this case the bridge is unused and the blocking diode is unnecessary.

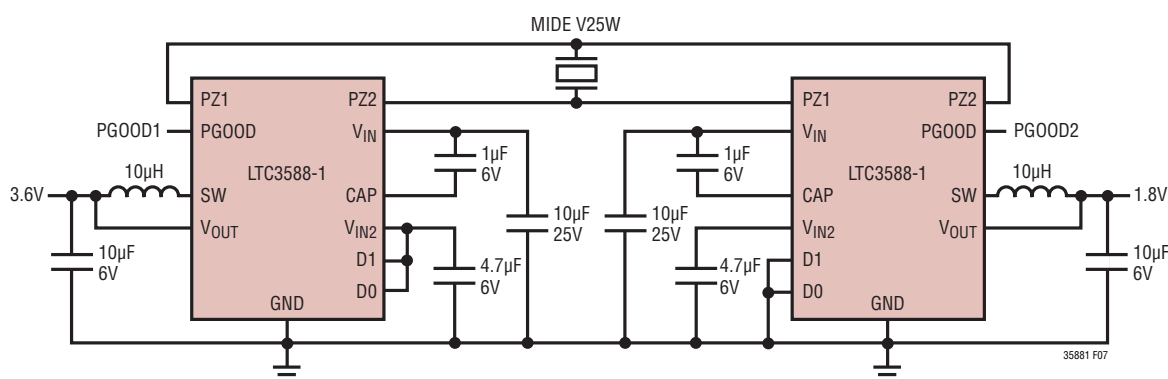


Figure 7. Dual Rail Power Supply with Single Piezo and Automatic Supply Sequencing

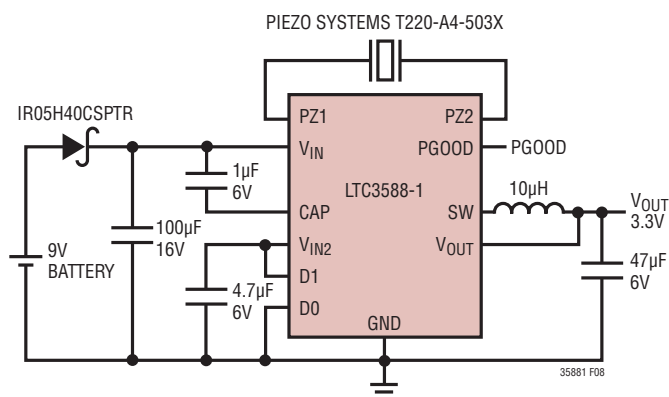


Figure 8. Piezo Energy Harvester with Battery Backup

APPLICATIONS INFORMATION

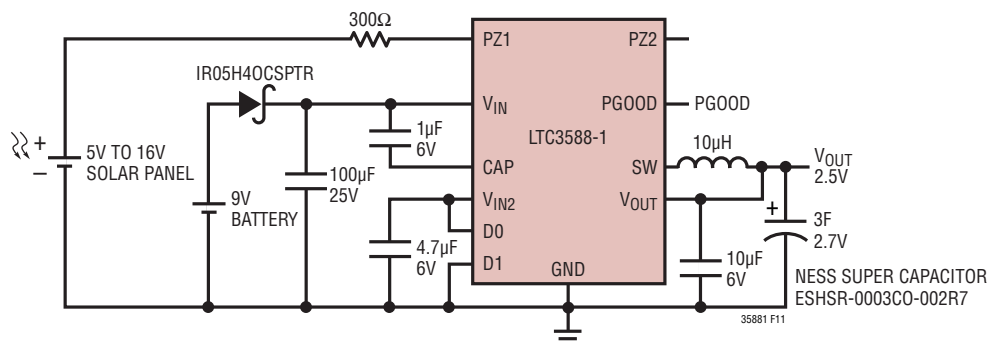


Figure 11. 5V to 16V Solar-Powered 2.5V Supply with Supercapacitor for Increased Output Energy Storage and Battery Backup

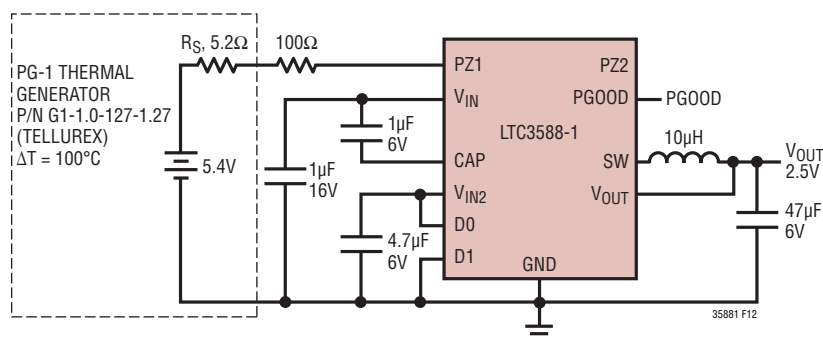


Figure 12. Thermoelectric Energy Harvester

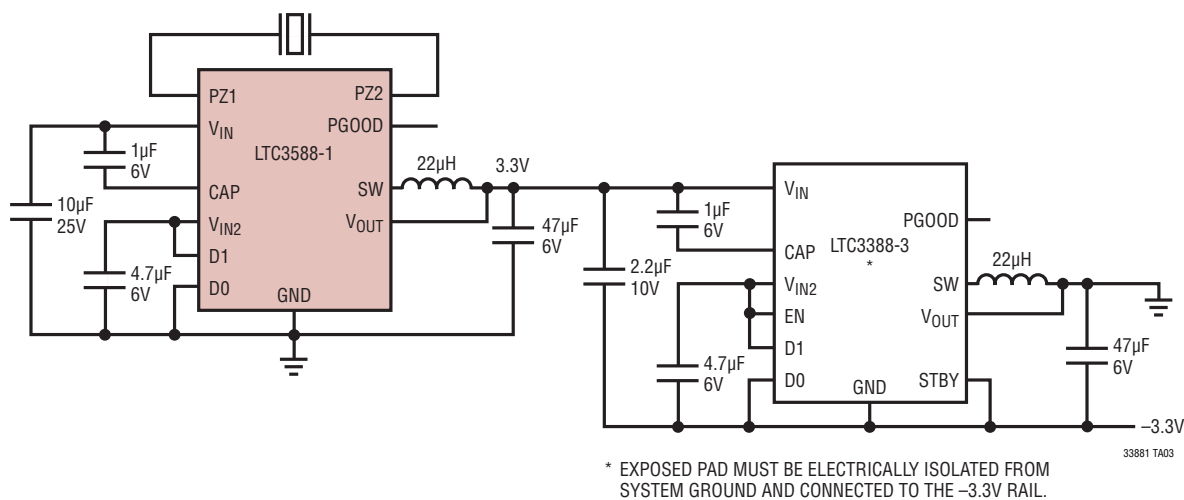
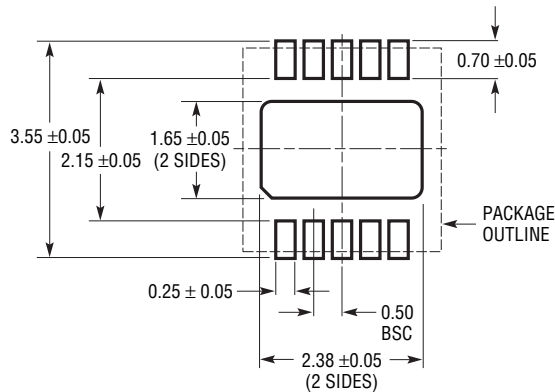


Figure 13. Piezoelectric Energy Harvester with ±3.3V Outputs

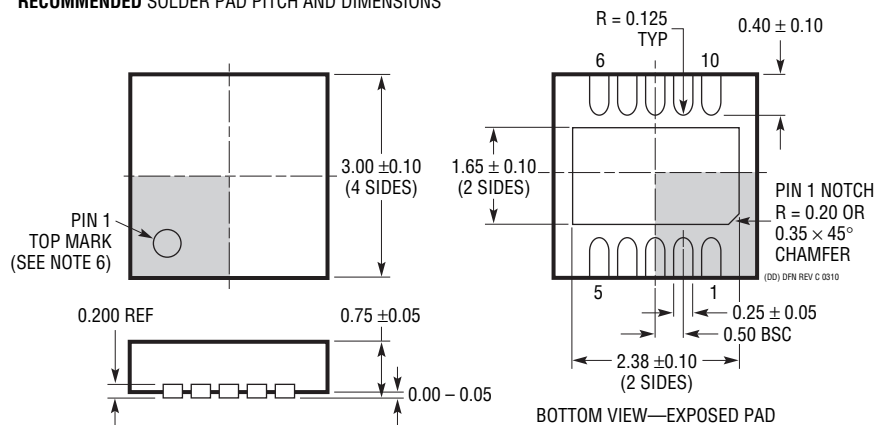
PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm x 3mm)
 (Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



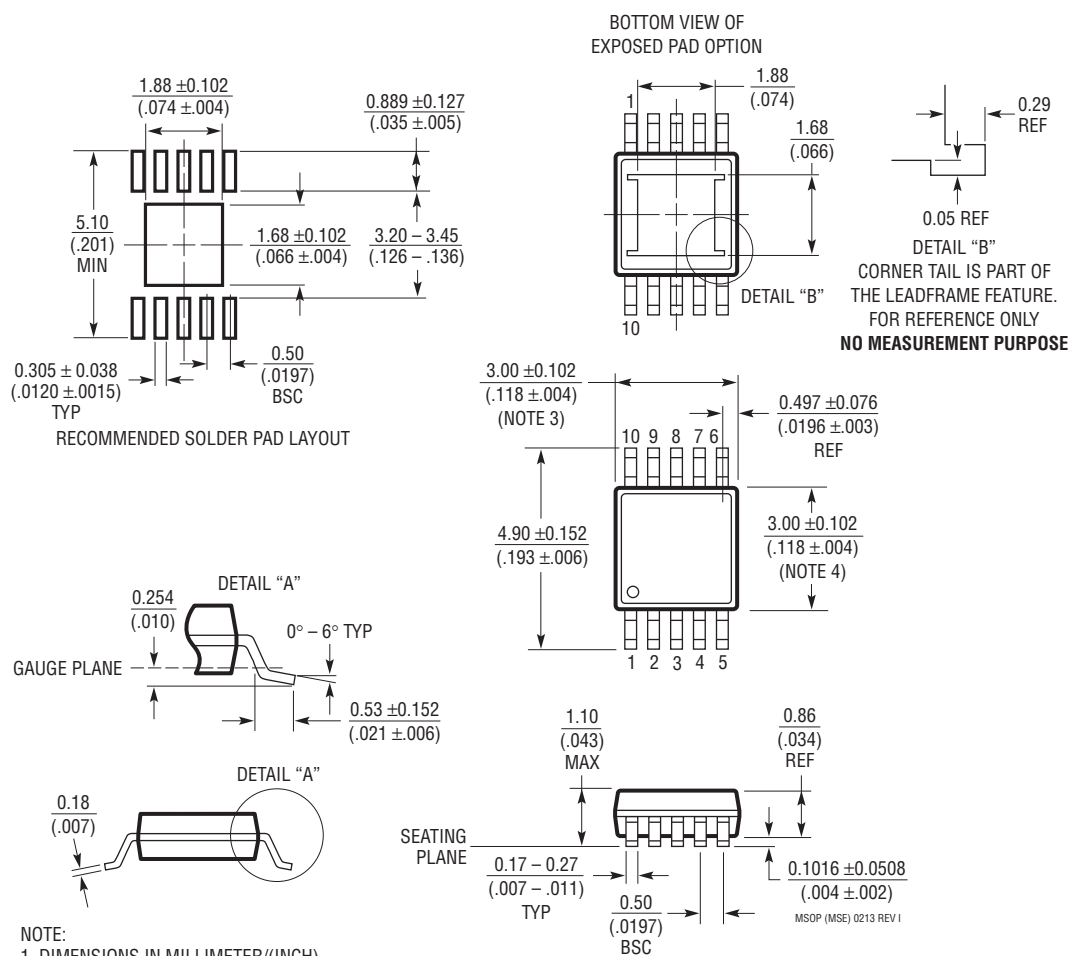
NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

MSE Package 10-Lead Plastic MSOP, Exposed Die Pad (Reference LTC DWG # 05-08-1664 Rev I)



NOTE:

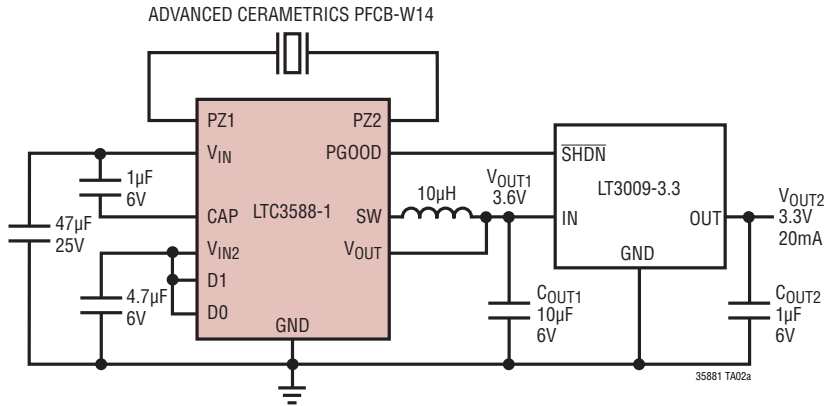
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm ($.006$) PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm ($.006$) PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm ($.004$) MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL NOT EXCEED 0.254mm ($.010$) PER SIDE.

REVISION HISTORY

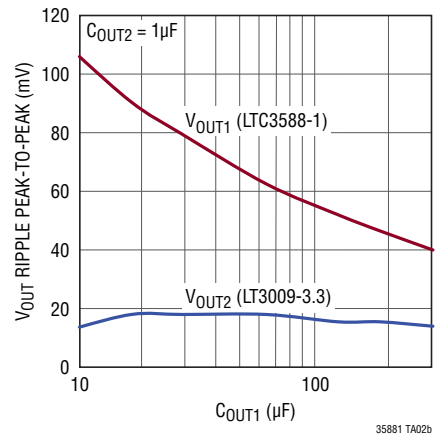
REV	DATE	DESCRIPTION	PAGE NUMBER
A	9/10	Updated/added part number on the Piezoelectric Transducer on the front and back page applications, and Figures 5, 6 and 7	1, 12, 13, 14, 20
		Updated Temperature Range in Order Information	2
		Changed $T_J = 25^\circ\text{C}$ to $T_A = 25^\circ\text{C}$ and I_{LOAD} to I_{BUCK} in Electrical Characteristics	3
		Updated Notes 2, 3 and 4	4
		Updated G21 in Typical Performance Characteristics	6
		Added Figure 13	16
		Updated Related Parts	20
B	7/14	Clarified title and Description	1
		Clarified x-axis label on Figure 1	8
		Clarified Figure 8	14
		Clarified Related Parts list	20
C	8/15	Modified C_{OUT} Equation	13

TYPICAL APPLICATION

Piezoelectric 3.3V Power Supply with LDO Post Regulator for Reduced Output Ripple



Peak-to-Peak Output Ripple vs C_{OUT1}



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1389	Nanopower Precision Shunt Voltage Reference	800nA Operating Current, 1.25V/2.5V/4.096V
LTC1540	Nanopower Comparator with Reference	0.3µA I _Q , Drives 0.01µF, Adjustable Hysteresis, 2V to 11V Input Range
LT3009	3µA I _Q , 20mA Low Dropout Linear Regulator	Low 3µA I _Q , 1.6V to 20V Range, 20mA Output Current
LTC3388-1/ LTC3388-3	20V High Efficiency Nanopower Step-Down Regulator	860nA I _Q in Sleep, 2.7V to 20V Input, V _{OUT} : 1.2V to 5.0V, Enable and Standby Pins
LTC3588-2	Nanopower Energy Harvesting Power Supply	<1µA I _Q in Regulation, UVLO Rising = 16V, UVLO Falling = 14V, V _{OUT} = 3.45V, 4.1V, 4.5V 5.0V
LT3652	Power Tracking 2A Battery Charger for Solar Power	MPPT for Solar, 4.95V to 32V, Up to 2A Charge Current
LT3970	40V, 350mA Step-Down Regulator with 2.5µA I _Q	Integrated Boost and Catch Diodes, 4.2V to 40V Operating Range
LT3971	38V, 1.2A, 2MHz Step-Down Regulator with 2.8µA I _Q	4.3V to 38V Operating Range, Low Ripple Burst Mode [®] Operation
LT3991	55V, 1.2A 2MHz Step-Down Regulator with 2.8µA I _Q	4.3V to 55V Operating Range, Low Ripple Burst Mode Operation
LTC3631	45V, 100mA, Synchronous Step-Down Regulator with 12µA I _Q	4.5V to 45V Operating Range, Overvoltage Lockout Up to 60V
LTC3642	45V, 50mA, Synchronous Step-Down Regulator with 12µA I _Q	4.5V to 45V Operating Range, Overvoltage Lockout Up to 60V
LTC3330	Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Life Extender	V _{IN} : 2.7V to 20V, BAT: 1.8V to 5.5V, 750nA I _Q , 5mm × 5mm QFN-32 Package
LTC3331	Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Charger	V _{IN} : 2.7V to 20V, BAT: Up to 4.2V, Shunt Charger, Low Battery Disconnect, 950nA I _Q , 5mm × 5mm QFN-32 Package