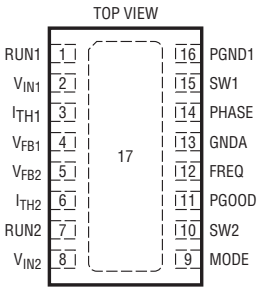
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN1}, V_{IN2} Voltages ..... –0.3V to 6V
MODE, SW1, SW2, RUN1,
RUN2, V_{FB1}, V_{FB2}, PHASE, FREQ,
I_{TH1}, I_{TH2} Voltages ..... –0.3V to (V_{IN1}/V_{IN2} + 0.3V)
$V_{IN1} – V_{IN2}$, $V_{IN2} – V_{IN1}$ 0.3V
PGOOD Voltage ..... –0.3V to 6V

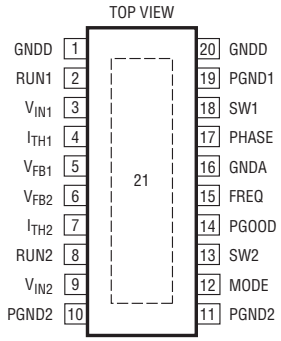
Operating Ambient Temperature Range
(Note 2) ..... –40°C to 85°C
Junction Temperature (Notes 7, 8) ..... 125°C
Storage Temperature Range
DFN Package ..... –65°C to 125°C
TSSOP Package ..... –65°C to 150°C

PIN CONFIGURATION



DHC PACKAGE
16-LEAD (3mm × 5mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 17) IS PGND2/GNDD, MUST BE SOLDERED TO PCB



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS PGND2/GNDD, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3417EDHC#PBF	LTC3417EDHC#TRPBF	3417	16-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3417EFE#PBF	LTC3417EFE#TRPBF	LTC3417EFE	20-Lead Plastic TSSOP	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3417EDHC	LTC3417EDHC#TR	3417	16-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3417EFE	LTC3417EFE#TR	LTC3417EFE	20-Lead Plastic TSSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1}, V_{IN2}	Operating Voltage Range	V_{IN1} = V_{IN2}	●	2.25		5.5	V
I_{FB1}, I_{FB2}	Feedback Pin Input Current	(Note 3)				±0.1	µA
V_{FB1}, V_{FB2}	Feedback Voltage	(Note 3)	●	0.784	0.8	0.816	V
$\Delta V_{LINEREG}$	Reference Voltage Line Regulation. %/V is the Percentage Change in V_{OUT} with a Change in V_{IN}	V_{IN} = 2.25V to 5V (Note 3)			0.04	0.2	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	I_{TH1}, I_{TH2} = 0.36V (Note 3) I_{TH1}, I_{TH2} = 0.84V (Note 3)			0.02 –0.02	0.2 –0.2	% %

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$g_{m(EA)}$	Error Amplifier Transconductance	I_{TH1}, $I_{TH2(PINLOAD)}$ = ±5µA (Note 3)			1400		µS
I_S	Input DC Supply Current (Note 4) Active Mode	V_{FB1} = V_{FB2} = 0.75V, V_{MODE} = V_{IN}, V_{RUN1} = V_{RUN2} = V_{IN}			400	600	µA
	Half Active Mode (V_{RUN2} = 0V, 1.4A Only)	V_{FB1} = 0.75V, V_{MODE} = V_{IN}, V_{RUN1} = V_{IN}			260	400	µA
	Half Active Mode (V_{RUN1} = 0V, 800mA Only)	V_{FB2} = 0.75V, V_{MODE} = V_{IN}, V_{RUN2} = V_{IN}			260	400	µA
	Both Channels in Sleep Mode	V_{FB1} = V_{FB2} = 1V, V_{MODE} = V_{IN}, V_{RUN1} = V_{RUN2} = V_{IN}			125	250	µA
	Shutdown	V_{RUN1} = V_{RUN2} = 0V			0.1	1	µA
f_{OSC}	Oscillator Frequency	V_{FREQ} = V_{IN} V_{FREQ}: R_T = 143k V_{FREQ}: Resistor (Note 6)		1.2 0.85	1.5 1	1.8 1.25 4	MHz MHz MHz
I_{LIM1}	Peak Switch Current Limit on SW1 (1.4A)			1.8	2.25		A
I_{LIM2}	Peak Switch Current Limit on SW2 (800mA)			1	1.2		A
$R_{DS(ON)1}$	SW1 Top Switch On-Resistance (1.4A) SW1 Bottom Switch On-Resistance	V_{IN1} = 3.6V (Note 5) V_{IN1} = 3.6V (Note 5)			0.088 0.084		Ω Ω
$R_{DS(ON)2}$	SW2 Top Switch On-Resistance (800mA) SW2 Bottom Switch On-Resistance	V_{IN2} = 3.6V (Note 5) V_{IN2} = 3.6V (Note 5)			0.16 0.15		Ω Ω
$I_{SW1(LKG)}$	Switch Leakage Current SW1 (1.4A)	V_{IN1} = 6V, V_{ITH1} = 0V, V_{RUN1} = 0V			0.01	1	µA
$I_{SW2(LKG)}$	Switch Leakage Current SW2 (800mA)	V_{IN2} = 6V, V_{ITH2} = 0V, V_{RUN2} = 0V			0.01	1	µA
V_{UVLO}	Undervoltage Lockout Threshold	V_{IN1}, V_{IN2} Ramping Down V_{IN1}, V_{IN2} Ramping Up		1.9 1.95	2.07 2.12	2.2 2.25	V V
T_{PGOOD}	Threshold for Power Good. Percentage Deviation from V_{FB} Steady State (Typically 0.8V)	V_{FB1} or V_{FB2} Ramping Up V_{FB1} or V_{FB2} Ramping Down			–6 –6		% %
R_{PGOOD}	Power Good Pull-Down On-Resistance				160	300	Ω
V_{RUN1}, V_{RUN2}	RUN1, RUN2 Threshold			0.3	0.85	1.5	V
V_{PHASE}	PHASE Threshold High-CMOS Levels			V_{IN} –0.5			V
	PHASE Threshold Low-CMOS Levels					0.5	V
I_{RUN1}, I_{RUN2}, I_{PHASE}, I_{MODE}	RUN1, RUN2, PHASE and MODE Leakage Current	V_{IN} = 6V, V_{PIN} = 3V			0.01	1	µA
VTL_{MODE}	MODE Threshold Voltage Low					0.5	V
VTH_{MODE}	MODE Threshold Voltage High			V_{IN} –0.5			V
VTH_{FREQ}	FREQ Threshold Voltage High			V_{IN} –0.5			V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3417 is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 85°C operating ambient temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC3417 is tested in feedback loop which servos V_{FB1} to the midpoint for the error amplifier (V_{ITH1} = 0.6V) and V_{FB2} to the midpoint for the error amplifier (V_{ITH2} = 0.6V).

Note 4: Total supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 5: Switch on-resistance is guaranteed by design and test correlation on the DHC package and by final test correlation on the FE package.

Note 6: Variable frequency operation with resistor is guaranteed by design but not production tested and is subject to duty cycle limitations.

Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 8: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formula:

LTC3417EDHC: $T_J = T_A + (P_D \bullet 43°C/W)$

LTC3417EFE: $T_J = T_A + (P_D \bullet 38°C/W)$

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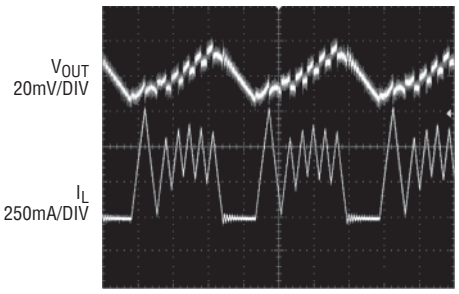
TYPICAL PERFORMANCE CHARACTERISTICS

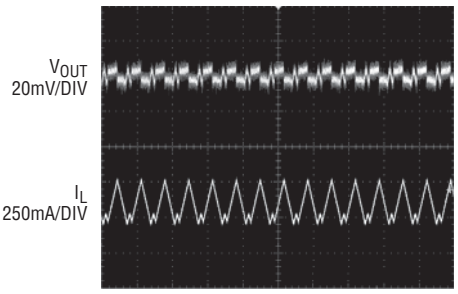
OUT1 Burst Mode Operation



V_{IN} = 3.6V 2µs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 100mA
REFER TO FIGURE 4

3417 G01

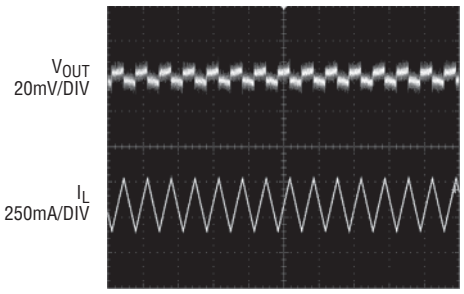
OUT1 Pulse Skipping Mode Operation



V_{IN} = 3.6V 2µs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 100mA
REFER TO FIGURE 4

3417 G02

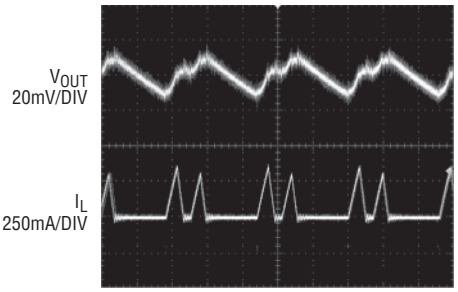
OUT1 Forced Continuous Mode Operation



V_{IN} = 3.6V 2µs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 100mA
REFER TO FIGURE 4

3417 G03

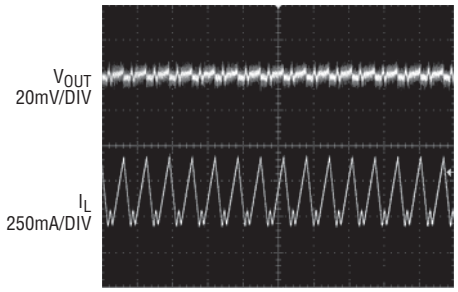
OUT2 Burst Mode Operation



V_{IN} = 3.6V 2µs/DIV
V_{OUT} = 2.5V
I_{LOAD} = 60mA
REFER TO FIGURE 4

3417 G04

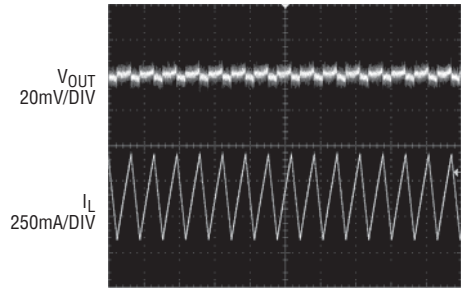
OUT2 Pulse Skipping Mode Operation



V_{IN} = 3.6V 2µs/DIV
V_{OUT} = 2.5V
I_{LOAD} = 60mA
REFER TO FIGURE 4

3417 G05

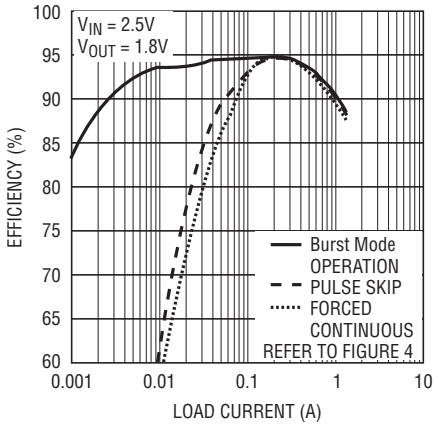
OUT2 Forced Continuous Mode Operation



V_{IN} = 3.6V 2µs/DIV
V_{OUT} = 2.5V
I_{LOAD} = 60mA
REFER TO FIGURE 4

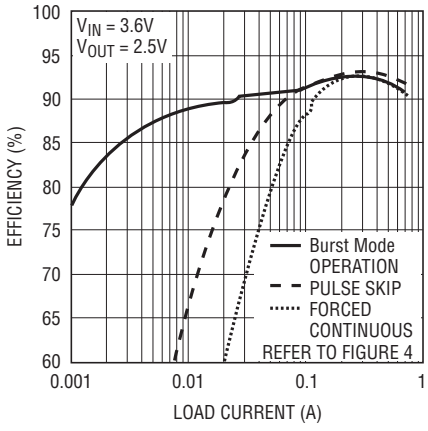
3417 G06

OUT1 Efficiency vs Load Current



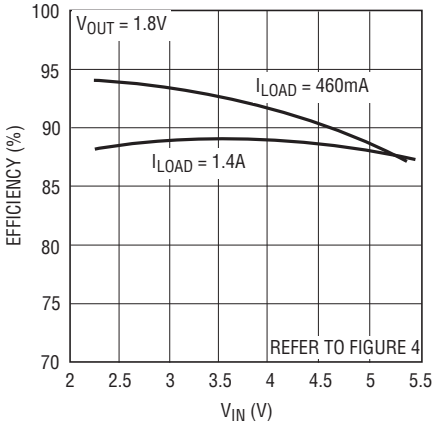
3417 G07

OUT2 Efficiency vs Load Current



3417 G08

OUT1 Efficiency vs V_{IN} (Burst Mode Operation)



3417 G09

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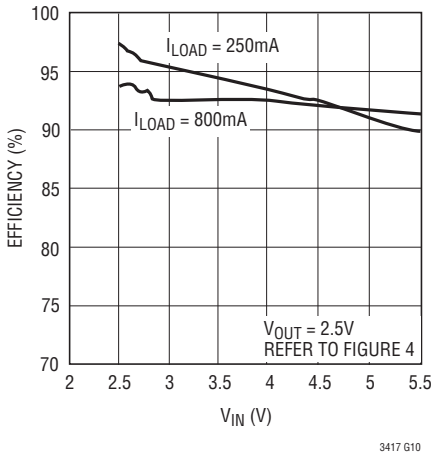
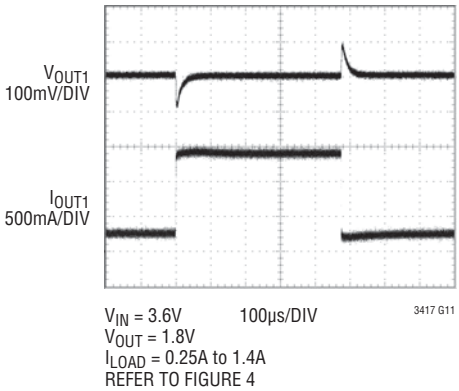
TYPICAL PERFORMANCE CHARACTERISTICS

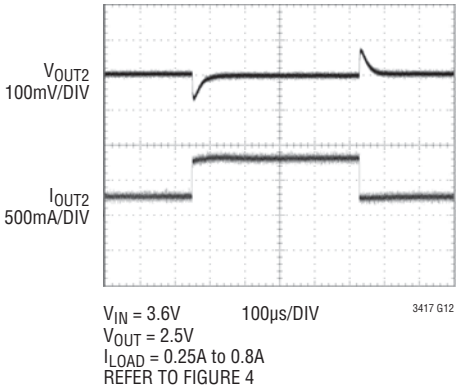
OUT2 Efficiency vs V_{IN} (Pulse Skipping Mode)



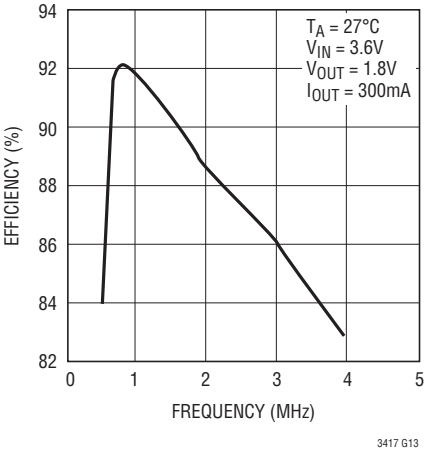
Load Step OUT1



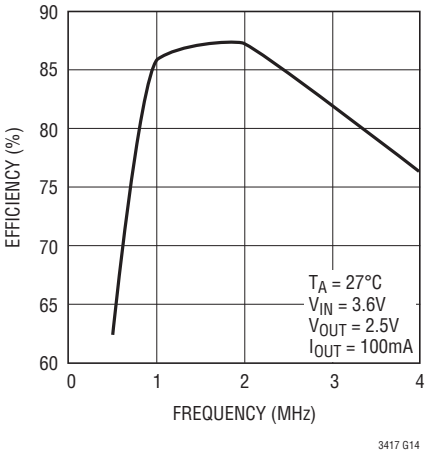
Load Step OUT2



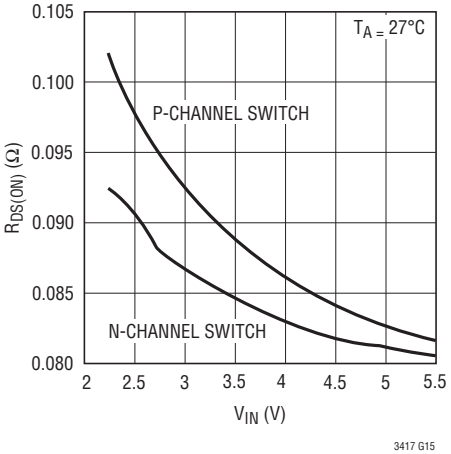
Efficiency vs Frequency OUT1



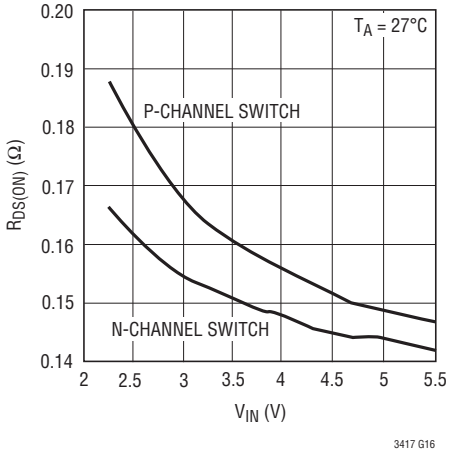
Efficiency vs Frequency OUT2



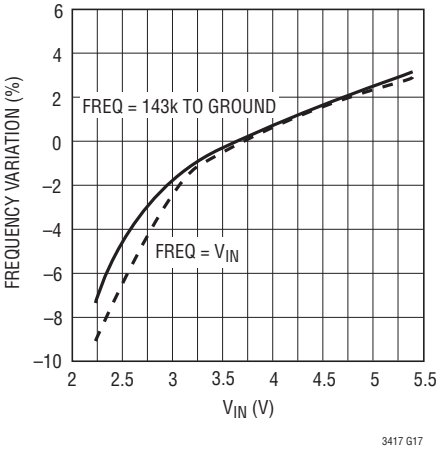
$R_{DS(ON)}$ vs V_{IN} OUT1



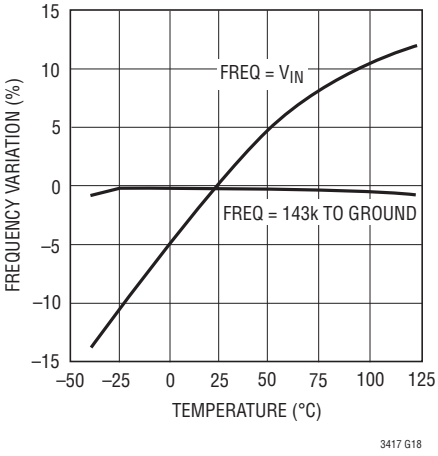
$R_{DS(ON)}$ vs V_{IN} OUT2



Frequency vs V_{IN}



Frequency vs Temperature



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PIN FUNCTIONS (DFN/TSOP)

RUN1 (Pin 1/Pin 2): Enable for 1.4A Regulator. When at Logic 1, 1.4A regulator is running. When at 0V, 1.4A regulator is off. When both RUN1 and RUN2 are at 0V, the part is in shutdown.

V_{IN1} (Pin 2/Pin 3): Supply Pin for P-channel Switch of 1.4A Regulator.

I_{TH1} (Pin 3/Pin 4): Error Amplifier Compensation Point for 1.4A Regulator. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 1.5V.

V_{FB1} (Pin 4/Pin 5): Receives the feedback voltage from external resistive divider across the 1.4A regulator output. Nominal voltage for this pin is 0.8V.

V_{FB2} (Pin 5/Pin 6): Receives the feedback voltage from external resistive divider across the 800mA regulator output. Nominal voltage for this pin is 0.8V.

I_{TH2} (Pin 6/Pin 7): Error Amplifier Compensation Point for 800mA regulator. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 1.5V.

RUN2 (Pin 7/Pin 8): Enable for 800mA Regulator. When at Logic 1, 800mA regulator is running. When at 0V, 800mA regulator is off. When both RUN1 and RUN2 are at 0V, the part is in shutdown.

V_{IN2} (Pin 8/Pin 9): Supply Pin for P-channel Switch of 800mA Regulator and Supply for Analog Circuitry.

MODE (Pin 9/Pin 12): Mode Selection Pin. This pin controls the operation of the device. When the voltage on the MODE pin is $>(V_{IN} – 0.5V)$, Burst Mode operation is selected. When the voltage on the MODE pin is <0.5V, pulse skipping mode is selected. When the MODE pin is held at $V_{IN}/2$, forced continuous mode is selected.

SW2 (Pin 10/Pin 13): Switch Node Connection to the Inductor for the 800mA Regulator. This pin swings from V_{IN2} to PGND2.

PGOOD (Pin 11/Pin 14): Power Good Pin. This common drain-logic output is pulled to GND when the output voltage of either regulator is –6% of regulation. If either RUN1 or RUN2 is low (the respective regulator is in sleep mode and therefore the output voltage is low), then PGOOD reflects the regulation of the running regulator.

FREQ (Pin 12/Pin 15): Frequency Set Pin. When FREQ is at V_{IN}, internal oscillator runs at 1.5MHz. When a resistor is connected from this pin to ground, the internal oscillator frequency can be varied from 0.6MHz to 4MHz.

GNDA (Pin 13/Pin 16): Analog Ground Pin for Internal Analog Circuitry.

PHASE (Pin 14/Pin 17): Selects 800mA regulator switching phase with respect to 1.4A regulator switching. Set to V_{IN}, the 1.4A regulator and the 800mA regulator are in phase. When PHASE is at 0V, the 1.4A regulator and the 800mA regulator are switching 180 degrees out-of-phase.

SW1 (Pin 15/Pin 18): Switch Node Connection to the Inductor for the 1.4A Regulator. This pin swings from V_{IN1} to PGND1.

PGND1 (Pin 16/Pin 19): Ground for SW1 N-channel Driver.

PGND2, GNDD (Pins 1,10,11,20): TSSOP Package Only. Ground for SW2 N-channel driver and digital ground for circuit.

Exposed Pad (Pin 17/Pin 21): PGND2, GNDD. Ground for SW2 N-channel driver and digital ground for circuit. The Exposed Pad must be soldered to PCB ground.

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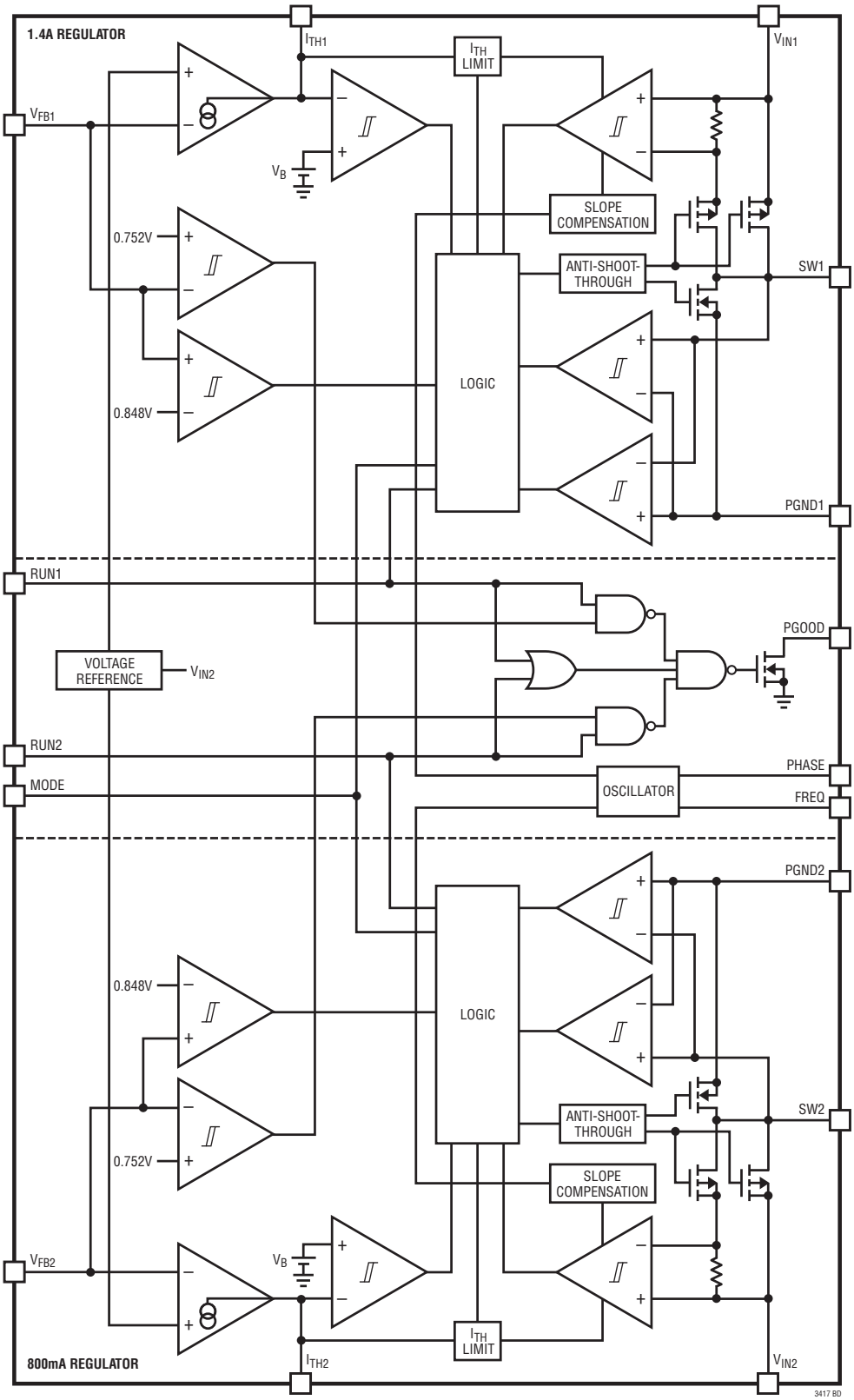
FUNCTIONAL DIAGRAM



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OPERATION

The LTC3417 uses a constant frequency, current mode architecture. Both channels share the same clock frequency. The PHASE pin sets whether the channels are running in-phase or out of phase. The operating frequency is determined by connecting the FREQ pin to V_{IN} for 1.5MHz operation or by connecting a resistor from FREQ to ground for a frequency from 0.6MHz to 4MHz. To suit a variety of applications, the MODE pin allows the user to trade off noise for efficiency.

The output voltages are set by external dividers returned to the V_{FB1} and V_{FB2} pins. An error amplifier compares the divided output voltage with a reference voltage of 0.8V and adjusts the peak inductor current accordingly. Undervoltage comparators will pull the PGOOD output low when either output voltage is 6% below its targeted value.

Main Control Loop

For each regulator, during normal operation, the P-channel MOSFET power switch is turned on at the beginning of a clock cycle when the V_{FB} voltage is below the reference voltage. The current into the inductor and the load increases until the current limit is reached. The switch turns off and energy stored in the inductor flows through the bottom N-channel MOSFET switch into the load until the next clock cycle.

The peak inductor current is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier. This amplifier compares the V_{FB} pin to the 0.8V reference. When the load current increases the V_{FB} voltage decreases slightly below the reference. This decrease causes the error amplifier to increase the I_{TH} voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the RUN pin to ground. A digital soft-start is enabled after shutdown, which will slowly ramp the peak inductor current up over 1024 clock cycles.

Low Current Operation

Three modes are available to control the operation of the LTC3417 at low currents. Each of the three modes automatically switch from continuous operation to the selected mode when the load current is low.

To optimize efficiency, Burst Mode operation can be selected. When the load is relatively light, the LTC3417 automatically switches into Burst Mode operation in which the PMOS switches operate intermittently based on load demand. By running cycles periodically, the switching losses, which are dominated by the gate charge losses of the power MOSFETs, are minimized. The main control loop is interrupted when the output voltage reaches the desired regulated value. The hysteresis voltage comparator trips when I_{TH} is below 0.24V, shutting off the switch and reducing the power. The output capacitor and the inductor supply the power to the load until I_{TH} exceeds 0.31V, turning on the switch and the main control loop which starts another cycle.

For lower output voltage ripple at low currents, pulse skipping mode can be used. In this mode, the LTC3417 continues to switch at constant frequency down to very low currents, where it will begin skipping pulses used to control the power MOSFETs.

Finally, in forced continuous mode, the inductor current is constantly cycled creating a fixed output voltage ripple at all output current levels. This feature is desirable in telecommunications since the noise is a constant frequency and is thus easy to filter out. Another advantage of this mode is that the regulator is capable of both sourcing current into a load and sinking some current from the output.

The mode selection for the LTC3417 is set using the MODE pin. The MODE pin sets the mode for both the 800mA and the 1.4A step-down DC/DC converters.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases to 100%. In this dropout condition, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal P-channel MOSFET and inductor.

Low Supply Operation

The LTC3417 incorporates an undervoltage lockout circuit which shuts down the part when the input voltage drops below about 2.07V to prevent unstable operation.

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APPLICATIONS INFORMATION

A general LTC3417 application circuit is shown in Figure 4. External component selection is driven by the load requirement, and begins with the selection of the inductors L1 and L2. Once L1 and L2 are chosen, C_{IN}, C_{OUT1} and C_{OUT2} can be selected.

Operating Frequency

Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency, f_O, of the LTC3417 is determined by pulling the FREQ pin to V_{IN} for 1.5MHz operation or by connecting an external resistor from FREQ to ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_T = \frac{1.61 \bullet 10^{11}}{f_O}(\Omega) - 16.586k\Omega$$

for 0.6MHz ≤ f_O ≤ 4MHz. Alternatively, use Figure 1 to select the value for R_T.

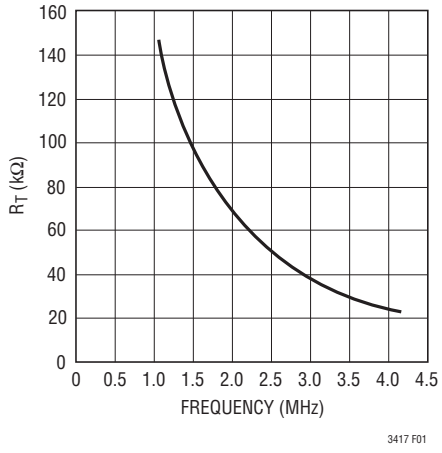

Figure 1. Frequency vs R_T

The maximum operating frequency is also constrained by the minimum on-time and duty cycle. This can be calculated as:

$$f_{O(MAX)} \approx 6.67\left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)(MHz)$$

The minimum frequency is limited by leakage and noise coupling due to the large resistance of R_T.

Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current, ΔI_L, decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

$$\Delta I_L = \frac{V_{OUT}}{f_O \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple, greater core losses and lower output current capability.

A reasonable starting point for setting ripple current is $\Delta I_L = 0.35 I_{LOAD(MAX)}$, where $I_{LOAD(MAX)}$ is the maximum current output. The largest ripple, ΔI_L, occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \frac{V_{OUT}}{f_O \bullet \Delta I_L}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor value will also have an effect on Burst Mode operation. The transition from low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductor values will cause the burst frequency to increase.

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Inductor Core Selection

Different core materials and shapes will change the size/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements of any radiated field/EMI requirements than on what the LTC3417 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3417 applications.

Input Capacitor (C_{IN}) Selection

In continuous mode, the input current of the converter can be approximated by the sum of two square waves with duty cycles of approximately V_{OUT1}/V_{IN} and V_{OUT2}/V_{IN}. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. Some capacitors have a de-rating spec for maximum RMS current. If the capacitor being used has this requirement, it is necessary to calculate the maximum RMS current. The RMS current calculation is different if the part is used in "in phase" or "out of phase".

For "in phase", there are two different equations:

$V_{OUT1} > V_{OUT2}$:

$$I_{RMS} = \sqrt{2 \bullet I_1 \bullet I_2 \bullet D2(1-D1) + I_2^2(D2-D2^2) + I_1^2(D1-D1^2)}$$

$V_{OUT2} > V_{OUT1}$:

$$I_{RMS} = \sqrt{2 \bullet I_1 \bullet I_2 \bullet D1(1-D2) + I_2^2(D2-D2^2) + I_1^2(D1-D1^2)}$$

where:

$$D1 = \frac{V_{OUT1}}{V_{IN}} \text{ and } D2 = \frac{V_{OUT2}}{V_{IN}}$$

Table 1

MANUFACTURER	PART NUMBER	VALUE (µH)	MAX DC CURRENT (A)	DCR	DIMENSIONS L × W × H (mm)
L1 on OUT1					
Toko	A920CY-1R5M-D62CB	1.5	2.8	0.014	6 × 6 × 2.5
	A918CY-1R5M-D62LCB	1.5	2.9	0.018	6 × 6 × 2
Coilcraft	DO1608C-152ML	1.5	2.6	0.06	6.6 × 4.5 × 2.9
Sumida	CDRH4D22/HP 1R5	1.5	3.9	0.031	5 × 5 × 2.4
	CDRH2D18/HP 1R7	1.7	1.8	0.035	3.2 × 3.2 × 2
Midcom	DUP-1813-1R4R	1.4	5.5	0.033	4.3 × 4.8 × 3.5
L2 on OUT2					
Toko	A915AY-2R0M-D53LC	2.0	3.9	0.027	5 × 5 × 3
Coilcraft	DO1608C-222ML	2.2	2.3	0.07	6.6 × 4.5 × 2.9
Sumida	CDRH3D16/HP 2R2	2.2	1.75	0.047	4 × 4 × 1.8
	CDRH2D18/HP 2R2	2.2	1.6	0.035	3.2 × 3.2 × 2
Midcom	DUP-1813-2R2R	2.2	3.9	0.047	4.3 × 4.8 × 3.5

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When D1 = D2 then the equation simplifies to:

$$I_{RMS} = (I_1 + I_2)\sqrt{D(1-D)}$$

or

$$I_{RMS} = (I_1 + I_2)\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where the maximum average output currents I_1 and I_2 equal the respective peak currents minus half the peak-to-peak ripple currents:

$$I_1 = I_{LIM1} - \frac{\Delta I_{L1}}{2}$$

$$I_2 = I_{LIM2} - \frac{\Delta I_{L2}}{2}$$

These formula have a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = (I_1 + I_2)/2$. This simple worst case is commonly used to determine the highest I_{RMS}.

For "out of phase" operation, the ripple current can be lower than the "in phase" current.

In the "out of phase" case, the maximum I_{RMS} does not occur when $V_{OUT1} = V_{OUT2}$. The maximum typically occurs when $V_{OUT1} - V_{IN}/2 = V_{OUT2}$ or when $V_{OUT2} - V_{IN}/2 = V_{OUT1}$. As a good rule of thumb, the amount of worst case ripple is about 75% of the worst case ripple in the "in phase" mode. Also note that when $V_{OUT1} = V_{OUT2} = V_{IN}/2$ and $I_1 = I_2$, the ripple is zero.

Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1µF to 1µF ceramic capacitor is also recommended on V_{IN} for high frequency decoupling, when not using an all ceramic capacitor solution.

Output Capacitor (C_{OUT1} and C_{OUT2}) Selection

The selection of C_{OUT1} and C_{OUT2} is driven by the required ESR to minimize voltage ripple and load step transients. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR_{COUT} + \frac{1}{8 \bullet f_O \bullet C_{OUT}} \right)$$

where f_O = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage, since ΔI_L increases with input voltage. With $\Delta I_L = 0.35 I_{LOAD(MAX)}$, the output ripple will be less than 100mV at maximum V_{IN} and f_O = 1MHz with:

$$ESR_{COUT} < 150m\Omega$$

Once the ESR requirements for C_{OUT} have been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement, except for an all ceramic solution.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and dry tantalum capacitors are all available in surface mount packages. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR(size) product of any aluminum electrolytic at a somewhat higher price. Special polymer capacitors, such as Sanyo POSCAP, offer very low ESR, but have a lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it has a larger ESR and it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface tantalums, available in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors have a significantly larger ESR, and are often used in extremely cost-sensitive applications provided that consideration

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is given to ripple current ratings and long term reliability. Ceramic capacitors have the lowest ESR and cost but also have the lowest capacitance density, high voltage and temperature coefficient and exhibit audible piezoelectric effects. In addition, the high Q of ceramic capacitors along with trace inductance can lead to significant ringing. Other capacitor types include the Panasonic specialty polymer (SP) capacitors.

In most cases, 0.1µF to 1µF of ceramic capacitors should also be placed close to the LTC3417 in parallel with the main capacitors for high frequency decoupling.

Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Because the LTC3417 control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size. When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Great care must be taken when using only ceramic input and output capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 2 to 3 times the linear droop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx 2.5 \frac{\Delta I_{OUT}}{f_O \bullet V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 10µF ceramic capacitor is usually enough for these conditions.

Setting the Output Voltage

The LTC3417 develops a 0.8V reference voltage between the feedback pins, V_{FB1} and V_{FB2}, and the signal ground as shown in Figure 4. The output voltages are set by two resistive dividers according to the following formulas:

$$V_{OUT1} \approx 0.8V\left(1+\frac{R1}{R2}\right)$$

$$V_{OUT2} \approx 0.8V\left(1+\frac{R3}{R4}\right)$$

Keeping the current small (<5µA) in these resistors maximizes efficiency, but making the current too small may allow stray capacitance to cause noise problems and reduce the phase margin of the error amp loop.

To improve the frequency response, a feed-forward capacitor, C_F, may also be used. Great care should be taken to route the V_{FB} node away from noise sources, such as the inductor or the SW line.

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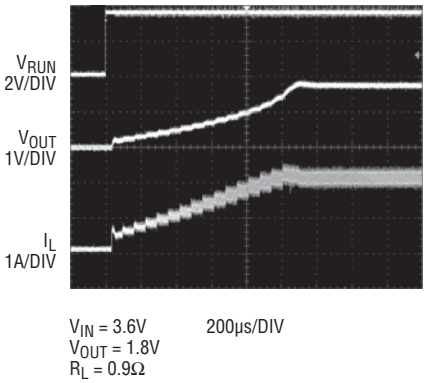

Figure 2. Digital Soft-Start Out1

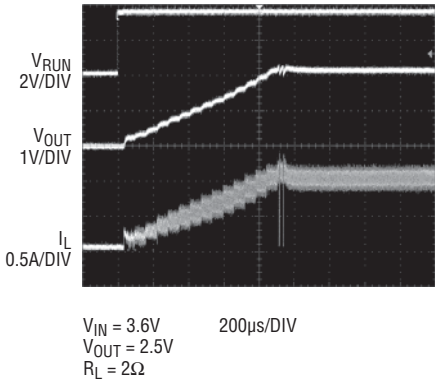

Figure 3. Digital Soft-Start Out2

Soft-Start

Soft-start reduces surge currents from V_{IN} by gradually increasing the peak inductor current. Power supply sequencing can also be accomplished by controlling the I_{TH} pin. The LTC3417 has an internal digital soft-start for each regulator output, which steps up a clamp on I_{TH} over 1024 clock cycles, as can be seen in Figures 2 and 3. As the voltage on I_{TH} ramps through its operating range, the internal peak current limit is also ramped at a proportional linear rate.

Mode Selection

The MODE pin provides mode selection. Connecting this pin to V_{IN} enables Burst Mode operation for both regulators, which provides the best low current efficiency at the cost of a higher output voltage ripple. When MODE is connected to ground, pulse skipping operation is selected for both regulators, which provides the lowest output voltage and current ripple at the cost of low current efficiency. Applying a voltage that is more than 1V from either supply results in forced continuous mode for both regulators, which creates a fixed output ripple and allows the sinking of some current (about $1/2\Delta I_L$). Since the switching noise is constant in this mode, it is also the easiest to filter out. In many cases, the output voltage can be simply connected to the MODE pin, selecting the forced continuous mode except at start-up.

Checking Transient Response

The I_{TH} pin compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the I_{TH} pin not only allows optimization of the control loop behavior, but also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time, and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated using the percentage of overshoot seen at this pin or by examining the rise time at this pin.

The I_{TH} external components shown in the Figure 4 circuit will provide an adequate starting point for most applications. The series RC filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because of various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of overall loop stability without breaking the feedback loop.

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Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR_{COUT}$, where ESR_{COUT} is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with R_{ITH} and the bandwidth of the loop increases with decreasing C_{ITH}. If R_{ITH} is increased by the same factor that C_{ITH} is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, feedforward capacitors, C1 and C2, can be added to improve the high frequency response, as shown in Figure 4. Capacitor C1 provides phase lead by creating a high frequency zero with R1 which improves the phase margin for the 1.4A SW1 channel. Capacitor C2 provides phase lead by creating a high frequency zero with R3 which improves the phase margin for the 800mA SW2 channel.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76.

Although a buck regulator is capable of providing the full output current in dropout, it should be noted that as the input voltage V_{IN} drops toward V_{OUT}, the load step capability does decrease due to the decreasing voltage across the inductor. Applications that require large load step capability near dropout should use a different topology such as SEPIC, Zeta, or single inductor, positive buck boost.

In some applications, a more severe transient can be caused by switching in loads with large (>1µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft- starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (P1 + P2 + P3 + \ldots)$$

where P1, P2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3417 circuits: 1) LTC3417 I_S current, 2) switching losses, 3) I^2R losses, 4) other losses.

1) The I_S current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. I_S current results in a small (<0.1%) loss that increases with V_{IN}, even at no load.

2) The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge moves from V_{IN} to ground. The resulting charge over the switching period is a current out of V_{IN} that is typically much larger than the DC bias current. The gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

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3) I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and the external inductor, R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)}TOP)(DC) + (R_{DS(ON)}BOT)(1 – DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

$$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$$

where R_L is the resistance of the inductor.

4) Other "hidden" losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR_{COUT} at the switching frequency. Other losses including diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

The LTC3417 requires the package Exposed Pad (PGND2/GNDD pin) to be well soldered to the PC board. This gives the DFN and TSSOP packages exceptional thermal properties, compared to similar packages of this size, making it difficult in normal operation to exceed the maximum junction temperature of the part. In a majority of applications, the LTC3417 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3417 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both switches in both regulators will be turned off and the SW nodes will become high impedance.

To prevent the LTC3417 from exceeding its maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_{RISE} + T_{AMBIENT}$$

As an example, consider the case when the LTC3417 is in dropout in both regulators at an input voltage of 3.3V with load currents of 1.4A and 800mA. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{DS(ON)}$ resistance of the 1.4A P-channel switch is 0.09Ω and the $R_{DS(ON)}$ of the 800mA P-channel switch is 0.163Ω. The power dissipated by the part is:

$$PD = I_1^2 \bullet R_{DS(ON)1} + I_2^2 \bullet R_{DS(ON)2}$$

$$PD = 1.4^2 \bullet 0.09 + 0.8^2 \bullet 0.163$$

$$PD = 281mW$$

The DFN package junction-to-ambient thermal resistance, θ_{JA}, is about 43°C/W. Therefore, the junction temperature of the regulator operating in a 70°C ambient temperature is approximately:

$$T_J = 0.281 \bullet 43 + 70$$

$$T_J = 82.1°C$$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. However, we can safely assume that the actual junction temperature will not exceed the absolute maximum junction temperature of 125°C.

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Design Example

As a design example, consider using the LTC3417 in a portable application with a Li-Ion battery. The battery provides a V_{IN} from 2.5V to 4.2V. One output requires 1.8V at 1.3A in active mode, and 1mA in standby mode. The other output requires 2.5V at 700mA in active mode, and 500µA in standby mode. Since both loads still need power in standby, Burst Mode operation is selected for good low load efficiency (MODE = V_{IN}).

First, determine what frequency should be used. Higher frequency results in a lower inductor value for a given ΔI_L (ΔI_L is estimated as $0.35I_{LOAD(MAX)}$). Reasonable values for wire wound surface mount inductors are usually in the range of 1µH to 10µH.

CONVERTER OUTPUT	$I_{LOAD(MAX)}$	ΔI_L
SW1	1.4A	490mA
SW2	800mA	280mA

Using the 1.5MHz frequency setting (FREQ = V_{IN}), we get the following equations for L_1 and L_2:

$$L1 = \frac{1.8V}{1.5MHz \bullet 490mA}\left(1 - \frac{1.8V}{4.2V}\right) = 1.4\mu H$$

Use 1.5µH.

$$L2 = \frac{2.5V}{1.5MHz \bullet 280mA}\left(1 - \frac{2.5V}{4.2V}\right) = 2.4\mu H$$

Use 2.2µH.

C_{OUT} selection is based on load step droop instead of ESR requirements. For a 5% output droop:

$$C_{OUT1} = 2.5 \bullet \frac{1.3A}{1.5MHz(5\% \bullet 1.8V)} = 24\mu F$$

$$C_{OUT2} = 2.5 \bullet \frac{0.7A}{1.5MHz(5\% \bullet 2.5V)} = 9.3\mu F$$

The closest standard values are 22µF and 10µF.

The output voltages can now be programmed by choosing the values of R1, R2, R3, and R4. To maintain high efficiency, the current in these resistors should be kept small. Choosing 2µA with the 0.8V feedback voltages makes R2 and R4 equal to 400k. A close standard 1% resistor is 412k. This then makes R1 = 515k. A close standard 1% is 511k. Similarily, with R4 at 412k, R3 is equal to 875k. A close 1% resistor is 866k.

The compensation should be optimized for these components by examining the load step response, but a good place to start for the LTC3417 is with a 5.9kΩ and 2200pF filter on I_{TH1} and 2.87k and 6800pF on I_{TH2}. The output capacitor may need to be increased depending on the actual undershoot during a load step.

The PGOOD pin is a common drain output and requires a pull-up resistor. A 100k resistor is used for adequate speed. Figure 4 shows a complete schematic for this design.

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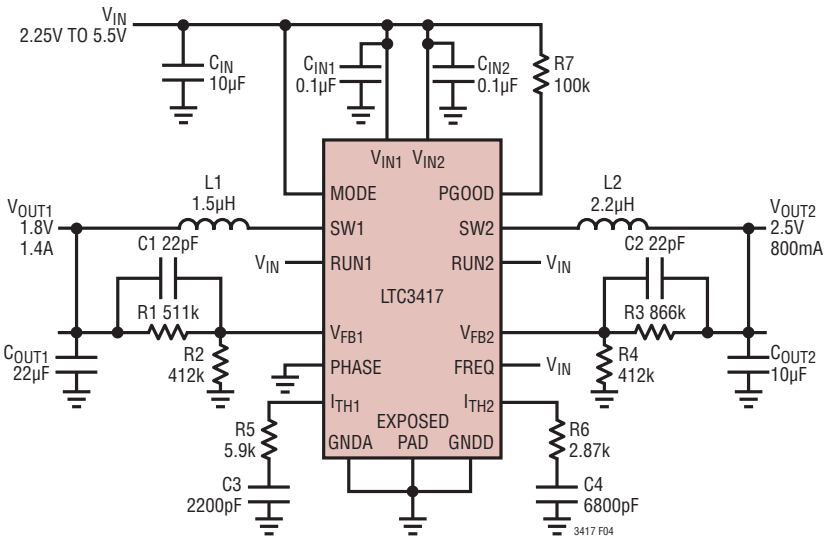

L1: MIDCOM DUS-5121-1R5R
C_{OUT1}: KEMET C1210C226K8PAC

L2: MIDCOM DUS-5121-2R2R
C_{OUT2}, C_{IN}: KEMET C1206C106K4PAC

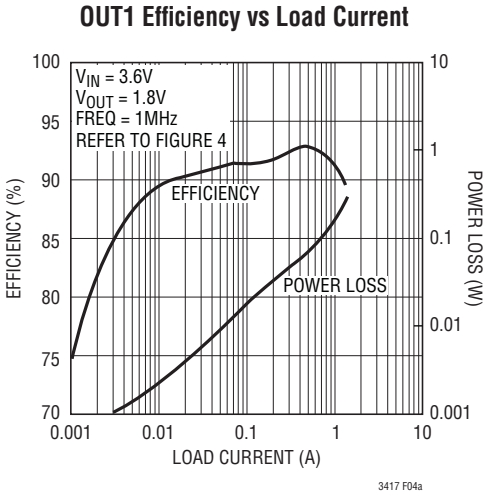

Figure 4. 1.8V at 1.4A/2.5V at 800mA Step-Down Regulators

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Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3417. These items are also illustrated graphically in the layout diagram of Figure 5. Check the following in your layout.

1. Does the capacitor C_{IN} connect to the power V_{IN1} (Pin 2), V_{IN2} (Pin 8), and PGND2/GNDD (Pin 17) as close as possible (DFN package)? It may be necessary to split C_{IN} into two capacitors. This capacitor provides the AC current to the internal power MOSFETs and their drivers.
2. Are the C_{OUT1}, L_1 and C_{OUT2}, L_2 closely connected? The (–) plate of C_{OUT1} returns current to PGND1, and the (–) plate of C_{OUT2} returns current to the PGND2/GNDD and the (–) plate of C_{IN}.
3. The resistor divider, R1 and R2, must be connected between the (+) plate of C_{OUT1} and a ground line terminated near GNDA. The resistor divider, R3 and R4, must be connected between the (+) plate of C_{OUT2} and a ground line terminated near GNDA. The feedback signals V_{FB1} and V_{FB2} should be routed away from noise components and traces, such as the SW lines, and its trace should be minimized.
4. Keep sensitive components away from the SW pins. The input capacitor C_{IN}, the compensation capacitors C_{C1}, C_{C2}, C_{ITH1} and C_{ITH2} and all resistors R1, R2, R3, R4, R_{ITH1} and R_{ITH2} should be routed away from the SW traces and the inductors L1 and L2.
5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the GNDA pin at one point which is then connected to the PGND2/GNDD pin.
6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to one of the input supplies.

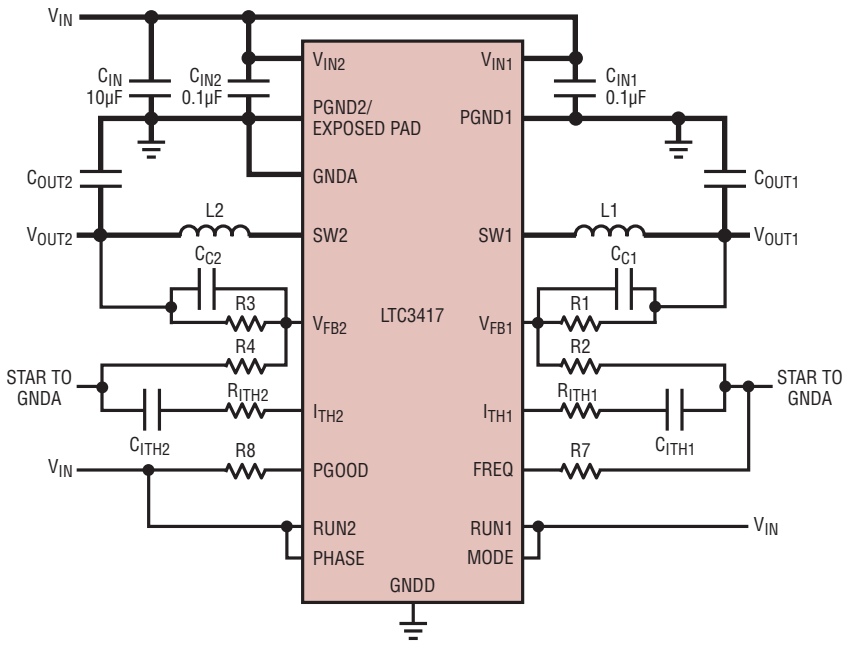

Figure 5

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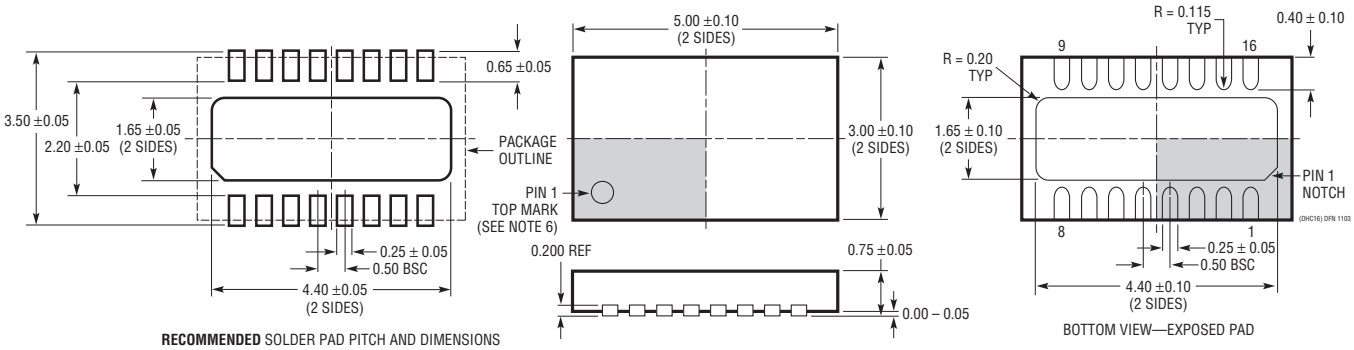
PACKAGE DESCRIPTION

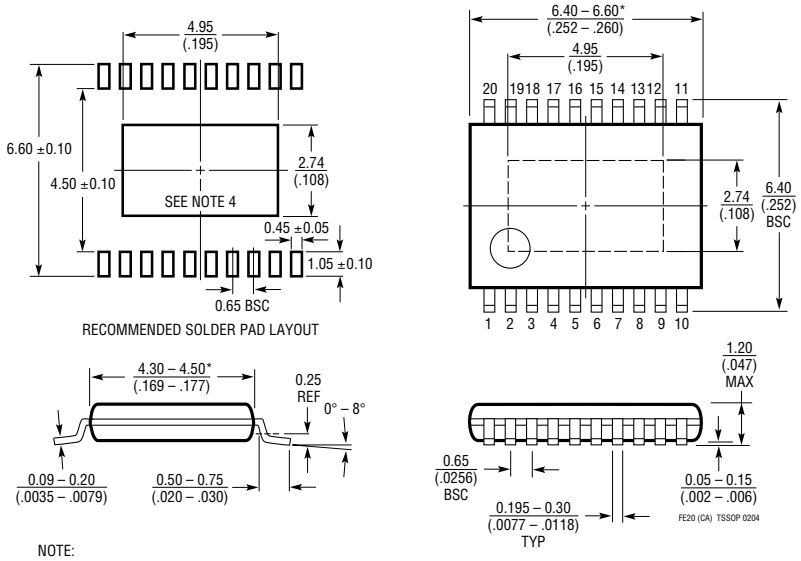
DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706)



NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)

Exposed Pad Variation CA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

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RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3404	600mA (I_{OUT}), 1.4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.7V to 6V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 10µA, I_{SD} < 1µA, MS8 Package
LTC3405/LTC3405A	300mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converters	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT™ Package
LTC3406/LTC3406B	600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converters	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT Package
LTC3407	Dual 600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MSE/DFN Packages
LTC3407-2	Dual 800mA (I_{OUT}), 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MSE/DFN Packages
LTC3409	600mA, Low V_{IN} (1.6V to 5.5V), Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 1.6V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 65µA, I_{SD} < 1µA, DFN Packages
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, MS Package
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} < 1µA, TSSOP16E Package
LTC3413	3A (I_{OUT} Sink/Source), 2MHz, Monolithic Synchronous Regulator for DDR/QDR Memory Termination	90% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = V_{REF}/2, I_Q = 280µA, I_{SD} < 1µA, TSSOP16E Package
LTC3414	4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} < 1µA, TSSOP20E Package
LTC3416	4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter with Tracking	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} < 1µA, TSSOP20E Package
LTC3418	8A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 380µA, I_{SD} < 1µA, QFN Package
LTC3440	600mA (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.4V, I_Q = 25µA, I_{SD} < 1µA, MS/DFN Packages
LTC3441	600mA (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.4V, I_Q = 25µA, I_{SD} < 1µA, DFN Package
LTC3443	1.2A (I_{OUT}), 600kHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MIN)}$ = 2.4V, I_Q = 28µA, I_{SD} < 1µA, MS Package
LTC3448	1.5MHz/2.25MHz, 600mA Synchronous Step-Down DC/DC Converter with LDO Mode	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 32µA, I_{SD} < 1µA, DFN/MS8E
LTC3548	Dual 800mA and 400mA (I_{OUT}), 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MSE/DFN Packages

ThinSOT is a trademark of Linear Technology Corporation.

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