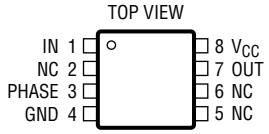
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 14V
Inputs (IN, PHASE) ..... –0.3V to 14V
Driver Output ..... –0.3V to V_{CC} + 0.3V
Junction Temperature ..... 150°C
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 200°C/W

ORDER PART NUMBER
LTC1693-5CMS8
MS8 PART MARKING
LTSG

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 12V, unless otherwise noted.

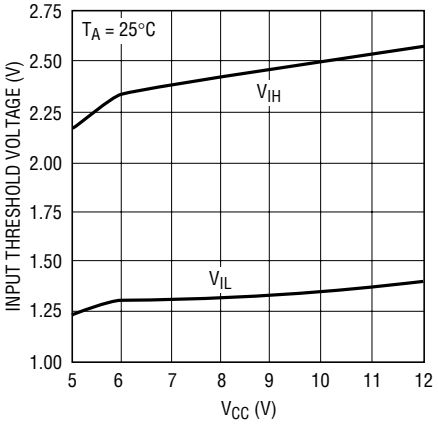
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage Range			4.5		13.2	V
I_{CC}	Quiescent Current	PHASE = 12V, IN = 0V	●	200	360	550	µA
$I_{CC(SW)}$	Switching Supply Current	C_{OUT} = 4.7nF, f_{IN} = 100kHz	●		7.2	10	mA
Input							
V_{IH}	High Input Threshold		●	2.2	2.6	3.1	V
V_{IL}	Low Input Threshold		●	1.1	1.4	1.7	V
I_{IN}	Input Pin Bias Current		●		±0.01	±10	µA
V_{PH}	PHASE Pin High Input Threshold		●	4.5	5.5	6.5	V
I_{PH}	PHASE Pin Pull-Up Current	PHASE = 0V	●	10	20	45	µA
Output							
V_{OH}	High Output Voltage	I_{OUT} = –10mA	●	11.92	11.97		V
V_{OL}	Low Output Voltage	I_{OUT} = 10mA	●		30	75	mV
R_{ONL}	Output Pull-Down Resistance				2.85		Ω
R_{ONH}	Output Pull-Up Resistance				3.00		Ω
I_{PKL}	Output Low Peak Current				1.70		A
I_{PKH}	Output High Peak Current				1.40		A
Switching Timing (Note 2)							
t_{RISE}	Output Rise Time	C_{OUT} = 1nF C_{OUT} = 4.7nF	● ●		17.5 48.0	35 85	ns ns
t_{FALL}	Output Fall Time	C_{OUT} = 1nF C_{OUT} = 4.7nF	● ●		16.5 42.0	35 75	ns ns
t_{PLH}	Output Low-High Propagation Delay	C_{OUT} = 1nF C_{OUT} = 4.7nF	● ●		38.0 40.0	70 75	ns ns
t_{PHL}	Output High-Low Propagation Delay	C_{OUT} = 1nF C_{OUT} = 4.7nF	● ●		32 35	70 75	ns ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All AC timing specificatons are guaranteed by design and are not production tested.

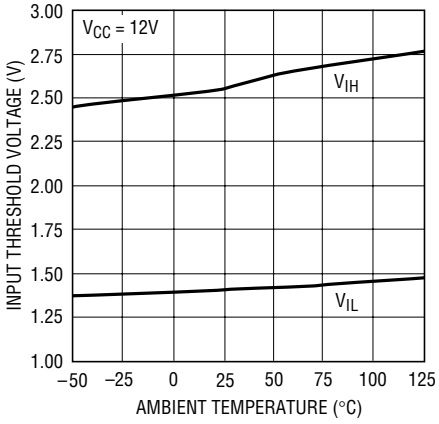
TYPICAL PERFORMANCE CHARACTERISTICS

IN Threshold Voltage vs V_{CC}



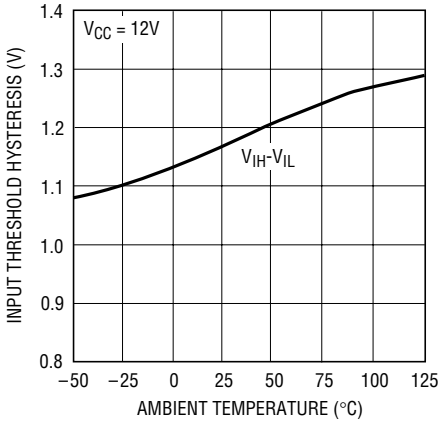
1693-5 G01

IN Threshold Voltage vs Ambient Temperature



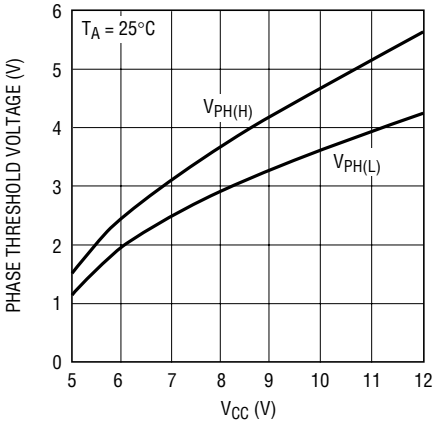
1693-5 G02

IN Threshold Hysteresis vs Ambient Temperature



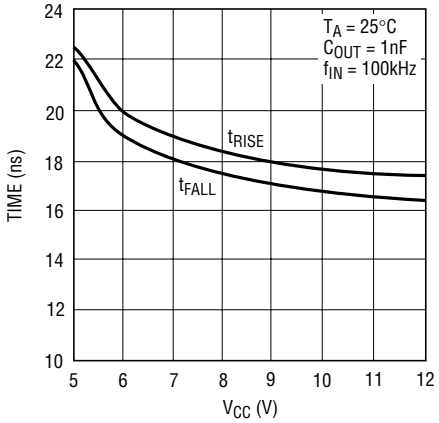
1693-5 G03

PHASE Threshold Voltage vs V_{CC}



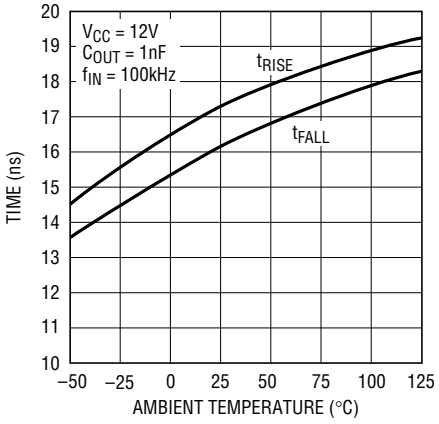
1693-5 G04

Rise/Fall Time vs V_{CC}



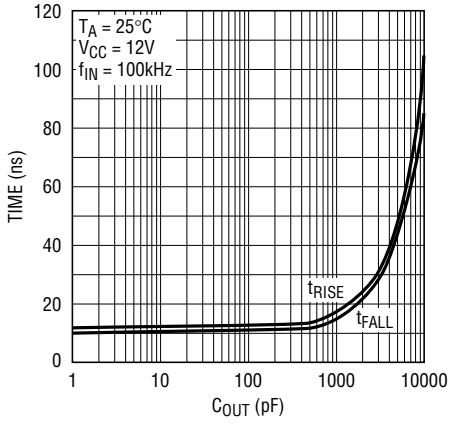
1693-5 G05

Rise/Fall Time vs Ambient Temperature



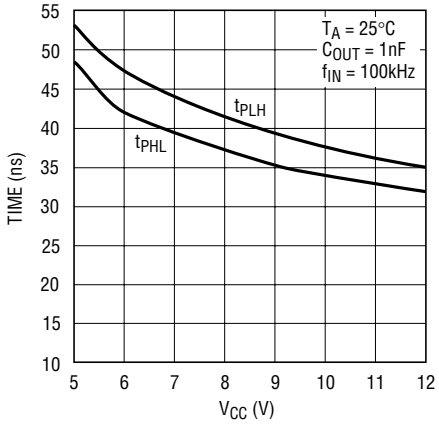
1693-5 G06

Rise/Fall Time vs C_{OUT}



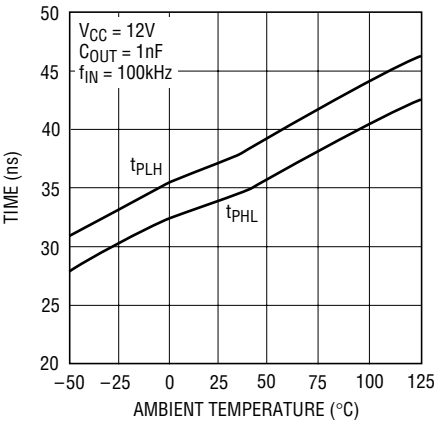
1693-5 G07

Propagation Delay vs V_{CC}



1693-5 G08

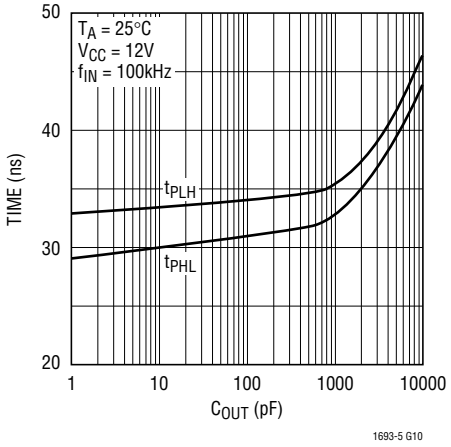
Propagation Delay vs Ambient Temperature



1693-5 G09

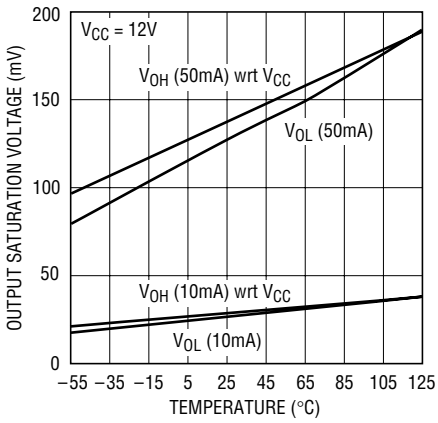
TYPICAL PERFORMANCE CHARACTERISTICS

Propagation Delay vs C_{OUT}



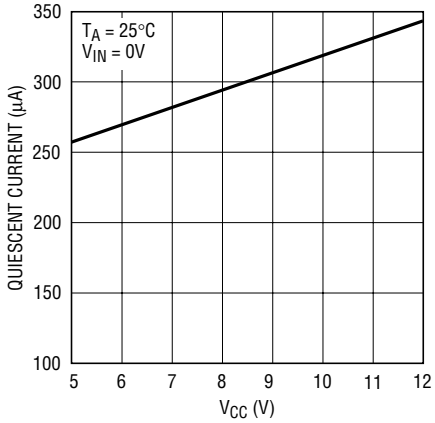
1693-5 G10

Output Saturation Voltage vs Temperature



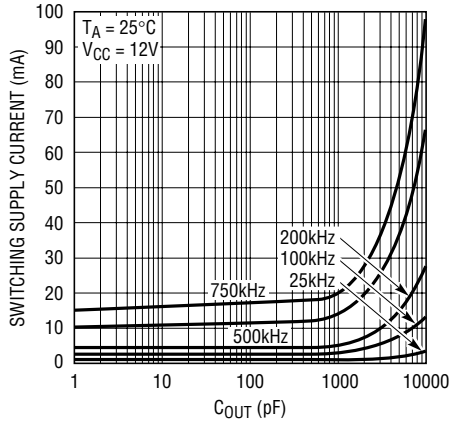
1693-5 G11

Quiescent Current vs V_{CC}



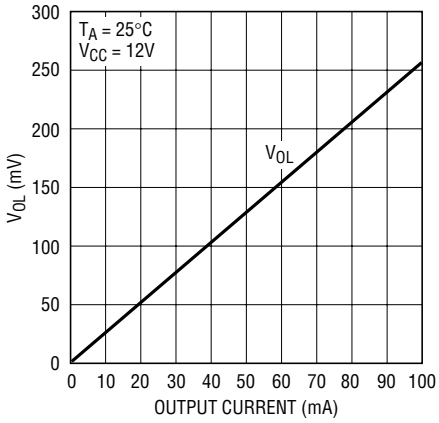
1693-5 G12

Switching Supply Current vs C_{OUT}



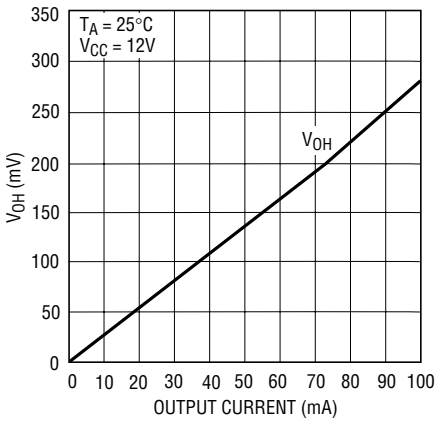
1693-5 G13

V_{OL} vs Output Current



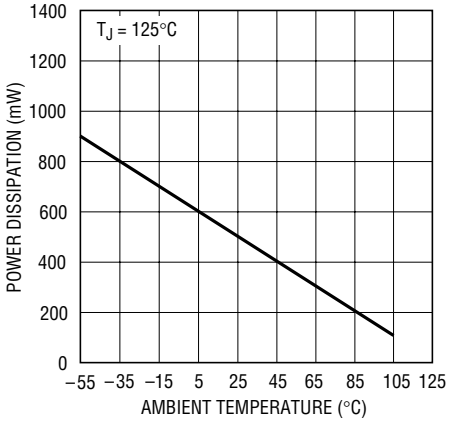
1693-5 G14

V_{OH} vs Output Current



1693-5 G15

Thermal Derating Curve



1693-5 G16

PIN FUNCTIONS

IN (Pin 1): Driver Input. The input has V_{CC} independent thresholds with hysteresis to improve noise immunity.

NC (Pins 2, 5, 6): No Connect.

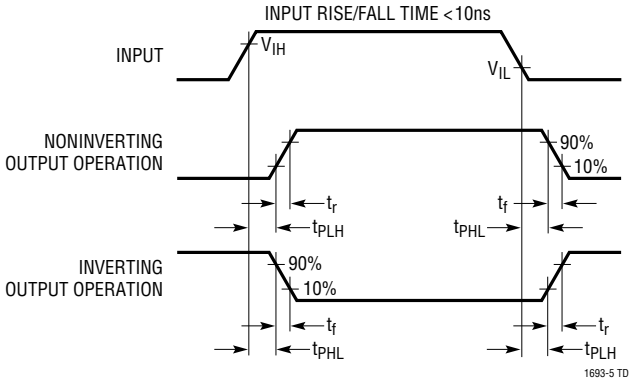
PHASE (Pin 3): Output Polarity Select. Connect this pin to V_{CC} or leave it floating for noninverting operation. Ground this pin for inverting operation. The typical PHASE pin input current when pulled low is 20µA.

GND (Pin 4): Driver Ground. Connect to a low impedance ground. The V_{CC} bypass capacitor should connect directly to this pin.

OUT (Pin 7): Driver Output.

V_{CC} (Pin 8): Power Supply Input. The source of the external P-MOSFET should also connect directly to this pin. This minimizes the AC current path and improves signal integrity.

TIMING DIAGRAM



APPLICATIONS INFORMATION

Overview

The LTC1693-5 single driver allows 3V- or 5V-based digital circuits to drive power P-channel MOSFETs at high speeds. A power MOSFET's gate-charge loss increases with switching frequency and transition time. The LTC1693-5 is capable of driving a 1nF load with 16ns rise and fall times using a V_{CC} of 12V. This eliminates the need for higher voltage supplies, such as 18V, to reduce the gate charge losses.

The LTC1693-5's 360µA quiescent current is an order of magnitude lower than most other drivers/buffers. This improves system efficiency in both standby and switching operation. Since a power MOSFET generally accounts for the majority of power loss in a converter, addition of the LT1693-5 to a high power converter design greatly improves efficiency, using very little board space.

Input Stage

The LTC1693-5 employs 3V CMOS compatible input thresholds that allow a low voltage digital signal to drive *standard* power P-channel MOSFETs. The LTC1693-5 incorporates a 4V internal regulator to bias the input buffer. This allows the 3V CMOS compatible input thresholds (V_{IH} = 2.6V, V_{IL} = 1.4V) to be independent of variations in V_{CC}. The 1.2V hysteresis between V_{IH} and V_{IL} eliminates false triggering due to ground noise during switching transitions. The LTC1693-5's input buffer has a high input impedance and draws less than 10µA during standby.

Output Stage

The LTC1693-5's output stage is essentially a CMOS inverter, as shown by the P- and N-channel MOSFETs in Figure 1 (P1 and N1). The CMOS inverter swings rail-to-rail, giving maximum voltage drive to the load. This large voltage swing is important in driving external power P-channel MOSFETs, whose $R_{DS(ON)}$ is inversely proportional to its gate overdrive voltage ($V_{GS} - V_T$).

The LTC1693-5's peak output currents are 1.4A (P1) and 1.7A (N1) respectively. The N-channel MOSFET (N1) has higher current drive capability so it can charge the power MOSFET's gate capacitance during high-to-low signal transitions. When the power MOSFET's gate is pulled high by the LTC1693-5, its drain voltage is pulled low by its load (e.g., a resistor or inductor). The slew rate of the drain voltage causes current to flow back to the MOSFETs gate through its gate-to-drain capacitance. If the MOSFET driver does not have sufficient source current capability (low output impedance), the current through the power MOSFET's Miller capacitance (C_{GD}) can momentarily pull the gate low, turning the MOSFET back on.

Rise/Fall Time

Since the power MOSFET generally accounts for the majority of power lost in a converter, it's important to quickly turn it either fully "on" or "off" thereby minimizing the transition time in its linear region. The LTC1693-5 has rise and fall times on the order of 16ns, delivering about 1.4A to 1.7A of peak current to a 1nF load with a V_{CC} of only 12V.

The LTC1693-5 rise and fall times are determined by the peak current capabilities of P1 and N1. The predriver, shown in Figure 1 driving P1 and N1, uses an adaptive method to minimize cross-conduction currents. This is done with a 6ns nonoverlapping transition time. N1 is fully turned off before P1 is turned-on and vice-versa using this 6ns buffer time. This minimizes any cross-conduction currents while N1 and P1 are switching on and off yet is short enough to not prolong their rise and fall times.

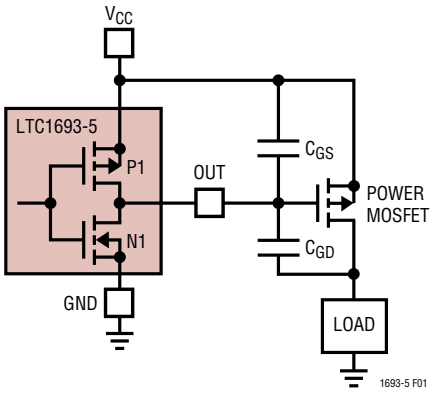


Figure 1. Capacitance Seen by OUT During Switching

APPLICATIONS INFORMATION

UVLO and Thermal Shutdown

The LTC1693-5's UVLO detector disables the input buffer and pulls the output pin to V_{CC} if V_{CC} < 4V. The output remains off from V_{CC} = 1V to V_{CC} = 4V. This ensures that during start-up or improper supply voltage values, the LTC1693-5 will keep the output power P-channel MOSFET off.

The LTC1693-5 also has a thermal detector that similarly disables the input buffer and pulls the output pin to V_{CC} if junction temperature exceeds 145°C. The thermal shutdown circuit has 20°C of hysteresis. This thermal limit helps to shut down the system should a fault condition occur.

Input Voltage Range

LTC1693-5's input pin is a high impedance node and essentially draws neligible input current. This simplifies the input drive circuitry required for the input.

The LTC1693-5 typically has 1.2V of hysteresis between its low and high input thresholds. This increases the driver's robustness against any ground bounce noises. However, care should still be taken to keep this pin from any noise pickup, especially in high frequency switching applications.

In applications where the input signal swings below the GND pin potential, the input pin voltage must be clamped to prevent the LTC1693-5's parastic substrate diode from turning on. This can be accomplished by connecting a series current limiting resistor R1 and a shunting Schottky diode D1 to the input pin (Figure 2). R1 ranges from 100Ω to 470Ω while D1 can be a BAT54 or 1N5818/9.

Bypassing and Grounding

LTC1693-5 requires proper V_{CC} bypassing and grounding due to its high speed switching (ns) and large AC currents (A). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot.

To obtain the optimum performance from the LTC1693-5:

A. Mount the bypass capacitors as close as possible to the V_{CC} and GND pins. The leads should be shortened as much as possible to reduce lead inductance. It is recommended to have a 0.1µF ceramic in parallel with a low ESR 4.7µF bypass capacitor.

   For high voltage switching in an inductive environment, ensure that the bypass capacitors' V_{MAX} ratings are high enough to prevent breakdown. This is especially important for floating driver applications.

B. Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LTC1693-5 switches 1.5A peak currents and any significant ground drop will degrade signal integrity.

C. Plan the ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and output pin. Terminate these two ground traces only at the GND pin of the driver (STAR network).

D. Keep the copper trace between the driver output pin and the load short and wide.

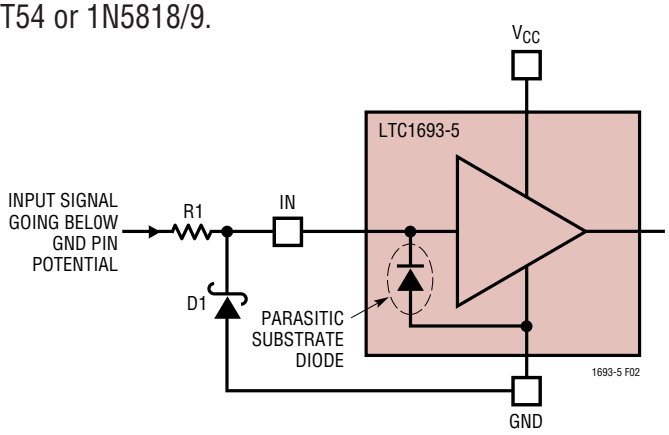
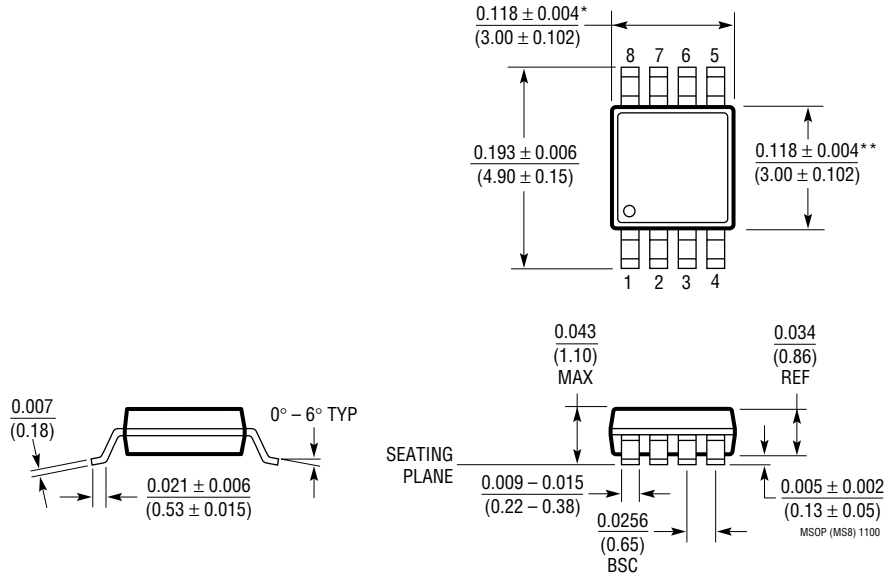


Figure 2. Input Protection Against Negative Input Signals

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1154	High Side Micropower MOSFET Drivers	Internal Charge Pump, 4.5V to 48V Supply Range, t_{ON} = 80µs, t_{OFF} = 28µs
LTC1155/LTC1156	Dual Micropower High/Low Side Drivers with Internal Charge Pump	4.5V to 18V Supply Range
LTC1157	3.3V Dual Micropower High/Low Side Driver	3.3V or 5V Supply Range
LT®1160/LT1162	Half/Full Bridge N-Channel Power MOSFET Driver	Dual Driver with Topside Floating Driver, 10V to 15V Supply Range
LT1161	Quad Protected High Side MOSFET Driver	8V to 48V Supply Range, t_{ON} = 200µs, t_{OFF} = 28µs
LTC1163	Triple 1.8V to 6V High Side MOSFET Driver	1.8V to 6V Supply Range, t_{ON} = 95µs, t_{OFF} = 45µs
LT1339	High Power Synchronous DC/DC Controller	Current Mode Operation Up to 60V, Dual N-Channel Synchronous Drive
LTC1735	High Efficiency, Low Noise Current Mode Step-Down DC/DC Controller	3.5V to 36V Operation with Ultrahigh Efficiency, Dual N-Channel MOSFET Synchronous Drive
LTC1693-1/LTC1693-2/ LTC1693-3	Single/Dual N-Channel MOSFET Drivers	1.5A Peak Output Current, Dual Drivers Permit High/Low Side Drive
LTC1981/LTC1982	SOT-23 High Side Drivers	Integrated Voltage Triplers, 10µA Quiescent per Driver

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