ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND 12V

Voltage

- Analog Reference ..... –0.3V to (V_{CC} + 0.3V)
- Analog Inputs ..... –0.3V to (V_{CC} + 0.3V)
- Digital Inputs .....–0.3V to 12V
- Digital Output ..... –0.3V to (V_{CC} + 0.3V)

Power Dissipation 500mW

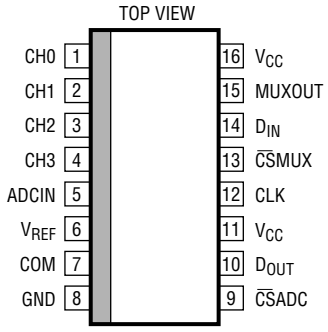
Operating Temperature Range

- LTC1594LCS/LTC1598LCG ..... 0°C to 70°C
- LTC1594LIS/LTC1598LIG ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

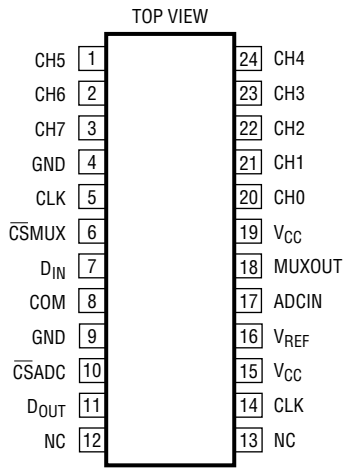


S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER PART NUMBER

LTC1594LCS
LTC1594LIS



G PACKAGE
24-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC1598LCG
LTC1598LIG

Consult factory for Military grade parts.

RECOMMENDED OPERATING CONDITIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage (Note 3)			2.7		3.6	V
f_{CLK}	Clock Frequency	V_{CC} = 2.7V		(Note 4)		200	kHz
t_{CYC}	Total Cycle Time	f_{CLK} = 200kHz		95			µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 2.7V		450			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence)	V_{CC} = 2.7V		2			µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 2.7V		600			ns
t_{WHCLK}	CLK High Time	V_{CC} = 2.7V		1.5			µs
t_{WLCLK}	CLK Low Time	V_{CC} = 2.7V		1.5			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	f_{CLK} = 200kHz		25			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	f_{CLK} = 200kHz		70			µs

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CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		LTC1594LCS/LTC1598LCG MIN	TYP	MAX	LTC1594LIS/LTC1598LIG MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 6)	●			±3			±3	LSB
Differential Linearity Error		●			±3/4			±1	LSB
Offset Error		●			±3			±3	LSB
Gain Error		●			±8			±8	LSB
REF Input Range	(Notes 7, 8)			1.5V to V_{CC} + 0.05V					V
Analog Input Range	(Notes 7, 8)			−0.05V to V_{CC} + 0.05V					V
MUX Channel Input Leakage Current	Off Channel	●			±200			±200	nA
MUXOUT Leakage Current	Off Channel	●			±200			±200	nA
ADCIN Input Leakage Current	(Note 9)	●			±1			±1	µA

DYNAMIC ACCURACY

T_A = 25°C, f_{SMPL} = 10.5kHz. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	1kHz Input Signal		68		dB
THD	Total Harmonic Distortion (Up to 5th Harmonic)	1kHz Input Signal		−78		dB
SFDR	Spurious-Free Dynamic Range	1kHz Input Signal		80		dB
	Peak Harmonic or Spurious Noise	1kHz Input Signal		−80		dB

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = 10µA V_{CC} = 2.7V, I_O = 360µA	● ●	2.4 2.1	2.64 2.30		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = High	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			15		mA
R_{REF}	Reference Input Resistance	$\overline{CS}$ = V_{IH} $\overline{CS}$ = V_{IL}			2700 60		MΩ kΩ
I_{REF}	Reference Current	$\overline{CS}$ = V_{CC} t_{CYC} ≥ 760µs, f_{CLK} ≤ 25kHz t_{CYC} ≥ 60µs, f_{CLK} ≤ 200kHz	● ●		0.001 50 50	2.5 70	µA µA µA
I_{CC}	Supply Current	$\overline{CS}$ = V_{CC}, CLK = V_{CC}, D_{IN} = V_{CC} t_{CYC} ≥ 760µs, f_{CLK} ≤ 25kHz t_{CYC} ≥ 60µs, f_{CLK} ≤ 200kHz	● ●		0.001 160 160	±5 400	µA µA µA

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AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.(Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Figure 1 in Applications Information		1.5			CLK Cycles
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	See Figure 1 in Applications Information	●	10.5			kHz
t_{CONV}	Conversion Time	See Figure 1 in Applications Information			12		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		600	1500	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		220	600	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		180	500	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			520		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		60	180	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		80	180	ns
t_{ON}	Enable Turn-On Time	See Figure 1 in Applications Information	●		540	1200	ns
t_{OFF}	Enable Turn-Off Time	See Figure 2 in Applications Information	●		190	500	ns
t_{OPEN}	Break-Before-Make Interval		●	125	350		ns
C_{IN}	Input Capacitance	Analog Inputs On-Channel			20		pF
		Off-Channel			5		pF
		Digital Input			5		pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: These devices are specified at 3V. Consult factory for 5V specified devices (LTC1594/LTC1598).

Note 4: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that $f_{CLK} \geq$ 200kHz at 85°C, $f_{CLK} \geq$ 75kHz at 70°C and $f_{CLK} \geq$ 1kHz at 25°C.

Note 5: V_{CC} = 2.7V, V_{REF} = 2.5V and CLK = 200kHz unless otherwise specified. $\overline{CS}$ADC and $\overline{CS}$MUX pins are tied together during the test.

Note 6: Linearity error is specified between the actual end points of the A/D transfer curve.

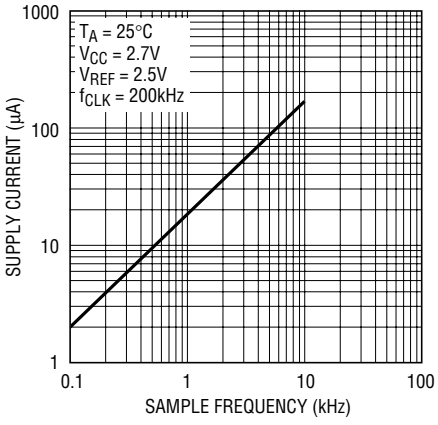
Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. This spec allows 50mV forward bias of either diode for 2.7V ≤ V_{CC} ≤ 3.6V. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 3V input voltage range, it will therefore require a minimum supply voltage of 2.950V over initial tolerance, temperature variations and loading.

Note 8: Recommended operating condition.

Note 9: Channel leakage current is measured after the channel selection.

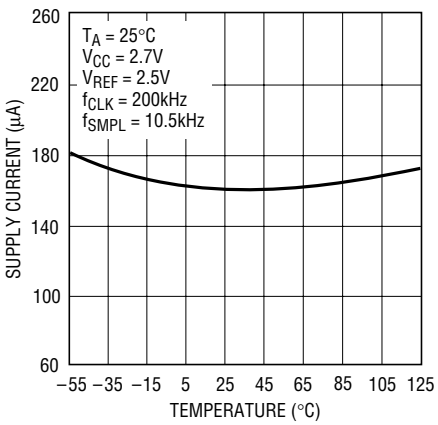
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Sample Rate



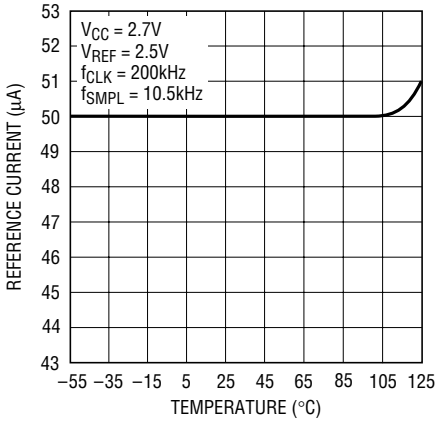
1594L/98L G01

Supply Current vs Temperature



1594L/98L G02

Reference Current vs Temperature



1594L/98L G03

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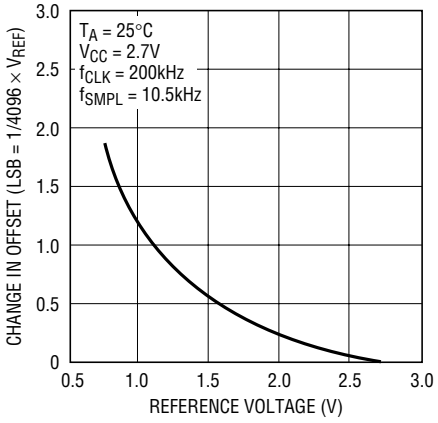
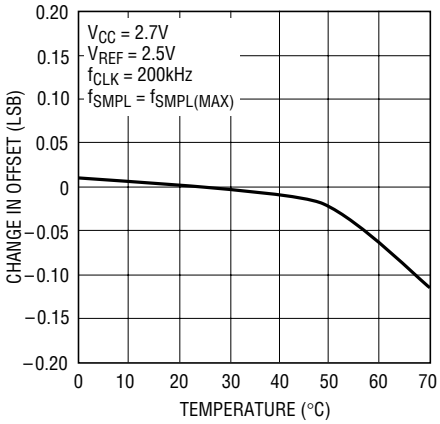
TYPICAL PERFORMANCE CHARACTERISTICS

Change in Offset vs Reference Voltage



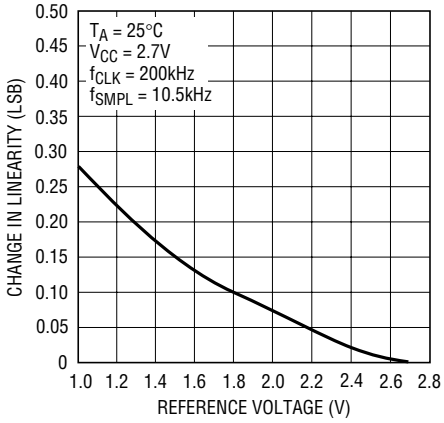
1594L/98L G04

Change in Offset vs Temperature



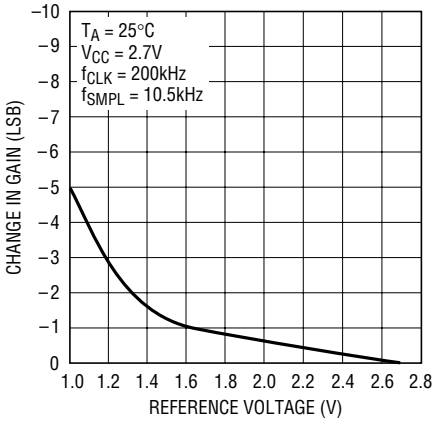
1594L/98L G05

Change in Linearity vs Reference Voltage



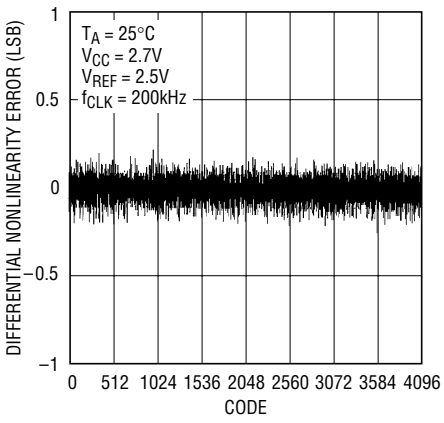
1594L/98L G06

Change in Gain vs Reference Voltage



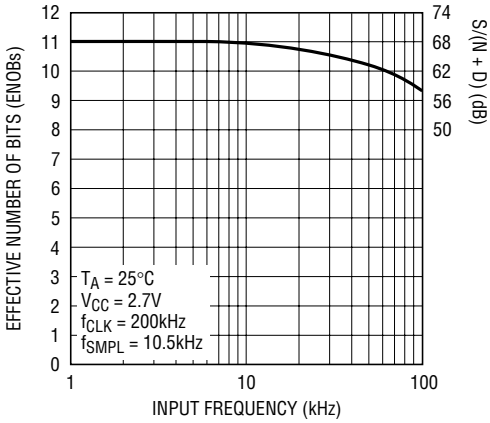
1594L/98L G07

Differential Nonlinearity vs Code



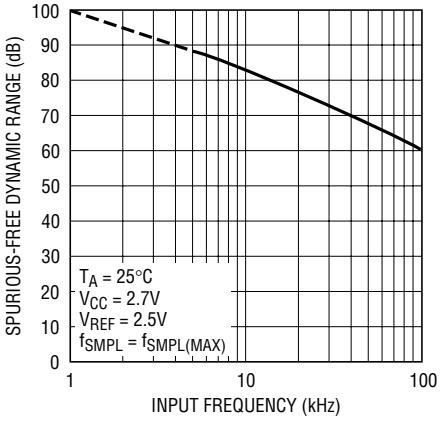
1594L/98L G08

Effective Bits and S/(N + D) vs Input Frequency



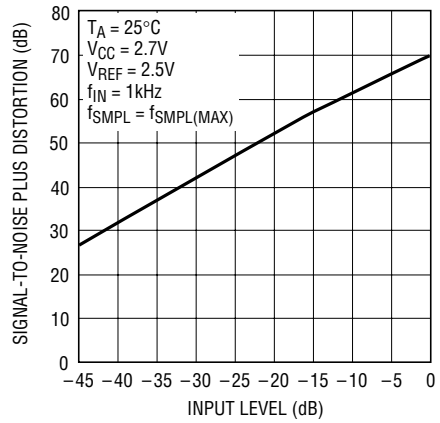
1594L/98L G09

Spurious Free Dynamic Range vs Input Frequency



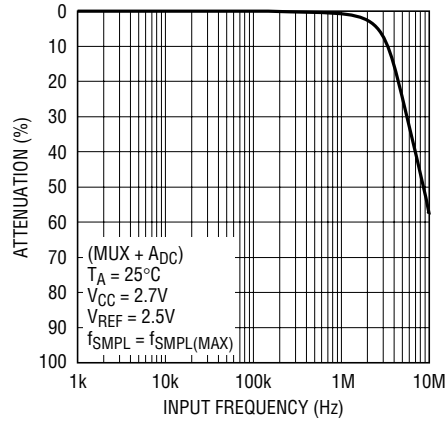
1594L/98L G10

S/(N + D) vs Input Level



1594L/98/ G11

Frequency Response



1594L/98L G12

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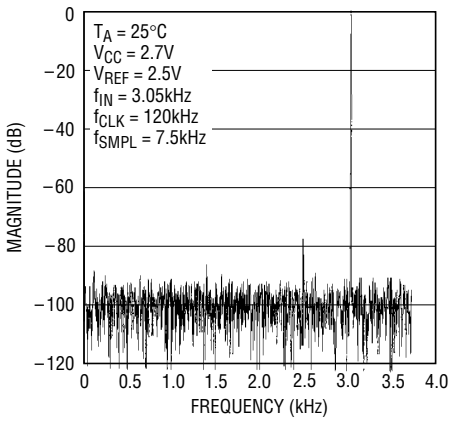
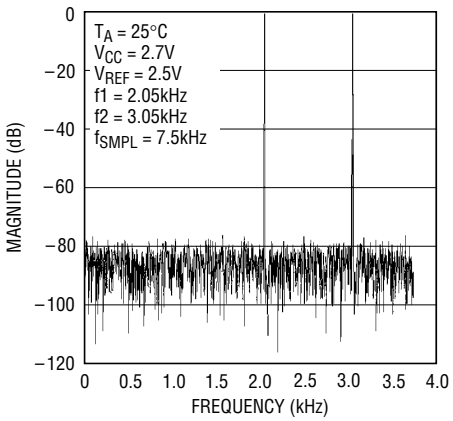
TYPICAL PERFORMANCE CHARACTERISTICS

4096 Point FFT Plot



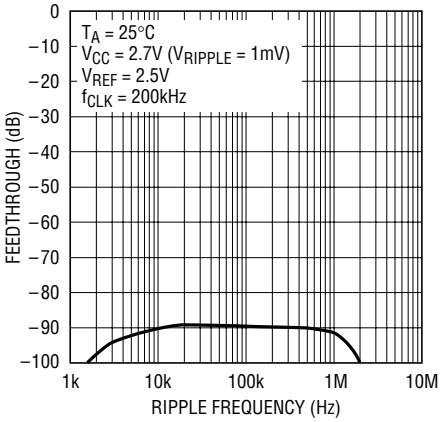
1594L/98L G13

Intermodulation Distortion



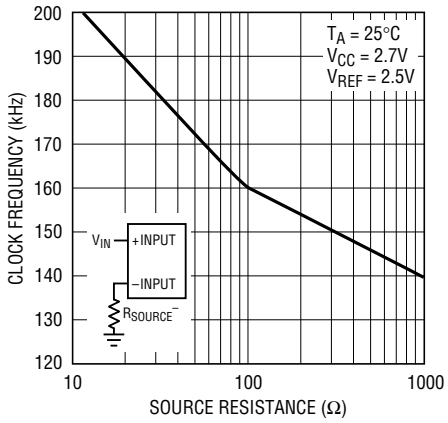
1594L/98L G14

Power Supply Feedthrough vs Ripple Frequency



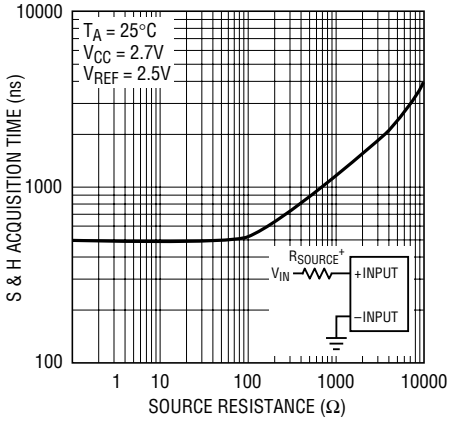
1594L/98L G15

Maximum Clock Frequency vs Source Resistance



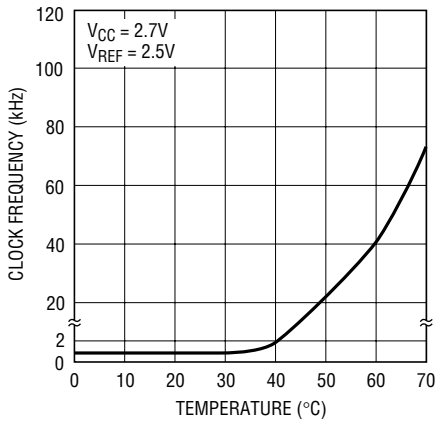
1594L/98L G16

Sample-and-Hold Acquisition Time vs Source Resistance



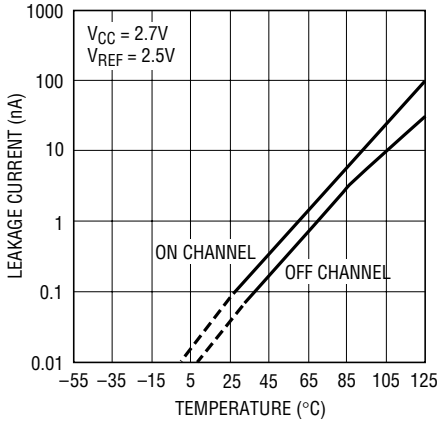
1594L/98L G17

Minimum Clock Frequency for 0.1LSB Error vs Temperature



1594L/98L G18

Input Channel Leakage Current vs Temperature



1594L/98L G19

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PIN FUNCTIONS

LTC1594L

CH0 (Pin 1): Analog Multiplexer Input.

CH1 (Pin 2): Analog Multiplexer Input.

CH2 (Pin 3): Analog Multiplexer Input.

CH3 (Pin 4): Analog Multiplexer Input.

ADCIN (Pin 5): ADC Input. This input is the positive analog input to the ADC. Connect this pin to MUXOUT for normal operation.

V_{REF} (Pin 6): Reference Input. The reference input defines the span of the ADC.

COM (Pin 7): Negative Analog Input. This input is the negative analog input to the ADC and must be free of noise with respect to GND.

GND (Pin 8): Analog Ground. GND should be tied directly to an analog ground plane.

$\overline{CS}$ADC (Pin 9): ADC Chip Select Input. A logic high on this input powers down the ADC and three-states D_{OUT}. A logic low on this input enables the ADC to sample the selected channel and start the conversion. For normal operation, drive this pin in parallel with $\overline{CS}$MUX.

D_{OUT} (Pin 10): Digital Data Output. The A/D conversion result is shifted out of this output.

V_{CC} (Pin 11): Power Supply Voltage. This pin provides power to the ADC. It must be bypassed directly to the analog ground plane.

CLK (Pin 12): Shift Clock. This clock synchronizes the serial data transfer to both MUX and ADC.

$\overline{CS}$MUX (Pin 13): MUX Chip Select Input. A logic high on this input allows the MUX to receive a channel address. A logic low enables the selected MUX channel and connects it to the MUXOUT pin for A/D conversion. For normal operation, drive this pin in parallel with $\overline{CS}$ADC.

D_{IN} (Pin 14): Digital Data Input. The multiplexer address is shifted into this input.

MUXOUT (Pin 15): MUX Output. This pin is the output of the multiplexer. Tie to ADCIN for normal operation.

V_{CC} (Pin 16): Power Supply Voltage. This pin should be tied to Pin 11.

LTC1598L

CH5 (Pin 1): Analog Multiplexer Input.

CH6 (Pin 2): Analog Multiplexer Input.

CH7 (Pin 3): Analog Multiplexer Input.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

CLK (Pin 5): Shift Clock. This clock synchronizes the serial data transfer to both MUX and ADC. It also determines the conversion speed of the ADC.

$\overline{CS}$MUX (Pin 6): MUX Chip Select Input. A logic high on this input allows the MUX to receive a channel address. A logic low enables the selected MUX channel and connects it to the MUXOUT pin for A/D conversion. For normal operation, drive this pin in parallel with $\overline{CS}$ADC.

D_{IN} (Pin 7): Digital Data Input. The multiplexer address is shifted into this input.

COM (Pin 8): Negative Analog Input. This input is the negative analog input to the ADC and must be free of noise with respect to GND.

GND (Pin 9): Analog Ground. GND should be tied directly to an analog ground plane.

$\overline{CS}$ADC (Pin 10): ADC Chip Select Input. A logic high on this input deselects and powers down the ADC and three-states D_{OUT}. A logic low on this input enables the ADC to sample the selected channel and start the conversion. For normal operation drive this pin in parallel with $\overline{CS}$MUX.

D_{OUT} (Pin 11): Digital Data Output. The A/D conversion result is shifted out of this output.

NC (Pin 12): No Connection.

NC (Pin 13): No Connection.

CLK (Pin 14): Shift Clock. This input should be tied to Pin 5.

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PIN FUNCTIONS

V_{CC} (Pin 15): Power Supply Voltage. This pin provides power to the A/D Converter. It must be bypassed directly to the analog ground plane.

V_{REF} (Pin 16): Reference Input. The reference input defines the span of the ADC.

ADCIN (Pin 17): ADC Input. This input is the positive analog input to the ADC. Connect this pin to MUXOUT for normal operation.

MUXOUT (Pin 18): MUX Output. This pin is the output of the multiplexer. Tie to ADCIN for normal operation.

V_{CC} (Pin 19): Power Supply Voltage. This pin should be tied to Pin 15.

CH0 (Pin 20): Analog Multiplexer Input.

CH1 (Pin 21): Analog Multiplexer Input.

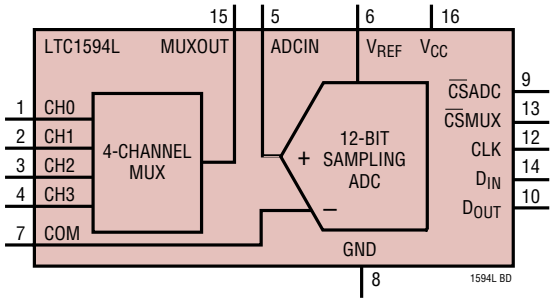
CH2 (Pin 22): Analog Multiplexer Input.

CH3 (Pin 23): Analog Multiplexer Input.

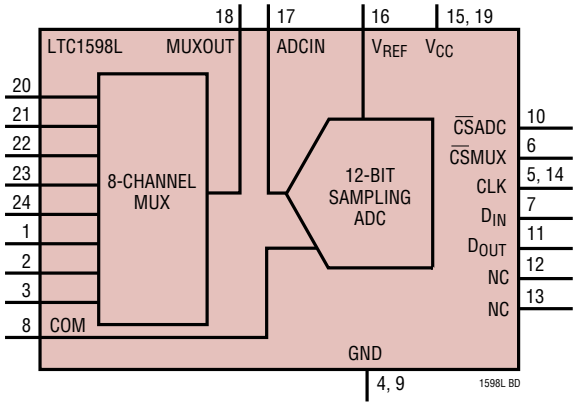
CH4 (Pin 24): Analog Multiplexer Input.

BLOCK DIAGRAMS

LTC1594L

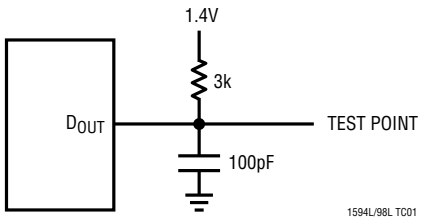


LTC1598L



TEST CIRCUITS

Load Circuit for t_{dDO}, t_r and t_f



Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f

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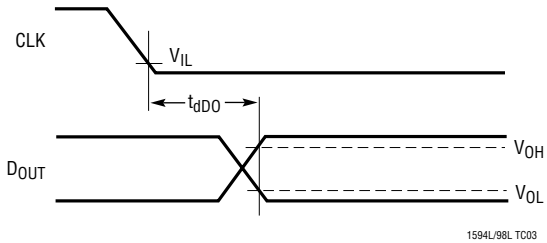
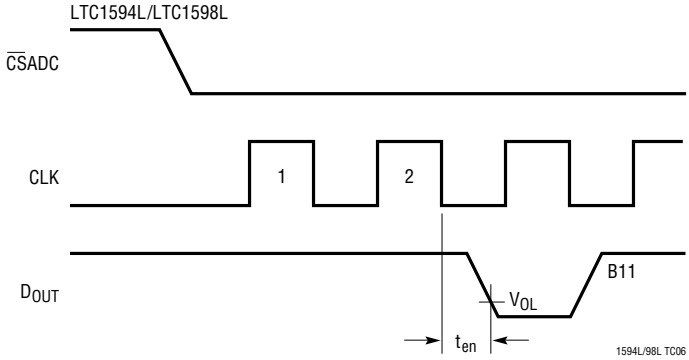
TEST CIRCUITS

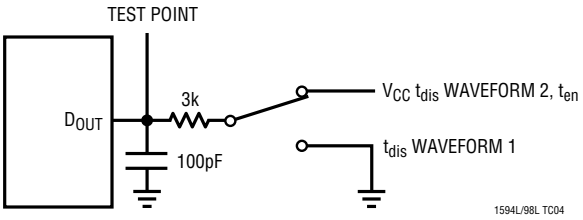
Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}



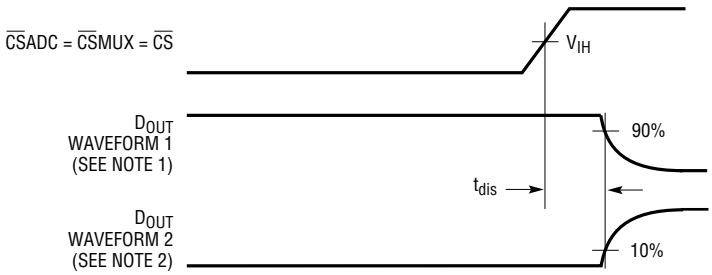
Voltage Waveforms for t_{en}



Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

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OVERVIEW

The LTC1594L/LTC1598L are 3V micropower, 12-bit sampling A/D converters that feature 4- and 8-channel multiplexers respectively. They typically draw only 160µA of supply current when sampling at 10.5kHz. Supply current drops linearly as the sample rate is reduced (see Supply Current vs Sample Rate). The ADCs automatically power down when not performing conversions, drawing only leakage current. The LTC1594L is available in a 16-pin narrow SO package and the LTC1598L is packaged in a 24-pin SSOP. Both devices operate on a single supply from 2.7V to 3.6V.

The LTC1594L/LTC1598L contain a 12-bit, switched-capacitor ADC, sample-and-hold, serial port and an external reference input pin. In addition, the LTC1594L has a 4-channel multiplexer and the LTC1598L provides an 8-channel multiplexer (see Block Diagram). They can measure signals floating on a DC common mode voltage and can operate with reduced spans to 1.5V. Reducing the spans allow them to achieve 366µV resolution.

The LTC1594L/LTC1598L provide separate MUX output and ADC input pins to form an ideal MUXOUT/ADCIN loop which economizes signal conditioning. The MUX and ADC of the devices can also be controlled individually through separate chip selects to enhance flexibility.

SERIAL INTERFACE

For this discussion, we will assume that $\overline{CS}$MUX and $\overline{CS}$ADC are tied together and will refer to them as simply $\overline{CS}$, unless otherwise specified.

The LTC1594L/LTC1598L communicate with the microprocessor and other external circuitry via a synchronous, half duplex, 4-wire interface (see Operating Sequences in Figures 1 and 2).

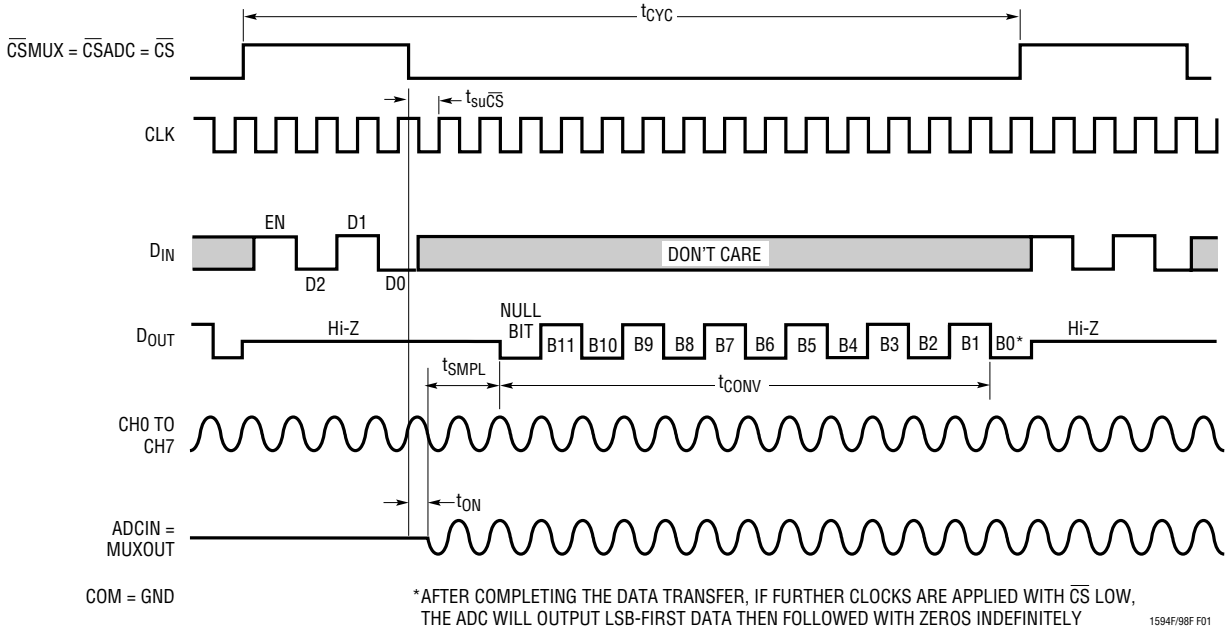

Figure 1. LTC1594L/LTC1598L Operating Sequence Example: CH2, GND

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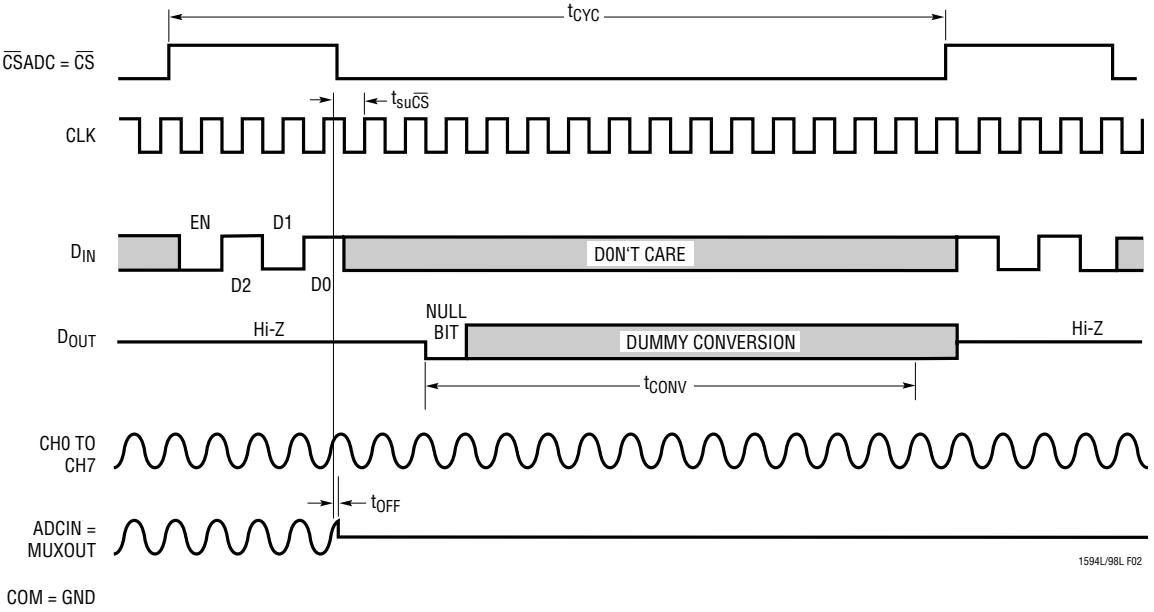


Figure 2. LTC1594L/LTC1598L Operating Sequence Example: All Channels Off

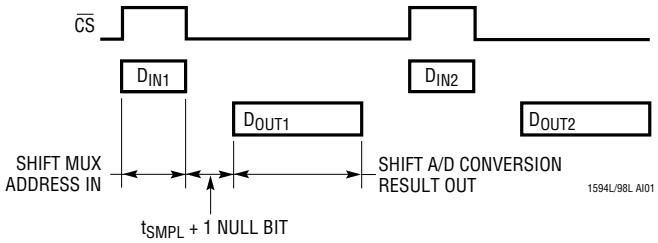
Data Transfer

The CLK synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems.

The LTC1594L/LTC1598L first receive input data and then transmit back the A/D conversion results (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a rising chip select ($\overline{CS}$) signal. After $\overline{CS}$ rises, the input data on the D_{IN} pin is latched into a 4-bit register on the rising edge of the clock. More than four input bits can be sent to the D_{IN} pin without problems, but only the last four bits clocked in before $\overline{CS}$ falls will be stored into the 4-bit register. This 4-bit input data word will select the channel in the muliplexer (see Input Data Word and Tables 1 and 2). To ensure correct operation, the $\overline{CS}$ must be pulled low before the next rising edge of the clock.

Once the $\overline{CS}$ is pulled low, all channels are simultaneously switched off after a delay of t_{OFF} to ensure a break-before-make interval, t_{OPEN}. After a delay of t_{ON} (t_{OFF} + t_{OPEN}), the selected channel is switched on, allowing the ADC in the chip to acquire input signal and start the conversion (see Figures 1 and 2). After 1 null bit, the result of the conversion is output on the D_{OUT} line. The selected channel remains on, until the next falling edge of $\overline{CS}$. At the end of the data exchange, $\overline{CS}$ should be brought high. This resets the LTC1594L/LTC1598L and initiates the next data exchange.



Break-Before-Make

The LTC1594L/LTC1598L provide a break-before-make interval from switching off all the channels simultaneously to switching on the next selected channel once $\overline{CS}$ is pulled low. In other words, once $\overline{CS}$ is pulled low,

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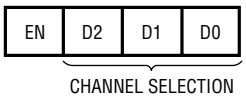
after a delay of t_{OFF}, all the channels are switched off to ensure a break-before-make interval. After this interval, the selected channel is switched on allowing signal transmission. The selected channel remains on until the next falling edge of $\overline{CS}$ and the process repeats itself with the "EN" bit being logic high. If the "EN" bit is logic low, all the channels are switched off simultaneously after a delay of t_{OFF} from $\overline{CS}$ being pulled low and all the channels remain off until the next falling edge of $\overline{CS}$.

Input Data Word

When $\overline{CS}$ is high, the LTC1594L/LTC1598L clock data into the D_{IN} inputs on the rising edge of the clock and store the data into a 4-bit register. The input data words are defined as follows:



"EN" Bit

The first bit in the 4-bit register is an "EN" bit. If the "EN" bit is a logic high, as illustrated in Figure 1, it enables the selected channel after a delay of t_{ON} when the $\overline{CS}$ is pulled low. If the "EN" bit is logic low, as illustrated in Figure 2, it disables all channels after a delay of t_{OFF} when the $\overline{CS}$ is pulled low.

Multiplexer (MUX) Address

The 3 bits of input word following the "EN" bit select the channel in the MUX for the requested conversion. For a given channel selection, the converter will measure the voltage of the selected channel with respect to the voltage on the COM pin. Tables 1 and 2 show the various bit combinations for the LTC1594L/LTC1598L channel selection.

Table 1. Logic Table for the LTC1594L Channel Selection

CHANNEL STATUS	EN	D2	D1	D0
All Off	0	X	X	X
CH0	1	0	0	0
CH1	1	0	0	1
CH2	1	0	1	0
CH3	1	0	1	1

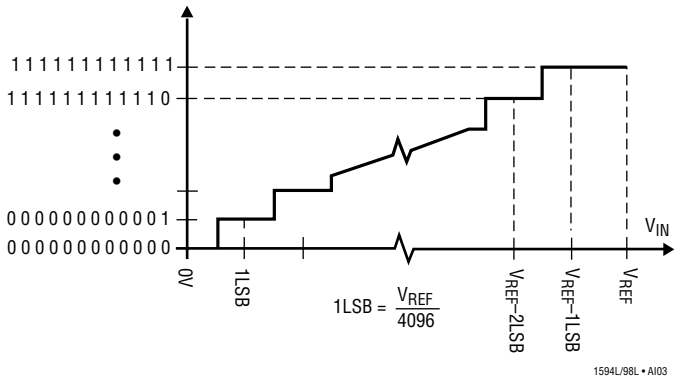
Table 2. Logic Table for the LTC1598L Channel Selection

CHANNEL STATUS	EN	D2	D1	D0
All Off	0	X	X	X
CH0	1	0	0	0
CH1	1	0	0	1
CH2	1	0	1	0
CH3	1	0	1	1
CH4	1	1	0	0
CH5	1	1	0	1
CH6	1	1	1	0
CH7	1	1	1	1

Transfer Curve

The LTC1594L/LTC1598L are permanently configured for unipolar only. The input span and code assignment for this conversion type is illustrated below.

Transfer Curve



Output Code

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 2.500V)
111111111111111	V_{REF} – 1LSB	2.49939V
111111111111110	V_{REF} – 2LSB	2.49878V
•	•	•
•	•	•
•	•	•
000000000000001	1LSB	0.00061V
000000000000000	0V	0V

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Operation with D_{IN} and D_{OUT} Tied Together

The LTC1594L/LTC1598L can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the microprocessor (MPU). Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1594L/LTC1598L will take control of the data line after $\overline{CS}$ falling and before the 6th falling CLK while the processor takes control of the data line when $\overline{CS}$ is high (see Figure 3). Therefore the processor port line must be switched to an input with $\overline{CS}$ being low to avoid a conflict.

Separate Chip Selects for MUX and ADC

The LTC1594L/LTC1598L provide separate chip selects, $\overline{CS}$MUX and $\overline{CS}$ADC, to control MUX and ADC separately. This feature not only provides the flexibility to select a particular channel once for multiple conversions (see Figure 4) but also maximizes the sample rate up to 20ksps (see Figure 5).

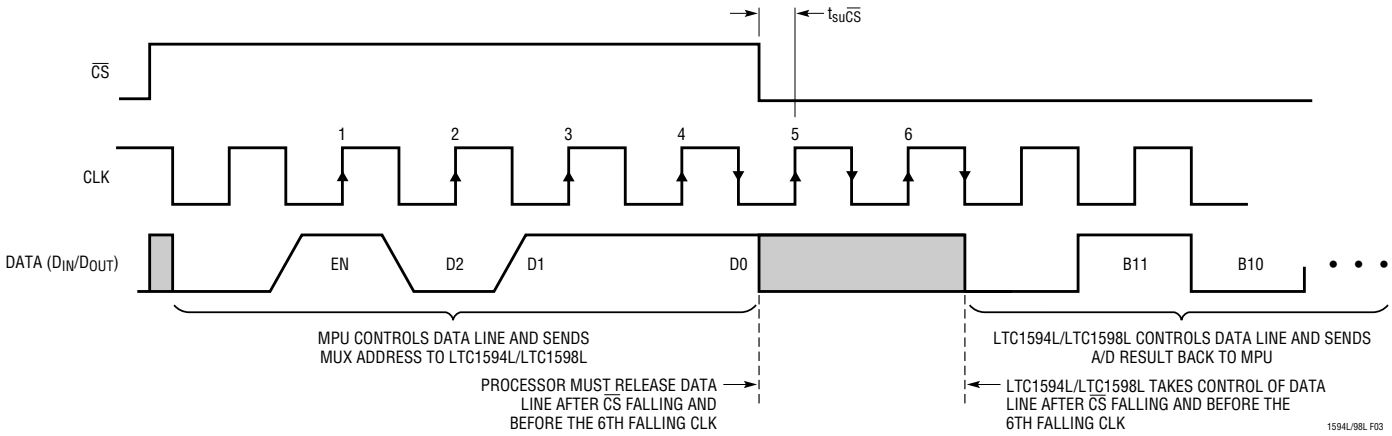

Figure 3. LTC1594L/LTC1598L Operation with D_{IN} and D_{OUT} Tied Together

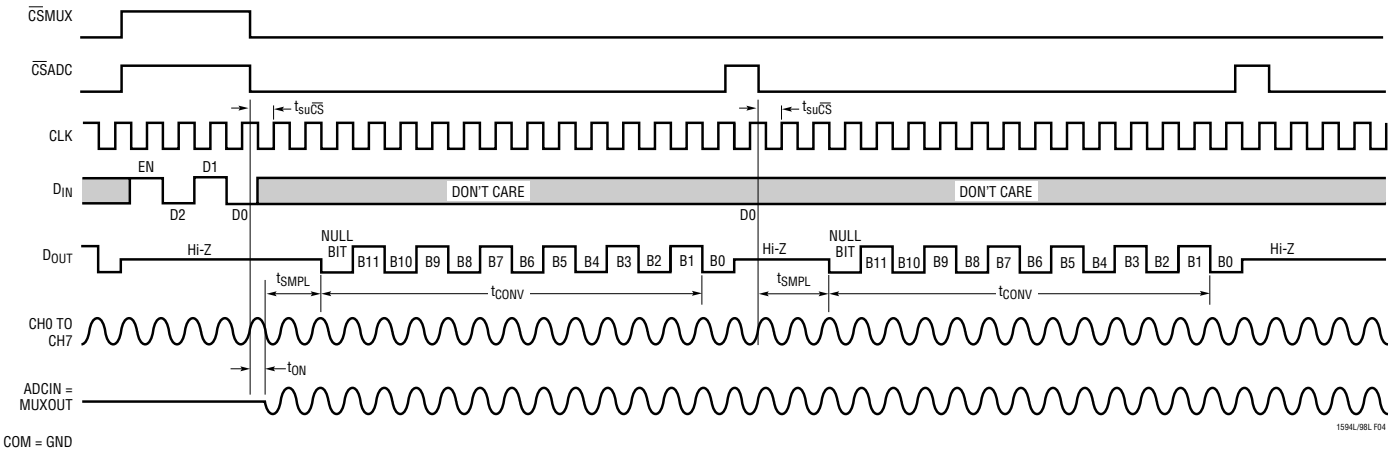

Figure 4. Selecting a Channel Once for Multiple Conversions

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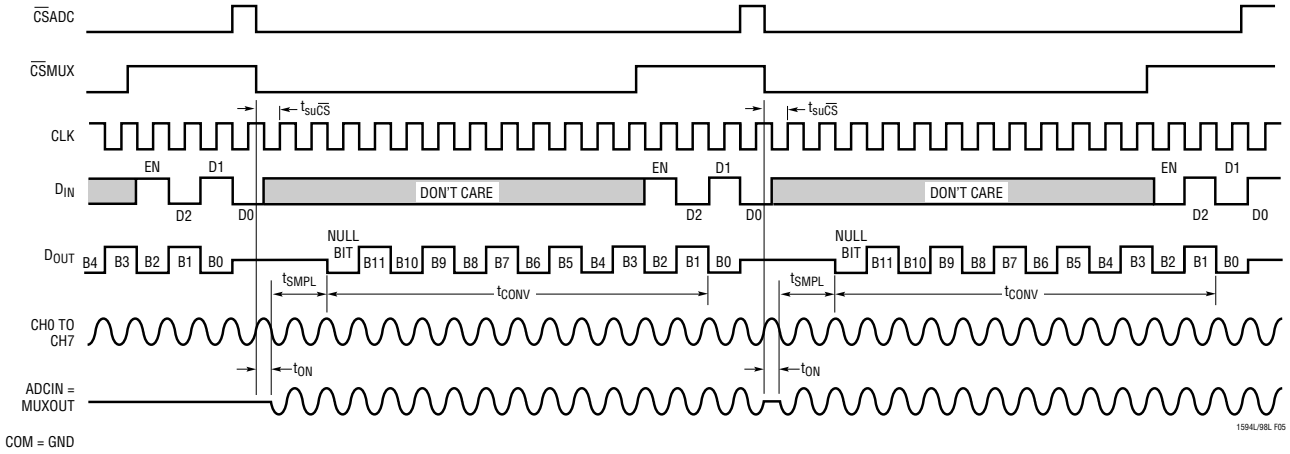

Figure 5. Use Separate Chip Selects to Maximize Sample Rate

MUXOUT/ADCIN Loop Economizes Signal Conditioning

The MUXOUT and ADCIN pins of the LTC1594L/LTC1598L form a very flexible external loop that allows Programmable Gain Amplifier (PGA) and/or processing analog input signals prior to conversion. This loop is also a cost effective way to perform the conditioning, because only one circuit is needed instead of one for each channel.

In the Typical Applications section, there are a few examples illustrating how to use the MUXOUT/ADCIN loop to form a PGA and to antialias filter several analog inputs.

ACHIEVING MICROPOWER PERFORMANCE

With typical operating currents of 160µA and automatic shutdown between conversions, the LTC1594L/LTC1598L achieve extremely low power consumption over a wide range of sample rates (see Figure 6). The auto shutdown allows the supply current to drop with reduced sample rate. Several things must be taken into account to achieve such a low power consumption.

Shutdown

The LTC1594L/LTC1598L are equipped with automatic shutdown features. They draw power when the $\overline{CS}$ pin is low. The bias circuits and comparator of the ADC powers down and the reference input becomes high impedance at the end of each conversion leaving the CLK running to clock out the LSB first data or zeroes (see Figures 1 and 2). When the $\overline{CS}$ pin is high, the ADC powers down completely

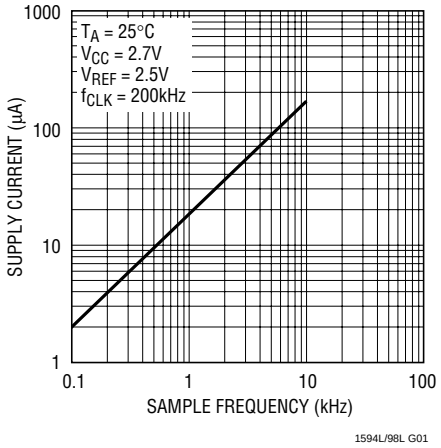

Figure 6. Automatic Power Shutdown Between Conversions Allows Power Consumption to Drop with Sample Rate

leaving the $\overline{CLK}$ running to clock the input data word into MUX. If the $\overline{CS}$, D_{IN} and CLK are not running rail-to-rail, the input logic buffers will draw currents. These currents may be large compared to the typical supply current. To obtain the lowest supply current, run the $\overline{CS}$, D_{IN} and CLK pins rail-to-rail.

D_{OUT} Loading

Capacitive loading on the digital output can increase power consumption. A 100pF capacitor on the D_{OUT} pin can add more than 50µA to the supply current at a 200kHz clock frequency. An extra 50µA or so of current goes into charging and discharging the load capacitor. The same goes for digital lines driven at a high frequency by any logic. The (C)(V)(f) currents must be evaluated and the troublesome ones minimized.

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BOARD LAYOUT CONSIDERATIONS

Grounding and Bypassing

The LTC1594L/LTC1598L are easy to use if some care is taken. They should be used with an analog ground plane and single point grounding techniques. The GND pin should be tied directly to the ground plane.

The V_{CC} pin should be bypassed to the ground plane with a 10µF tantalum capacitor with leads as short as possible. If the power supply is clean, the LTC1594L/LTC1598L can also operate with smaller 1µF or less surface mount or ceramic bypass capacitors. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

SAMPLE-AND-HOLD

Both the LTC1594L/LTC1598L provide a built-in sample-and-hold (S&H) function to acquire signals through the selected channel, assuming the ADCIN and MUXOUT pins are tied together. The S & H of these parts acquire input signals through the selected channel relative to COM input during the t_{SMPL} time (see Figure 7).

Single-Ended Inputs

The sample-and-hold of the LTC1594L/LTC1598L allows conversion of rapidly varying signals. The input voltage is sampled during the t_{SMPL} time as shown in Figure 7. The sampling interval begins after t_{ON} time once the $\overline{CS}$ is pulled low and continues until the second falling CLK edge after the $\overline{CS}$ is low (see Figure 7). On this falling CLK

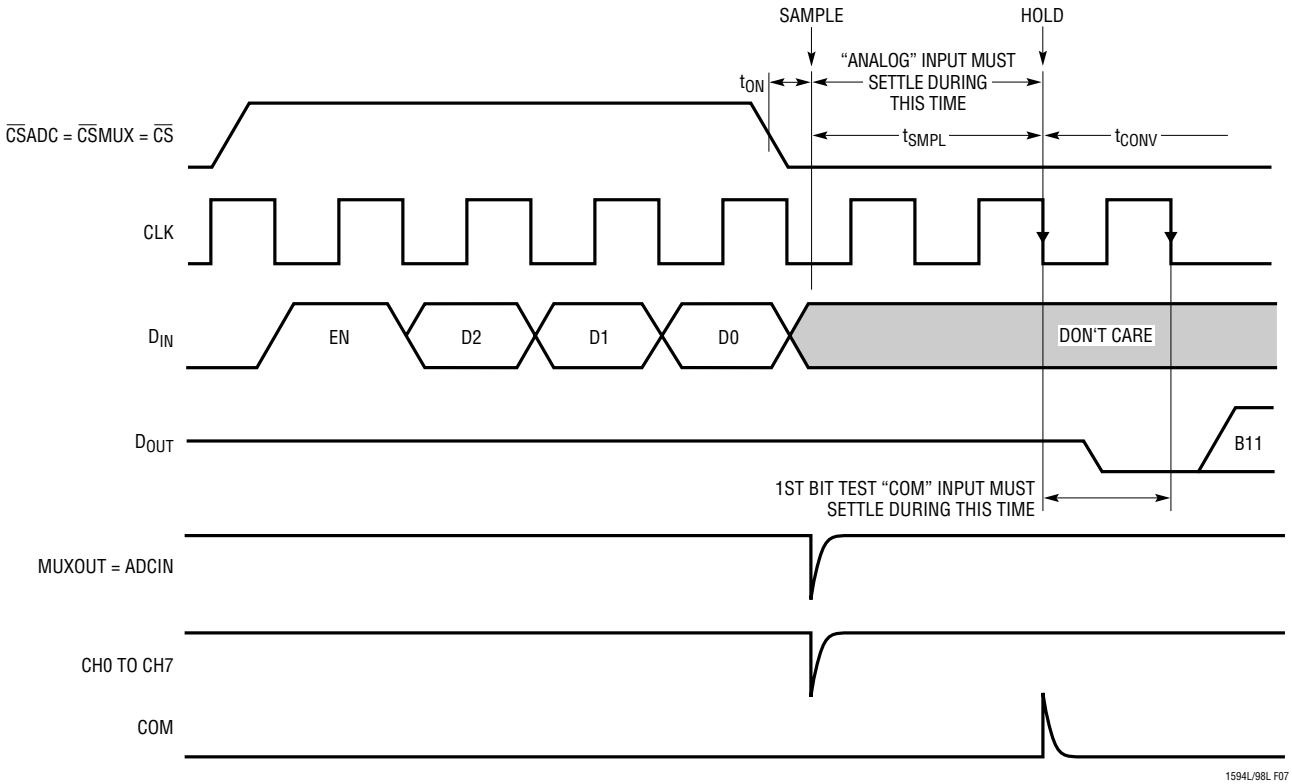

Figure 7. LTC1594L/LTC1598L ADCIN and COM Input Settling Windows

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edge, the S & H goes into hold mode and the conversion begins. The voltage on the "COM" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the conversion operation may not be performed accurately. The conversion time is 12 CLK cycles. Therefore, a change in the "COM" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "COM" input this error would be:

$$V_{ERROR(MAX)} = V_{PEAK}(2\pi)(f)(\text{"COM"})12/f_{CLK}$$

Where f("COM") is the frequency of the "COM" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. In most cases, V_{ERROR} will not be significant. For a 60Hz signal on the "COM" input to generate a 0.5LSB error (305µV) with the converter running at CLK = 200kHz, its peak value would have to be 5.266mV.

ANALOG INPUTS

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1594L/LTC1598L have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

"Analog" Input Settling

The input capacitor of the LTC1594L/LTC1598L is switched onto the selected channel input during the t_{SMPL} time (see Figure 7) and samples the input signal within that time. The sample phase is at least 1 1/2 CLK cycles before conversion starts. The voltage on the "analog" input must settle completely within t_{SMPL}. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If a large "analog" input source resistance must be used, the sample time can be increased by using a slower CLK frequency.

"COM" Input Settling

At the end of the t_{SMPL}, the input capacitor switches to the "COM" input and conversion starts (see Figures 1 and 7). During the conversion, the "analog" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "COM" input voltage settles completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE}^- and C2 will improve settling time. If a large "COM" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 7). Again, the "analog" and "COM" input sampling times can be extended as described above to accommodate slower op amps. Most op amps, including the LT®1006 and LT1413 single supply op amps, can be made to settle well even with the minimum settling windows of 7.5µs ("analog" input) which occur at the maximum clock rate of 200kHz.

Source Resistance

The analog inputs of the LTC1594L/LTC1598L look like a 20pF capacitor (C_{IN}) in series with a 1k resistor (R_{ON}) and a 90Ω channel resistance as shown in Figure 8. C_{IN} gets switched between the selected "analog" and "COM" inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

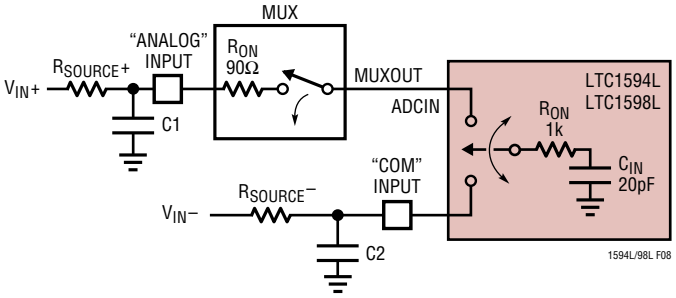

Figure 8. Analog Input Equivalent Circuit

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Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 200nA (at 85°C) flowing through a source resistance of 600Ω will cause a voltage drop of 120μV or 0.2LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve Input Channel Leakage Current vs Temperature).

REFERENCE INPUTS

The reference input of the LTC1594L/LTC1598L is effectively a 50k resistor from the time $\overline{CS}$ goes low to the end of the conversion. The reference input becomes a high impedance node at any other time (see Figure 9). Since the voltage on the reference input defines the voltage span of the A/D converter, the reference input should be driven by a reference with low R_{OUT} (ex. LT1004, LT1019 and LT1021) or a voltage source with low R_{OUT}.

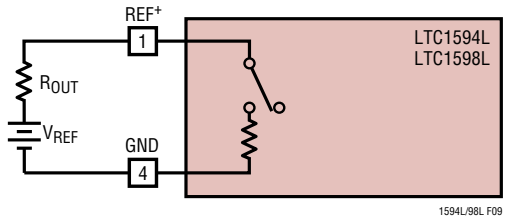

Figure 9. Reference Input Equivalent Circuit

Reduced Reference Operation

The effective resolution of the LTC1594L/LTC1598L can be increased by reducing the input span of the converters. The LTC1594L/LTC1598L exhibit good linearity and gain over a wide range of reference voltages (see typical curves Change in Linearity vs Reference Voltage and Change in Gain vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converters. The following factors must be considered when operating at low V_{REF} values:

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

Offset with Reduced V_{REF}

The offset of the LTC1594L/LTC1598L has a larger effect on the output code when the ADCs are operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Change in Offset vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 122μV which is 0.2LSB with a 2.5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "COM" input of the LTC1594L/LTC1598L.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1594L/LTC1598L can be reduced to approximately 400μV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced.

For operation with a 2.5V reference, the 400μV noise is only 0.66LSB peak-to-peak. In this case, the LTC1594L/LTC1598L noise will contribute virtually no uncertainty to the output code. However, for reduced references the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference this same 400μV noise is 1.32LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 1LSB. If the reference is further reduced to 1V, the 400μV noise becomes equal to 1.65LSBs and a stable code may be difficult to achieve. In this case, averaging multiple readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage to be used the more critical it becomes to have a clean, noise free setup.

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Conversion Speed with Reduced V_{REF}

With reduced reference voltages, the LSB step size is reduced and the LTC1594L/LTC1598L internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low values of V_{REF} are used.

DYNAMIC PERFORMANCE

The LTC1594L/LTC1598L have exceptional sampling capability. Fast Fourier Transform (FFT) test techniques are used to characterize the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 10 shows a typical LTC1594L/LTC1598L plot.

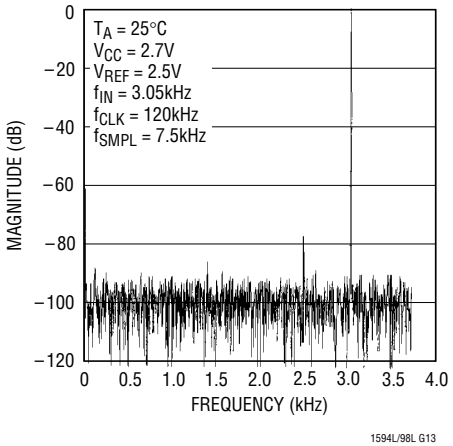

Figure 10. LTC1594L/LTC1598L Nonaveraged, 4096 Point FFT Plot

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio (S/N + D) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the ADC's output. The output is band limited to frequencies above DC and below one half the sampling frequency. Figure 11 shows a typical spectral content with a 10.5kHz sampling rate.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to S/(N + D) by the equation:

$$ENOB = [S/(N + D) – 1.76]/6.02$$

where S/(N + D) is expressed in dB. At the maximum sampling rate of 10.5kHz with a 5V supply, the LTC1594L/LTC1598L maintain above 10.7 ENOBs at 10kHz input frequency. Above 10kHz the ENOBs gradually decline, as shown in Figure 11, due to increasing second harmonic distortion. The noise floor remains low.

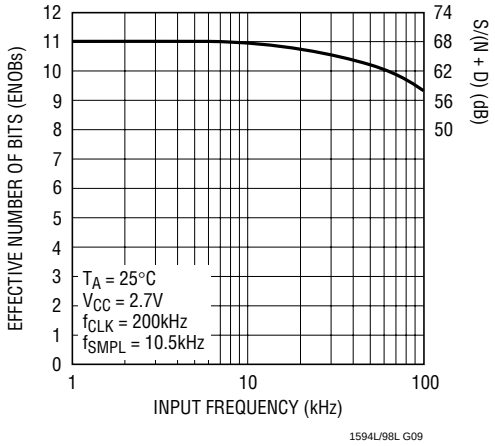

Figure 11. Effective Bits and S/(N + D) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half of the sampling frequency. THD is defined as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + ... + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through the N^{th} harmonics. The typical THD

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specification in the Dynamic Accuracy table includes the 2nd through 5th harmonics. With a 1kHz input signal, the LTC1594L/LTC1598L have typical THD of 78dB with V_{CC} = 2.7V.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of $mf_a \pm nf_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include ($f_a + f_b$) and ($f_a - f_b$) while 3rd order IMD terms include ($2f_a + f_b$), ($2f_a - f_b$), ($f_a + 2f_b$), and ($f_a - 2f_b$). If the two input sine waves are equal in magnitudes, the value (in dB) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\left(f_a \pm f_b\right) = 20\log\left[\frac{\text{amplitude}\left(f_a \pm f_b\right)}{\text{amplitude at } f_a}\right]$$

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in dBs relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the effective bits rating of the ADC falls to 11 bits. Beyond this frequency, distortion of the sampled input signal increases. The LTC1594L/LTC1598L have been designed to optimize input bandwidth, allowing the ADCs to undersample input signals with frequencies above the converters' Nyquist Frequency.

TYPICAL APPLICATIONS

Microprocessor Interfaces

The LTC1594L/LTC1598L can interface directly (without external hardware) to most popular microprocessors' (MPU) synchronous serial formats including MICROWIRE, SPI and QSPI. If an MPU without a dedicated serial port is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1594L/LTC1598L. Included here is one serial interface example.

Motorola SPI (MC68HC05)

The MC68HC05 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB-first and in 8-bit increments. The D_{IN} word sent to the data register starts the SPI process. With three 8-bit transfers the A/D result is read into the MPU. The second 8-bit transfer clocks B11 through B7 of the A/D conversion result into the processor. The third 8-bit transfer clocks the remaining bits B6 through B0 into the MPU. ANDing the second byte with $1F_{HEX}$ clears the three most significant bits and ANDing the third byte with FE_{HEX} clears the least significant bit. Shifting the data to the right by one bit results in a right justified word.

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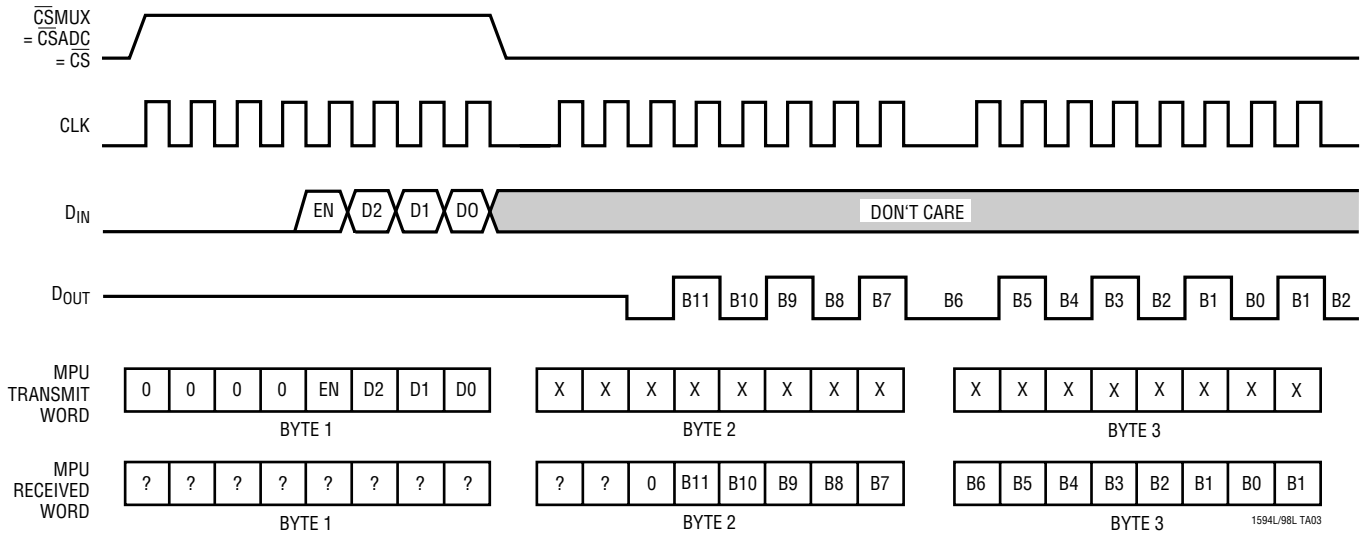
TYPICAL APPLICATIONS

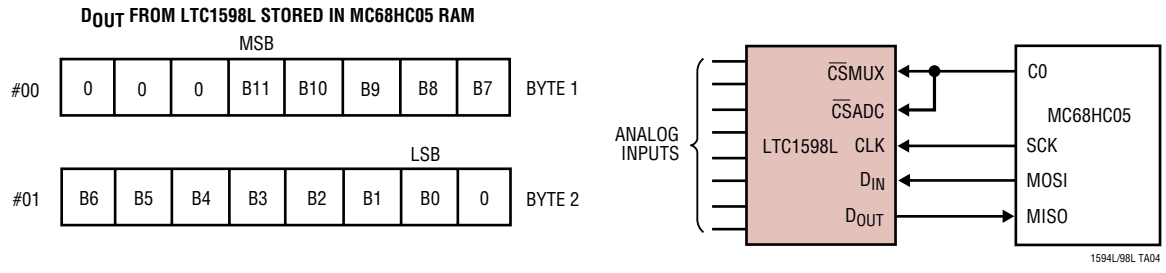
MC68HC05 CODE

```
        LDA  #$52    Configuration data for serial peripheral
                     control register (Interrupts disabled, output
                     enabled, master, Norm = 0, Ph = 0, Clk/16)
        STA  $0A     Load configuration data into location $0A (SPCR)
        LDA  #$FF    Configuration data for I/O ports
                     (all bits are set as outputs)
        STA  $04     Load configuration data into Port A DDR ($04)
        STA  $05     Load configuration data into Port B DDR ($05)
        STA  $06     Load configuration data into Port C DDR ($06)
        LDA  #$08    Put DIN word for LTC1598L into Accumulator
                     (CH0 with respect to GND)
        STA  $50     Load DIN word into memory location $50
START   BSET 0,$02   Bit 0 Port C ($02) goes high (CS goes high)
        LDA  $50     Load DIN word at $50 into Accumulator
        STA  $0C     Load DIN word into SPI data register ($0C) and
                     start clocking data
LOOP1   TST  $0B     Test status of SPIF bit in SPI status register ($0B)
        BPL  LOOP1   Loop if not done with transfer to previous instruction
        BCLR 0,$02   Bit 0 Port C ($02) goes low (CS goes low)
        LDA  $0C     Load contents of SPI data register into Accumulator
        STA  $0C     Start next SPI cycle
LOOP2   TST  $0B     Test status of SPIF
        BPL  LOOP2   Loop if not done
        LDA  $0C     Load contents of SPI data register into Accumulator
        STA  $0C     Start next SPI cycle
        AND  #$IF    Clear 3 MSBs of first DOUT word
        STA  $00     Load Port A ($00) with MSBs
LOOP3   TST  $0B     Test status of SPIF
        BPL  LOOP3   Loop if not done
        LDA  $0C     Load contents of SPI data register into Accumulator
        AND  #$FE    Clear LSB of second DOUT word
        STA  $01     Load Port B ($01) with LSBs
        JMP  START   Go back to start and repeat program
```

Data Exchange Between LTC1598L and MC68HC05



Hardware and Software Interface to Motorola MC68HC05



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TYPICAL APPLICATIONS

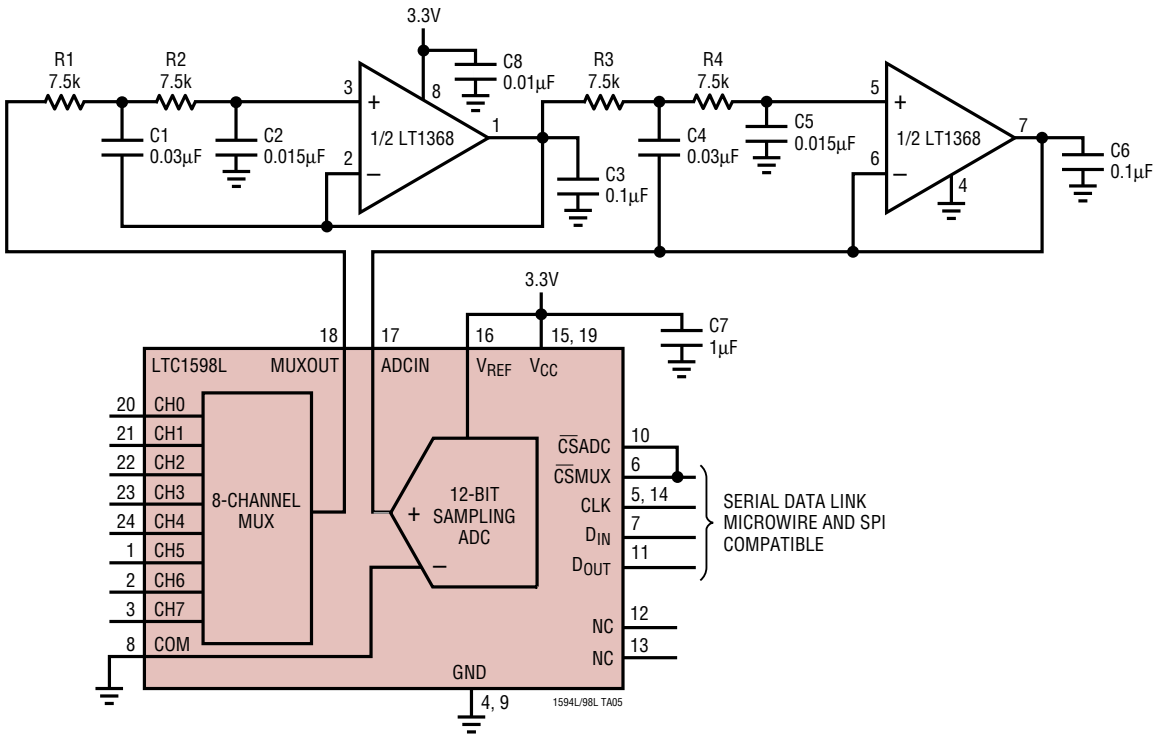
MULTICHANNEL A/D USES A SINGLE ANTIALIASING FILTER

This circuit demonstrates how the LTC1598L's independent analog multiplexer can simplify design of a 12-bit data acquisition system. All eight channels are MUXed into a single 1kHz, 4th order Sallen-Key antialiasing filter, which is designed for single supply operation. Since the LTC1598L's data converter accepts inputs from ground to the positive supply, rail-to-rail op amps were chosen for the filter to maximize dynamic range. The LT1368 dual rail-to-rail op amp is designed to operate with 0.1µF load capacitors (C1 and C2). These capacitors provide frequency compensation for the amplifiers and help reduce the amplifier's output impedance and improve supply rejection at high frequencies. The filter contributes less than 1LSB of error due to offsets and bias currents. The filter's noise and distortion are less than –72dB for a 100Hz, $2V_{P-P}$ offset sine input.

The combined MUX and A/D errors result in an integral nonlinearity error of ±3LSB (maximum) and a differential nonlinearity error of ±3/4LSB (maximum). The typical signal-to-noise plus distortion ratio is 68dB, with approximately –78dB of total harmonic distortion. The LTC1598L is programmed through a 4-wire serial interface that is compatible with MICROWIRE, SPI and QSPI. Maximum serial clock speed is 200kHz, which corresponds to a 10.5kHz sampling rate.

The complete circuit consumes approximately 600µA from a single 3V supply.

Simple Data Acquisition System Takes Advantage of the LTC1598L's MUXOUT/ADCIN Pins to Filter Analog Signals Prior to A/D Conversion



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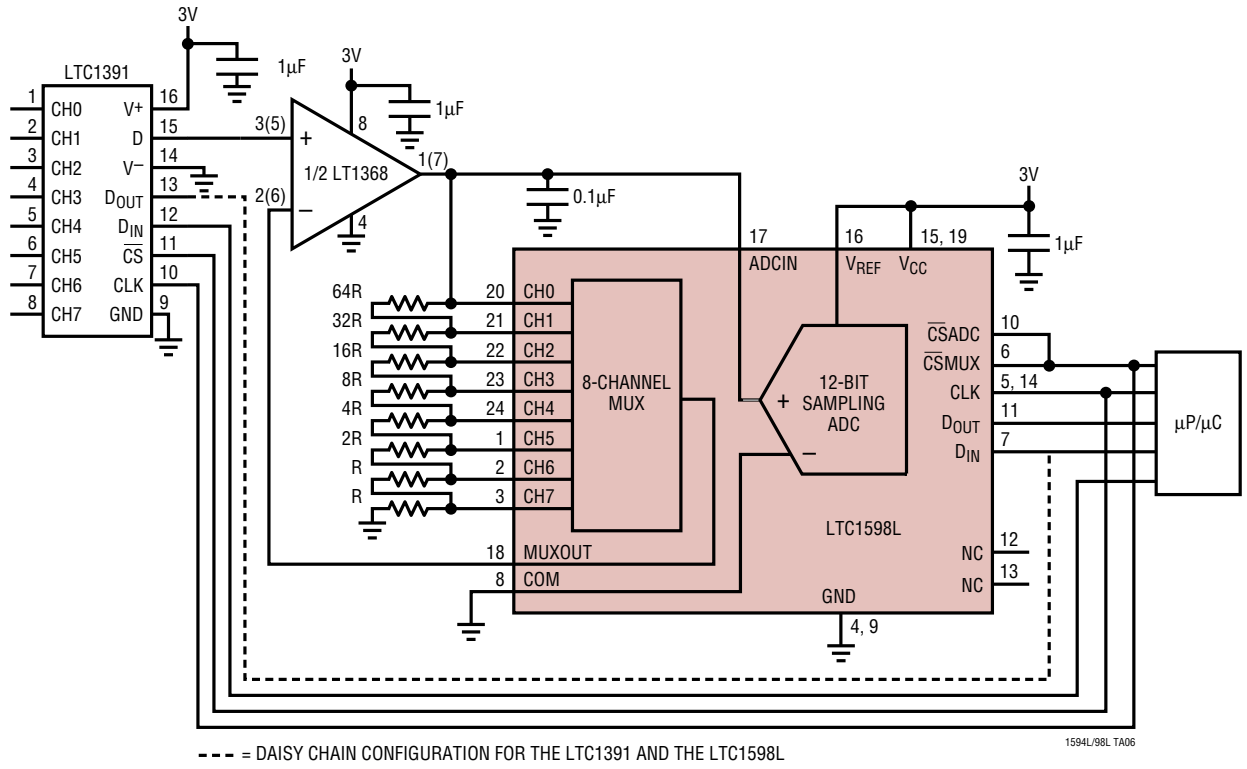
TYPICAL APPLICATIONS

Using MUXOUT/ADCIN Loop as PGA

This figure shows the LTC1598L's MUXOUT/ADCIN pins and an LT1368 being used to create a single channel PGA with eight noninverting gains. Combined with the LTC1391, the system can expand to eight channels and eight gains for each channel. Using the LTC1594L, the PGA is reduced to four gains. The output of the LT1368 drives the ADCIN and the resistor ladder. The resistors above the selected MUX channel form the feedback for the LT1368. The gain for this amplifier is $R_{S1}/R_{S2} + 1$. R_{S1} is the summation of the resistors above the selected MUX channel and R_{S2} is the summation of the resistors below the selected MUX channel. If CH0 is selected, the gain is 1 since R_{S1} is 0. Table 1 shows the gain for each MUX channel. The LT1368 dual rail-to-rail op amp is designed to operate with 0.1µF load capacitors. These capacitors provide frequency compensation for the amplifiers, help reduce the amplifiers' output impedance and improve supply rejection at high frequencies. Because the LT1368's I_B is low, the R_{ON} of the selected channel will not affect the gain given by the formula above.

Using the MUXOUT/ADCIN Pins of the LTC1598L to Form a PGA. The LTC1391 MUX Allows Eight Input Channels to be Digitized



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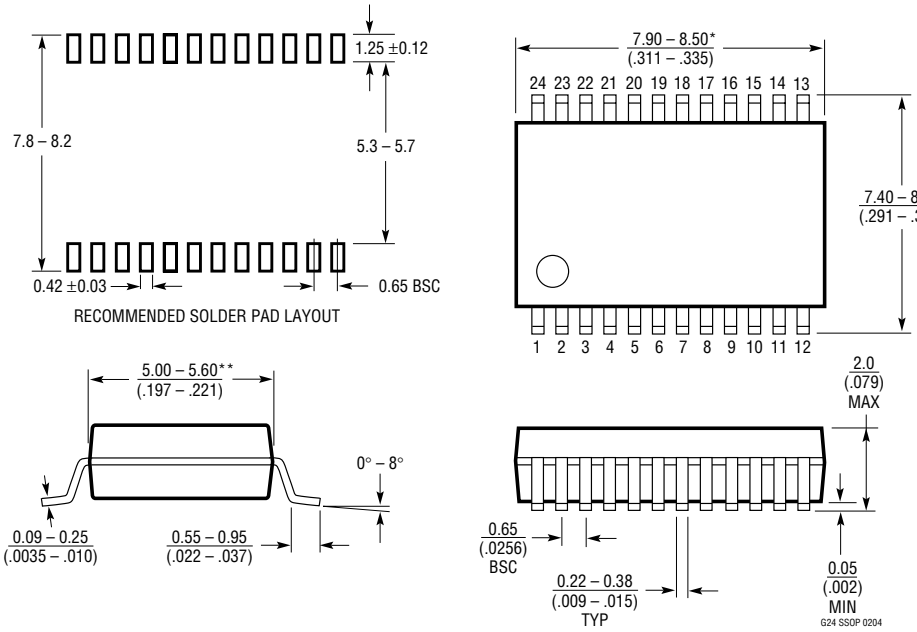
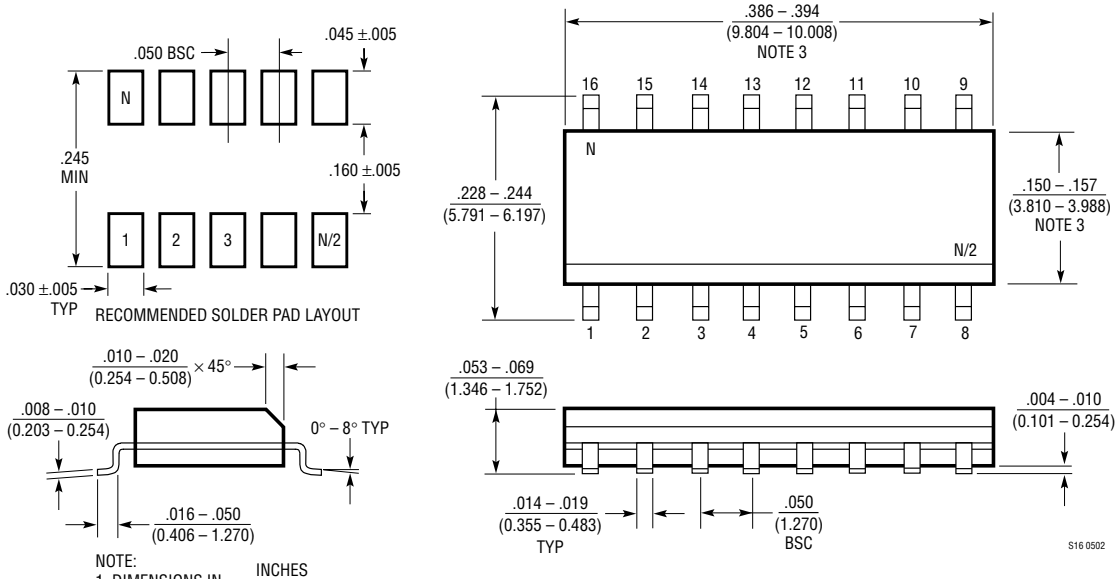
PACKAGE DESCRIPTION

G Package
24-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

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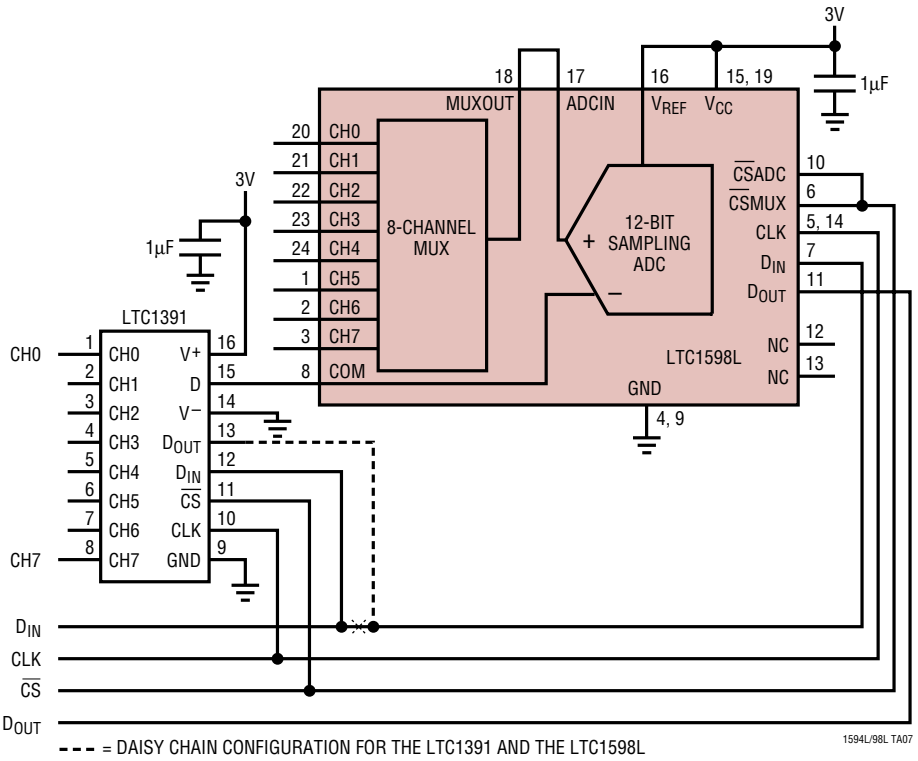
TYPICAL APPLICATION

Using the LTC1598L and LTC1391 as an 8-Channel Differential 12-Bit ADC System



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1096/LTC1098	8-Pin SO, Micropower 8-Bit ADCs	Low Power, Small Size, Low Cost
LTC1096L/LTC1098L	8-Pin SO, 2.65V Micropower 8-Bit ADCs	Low Power, Small Size, Low Cost
LTC1196/LTC1198	8-Pin SO, 1Msps 8-Bit ADCs	Low Power, Small Size, Low Cost
LTC1282	3V High Speed Parallel 12-Bit ADC	140ksps, Complete with V_{REF}, CLK, Sample-and-Hold
LTC1285/LTC1288	8-Pin SO, 3V, Micropower 12-Bit ADCs	1- or 2-Channel, Auto Shutdown
LTC1286/LTC1298	8-Pin SO, 5V, Micropower 12-Bit ADCs	1- or 2-Channel, Auto Shutdown
LTC1289	Multiplexed 3V, 12-Bit ADC	8-Channel 12-Bit Serial I/O
LTC1296	Multiplexed 5V, 12-Bit ADC	8-Channel 12-Bit Serial I/O
LTC1415	5V High Speed Parallel 12-Bit ADC	1.25Msps, Complete with V_{REF}, CLK, Sample-and-Hold
LTC1594	4-Channel, 5V Micropower 12-Bit ADC	Low Power, Small Size, Low Cost
LTC1598	8-Channel, 5V Micropower 12-Bit ADC	Low Power, Small Size, Low Cost

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