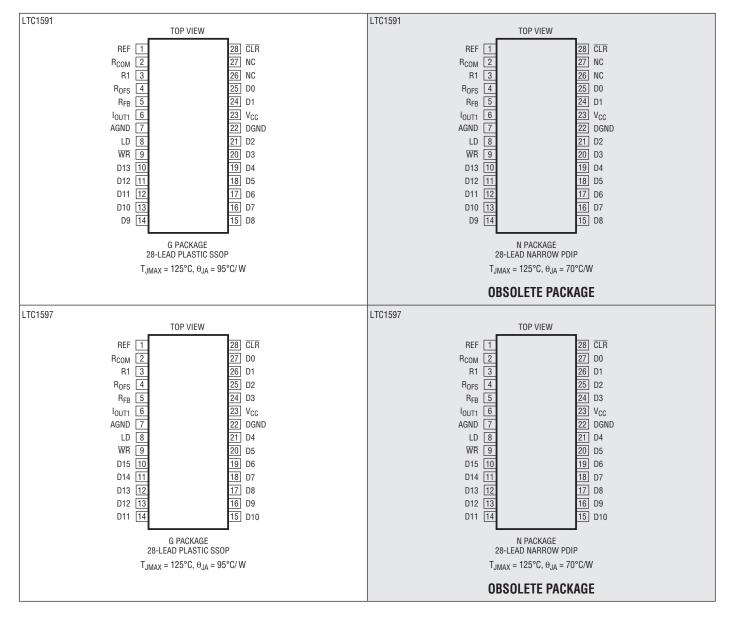
ABSOLUTE MAXIMUM RATINGS (Note 1)

V _{CC} to AGND	0.5V to 7V
V _{CC} to DGND	0.5V to 7V
AGND to DGND	$V_{CC} + 0.5V$
DGND to AGND	V _{CC} + 0.5V
REF, ROFS, RFB, R1, RCOM to AGND, D	GND ±25V
Digital Inputs to DGND0	$.5V \text{ to } (V_{CC} + 0.5V)$
I _{OUT1} to AGND0	$.5V \text{ to}(V_{CC} + 0.5V)$
Maximum Junction Temperature	125°C

Operating Temperature Range	
LTC1591C/LTC1591-1C	
LTC1597C/LTC1597-1C	0°C to 70°C
LTC1591I/LTC1591-1I	
LTC1597I/LTC1597-1I	40°C to 85°C
Storage Temperature Range	65°C to 150°C
Lead Temperature (Soldering, 10	sec) 300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1591CG#PBF	LTC1591CG#TRPBF	LTC1591CG	28-Lead Plastic SSOP	0°C to 70°C
LTC1591-1CG#PBF	LTC1591-1CG#TRPBF	LTC1591-1CG	28-Lead Plastic SSOP	0°C to 70°C
LTC1591IG#PBF	LTC1591IG#TRPBF	LTC1591IG	28-Lead Plastic SSOP	-40°C to 85°C
LTC1591-1IG#PBF	LTC1591-1IG#TRPBF	LTC1591-1IG	28-Lead Plastic SSOP	-40°C to 85°C
LTC1597ACG#PBF	LTC1597ACG#TRPBF	LTC1597ACG	28-Lead Plastic SSOP	0°C to 70°C
LTC1597-1ACG#PBF	LTC1597-1ACG#TRPBF	LTC1597-1ACG	28-Lead Plastic SSOP	0°C to 70°C
LTC1597BCG#PBF	LTC1597BCG#TRPBF	LTC1597BCG	28-Lead Plastic SSOP	0°C to 70°C
LTC1597-1BCG#PBF	LTC1597-1BCG#TRPBF	LTC1597-1BCG	28-Lead Plastic SSOP	0°C to 70°C
LTC1597AIG#PBF	LTC1597AIG#TRPBF	LTC1597AIG	28-Lead Plastic SSOP	-40°C to 85°C
LTC1597-1AIG#PBF	LTC1597-1AIG#TRPBF	LTC1597-1AIG	28-Lead Plastic SSOP	-40°C to 85°C
LTC1597BIG#PBF	LTC1597BIG#TRPBF	LTC1597BIG	28-Lead Plastic SSOP	-40°C to 85°C
LTC1597-1BIG#PBF	LTC1597-1BIG#TRPBF	LTC1597-1BIG	28-Lead Plastic SSOP	-40°C to 85°C
		OBSOLETE I	PACKAGE	
LTC1591CN#PBF	LTC1591CN#TRPBF	LTC1591CN	28-Lead Narrow PDIP	0°C to 70°C
LTC1591-1CN#PBF	LTC1591-1CN#TRPBF	LTC1591-1CN	28-Lead Narrow PDIP	0°C to 70°C
LTC1591IN#PBF	LTC1591IN#TRPBF	LTC1591IN	28-Lead Narrow PDIP	-40°C to 85°C
LTC1591-1IN#PBF	LTC1591-1IN#TRPBF	LTC1591-1IN	28-Lead Narrow PDIP	-40°C to 85°C
LTC1597ACN#PBF	LTC1597ACN#TRPBF	LTC1597ACN	28-Lead Narrow PDIP	0°C to 70°C
LTC1597-1ACN#PBF	LTC1597-1ACN#TRPBF	LTC1597-1ACN	28-Lead Narrow PDIP	0°C to 70°C
LTC1597BCN#PBF	LTC1597BCN#TRPBF	LTC1597BCN	28-Lead Narrow PDIP	0°C to 70°C
LTC1597-1BCN#PBF	LTC1597-1BCN#TRPBF	LTC1597-1BCN	28-Lead Narrow PDIP	0°C to 70°C
LTC1597AIN#PBF	LTC1597AIN#TRPBF	LTC1597AIN	28-Lead Narrow PDIP	-40°C to 85°C
LTC1597-1AIN#PBF	LTC1597-1AIN#TRPBF	LTC1597-1AIN	28-Lead Narrow PDIP	-40°C to 85°C
LTC1597BIN#PBF	LTC1597BIN#TRPBF	LTC1597BIN	28-Lead Narrow PDIP	-40°C to 85°C
LTC1597-1BIN#PBF	LTC1597-1BIN#TRPBF	LTC1597-1BIN	28-Lead Narrow PDIP	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part markings, go to: http://www.linear.com/leadfree/For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

 $V_{CC} = 5V \pm 10\%, \ V_{REF} = 10V, \ I_{OUT1} = AGND = DGND = 0V, \ T_A = T_{MIN} \ to \ T_{MAX}, \ unless \ otherwise \ noted.$

				LT	C1591	/-1	LTC	1597B,	/-1B	LT(C1597A/	-1A	
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Accuracy	1												
	Resolution		•	14			16			16			Bits
	Monotonicity		•	14			16			16			Bits
INL	Integral Nonlinearity	(Note 2) T _A = 25°C T _{MIN} to T _{MAX}	•			±1 ±1			± 2 ± 2		±0.25 ±0.35	±1 ±1	LSB LSB
DNL	Differential Nonlinearity	T _A = 25°C T _{MIN} to T _{MAX}	•			±1 ±1			±1		±0.2 ±0.2	±1 ±1	LSB LSB
GE	Gain Error	Unipolar Mode (Note 3) T _A = 25°C T _{MIN} to T _{MAX}	•			±4 ±6			±16 ±24		2	±16 ±16	LSB LSB
		Bipolar Mode (Note 3) T _A = 25°C T _{MIN} to T _{MAX}	•			±4 ±6			±16 ±24		2	±16 ±16	LSB LSB
	Gain Temperature Coefficient	(Note 4) ∆Gain/∆Temperature	•		1	2		1	2		1	2	ppm/°C
	Bipolar Zero-Scale Error	$T_A = 25$ °C T_{MIN} to T_{MAX}	•			±3 ±5			±10 ±16			±5 ±8	LSB LSB
I _{LKG}	OUT1 Leakage Current	(Note 5) T _A = 25°C T _{MIN} to T _{MAX}	•			±5 ±15			±5 ±15			±5 ±15	nA nA
PSRR	Power Supply Rejection Ratio	V _{CC} = 5V ±10	•		±0.1	±1		±0.4	±2		±0.4	±2	LSB/V

 $V_{CC} = 5V \pm 10\%, \ V_{REF} = 10V, \ I_{OUT1} = AGND = DGND = 0V, \ T_A = T_{MIN} \ to \ T_{MAX}, \ unless \ otherwise \ noted.$

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference	Input						
R _{REF}	DAC Input Resistance (Unipolar)	(Note 6)	•	4.5	6	10	kΩ
R1/R2	R1/R2 Resistance (Bipolar)	(Notes 6, 13)	•	9	12	20	kΩ
R _{OFS} , R _{FB}	Feedback and Offset Resistances	(Note 6)	•	9	12	20	kΩ
AC Perforn	nance (Note 4)						
	Output Current Settling Time	(Notes 7, 8)			1		μs
	Mid-Scale Glitch Impulse	(Note 12)			2		nV-s
	Digital-to-Analog Glitch Impulse	(Note 9)			1		nV-s
	Multiplying Feedthrough Error	V _{REF} = ±10V, 10kHz Sine Wave			1		mV _{P-P}
THD	Total Harmonic Distortion	(Note 10)			108		dB
	Output Noise Voltage Density	(Note 11)			10		nV/√Hz
	Harmonic Distortion (Digital Waveform Generation)	Unipolar Mode (Note 14) 2nd Harmonic 3rd Harmonic SFDR			94 101 94		dB dB dB
		Bipolar Mode (Note 14) 2nd Harmonic 3rd Harmonic SFDR			94 101 94		dB dB dB



ELECTRICAL CHARACTERISTICS The • denotes specifications that apply over the full operating temperature range. $V_{CC} = 5V \pm 10\%$, $V_{REF} = 10V$, $I_{OUT1} = AGND = DGND = 0V$, $I_{A} = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Ou	tputs (Note 4)	·					
C _{OUT}	Output Capacitance (Note 4)	DAC Register Loaded to All 1s: C _{OUT1} DAC Register Loaded to All 0s: C _{OUT1}	•		115 70	130 80	pF pF
Digital Inp	uts						
V_{IH}	Digital Input High Voltage		•	2.4			V
V _{IL}	Digital Input low Voltage		•			0.8	V
I _{IN}	Digital Input Current		•		0.001	±1	μА
C _{IN}	Digital Input Capacitance	(Note 4) V _{IN} = 0V	•			8	pF
Timing Ch	aracteristics						
t _{DS}	Data to WR Setup Time		•	60			ns
t _{DH}	Data to WR Hold Time		•	0			ns
t _{WR}	WR Pulse Width		•	60			ns
t _{LD}	LD Pulse Width		•	110			ns
t _{CLR}	Clear Pulse Width		•	60			ns
t _{LWD}	WR to LD Delay Time		•	0			ns
Power Sup	pply						
V_{DD}	Supply Voltage		•	4.5	5	5.5	V
I _{DD}	Supply Current	Digital Inputs = 0V or V _{CC}	•			10	μА

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: ± 1 LSB = $\pm 0.006\%$ of full scale = ± 61 ppm of full scale for the LTC1591/LTC1591-1. ± 1 LSB = $\pm 0.0015\%$ of full scale = ± 15.3 ppm of full scale for the LTC1597/LTC1597-1.

Note 3: Using internal feedback resistor.

Note 4: Guaranteed by design, not subject to test.

Note 5: I_(OUT1) with DAC register loaded to all 0s.

Note 6: Typical temperature coefficient is 100ppm/°C.

Note 7: I_{OUT1} load = 100Ω in parallel with 13pF.

Note 8: To 0.006% for a full-scale change, measured from the rising edge of LD for the LTC1591/LTC1591-1. To 0.0015% for a full-scale change, measured from the rising edge of LD for the LTC1597/LTC1597-1.

Note 9: $V_{REF} = 0V$. DAC register contents changed from all 0s to all 1s or all 1s to all 0s.

Note 10: $V_{REF} = 6V_{RMS}$ at 1kHz. DAC register loaded with all 1s.

Note 11: Calculation from $e_n = \sqrt{4kTRB}$ where: k = Boltzmann constant $(J)^{\circ}K)$, R = resistance (Ω) , T = temperature $({}^{\circ}K)$, B = bandwidth (Hz).

Note 13: R1 and R2 are measured between R1 and R_{COM} , REF and R_{COM} .

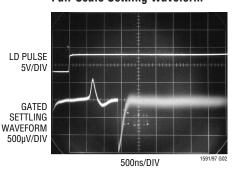
Note 14: Measured using the LT1468 op amp in unipolar mode for I/V converter and LT1468 I/V and LT1001 reference inverter in bipolar mode. Sample Rate = 50kHz, Signal Frequency = 1kHz, $V_{REF} = 5V$, $T_A = 25^{\circ}C$.



TYPICAL PERFORMANCE CHARACTERISTICS (LTC1591/LTC1597)

Mid-Scale Glitch Impulse 40 USING AN LT1468 C_{FEEDBACK} = 30pF V_{REF} = 10V 30 20 OUTPUT VOLTAGE (mV) 10 0 1nV-s TYPICAL -20 -30 -40 0.2 0.8 0.4 0.6 1.0 0 TIME (µs) 1591/97 G01

Full-Scale Settling Waveform

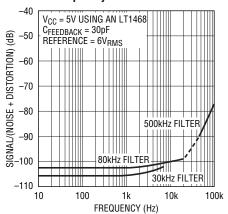


USING LT1468 OP AMP

C_{FEEDBACK} = 20pF

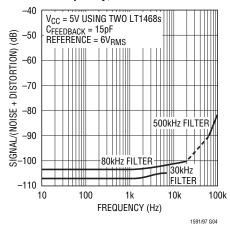
OV TO 10V STEP

Unipolar Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency

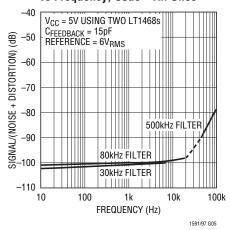


1591/97 G03

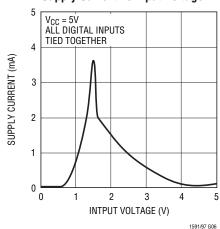
Bipolar Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency, Code = All Zeros



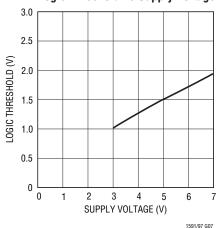
Bipolar Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency, Code = All Ones



Supply Current vs Input Voltage

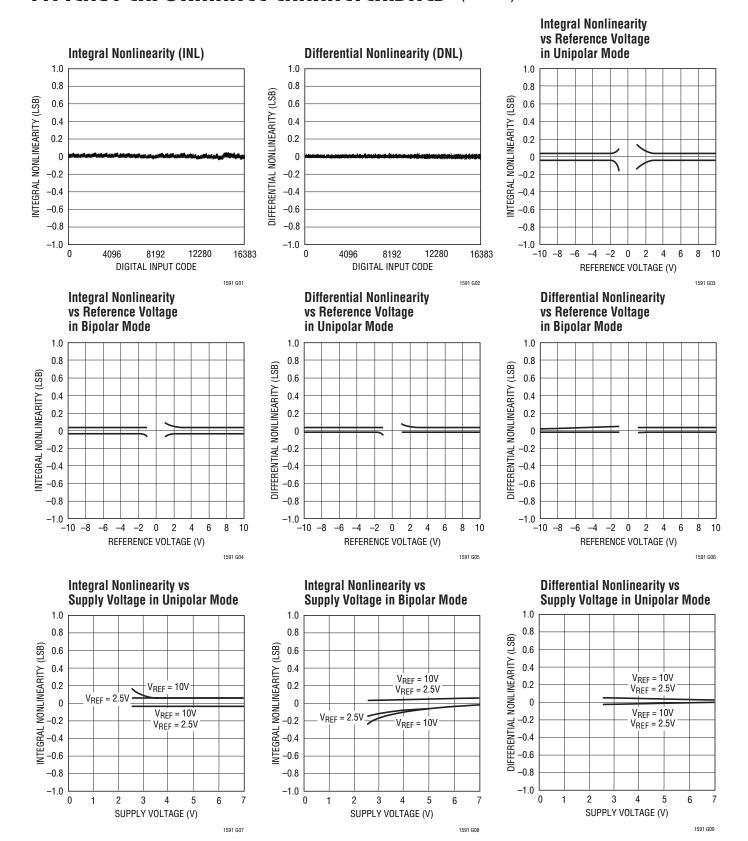


Logic Threshold vs Supply Voltage





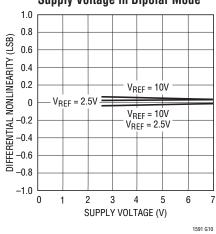
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1591)



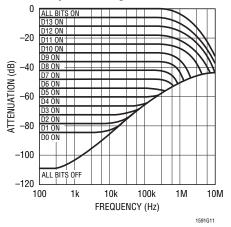
Downloaded from Arrow.com.

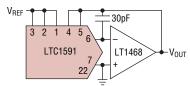
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1591)



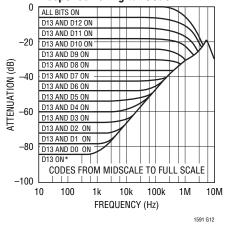


Unipolar Multiplying Mode Frequency Response vs Digital Code

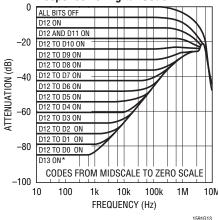




Bipolar Multiplying Mode Frequency Response vs Digital Code

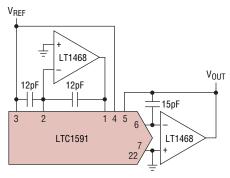


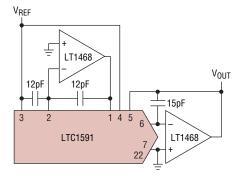
Bipolar Multiplying Mode Frequency Response vs Digital Code



*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO -84dB TYPICAL (-70dB MAX)



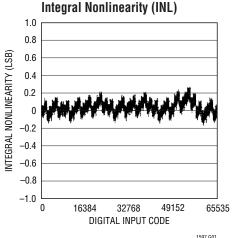


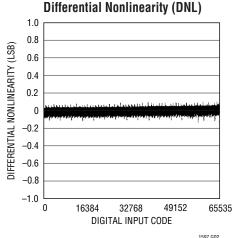


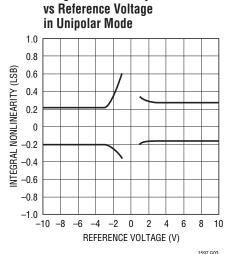


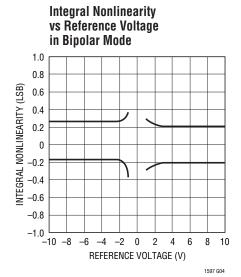
Integral Nonlinearity

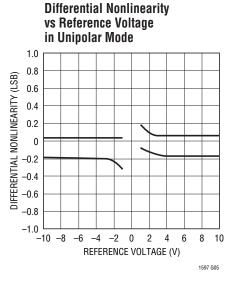
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1597)

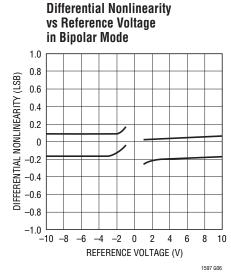


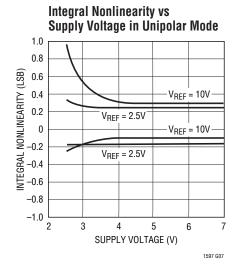


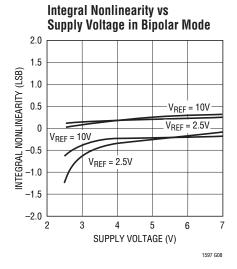


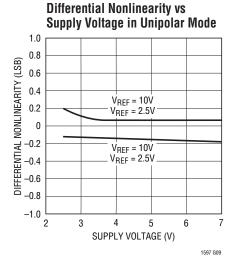




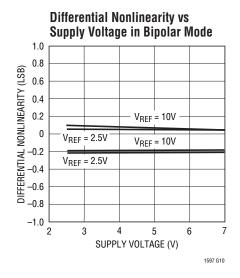




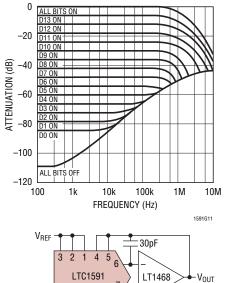




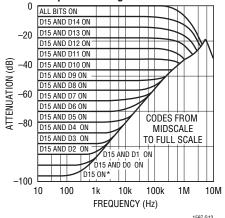
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1597)



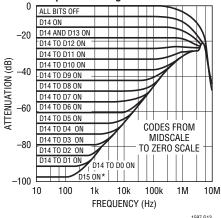
Unipolar Multiplying Mode Frequency Response vs Digital Code



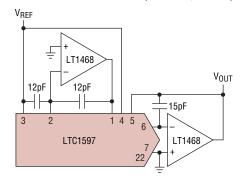
Bipolar Multiplying Mode Frequency Response vs Digital Code



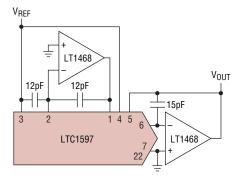
Bipolar Multiplying Mode Frequency Response vs Digital Code



*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO –96dB TYPICAL (–78dB MAX, A GRADE)



*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO -96dB TYPICAL (-78dB MAX, A GRADE)





PIN FUNCTIONS

LTC1591

REF (Pin 1): Reference Input and 4-Quadrant Resistor R2. Typically $\pm 10V$, accepts up to $\pm 25V$. In 2-Quadrant mode this is the reference input. In 4-quadrant mode, this pin is driven by external inverting reference amplifier.

R_{COM} (**Pin 2**): Center Tap Point of the Two 4-Quadrant Resistors R1 and R2. Normally tied to the inverting input of an external amplifier in 4-quadrant operation, otherwise shorted to the REF pin. See Figures 1a and 2a.

R1 (Pin 3): 4-Quadrant Resistor R1. In 2-quadrant operation short to the REF pin. In 4-quadrant mode tie to R_{OFS} (Pin 4).

 R_{OFS} (Pin 4): Bipolar Offset Resistor. Typically swings $\pm 10V$, accepts up to $\pm 25V$. In 2-quadrant operation tie to R_{FB} . In 4-quadrant operation tie to R1.

 R_{FB} (Pin 5): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp. Swings to $\pm V_{RFF}$. V_{RFF} is typically $\pm 10V$.

I_{OUT1} (Pin 6): DAC Current Output. Tie to the inverting input of the current to voltage converter op amp.

AGND (Pin 7): Analog Ground. Tie to ground.

LD (Pin 8): DAC Digital Input Load Control Input. When LD is taken to a logic high, data is loaded from the input register into the DAC register, updating the DAC output.

WR (Pin 9): DAC Digital Write Control Input. When WR is taken to a logic low, data is loaded from the digital input pins into the 14-bit wide input register.

DB13 to D2 (Pins 10 to 21): Digital Input Data Bits.

DGND (Pin 22): Digital Ground. Tie to ground.

V_{CC} (**Pin 23**): The Positive Supply Input. $4.5V \le V_{CC} \ge 5.5V$. Requires a bypass capacitor to ground.

DB1, DB0 (Pins 24, 25): Digital Input Data Bits.

NC (Pins 26, 27): No Connect.

CLR (**Pin 28**): Digital Clear Control Function for the DAC. When CLR is taken to a logic low, it sets the DAC output and all internal registers to zero code for the LTC1591 and mid-scale code for the LTC1591-1.

PIN FUNCTIONS

LTC1597

REF (Pin 1): Reference Input and 4-Quadrant Resistor R2. Typically $\pm 10V$, accepts up to $\pm 25V$. In 2-Quadrant mode this is the reference input. In 4-quadrant mode, this pin is driven by external inverting reference amplifier.

R_{COM} (**Pin 2**): Center Tap Point of the Two 4-Quadrant Resistors R1 and R2. Normally tied to the inverting input of an external amplifier in 4-quadrant operation, otherwise shorted to the REF pin. See Figures 1b and 2b.

R1 (Pin 3): 4-Quadrant Resistor R1. In 2-quadrant operation short to the REF pin. In 4-quadrant mode tie to R_{OFS} (Pin 4).

R_{OFS} (**Pin 4**): Bipolar Offset Resistor. Typically swings $\pm 10V$, accepts up to $\pm 25V$. In 2-quadrant operation tie to R_{FB}. In 4-quadrant operation tie to R1.

R_{FB} (Pin 5): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp. Swings to $\pm V_{RFF}$. V_{RFF} is typically $\pm 10V$.

I_{OUT1} **(Pin 6):** DAC Current Output. Tie to the inverting input of the current to voltage converter op amp.

AGND (Pin 7): Analog Ground. Tie to ground.

LD (Pin 8): DAC Digital Input Load Control Input. When LD is taken to a logic high, data is loaded from the input register into the DAC register, updating the DAC output.

WR (Pin 9): DAC Digital Write Control Input. When WR is taken to a logic low, data is loaded from the digital input pins into the 16-bit wide input register.

DB15 to D4 (Pins 10 to 21): Digital Input Data Bits.

DGND (Pin 22): Digital Ground. Tie to ground.

V_{CC} (**Pin 23**): The Positive Supply Input. $4.5V \le V_{CC} \ge 5.5V$. Requires a bypass capacitor to ground.

DB3 to DB0 (Pins 24 to 27): Digital Input Data Bits.

CLR (**Pin 28**): Digital Clear Control Function for the DAC. When CLR is taken to a logic low, it sets the DAC output and all internal registers to zero code for the LTC1597 and mid-scale code for the LTC1597-1.

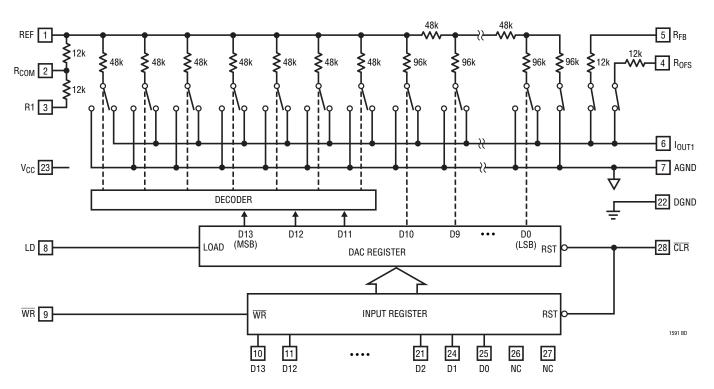
TRUTH TABLE

Table 1

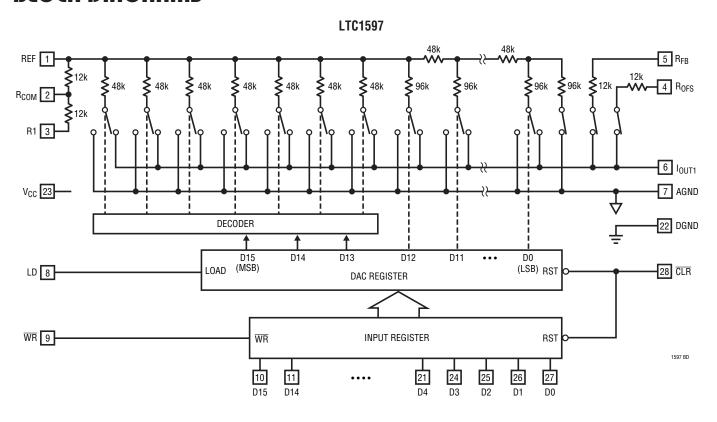
CONT	ROL IN	PUTS	
CLR	WR	LD	REGISTER OPERATION
0	Χ	Х	Reset Input and DAC Register to All 0s for LTC1591/LTC1597 and Mid-Scale for LTC1591-1/LTC1597-1 (Asynchronous Operation)
1	0	0	Load Input Register with All 14/16 Data Bits
1	1	1	Load DAC Register with the Contents of the Input Register
1	¬ ^г	¬¹ г	Input and DAC Register Are Transparent
1			$CLK = LD$ and \overline{WR} Tied Together. The 14/16 Data Bits Are Loaded into the Input Register on the Falling Edge of the CLK and Then Loaded into the DAC Register on the Rising Edge of the CLK
1	1	0	No Register Operation

BLOCK DIAGRAMS

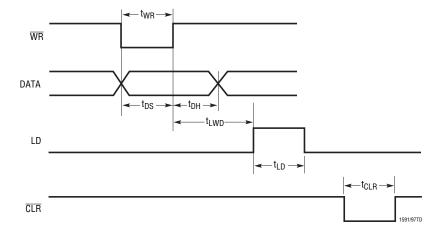
LTC1591



BLOCK DIAGRAMS



TIMING DIAGRAM





APPLICATIONS INFORMATION

Description

The LTC1591/LTC1597 are 14-/16-bit multiplying, current output DACs with a full parallel 14-/16-bit digital interface. The devices operate from a single 5V supply and provide both unipolar 0V to -10V or 0V to 10V and bipolar $\pm 10V$ output ranges from a 10V or -10V reference input. They have three additional precision resistors on chip for bipolar operation. Refer to the block diagrams regarding the following description.

The 14-/16-bit DACs consist of a precision R-2R ladder for the 11/13LSBs. The 3MSBs are decoded into seven segments of resistor value R. Each of these segments and the R-2R ladder carries an equally weighted current of one eighth of full scale. The feedback resistor R_{FR} and 4-quadrant resistor R_{OFS} have a value of R/4. 4-quadrant resistors R1 and R2 have a magnitude of R/4. R1 and R2 together with an external op amp (see Figure 2) inverts the reference input voltage and applies it to the 14-/16bit DAC input REF, in 4-quadrant operation. The REF pin presents a constant input impedance of R/8 in unipolar mode and R/12 in bipolar mode. The output impedance of the current output pin I_{OUT1} varies with DAC input code. The I_{OUT1} capacitance due to the NMOS current steering switches also varies with input code from 70pF to 115pF. An added feature of these devices, especially for waveform generation, is a proprietary deglitcher that reduces glitch energy to below 2nV-s over the DAC output voltage range.

Digital Section

The LTC1591/LTC1597 are 14-/16-bit wide full parallel data bus inputs. The devices are double-buffered with two 14-/16-bit registers. The double-buffered feature permits the update of several DACs simultaneously. The input register is loaded directly from a 16-bit microprocessor bus when the \overline{WR} pin is brought to a logic low level. The second register (DAC register) is updated with the data from the input register when the LD pin is brought to a logic high level. Updating the DAC register updates the DAC output with the new data. To make both registers transparent for flowthrough mode, tie WR low and LD high. However, this defeats the deglitcher operation and output glitch impulse may increase. The deglitcher is activated on the rising edge of the LD pin. The versatility of the interface also allows the use of the input and DAC registers in a master slave or edge-triggered configuration. This mode of operation occurs when WR and LD are tied together. The asynchronous clear pin resets the LTC1591/ LTC1597 to zero scale and the LTC1591-1/LTC1597-1 to mid-scale. CLR resets both the input and DAC registers. These devices also have a power-on reset. Table 1 shows the truth table for the LTC1591/LT1597.

Unipolar Mode (2-Quadrant Multiplying, $V_{OUT} = 0V$ to $-V_{REF}$)

The LTC1591/LTC1597 can be used with a single op amp to provide 2-quadrant multiplying operation as shown in Figure 1. With a fixed –10V reference, the circuits shown give a precision unipolar 0V to 10V output swing.

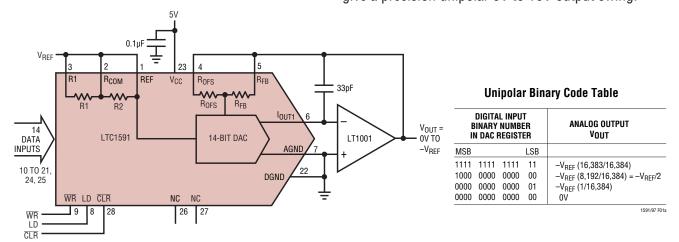


Figure 1a. Unipolar Operation (2-Quadrant Multiplication) $V_{OUT} = 0V$ to $-V_{REF}$



APPLICATIONS INFORMATION

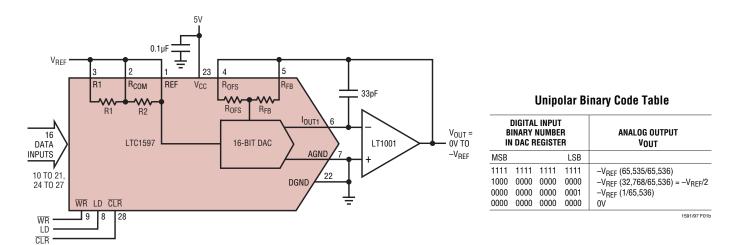


Figure 1b. Unipolar Operation (2-Quadrant Multiplication) $V_{OUT} = 0V$ to $-V_{REF}$

Bipolar Mode (4-Quadrant Multiplying, $V_{OUT} = -V_{REF}$ to V_{REF})

The LTC1591/LTC1597 contain on chip all the 4-quadrant resistors necessary for bipolar operation. 4-quadrant multiplying operation can be achieved with a minimum of external components, a capacitor and a dual op amp, as shown in Figure 2. With a fixed 10V reference, the circuit shown gives a precision bipolar – 10V to 10V output swing.

Op Amp Selection

Because of the extremely high accuracy of the 14-/16-bit LTC1591/LTC1597, thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Op amp offset will contribute mostly to output offset and gain and will have minimal effect on INL and DNL. For the LTC1597, a $500\mu V$ op amp offset will cause about 0.55LSB INL degradation and 0.15LSB DNL degradation with a 10V full-scale range. The main effects of op amp offset will be a degradation of zero-scale error equal to the op amp offset, and a degradation of full-scale error

equal to twice the op amp offset. For the LTC1597, the same $500\mu V$ op amp offset (2mV offset for LTC1591) will cause a 3.3LSB zero-scale error and a 6.5LSB full-scale error with a 10V full-scale range.

Op amp input bias current (I_{BIAS}) contributes only a zero-scale error equal to $I_{BIAS}(R_{FB}/R_{OFS}) = I_{BIAS}(6k)$. For a thorough discussion of 16-bit DAC settling time and op amp selection, refer to Application Note 74, "Component and Measurement Advances Ensure 16-Bit DAC Settling Time."

Reference Input and Grounding

For optimum performance the reference input of the LTC1597 should be driven by a source impedance of less than 1k Ω . However, these DACs have been designed to minimize source impedance effects. An 8k Ω source impedance degrades both INL and DNL by 0.2LSB.

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding should be used. AGND must be tied to the star ground with as low a resistance as possible.

LINEAR TECHNOLOGY

APPLICATIONS INFORMATION

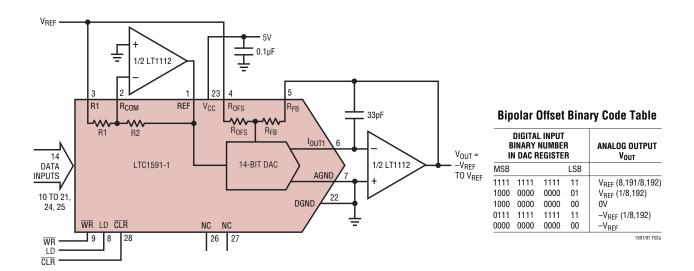


Figure 2a. Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}

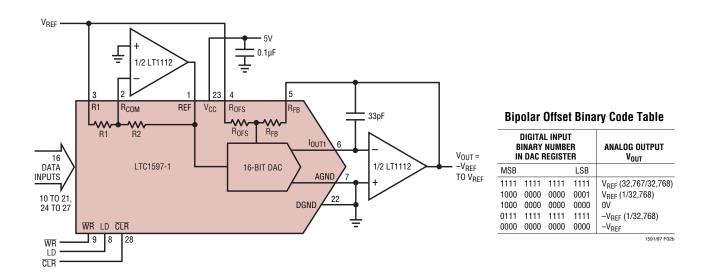
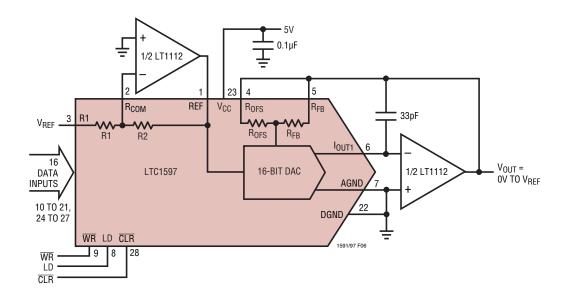


Figure 2b. Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}

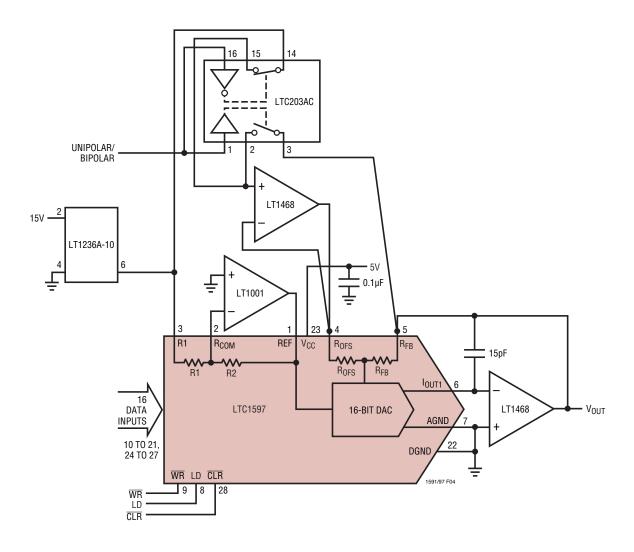
TYPICAL APPLICATIONS

Noninverting Unipolar Operation (2-Quadrant Multiplication) $V_{OUT} = 0V$ to V_{REF}



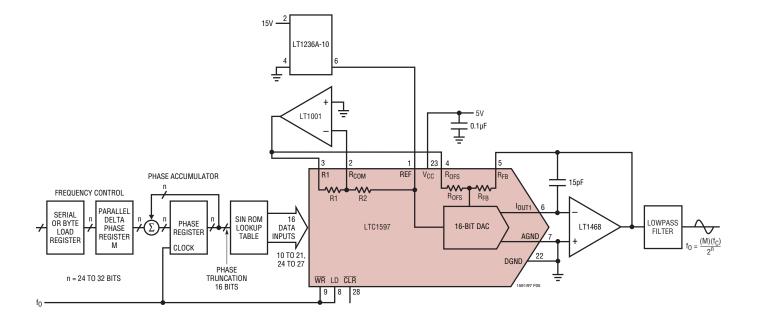
TYPICAL APPLICATIONS

16-Bit V_{OUT} DAC Programmable Unipolar/Bipolar Configuration



TYPICAL APPLICATIONS

Digital Waveform Generator

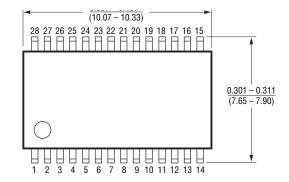


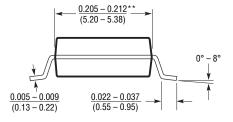
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

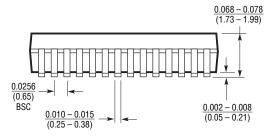
G Package 28-Lead Plastic SSOP (0.209)

(LTC DWG # 05-08-1640)





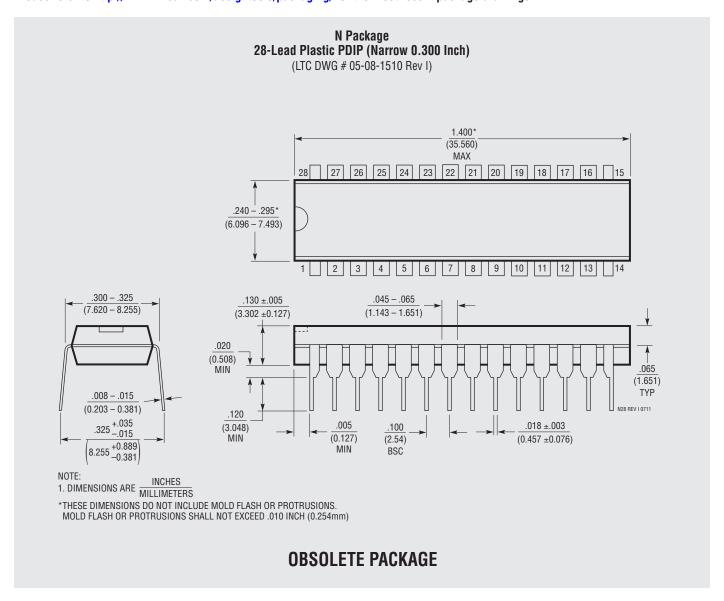
- *DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
- **DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE



G28 SSOP 0694

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

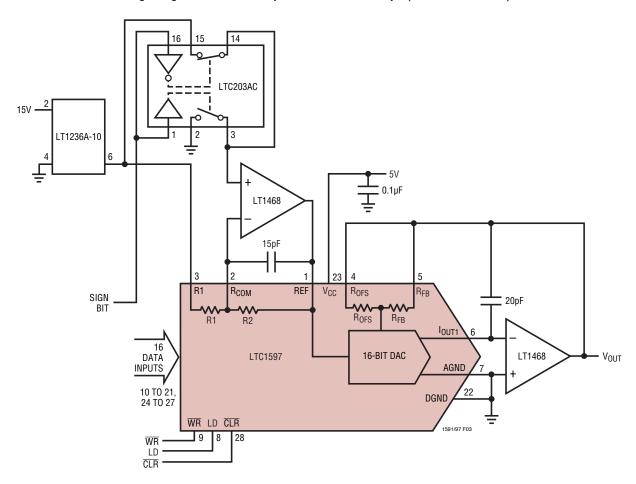


REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
В	07/15	Obsoleted 28-Lead PDIP Package	2, 3, 22

TYPICAL APPLICATION

17-Bit Sign Magnitude DAC with Bipolar Zero Error of 140µV (0.92LSB at 17 Bits) at 25°C



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Op Amps		
LT®1001	Precision Operational Amplifier	Low Offset, Low Drift
LT1112	Dual Low Power, Precision Picoamp Input Op Amp	Low Offset, Low Drift
LT1468	90MHz, 22V/µs, 16-Bit Accurate Op Amp	Precise, 1µs Settling to 0.0015%
DACs		
LTC1595/LTC1596	Serial 16-Bit Current Output DACs	Low Glitch, ±1LSB Maximum INL, DNL
LTC1650	Serial 16-Bit Voltage Output DAC	Low Noise and Glitch Rail-to-Rail V _{OUT}
LTC1658	Serial 14-Bit Voltage Output DAC	Low Power, 8-Lead MSOP Rail-to-Rail V _{OUT}
ADCs		
LTC1418	14-Bit, 200ksps 5V Sampling ADC	16mW Dissipation, Serial and Parallel Outputs
LTC1604	16-Bit, 333ksps Sampling ADC	±2.5V Input, SINAD = 90dB, THD = 100dB
LTC1605	Single 5V, 16-Bit 100ksps ADC	Low Power, ±10V Inputs
References		
LT1236	Precision Reference	Ultralow Drift, 5ppm/°C, High Accuracy 0.05%

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