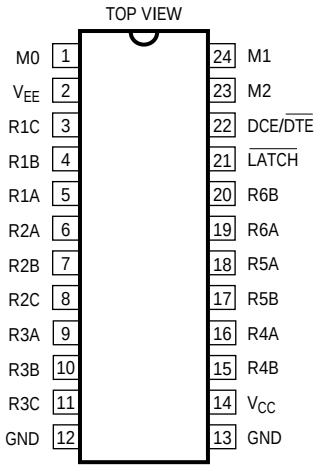
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Positive Supply Voltage (V_{CC}) 7V
Negative Supply Voltage (V_{EE}) ..... –13.2V
Input Voltage
(Logic Inputs) ..... (V_{EE} – 0.3V) to (V_{CC} + 0.3V)
Input Voltage (Load Inputs) ..... ±18V
Power Dissipation 600mW
Operating Temperature Range
LTC1344AC ..... 0°C to 70°C
LTC1344AI ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
24-LEAD PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC1344ACG
LTC1344AIG

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5%, V_{EE} = –5V ±5%, T_A = T_{MIN} to T_{MAX} (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
I_{CC}	Supply Current	All Digital Pins = GND or V_{CC}	●		0.4	1.0	mA
Terminator Pins							
$R_{V.35}$	Differential Mode Impedance Common Mode Impedance	All Loads (Figure 1), –2V ≤ V_{CM} ≤ 2V (Commercial) All Loads (Figure 2), –2V ≤ V_{CM} ≤ 2V (Commercial)	● ●	90 135	104 153	110 165	Ω Ω
		All Loads (Figure 1), –2V ≤ V_{CM} ≤ 2V (Industrial) All Loads (Figure 2), –2V ≤ V_{CM} ≤ 2V (Industrial)	● ●	90 130	104 153	115 170	Ω Ω
$R_{V.11}$	Differential Mode Impedance	All Loads (Figure 1), V_{CM} = 0V (Commercial) All Loads (Figure 1), –7V ≤ V_{CM} ≤ 7V (Commercial)	●	100 100	104 104	110	Ω Ω
		All Loads (Figure 1), V_{CM} = 0V (Industrial) All Loads (Figure 1), –7V ≤ V_{CM} ≤ 7V (Industrial)	●	95 100	104 104	115	Ω Ω
I_{LEAK}	High Impedance Leakage Current	All Loads, –7V ≤ V_{CM} ≤ 7V	●		±1	±50	µA
Logic Inputs							
V_{IH}	Input High Voltage	All Logic Input Pins	●	2			V
V_{IL}	Input Low Voltage	All Logic Input Pins	●			0.8	V
I_{IN}	Input Current	All Logic Input Pins	●			±10	µA

The ● denotes specifications which apply over the full operating temperature range.

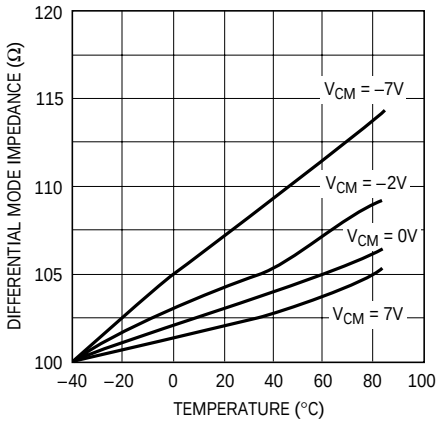
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 3: All typicals are given at V_{CC} = 5V, V_{EE} = –5V, T_A = 25°C.

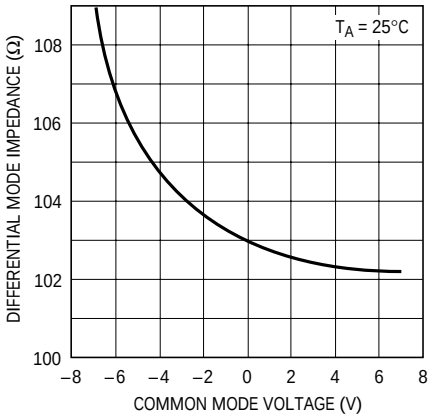
TYPICAL PERFORMANCE CHARACTERISTICS

V.11 or V.35 Differential Mode Impedance vs Temperature



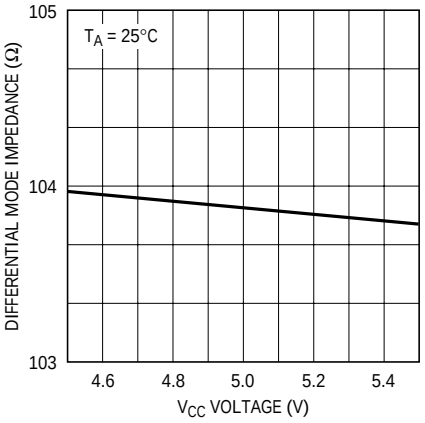
1344 G01

V.11 or V.35 Differential Mode Impedance vs Common Mode Voltage



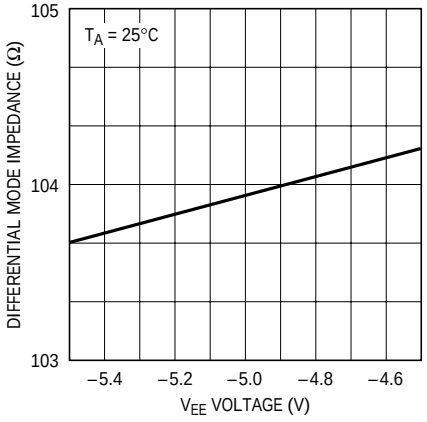
1344 G02

V.11 or V.35 Differential Mode Impedance vs Supply Voltage (V_{CC})



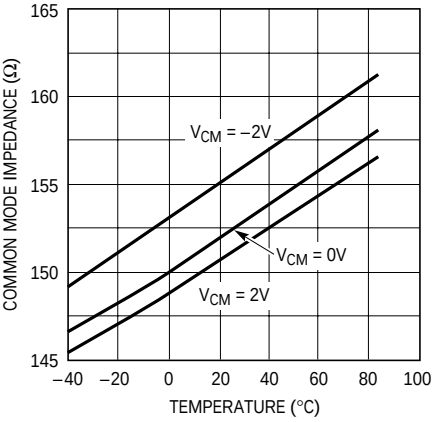
1344 G03

V.11 or V.35 Differential Mode Impedance vs Negative Supply Voltage (V_{EE})



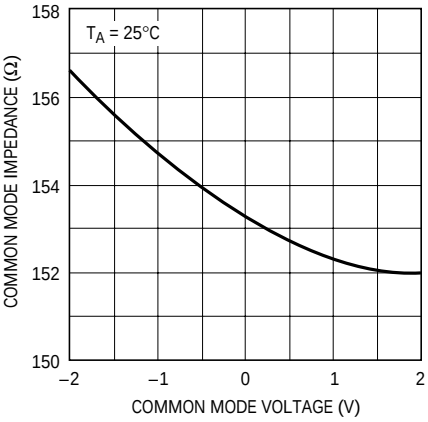
1344 G04

V.35 Common Mode Impedance vs Temperature



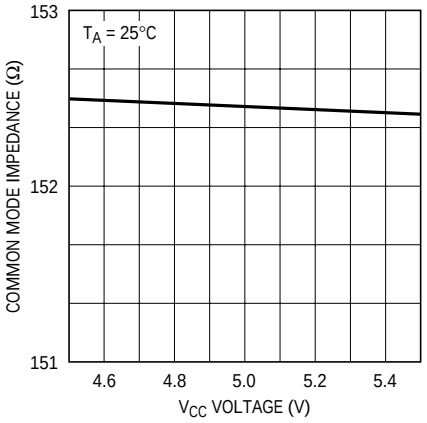
1344 G05

V.35 Common Mode Impedance vs Common Mode Voltage



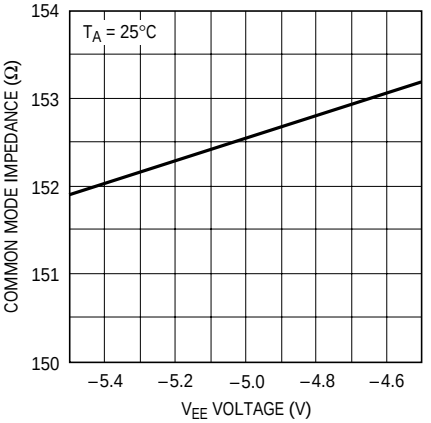
1344 G06

V.35 Common Mode Impedance vs Supply Voltage (V_{CC})



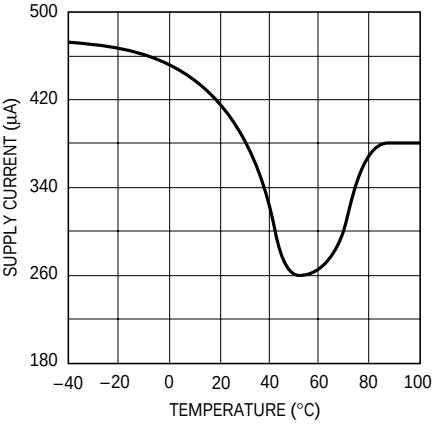
1344 G07

V.35 Common Mode Inpedance vs Negative Supply Voltage (V_{EE})



1344 G08

Supply Current vs Temperature



1344 G09

PIN FUNCTIONS

M0 (Pin 1): TTL Level Mode Select Input. The data on M0 is latched when LATCH is high.

V_{EE} (Pin 2): Negative Supply Voltage Input. Can connect directly to the LTC1543 V_{EE} pin. Connect a 1µF capacitor to ground.

R1C (Pin 3): Load 1 Center Tap.

R1B (Pin 4): Load 1 Node B.

R1A (Pin 5): Load 1 Node A.

R2A (Pin 6): Load 2 Node A.

R2B (Pin 7): Load 2 Node B.

R2C (Pin 8): Load 2 Center Tap.

R3A (Pin 9): Load 3 Node A.

R2B (Pin 10): Load 2 Node B.

R3C (Pin 11): Load 3 Center Tap.

GND (Pin 12): Ground Connection for Load 1 to Load 3.

GND (Pin 13): Ground Connection for Load 4 to Load 6.

V_{CC} (Pin 14): Positive Supply Input. $4.75V \leq V_{CC} \leq 5.25V$.

R4B (Pin 15): Load 4 Node B.

R4A (Pin 16): Load 4 Node A.

R5B (Pin 17): Load 5 Node B.

R5A (Pin 18): Load 5 Node A.

R6A (Pin 19): Load 6 Node A.

R6B (Pin 20): Load 6 Node B.

$\overline{\text{LATCH}}$ (Pin 21): TTL Level Logic Signal Latch Input. When LATCH is low the input buffers on M0, M1, M2 and DCE/DTE are transparent. When LATCH is high the logic pins are latched into their respective input buffers. The data latch allows the select lines to be shared between multiple I/O ports.

DCE/$\overline{\text{DTE}}$ (Pin 22): TTL Level Mode Select Input. DCE mode is selected when high and DTE mode when low. The data on DCE/DTE is latched when LATCH is high.

M2 (Pin 23): TTL Level Mode Select Input 1. The data on M2 is latched when LATCH is high.

M1 (Pin 24): TTL Level Mode Select Input 2. The data on M1 is latched when LATCH is high.

TEST CIRCUITS

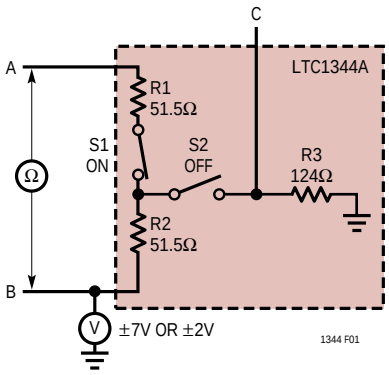


Figure 1. Differential V.11 or V.35 Impedance Measurement

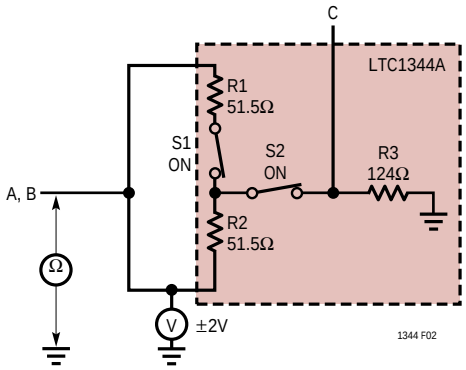
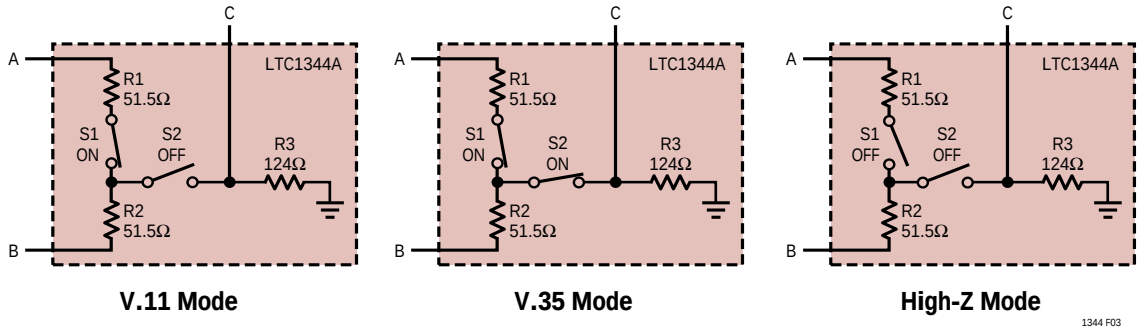


Figure 2. V.35 Common Mode Impedance Measurement

MODE SELECTION

LTC1344A MODE NAME	DCE/$\overline{\text{DTE}}$	M2	M1	M0	R1	R2	R3	R4	R5	R6
V.10/RS423	X	0	0	0	Z	Z	Z	Z	Z	Z
RS530A	0	0	0	1	Z	Z	Z	V.11	V.11	V.11
	1	0	0	1	Z	Z	Z	Z	V.11	V.11
RS530	0	0	1	0	Z	Z	Z	V.11	V.11	V.11
	1	0	1	0	Z	Z	Z	Z	V.11	V.11
X.21	0	0	1	1	Z	Z	Z	V.11	V.11	V.11
	1	0	1	1	Z	Z	Z	Z	V.11	V.11
V.35	0	1	0	0	V.35	V.35	Z	V.35	V.35	V.35
	1	1	0	0	V.35	V.35	V.35	Z	V.35	V.35
RS449/V.36	0	1	0	1	Z	Z	Z	V.11	V.11	V.11
	1	1	0	1	Z	Z	Z	Z	V.11	V.11
V.28/RS232	X	1	1	0	Z	Z	Z	Z	Z	Z
No Cable	X	1	1	1	V.11	V.11	V.11	V.11	V.11	V.11

X = don't care, 0 = logic low, 1 = logic high



V.11 Mode **V.35 Mode** **High-Z Mode**

Figure 3. LTC1344A Modes

APPLICATIONS INFORMATION

Multiprotocol Cable Termination

One of the most difficult problems facing the designer of a multiprotocol serial interface is how to allow the transmitters and receivers for different electrical standards to share connector pins. In some cases the transmitters and receivers for each interface standard can be simply tied together and the appropriate circuitry enabled. But the biggest problem still remains: how to switch the various cable termination required by the different standards.

Traditional implementations have included switching resistors with expensive relays or requiring the user to change termination modules every time the interface standard has changed. Custom cables have been used with the termination in the cable head. Another method uses separate termination built on the board, and a custom cable which routes the signals to the appropriate termination. Switching the termination using FETs is difficult because the FETs must remain off even though the signal voltage is beyond the supply voltage for the FET drivers or the power is off.

The LTC1344A solves the cable termination switching problem via software control. The LTC1344A provides termination for the V.10 (RS423), V.11 (RS422), V.28 (RS232) and V.35 electrical protocols.

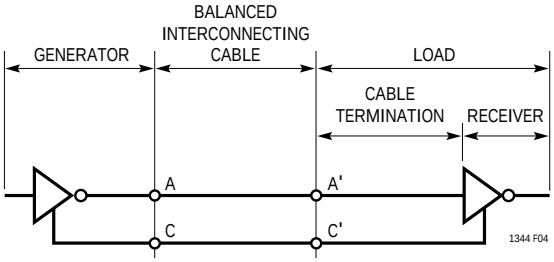


Figure 4. Typical V.10 Interface

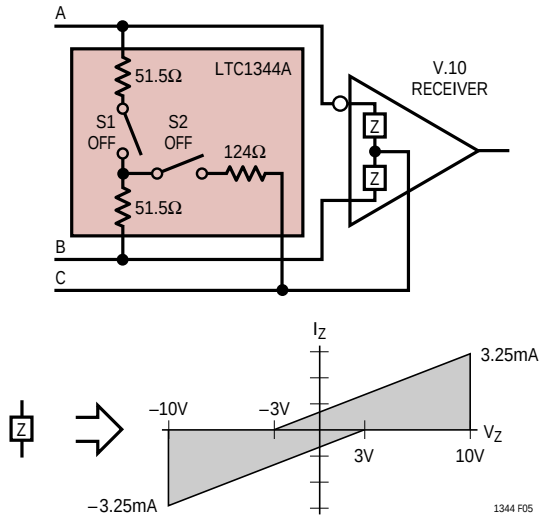


Figure 5. V.10 Interface Using the LTC1344A

V.10 (RS423) Termination

A typical V.10 unbalanced interface is shown in Figure 4. A V.10 single-ended generator output A with ground C is connected to a differential receiver with input A' connected to A and input C' connected to the signal return ground C. Usually no cable termination is required for V.10 interfaces but the receiver inputs must be compliant with the impedance curve shown in Figure 5.

In V.10 mode, both switches S1 and S2 are turned off so the only cable termination is the input impedance of the V.10 receiver.

V.11 (RS422) Termination

A typical V.11 balanced interface is shown in Figure 6. A V.11 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.11 interface requires a differential termination at the receiver end that has a minimum value of 100Ω. The receiver inputs must also be compliant with the impedance curve shown in Figure 7.

In V.11 mode, switch S1 is turned on and S2 is turned off so the cable is terminated with a 103Ω impedance.

APPLICATIONS INFORMATION

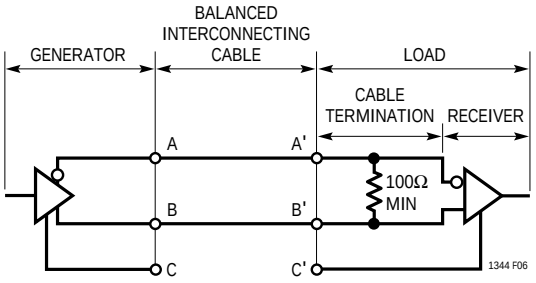


Figure 6. Typical V.11 Interface

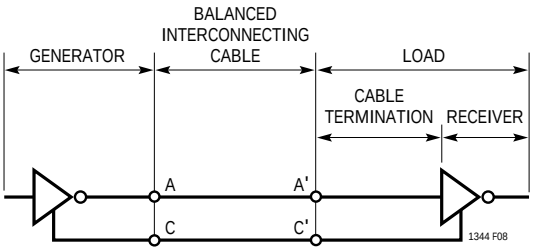


Figure 8. Typical V.28 Interface

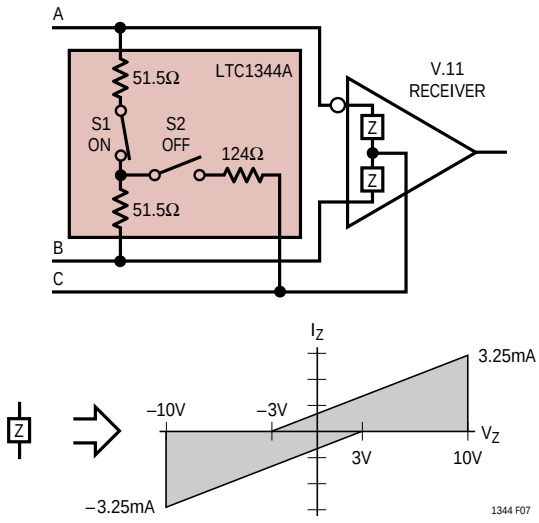


Figure 7. V.11 Interface Using the LTC1344A

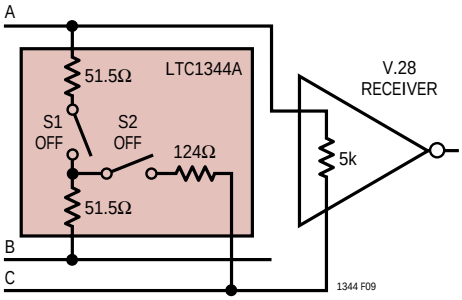


Figure 9. V.28 Interface Using the LTC1344A

V.28 (RS232) Termination

A typical V.28 unbalanced interface is shown in Figure 8. A V.28 single-ended generator output A with ground C is connected to a single-ended receiver with input A' connected to A, ground C' connected via the signal return ground to C. The V.28 standard requires a 5k terminating resistor to ground which is included in almost all compliant receivers as shown in Figure 9. Because the termination is included in the receiver, both switches S1 and S2 in the LTC1344A are turned off.

V.35 Termination

A typical V.35 balanced interface is shown in Figure 10. A V.35 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.35 interface requires a T-network termination at the receiver end and the generator end. In V.35 mode both switches S1 and S2 in the LTC1344A are turned on as shown in Figure 11.

The differential impedance measured at the connector must be 100Ω ±10Ω and the impedance between shorted terminals A' and B' to ground C' must be 150Ω ±15Ω. The input impedance of the V.35 receiver is connected in parallel with the T-network inside the LTC1344A, which could cause the overall impedance to fail the specification

APPLICATIONS INFORMATION

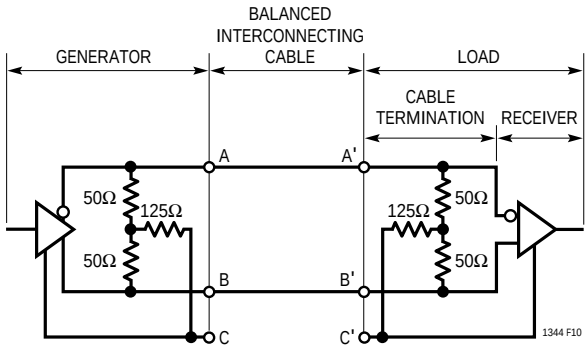


Figure 10. Typical V.35 Interface

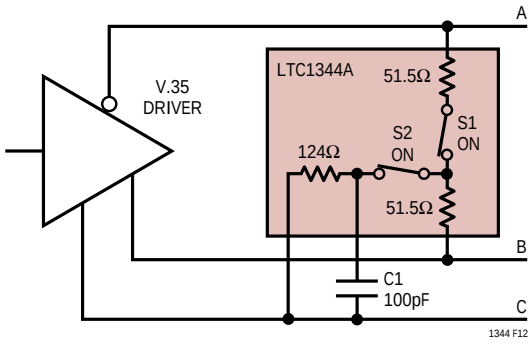


Figure 12. V.35 Driver Using the LTC1344A

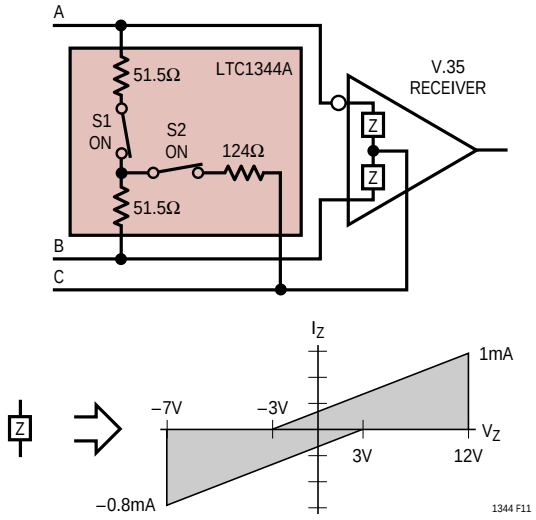


Figure 11. V.35 Receiver Using the LTC1344A

if the receiver input impedance is on the low side. All of Linear Technology's V.35 receivers meet the RS485 input impedance specification as shown in Figure 11, which insures compliance with the V.35 specification when used with the LTC1344A.

The generator differential impedance must be 50Ω to 150Ω and the impedance between shorted terminals A and B to ground C must be 150Ω ±15Ω. For the generator termination, switches S1 and S2 are both on and the top side of the center resistor is brought out to a pin so it can be bypassed with an external capacitor to reduce common mode noise as shown in Figure 12.

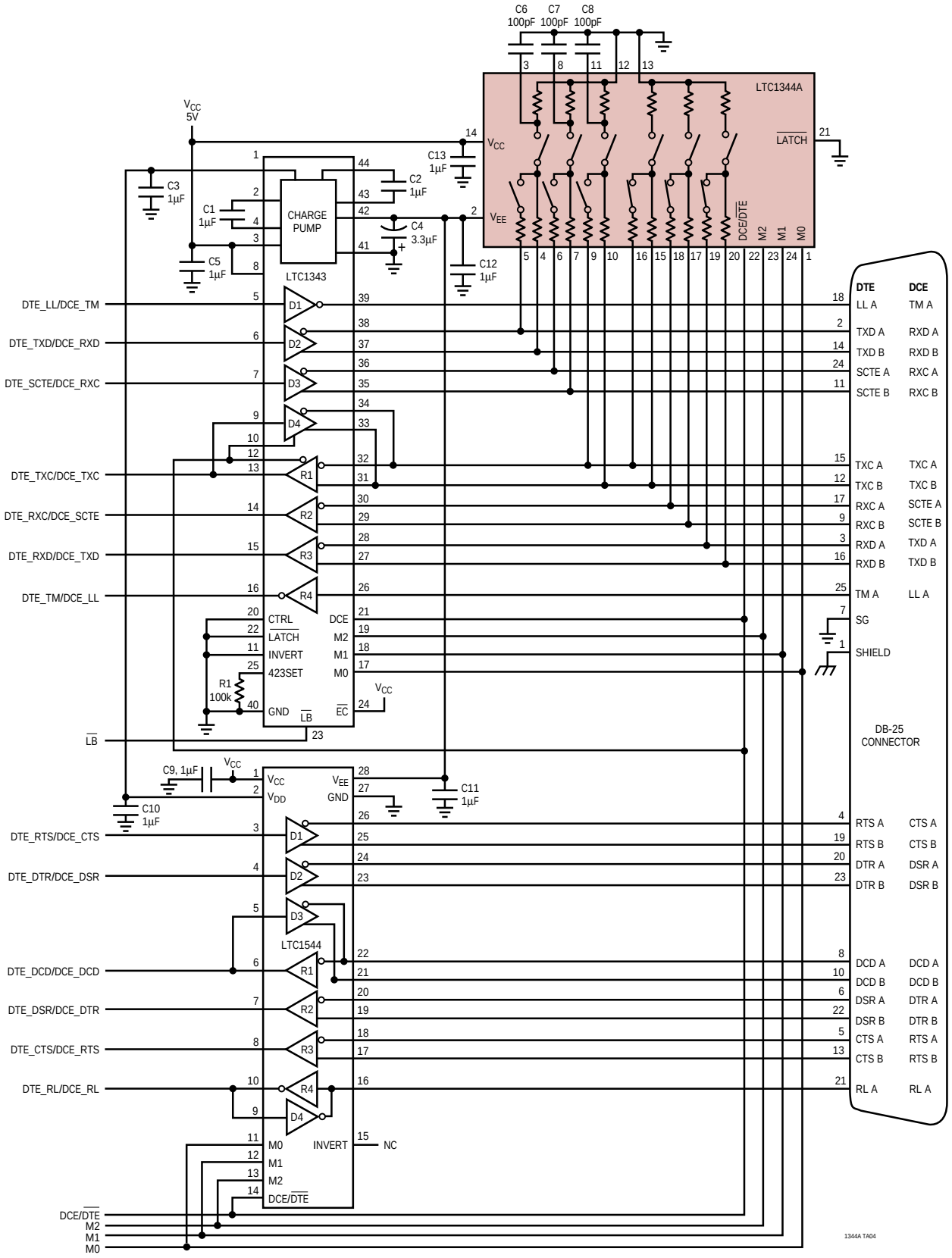
Any mismatch in the driver rise and fall times or skew in the driver propagation delays will force current through the center termination resistor to ground causing a high frequency common mode spike on the A and B terminals. The common mode spike can cause EMI problems that are reduced by capacitor C1 which shunts much of the common mode energy to ground rather than down the cable.

The $\overline{\text{LATCH}}$ Pin

The $\overline{\text{LATCH}}$ pin (21) allows the select lines (M0, M1, M2 and DCE/DTE) to be shared with multiple LTC1344As, each with its own $\overline{\text{LATCH}}$ signal. When the $\overline{\text{LATCH}}$ pin is held low the select line input buffers are transparent. When the $\overline{\text{LATCH}}$ pin is pulled high, the select line input buffers latch the state of the Select pins so that changes on the select lines are ignored until $\overline{\text{LATCH}}$ is pulled low again. If the latch feature is not used, the $\overline{\text{LATCH}}$ pin should be tied to ground.

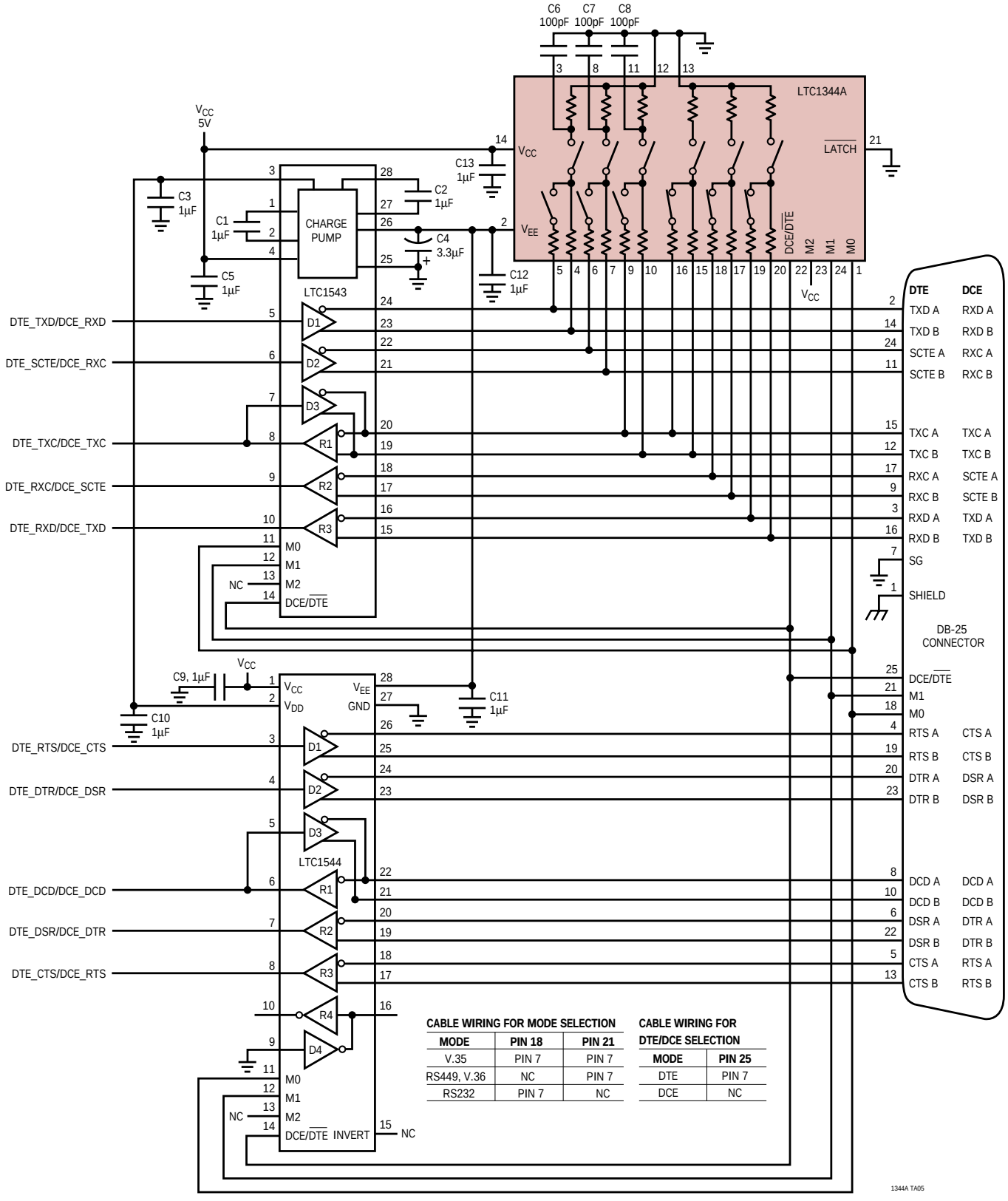
TYPICAL APPLICATIONS

Controller Selectable Multiprotocol DTE/DCE Port with DB-25 Connector



TYPICAL APPLICATIONS

Cable Selectable Multiprotocol DTE/DCE Port with DB-25 Connector



CABLE WIRING FOR MODE SELECTION

MODE	PIN 18	PIN 21
V.35	PIN 7	PIN 7
RS449, V.36	NC	PIN 7
RS232	PIN 7	NC

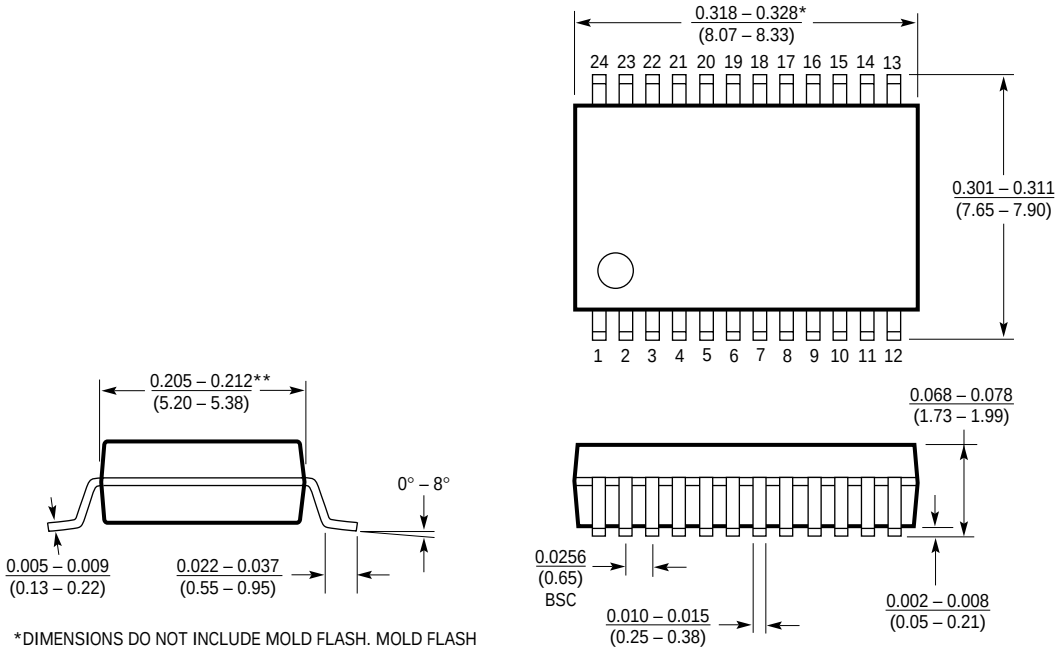
CABLE WIRING FOR DTE/DCE SELECTION

MODE	PIN 25
DTE	PIN 7
DCE	NC

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
24-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Figure 13 shows a typical application for the LTC1344A using the LTC1543 mixed mode transceiver chip to generate the clock and data signals for a serial interface. The LTC1344A V_{EE} supply is generated from the LTC1543 charge pump and the select lines M0, M1, M2 and DCE/$\overline{\text{DTE}}$ are shared by both chips. Each driver output and receiver input is connected to one of the LTC1344A termination ports. Each electrical protocol can then be chosen using the digital select lines.

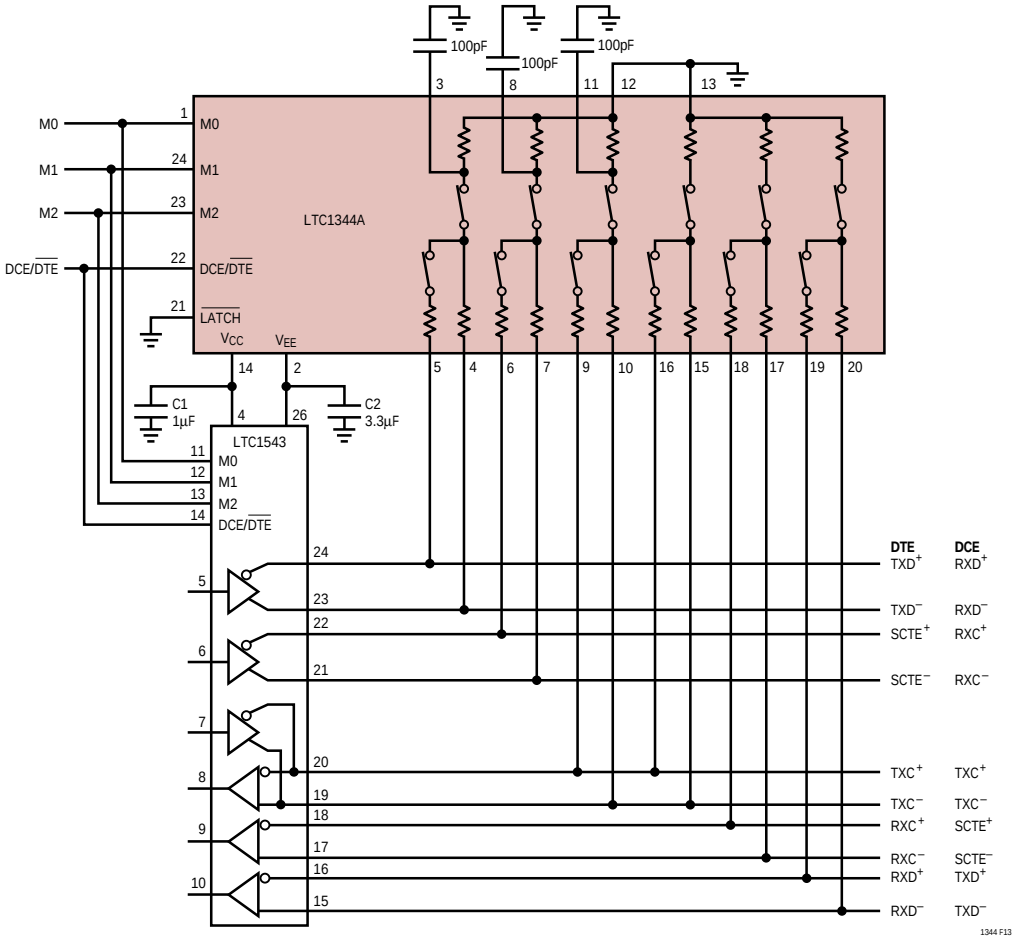


Figure 13. Typical Application Using the LTC1344A

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1334	Single Supply RS232/RS485 Transceiver	2 RS485 Dr/Rx or 4 RS232 Dr/Rx Pairs
LTC1343	Multiprotocol Serial Transceiver	Software Selectable Mulitprotocol Interface
LTC1345	Single Supply V.35 Transceiver	3 Dr/3 Rx for Data and CLK Signals
LTC1346A	Dual Supply V.35 Transceiver	3 Dr/3 Rx for Data and CLK Signals
LTC1543	Multiprotocol Serial Transceiver	Software-Selectable Transceiver for Data and CLK Signals
LTC1544	Multiprotocol Serial Transceiver	Software-Selectable Transceiver for Control Signals

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