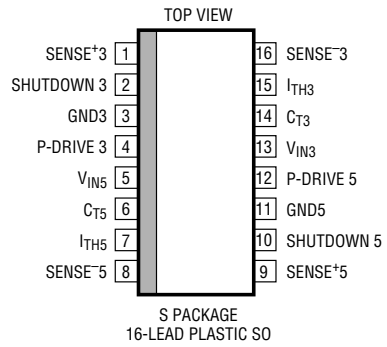
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pins 5,13) ..... 16V to –0.3V
Continuous Output Current (Pins 4,12) 50mA
Sense Voltages (Pins 1, 8, 9, 16)
  $V_{IN} \geq 12.7V$ ..... 13V to –0.3V
  $V_{IN} < 12.7V$ ..... (V_{IN} + 0.3V) to –0.3V
Shutdown Voltage
  (LTC1143, LTC1143L, Pins 2, 10) ..... 7V to –0.3V
V_{FB} Current (LTC1143L-ADJ, Pins 2, 10) 1mA
Operating Temperature Range
  Ambient ..... 0°C to 70°C
  Extended Commercial (Note 4) ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

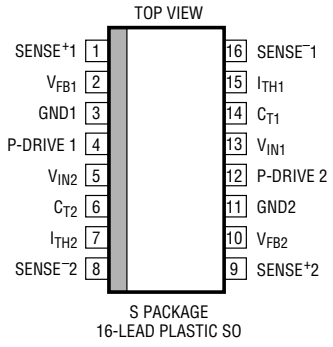


S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1143CS
LTC1143LCS



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1143LCS-ADJ

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_2, V_{10}	Feedback Voltage (LTC1143L-ADJ)	V_{IN} = 9V	●	1.21	1.25	1.29	V
I_2, I_{10}	Feedback Current (LTC1143L-ADJ)		●		0.2	1	µA
V_{OUT}	Regulated Output Voltage (LTC1143/LTC1143L)	V_{IN3}, V_{IN5} = 9V, V_2 = V_{10} = 0V					
	3.3V Output	I_{LOAD} = 700mA	●	3.23	3.33	3.43	V
	5V Output	I_{LOAD} = 700mA	●	4.90	5.05	5.20	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 7V to 12V, I_{LOAD} = 50mA		–40	0	40	mV
	Output Voltage Load Regulation LTC1143/LTC1143L	V_2 = V_{10} = 0V					
	3.3V Output	5mA < I_{LOAD} < 2.0A	●		40	65	mV
	5V Output	5mA < I_{LOAD} < 2.0A	●		60	100	mV
	Output Ripple (Burst Mode)	I_{LOAD} = 0A			50		mV_{P-P}
I_5, I_{13}	Input DC Supply Current (Note 2)						
	LTC1143: Normal Mode	V_2 = V_{10} = 0V, 4V < V_{IN} < 12V			1.6	2.1	mA
	Sleep Mode	V_2 = V_{10} = 0V, 4V < V_{IN3} < 12V, 6V < V_{IN5} < 12V			160	230	µA
	Shutdown	V_2 = V_{10} = 2.1V, 4V < V_{IN} < 12V			10	20	µA
	LTC1143L: Normal Mode	V_2 = V_{10} = 0V, 3.5V < V_{IN} < 12V			1.6	2.1	mA
	Sleep Mode	V_2 = V_{10} = 0V, 3.5V < V_{IN3} < 12V, 6V < V_{IN5} < 12V			160	230	µA
	Shutdown	V_2 = V_{10} = 2.1V, 3.5V < V_{IN} < 12V			10	20	µA
	LTC1143L-ADJ: Normal Mode	3.5V < V_{IN} < 12V			1.6	2.1	mA
	Sleep Mode	3.5V < V_{IN} < 12V, V_{OUT} ≤ 3.3V			160	230	µA

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_1 to V_{16}, V_8 to V_9	Current Sense Threshold Voltage LTC1143/LTC1143L	$V_2 = V_{10} = 0V$					
		V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	●	130	150	170	mV
	LTC1143L-ADJ	V_{SENSE}^- = 5V, V_{FB} = V_{OUT}/4 + 25mV (Forced)			25		mV
		V_{SENSE}^- = 5V, V_{FB} = V_{OUT}/4 – 25mV (Forced)	●	130	150	170	mV
V_2, V_{10}	Shutdown Pin Threshold LTC1143/LTC1143L			0.5	0.8	2	V
I_2, I_{10}	Shutdown Pin Input Current LTC1143/LTC1143L	0V < $V_{SHUTDOWN}$ = < 8V, V_{IN3}, V_{IN5} = 16V			1.2	5	µA
I_6, I_{14}	C_T Pin Discharge Current	V_{OUT} in Regulation, V_{SENSE-} = V_{OUT}		50	70	90	µA
		V_{OUT} = 0V			2	10	µA
t_{OFF}	Off-Time (Note 3)	C_T = 390pF, I_{LOAD} = 700mA		4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pins 4, 12), V_{IN} = 6V			100	200	ns

–40°C ≤ T_A ≤ 85°C (Note 4), V_{IN} = 10V unless otherwise noted.

V_2, V_{10}	Feedback Voltage (LTC1143L-ADJ)	V_{IN} = 9V		1.20	1.25	1.30	V
V_{OUT}	Regulated Output Voltage LTC1143/LTC1143L	V_{IN3}, V_{IN5} = 9V					
	3.3V Output	I_{LOAD} = 700mA		3.17	3.33	3.43	V
	5V Output	I_{LOAD} = 700mA		4.85	5.05	5.20	V
I_5, I_{13}	Input DC Supply Current (Note 2)						
	LTC1143: Normal Mode	$V_2 = V_{10} = 0V$, 4V < V_{IN} < 12V			1.6	2.4	mA
	Sleep Mode	$V_2 = V_{10} = 0V$, 4V < V_{IN3} < 12V, 6V < V_{IN5} < 12V			160	260	µA
	Shutdown	$V_2 = V_{10} = 2.1V$, 4V < V_{IN} < 12V			10	22	µA
	LTC1143L: Normal Mode	$V_2 = V_{10} = 0V$, 3.5V < V_{IN} < 12V			1.6	2.4	mA
	Sleep Mode	$V_2 = V_{10} = 0V$, 3.5V < V_{IN3} < 12V, 6V < V_{IN5} < 12V			160	260	µA
	Shutdown	$V_2 = V_{10} = 2.1V$, 3.5V < V_{IN} < 12V			10	22	µA
	LTC1143L-ADJ: Normal Mode	3.5V < V_{IN} < 12V			1.6	2.4	mA
	Sleep Mode	3.5V < V_{IN} < 12V, V_{OUT} ≤ 3.3V			160	260	µA
V_1 to V_{16}, V_8 to V_9	Current Sense Threshold Voltage LTC1143/LTC1143L	$V_2 = V_{10} = 0V$					
		V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)		125	150	185	mV
	LTC1143L-ADJ	V_{SENSE}^- = 5V, V_{FB} = V_{OUT}/4 + 25mV (Forced)			25		mV
		V_{SENSE}^- = 5V, V_{FB} = V_{OUT}/4 – 25mV (Forced)		125	150	185	mV
V_2, V_{10}	Shutdown Pin Threshold LTC1143/LTC1143L			0.55	0.8	2	V

The ● denotes specifications which apply over the specified temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC1143 series: $T_J = T_A + (P_D \bullet 125°C/W)$

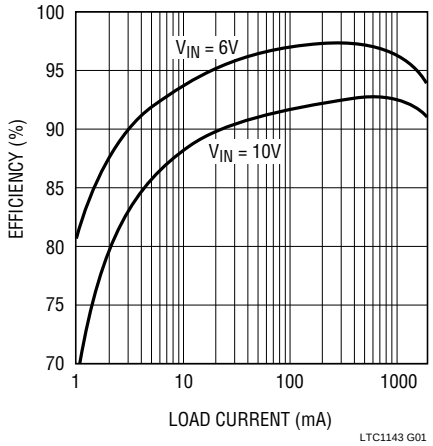
Note 2: This supply current is for one regulator block. Total supply current is the sum of Pin 5 and Pin 13 currents. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 3: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

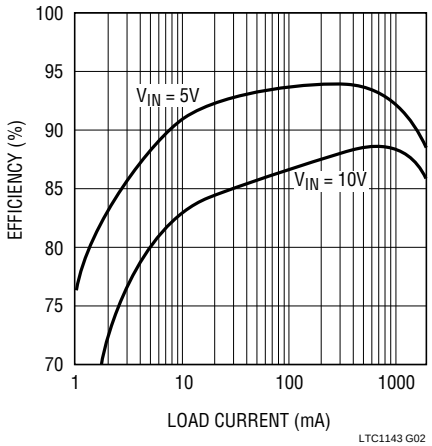
Note 4: The LTC1143 series is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended temperature limits, but is not tested at –40°C to 85°C.

TYPICAL PERFORMANCE CHARACTERISTICS

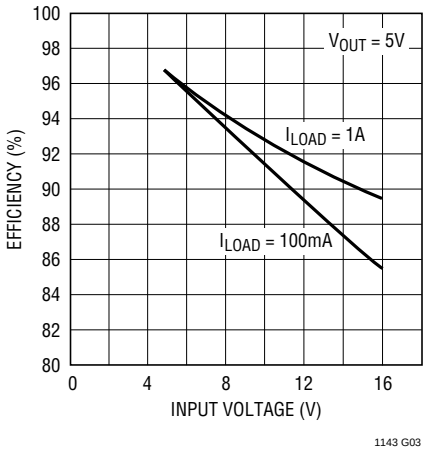
5V Output Efficiency



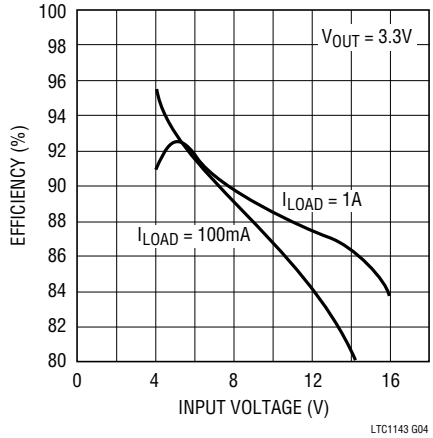
3.3V Output Efficiency



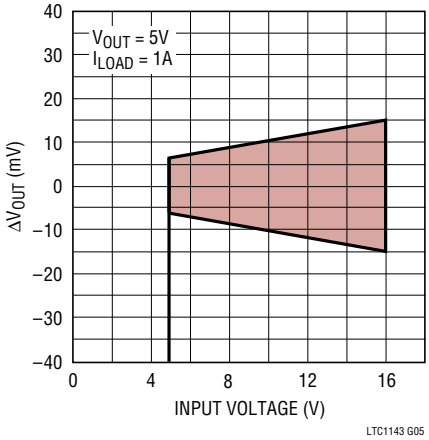
5V Efficiency vs Input Voltage



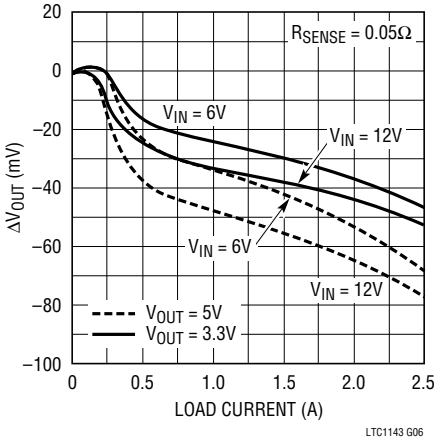
3.3V Efficiency vs Input Voltage



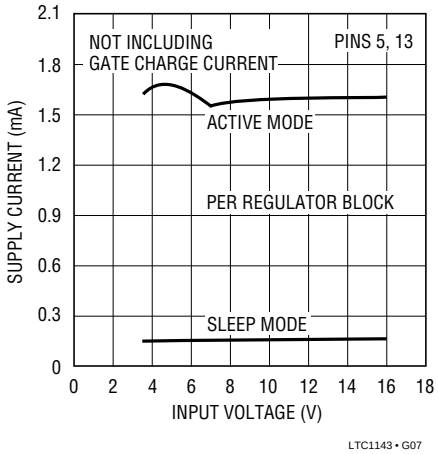
Line Regulation



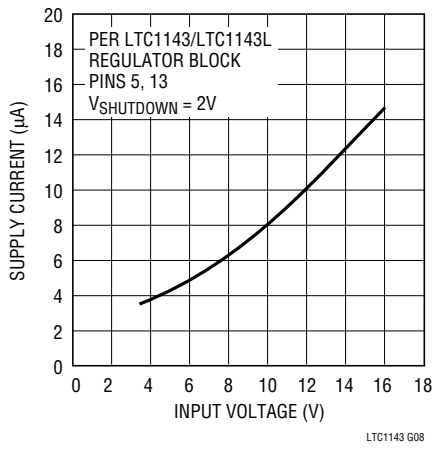
Load Regulation



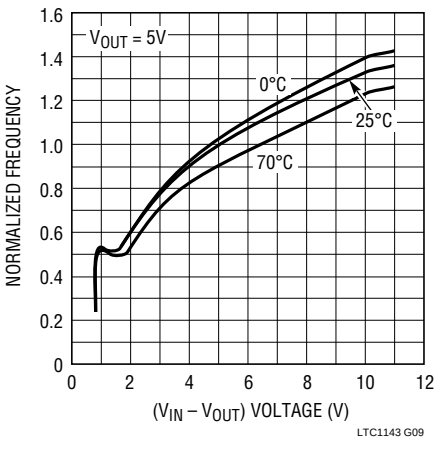
DC Supply Current



Supply Current in Shutdown

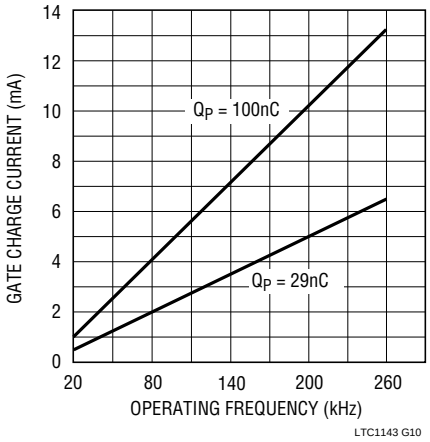


Operating Frequency vs $V_{IN} - V_{OUT}$

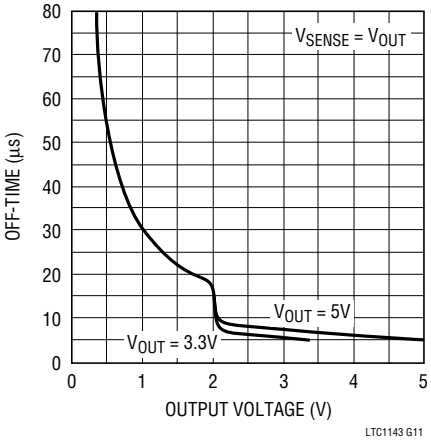


TYPICAL PERFORMANCE CHARACTERISTICS

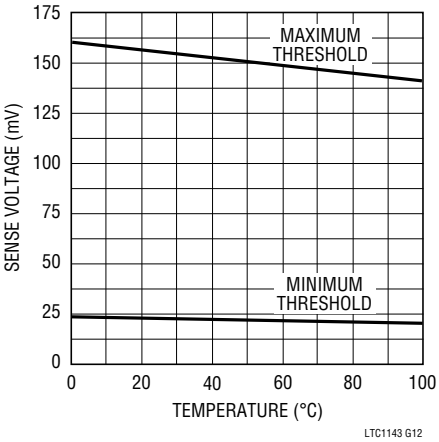
Gate Charge Supply Current



Off-Time vs V_{OUT}



Current Sense Threshold Voltage



PIN FUNCTIONS

LTC1143/LTC1143L

$SENSE^+3$ (Pin 1): The (+) Input to the 3.3V Section Current Comparator. A built-in offset between Pins 1 and 16 in conjunction with $R_{SENSE\ 3}$ sets the current trip threshold for the 3.3V section.

SHUTDOWN 3 (Pin 2): When grounded, the 3.3V section operates normally. Pulling Pin 2 high holds the MOSFET off and puts the 3.3V section in micropower shutdown mode. Requires CMOS logic level signal with t_r, $t_f < 1\mu s$. Do not "float" Pin 2.

GND3 (Pin 3): 3.3V Section Ground. Two independent ground lines must be routed separately from other grounds to: 1) the (–) terminal of the 3.3V section output capacitor and 2) the cathode of the Schottky diode D1 and (–) terminal of C_{IN3} (see Figure 9).

P-DRIVE 3 (Pin 4): High Current Drive for Top P-Channel MOSFET, 3.3V Section. Voltage swing at this pin is from V_{IN3} to ground.

V_{IN5} (Pin 5): Supply Pin, 5V Section. Must be closely decoupled to 5V power ground Pin 11.

C_{T5} (Pin 6): External capacitor C_{T5} from Pin 6 to ground sets the operating frequency for the 5V section. (The actual frequency is also dependent upon the input voltage.)

I_{TH5} (Pin 7): Gain Amplifier Decoupling Point, 5V Section. The 5V section current comparator threshold increases with the Pin 7 voltage.

$SENSE^-$ 5 (Pin 8): Connects to internal resistive divider which sets the output voltage for the 5V section. Pin 8 is also the (–) input for the current comparator on the 5V section.

$SENSE^+$ 5 (Pin 9): The (+) Input to the 5V Section Current Comparator. A built-in offset between Pins 9 and 8 in conjunction with $R_{SENSE\ 5}$ sets the current trip threshold for the 5V section.

SHUTDOWN 5 (Pin 10): When grounded, the 5V section operates normally. Pulling Pin 10 high holds the 5V section MOSFET off and puts the 5V section in micropower shutdown mode. Requires CMOS logic level signal with t_r, $t_f < 1\mu s$. Do not "float" Pin 10.

GND5 (Pin 11): 5V Section Ground. Two independent ground lines must be routed separately from other grounds to: 1) the (–) terminal of the 5V section output capacitor and 2) the cathode of the Schottky diode D2 and (–) terminal of C_{IN5} (see Figure 9).

P-DRIVE 5 (Pin 12): High Current Drive for Top P-Channel MOSFET, 5V Section. Voltage swing at this pin is from V_{IN5} to ground.

PIN FUNCTIONS

V_{IN3} (Pin 13): Supply Pin, 3.3V Section. Must be closely decoupled to 3.3V power ground Pin 3.

C_{T3} (Pin 14): External capacitor C_{T3} from Pin 14 to ground sets the operating frequency for the 3.3V section. (The actual frequency is also dependent upon the input voltage.)

I_{TH3} (Pin 15): Gain Amplifier Decoupling Point, 3.3V Section. The 3.3V section current comparator threshold increases with the Pin 15 voltage.

SENSE⁻ 3 (Pin 16): Connects to internal resistive divider which sets the output voltage for the 3.3V section. Pin 16 is also the (–) input for the current comparator on the 3.3V section.

LTC1143L-ADJ

SENSE⁺ 1 (Pin 1): The (+) Input to the Section 1 Current Comparator. A built-in offset between Pins 1 and 16 in conjunction with $R_{SENSE\ 1}$ sets the current trip threshold for section 1.

V_{FB1} (Pin 2): This pin serves as the feedback pin from an external resistive divider used to set the output voltage for section 1.

GND1 (Pin 3): Section 1 Ground. Two independent ground lines must be routed separately from other grounds to: 1) the (–) terminal of the section 1 output capacitor and 2) the cathode of the Schottky diode D1 and (–) terminal of C_{IN1} (see Figure 1).

P-DRIVE 1 (Pin 4): High Current Drive for Top P-Channel MOSFET, Section 1. Voltage swing at this pin is from V_{IN1} to ground.

V_{IN2} (Pin 5): Supply Pin, Section 2. Must be closely decoupled to power ground Pin 11.

C_{T2} (Pin 6): External capacitor C_{T2} from Pin 6 to ground sets the operating frequency for section 2. (The actual frequency is also dependent upon the input voltage.)

I_{TH2} (Pin 7): Gain Amplifier Decoupling Point, Section 2. The section 2 current comparator threshold increases with the Pin 7 voltage.

SENSE⁻ 2 (Pin 8): Pin 8 is the (–) input for the current comparator on section 2.

SENSE⁺ 2 (Pin 9): The (+) Input to the Section 2 Current Comparator. A built-in offset between Pins 9 and 8 in conjunction with $R_{SENSE\ 2}$ sets the current trip threshold for section 2.

V_{FB2} (Pin 10): This pin serves as the feedback pin from an external resistive divider used to set the output voltage for section 2.

GND2 (Pin 11): Section 2 Ground. Two independent ground lines must be routed separately from other grounds to: 1) the (–) terminal of section 2 output capacitor and 2) the cathode of the Schottky diode D2 and (–) terminal of C_{IN2} (see Figure 1).

P-DRIVE 2 (Pin 12): High Current Drive for Top P-Channel MOSFET, Section 2. Voltage swing at this pin is from V_{IN2} to ground.

V_{IN1} (Pin 13): Supply Pin, Section 1. Must be closely decoupled to power ground Pin 3.

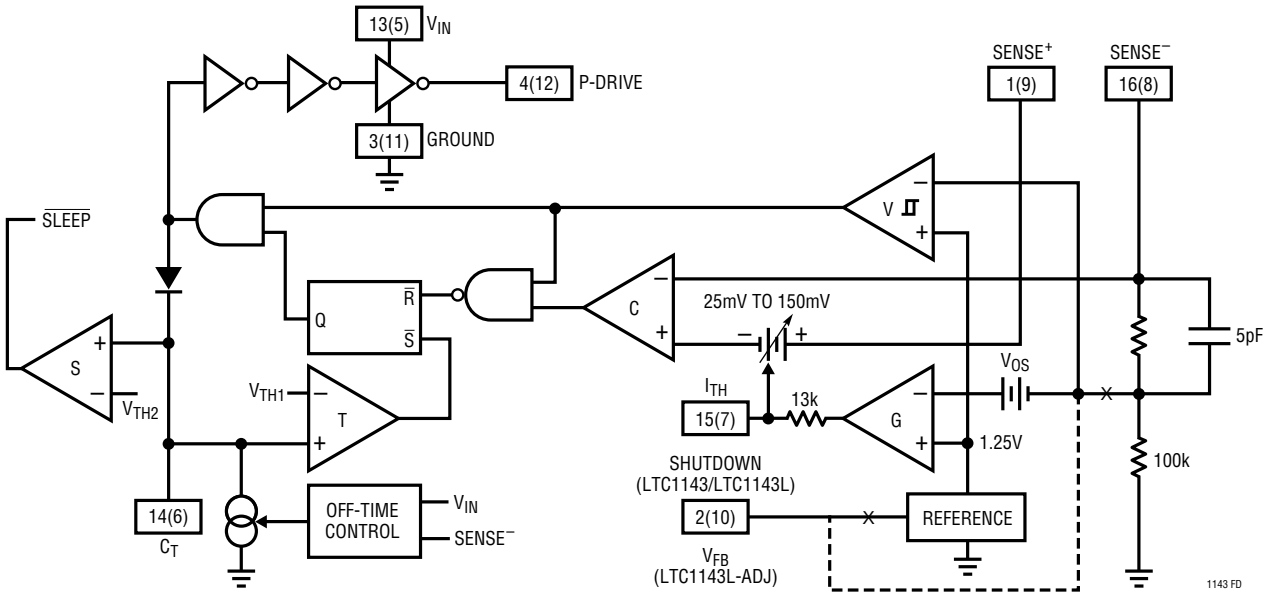
C_{T1} (Pin 14): External capacitor C_{T1} from Pin 14 to ground sets the operating frequency for section 1. (The actual frequency is also dependent upon the input voltage.)

I_{TH1} (Pin 15): Gain Amplifier Decoupling Point, Section 1. The section 1 current comparator threshold increases with the Pin 15 voltage.

SENSE⁻ 1 (Pin 16): Pin 16 is the (–) input for the current comparator on section 1.

FUNCTIONAL DIAGRAM

Only one regulator block shown. Connections shown for LT1143/LTC1143L; changes create LTC1143L-ADJ



OPERATION

Refer to Functional Diagram and Figure 1.

The LTC1143 series consists of two individual regulator blocks, each using current mode, constant off-time architectures to switch an external power MOSFET. The two LTC1143/LTC1143L regulators are internally set for 3.3V and 5V, while the two LTC1143L-ADJ regulators have externally programmable output voltages. Operating frequency is individually set on each section by external capacitors at the timing capacitor Pins 6 and 14.

The output voltage is sensed by voltage comparator V and gain block G, which compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1143 series automatically switches between two modes of operation, burst and continuous. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between Pins 1 (9) and 16 (8) connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the P-drive output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor connected to Pin 14 (6) is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the feedback voltage to model the inductor current, which decays at a rate that is also proportional to the output voltage.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the P-drive output to go low, turning the P-channel MOSFET back on. The cycle then repeats.

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage [Pin 15 (7)] to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal $\overline{sleep}$ line to go low.

OPERATION

Refer to Functional Diagram and Figure 1

The circuit now enters sleep mode with the power MOSFET turned off. In sleep mode a majority of the circuitry is turned off, dropping the quiescent current from 1.6mA to 160µA (for one regulator block). The load current is now being supplied from the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and the process repeats.

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset (V_{OS}) is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

Using constant off-time architecture the operating frequency is a function of the input voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the C_T discharge current as V_{IN} drops below V_{OUT} + 1.5V. In dropout the P-channel MOSFET is turned on continuously (100% duty cycle), providing extremely low dropout operation.

APPLICATIONS INFORMATION

The basic LTC1143L-ADJ application circuit is shown in Figure 1. The LTC1143 and LTC1143L are similar but omit the external resistive V_{OUT} dividers (see Figures 10 and 13). External component selection is driven by the load requirement and begins with V_{OUT} and the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFET and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. Since the two regulator sections are identical, the process of component selection is the same for both sections. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 16V.

Output Voltage Selection

The LTC1143/LTC1143L output voltages are internally set to 3.3V and 5V. The LTC1143L-ADJ requires an external resistive divider from V_{OUT} to V_{FB} on each section as shown in Figure 1. The regulated LTC1143L-ADJ output voltages are given by:

$$V_{OUT1} = 1.25\left(1+\frac{R2}{R1}\right)$$

$$V_{OUT2} = 1.25\left(1+\frac{R4}{R3}\right)$$

To prevent stray pickup, a 100pF capacitor is suggested across R1 and R3 located close to the LTC1143L-ADJ.

For Figure 1 applications with V_{OUT} below 2V, or when R_{SENSE} is moved to ground, the current sense comparator inputs operate near ground. When the current comparator is operated at less than 2V common mode, the off-time increases approximately 40%, requiring the use of a smaller timing capacitor C_T.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1143 series current comparators have a threshold range that extends from a minimum of 25mV/R_{SENSE} to a maximum of 150mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)}$ = 25mV/R_{SENSE}. (See C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1143 series and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2.

APPLICATIONS INFORMATION

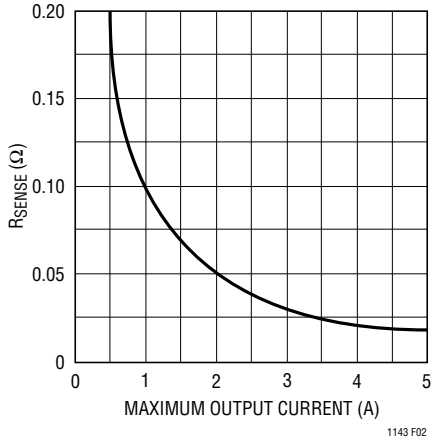


Figure 2. Selecting R_{SENSE}

The load current below which Burst Mode operation commences, I_{BURST}, and the peak short circuit current, $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

The LTC1143 series automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

L and C_T Selection for Operating Frequency

Each regulator section of the LTC1143 series uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current that is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency:

$$C_T = \frac{1}{1.3\left(10^4\right)f}\left(\frac{V_{IN}-V_{OUT}}{V_{IN}+V_D}\right)$$

where V_D is the drop across the diode.

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

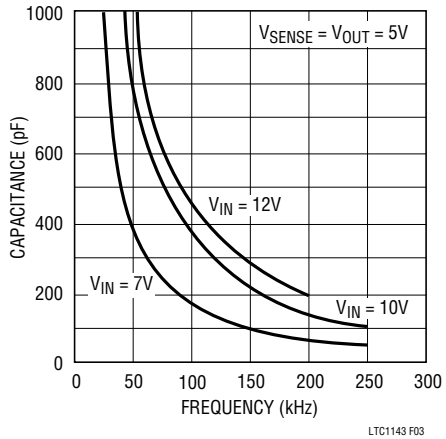


Figure 3. Timing Capacitor Value

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The complete expression for operating frequency of the circuit in Figure 1 is given by:

$$f \approx \frac{1}{t_{OFF}}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = 1.3\left(10^4\right)C_T\left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V). V_{OUT} is the measured output voltage. Thus $V_{REG}/V_{OUT} = 1$ in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input-to-output voltage differential drops below 1.5V for a particular section, the LTC1143 series reduces t_{OFF} in that section by increasing the discharge current in C_T. This prevents audible operation prior to dropout.

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Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than 25mV/R_{SENSE} of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1(10^5)(R_{SENSE})(C_T)V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the inductor current will become discontinuous before the LTC1143 series enters Burst Mode operation. A consequence of this is that the LTC1143 series will delay entering Burst Mode operation and efficiency will be degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. The highest efficiency will be obtained using Ferrite, Kool Mμ® or Molypermalloy (MPP) cores. Lower cost powdered iron cores provide suitable performance, but cut efficiency by 3% to 7%. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple that can cause Burst Mode operation to be falsely triggered. Do not allow the core to saturate!

Kool Mμ (from Magnetics, Inc.) is a very good, low loss core material for toroids with a "soft" saturation characteristic. Molypermalloy is slightly more efficient at high (> 200 kHz) switching frequencies but quite a bit more expensive. Toroids are very space efficient, especially when you can use several layers of wire, while inductors wound on bobbins are generally easier to surface mount. New designs for surface mount are available from Coiltronics, Coilcraft and Sumida.

Power MOSFET Selection

An external power MOSFET must be selected for use with each section of the LTC1143 series. The main selection criteria for the power MOSFETs are the threshold voltage $V_{GS(TH)}$, maximum V_{GS} rating and on resistance $R_{DS(ON)}$.

Surface mount P-channel power MOSFETs are widely available in both single and dual configurations. Logic level MOSFETs are specified for operation up to 20V maximum V_{GS} and guarantee a maximum $R_{DS(ON)}$ with V_{GS} = 4.5V. Newer 'sub' logic level MOSFETs allow only 8V maximum V_{GS} but guarantee $R_{DS(ON)}$ with V_{GS} = 2.7V. If V_{IN} will exceed 8V, logic level MOSFETs must be used; if conservatively specified, they are generally usable down to the 3.5V minimum V_{IN} rating of the LTC1143L and LTC1143L-ADJ.

The maximum output current I_{MAX} determines the $R_{DS(ON)}$ requirement for the two MOSFETs. When the LTC1143 series is operating in continuous mode, the simplifying assumption can be made that either the MOSFET or Schottky diode is always conducting the average load current. The duty cycles for the MOSFET and diode are given by:

$$\text{P-Ch Duty Cycle} \approx \frac{V_{OUT}}{V_{IN}}$$

$$\text{Schottky Diode Duty Cycle} = \frac{\left(V_{IN} - V_{OUT} + V_D\right)}{V_{IN}}$$

From the duty cycles the required $R_{DS(ON)}$ for each MOSFET can be derived:

$$\text{P-Ch } R_{DS(ON)} = \frac{V_{IN}\left(P_P\right)}{V_{OUT}\left(I_{MAX}^2\right)\left(1+\delta_P\right)}$$

where P_P is the allowable power dissipation and δ_P is the temperature dependencies of $R_{DS(ON)}$. P_P will be determined by efficiency and/or thermal requirements (see Efficiency Considerations). $(1+\delta_P)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve,

Kool Mμ is a registered trademark of Magnetics, Inc.

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but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

When selecting the P-channel power MOSFET for each section, consideration should be given to using a dual MOSFET with the other half used for the second regulator. Assuming both sections are operating at similar currents, the required $R_{DS(ON)}$ will be half the value of a single MOSFET to stay within the package dissipation limit. *Remember that worst-case MOSFET dissipation occurs at minimum V_{IN}.*

Output Diode Selection (D1, D2)

The Schottky diodes D1 and D2 shown in Figure 1 conduct during the off-time. It is important to adequately specify the diode peak current and average power dissipation to not exceed the diode ratings.

The most stressful condition for the output diode is under short circuit (V_{OUT} = 0V). Under this condition the diode must safely handle $I_{SC(PK)}$ at close to 100% duty cycle. Under normal load conditions the average current conducted by the diode is:

$$I_{DIODE} = \frac{\left(V_{IN} - V_{OUT} + V_D\right)}{V_{IN}}\left(I_{LOAD}\right)$$

Remember to keep lead lengths short and observe proper grounding (see Board Layout Checklist) to avoid ringing and increased dissipation.

The forward voltage drop allowable in the diode is calculated from the maximum short-circuit current as:

$$V_F \approx \frac{P_D}{I_{SC(PK)}}$$

where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements (see Efficiency Considerations).

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low effective series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question. An additional 0.1µF to 1µF ceramic capacitor is also required on each V_{IN} line (Pins 5, 13) for high frequency decoupling.

The selection of C_{OUT} is driven by the required (ESR). *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1143 series:*

$$C_{OUT} \text{ Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$ the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon and United Chemicon should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR size/ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be parallel to meet the capacitance, ESR or RMS current handling requirements of the application.

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Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, (2) AVX 100µF/10V (P/N TPSD 107M010) could be used. Consult the manufacturer for other specific recommendations.

At low supply voltages a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1143 series would normally be in continuous operation. The output remains in regulation at all times.

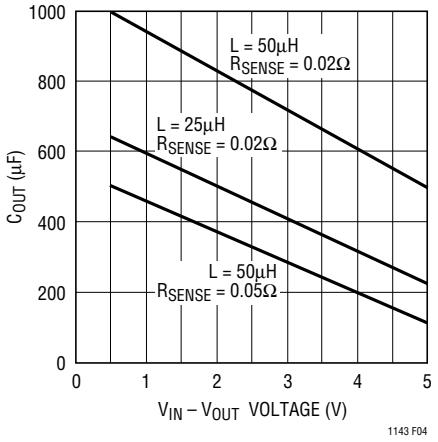

Figure 4. Minimum Value of C_{OUT}

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \times$ ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The Pin 15(7) external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT} causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power. (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power.)

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1143 series circuits:

1) DC bias current
2) MOSFET gate charge current
3) I^2R losses
4) Voltage drop of the Schottky diode.

1) The DC supply current is the current that flows into V_{IN} (Pin 13 and Pin 5) less the gate charge current. For V_{IN} = 10V the DC supply current for each section is 160µA for no load and increases proportionally with load up to a constant 1.6mA after the LTC1143 series has entered continuous mode. Because the DC bias current is

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drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 10V the DC bias losses are generally less than 1% for load currents over 30mA. However at very low load currents the DC bias current accounts for nearly all of the loss.

2) MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f(Q_P)$. The typical gate charge for a 0.05Ω P-channel power MOSFET is 40nC. This results in $I_{GATECHG}$ = 4mA in 100kHz continuous operation, for a 2% to 3% typical midcurrent loss with V_{IN} = 10V.

   Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using a larger MOSFET than necessary to control I^2R losses, since overkill can cost efficiency as well as money!

3) I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the P-channel MOSFET and Schottky diode. The MOSFET $R_{DS(ON)}$ multiplied by the P-channel duty cycle can be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if the $R_{DS(ON)}$ = 0.1Ω, R_L = 0.15Ω, and R_{SENSE} = 0.05Ω, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 10% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll off at high output currents.

4) The Schottky diode is a major source of power loss at high currents and gets worse at high input voltages. The diode loss is calculated by multiplying the forward voltage drop times the Schottky diode duty cycle multiplied by the load current. For example, assuming a duty cycle of 50% with a Schottky diode forward voltage drop of 0.4V, the loss increases from 0.5% to 8% as the load current increases from 0.5A to 2A. If Schotky diode losses routinely exceed 5% consider using the synchronously switched LTC1142 series.

Figure 5 shows how the efficiency losses in one section of a typical LTC1143 series regulator end up being apportioned. The gate charge loss is responsible for the majority of the efficiency lost in the midcurrent region. If Burst Mode operation was not employed at low currents, the gate charge loss alone would cause efficiency to drop to unacceptable levels. With Burst Mode operation, the DC supply current represents the lone (and unavoidable) loss component, which continues to become a higher percentage as output current is reduced. As expected, the I^2R losses and Schottky diode loss dominate at high load currents.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses and inductor core losses, generally account for less than 2% total additional loss.

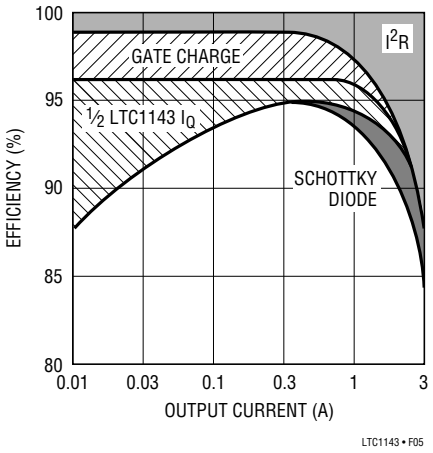

Figure 5. Efficiency Loss

Shutdown Considerations

Pins 2 and 10 on the LTC1143 and LTC1143L shut down their respective sections when pulled high. They require CMOS logic level signals with t_r, t_f < 1µs and must never be floated. The LTC1143L-ADJ gives up the pin-controlled shutdown function in order to gain feedback pins for programming the output voltages.

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The LTC1143L-ADJ outputs can be turned off in one of two ways: 1) by placing a power MOSFET switch in the V_{IN} line to the entire regulator or 2) by pulling the V_{FB} pin over 1.4V, which trips comparator V and forces P-DRIVE high (see Functional Diagram). V_{FB} can be pulled high with a small current, but any circuitry used to shut down the LTC1143L-ADJ in this manner must minimize V_{FB} lead length to prevent noise coupling during normal operation.

In the Figure 6 circuit, taking SHUTDOWN high turns on PNP Q_{SD} that sources a current into V_{FB}. To shut down properly, RSD must be chosen to pull V_{FB} above 1.4V with V_{OUT} at 0V and minimum V_{IN}. Note that this technique depends on the load resistance to prevent V_{OUT} from floating up due to the current flowing into V_{FB}.

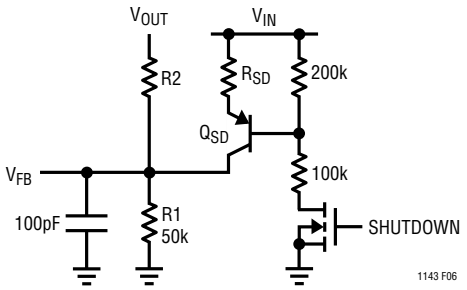

Figure 6. Local V_{FB} Pull-Up Shuts Down LTC1143L-ADJ

Design Example

As a design example, assume V_{IN} = 12V(nominal), V_{OUT} = 3.3V, I_{MAX} = 2A and f = 200kHz. R_{SENSE}, C_T and L can immediately be calculated:

R_{SENSE} = 100mV/2 = 0.05Ω
t_{OFF} = (1/200kHz)[1 – (3.3/12)] = 3.63µs
C_T = 3.63µs/(1.3 × 10^4) = 280pF (use 300pF)
L_{MIN} = 5.1(10^5)(0.05Ω)(300pF) 3.3V = 25µH

Assume a dual P-channel power MOSFET is to be used and dissipation is to be limited to 1W total at worst-case lowest V_{IN} = 4V. If T_A = 50°C and the thermal resistance of the MOSFET package is 50°C/W, then the junction temperature will be 100°C and δ_P = 0.005(100 – 25) = 0.38. The maximum $R_{DS(ON)}$ for each MOSFET can now be calculated:

$$\text{P-Ch } R_{DS(ON)} = \frac{1}{2}\left[\frac{4(1)}{3.3(2)^2(1.38)}\right] = 0.11\Omega$$

Allowing for V_{IN} being slightly below the V_{GS} used to specify $R_{DS(ON)}$, this requirement can be met by half of a Siliconix Si4953DY, Fairchild NDS8947 or similar SO-8 dual P-channel MOSFET.

The most stringent requirement for the Schottky diode is with V_{OUT} = 0V (i.e. short circuit). During a continuous short circuit, the worst-case Schottky diode dissipation rises to:

$$P_D = I_{SC(AVG)}(V_D)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

With the 0.05Ω sense resistor, $I_{SC(AVG)}$ = 2A will result, increasing the 0.4V Schottky diode dissipation to 0.8W.

C_{IN} will require an RMS current rating of at least 1A at temperature and C_{OUT} will require an ESR of 0.05Ω for optimum efficiency.

Troubleshooting Hints

Since efficiency is critical to LTC1143 series applications it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the timing capacitor Pins 6 and 14.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 7a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation occurs. The voltage on the C_T pin now falls to ground for periods of time as shown in Figure 7b.

If Pin 6 or Pin 14 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

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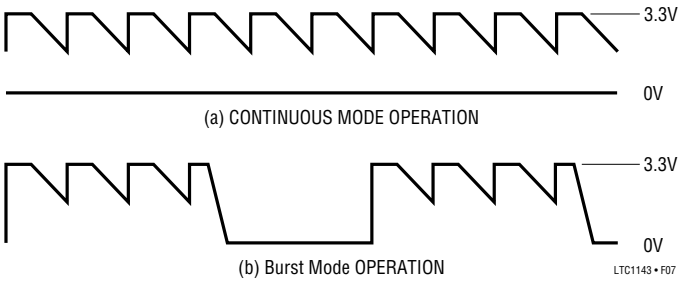

Figure 7. C_T Waveforms

Auxiliary Windings—Suppressing Burst Mode Operation

The LTC1143 series operates nonsynchronously with the normal limitation that the power drawn from the inductor primary winding must not be less than twice the power drawn from the auxiliary windings. (With synchronous switching, using the LTC1142 series, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.)

Burst Mode operation can be suppressed at low output currents with a simple external network that cancels the 25mV minimum current comparator threshold. This technique is also useful for eliminating audible noise from certain types of inductors in high current (I_{OUT} > 5A) applications when they are lightly loaded.

An external offset is put in series with the Sense$^-$ pin to subtract from the built-in 25mV offset. An example of this technique is shown in Figure 8. Two 100Ω resistors are inserted in series with the sense leads from the sense resistor.

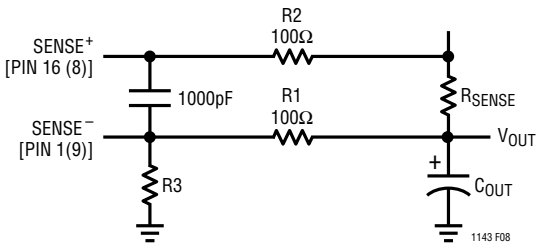

Figure 8. Suppression of Burst Mode Operation

With the addition of R3 a current is generated though R1, causing an offset of:

$$V_{OFFSET} = V_{OUT}\left(\frac{R1}{R1+R3}\right)$$

If V_{OFFSET} > 25mV, the built-in offset will be cancelled and Burst Mode operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be lower:

$$R_{SENSE} \approx \frac{75mV}{I_{MAX}}$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across Pins 1 (16) and 9 (8).

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1143 series. These items are also illustrated graphically in the layout diagram of Figure 9. In general, each block should be self-contained with little cross coupling for best performance. Check the following in your layout:

1) Are the signal and power grounds segregated? The LTC1143 series GND Pin 3 (11) must return separately to: a) the power and b) the signal grounds. The power ground returns to the anode of the Schottky diode and (–) plate of C_{IN}, which should have as short lead lengths as possible.The signal ground (b) connects to the (–) plate of C_{OUT}.
2) Does the LTC1143 series SENSE$^-$ Pin 16 (8) connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}?
3) Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The 1000pF capacitor between Pins 1 (9) and 16 (8) should be as close as possible to the LTC1143 series.
4) Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? This capacitor provides the AC current to the P-channel MOSFET.

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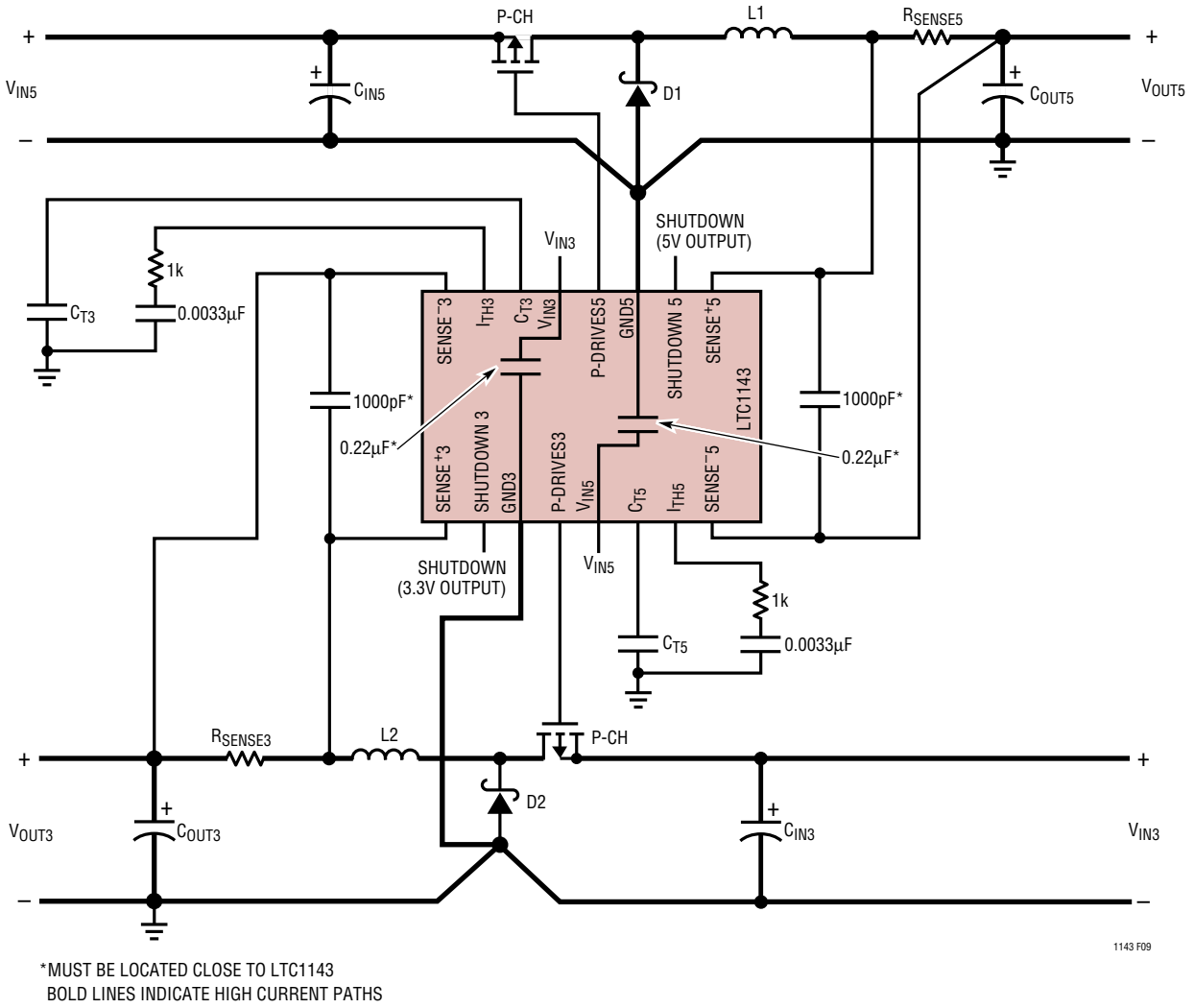
5) Is the V_{IN} decoupling capacitor (1µF, 0.1µF) connected closely between Pin 13 (5) and GND Pin 3 (11)? This capacitor carries the MOSFET driver peak currents.

6) For the LTC1143 and LTC1143L, are the SHUTDOWN Pins 2 and 10 actively pulled to ground during normal operation? Both SHUTDOWN pins are high impedance and must not be allowed to float. Both pins can be driven by the same external signal if needed.

7) For the LTC1143L-ADJ, are the V_{FB} Pins 2 and 10 decoupled with 100pF as close to the device as possible? The V_{FB} line is sensitive to noise pickup and should be kept away from the P-channel MOSFET.



*MUST BE LOCATED CLOSE TO LTC1143
BOLD LINES INDICATE HIGH CURRENT PATHS

Figure 9. LTC1143 Layout Diagram (see Board Layout Checklist)

TYPICAL APPLICATIONS

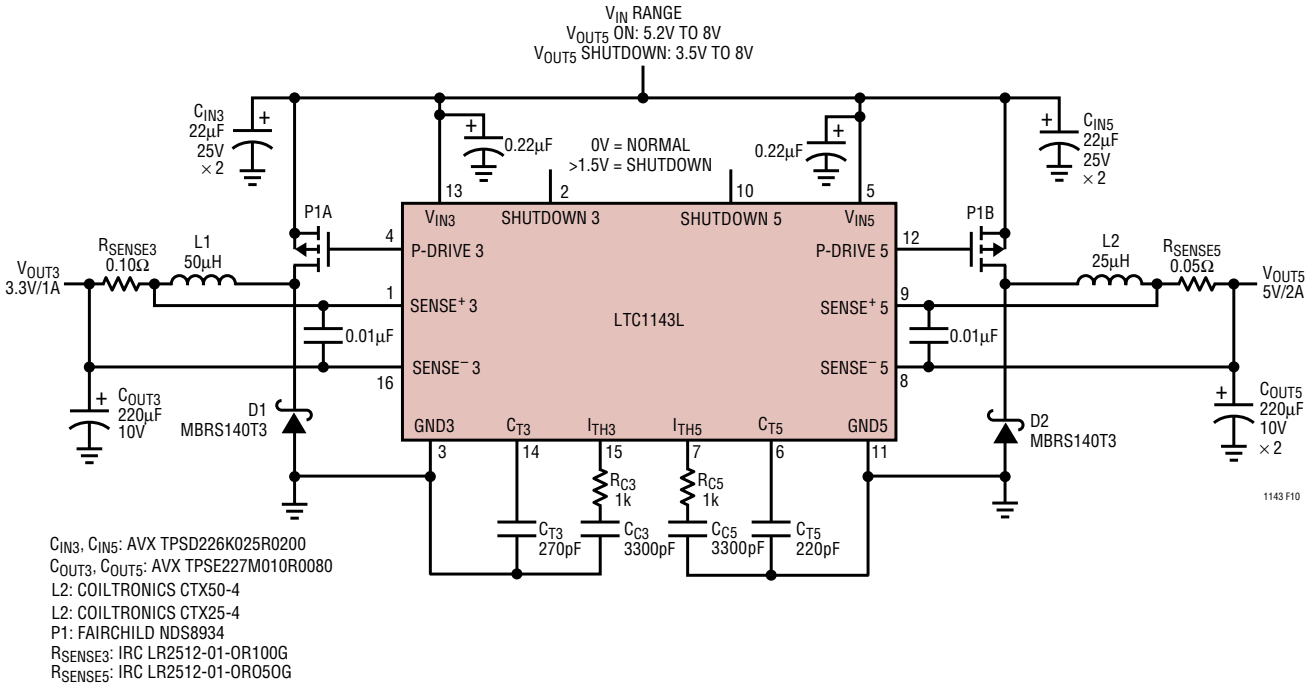


Figure 10. All Surface Mount Low Dropout Dual 5V/2A, 3.3V/1A Converter

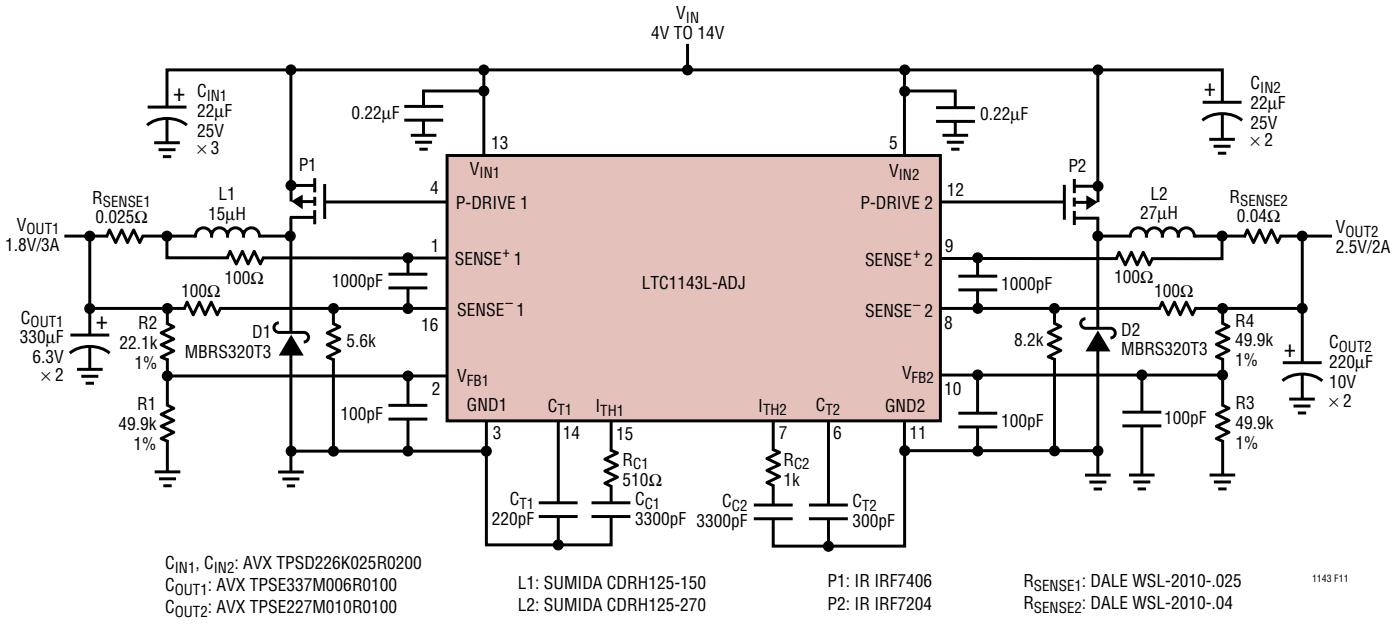
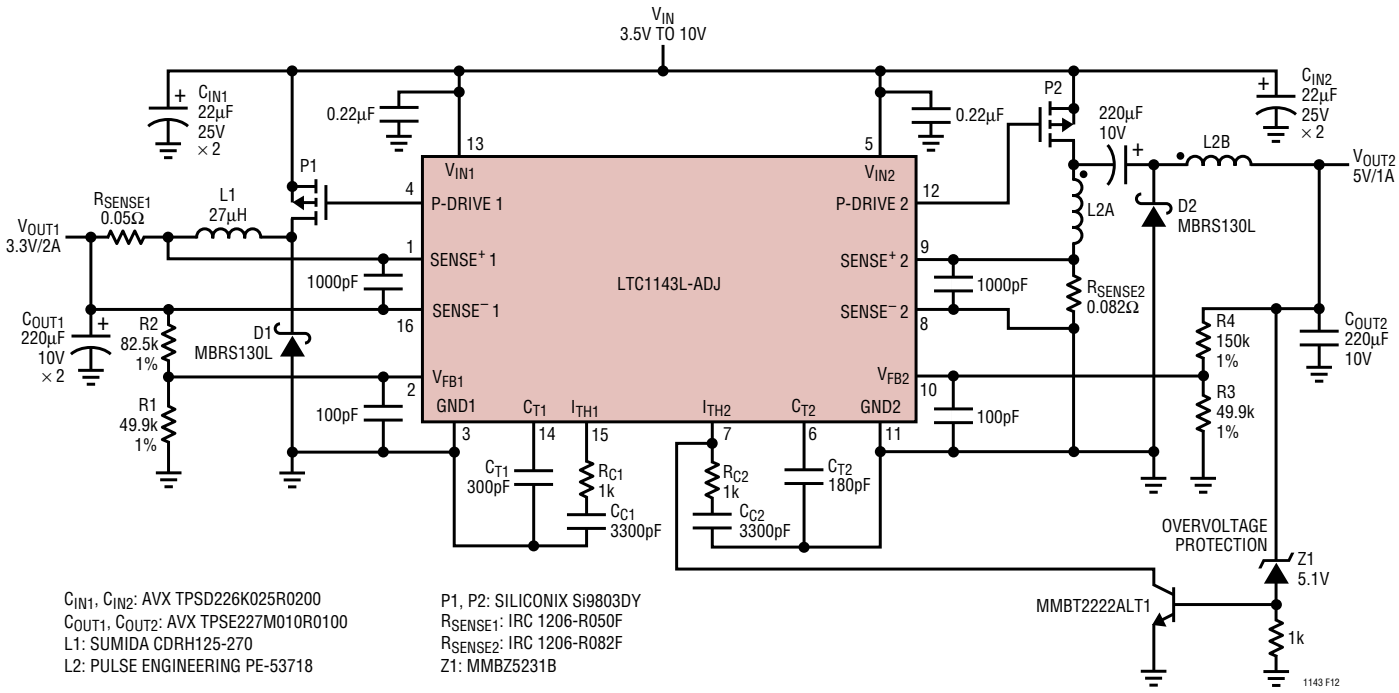


Figure 11. Dual 1.8V/3A and 2.5V/2A with Burst Mode Defeated

TYPICAL APPLICATIONS



CIN1, CIN2: AVX TPSD226K025R0200
COUT1, COUT2: AVX TPSE227M010R0100
L1: SUMIDA CDRH125-270
L2: PULSE ENGINEERING PE-53718

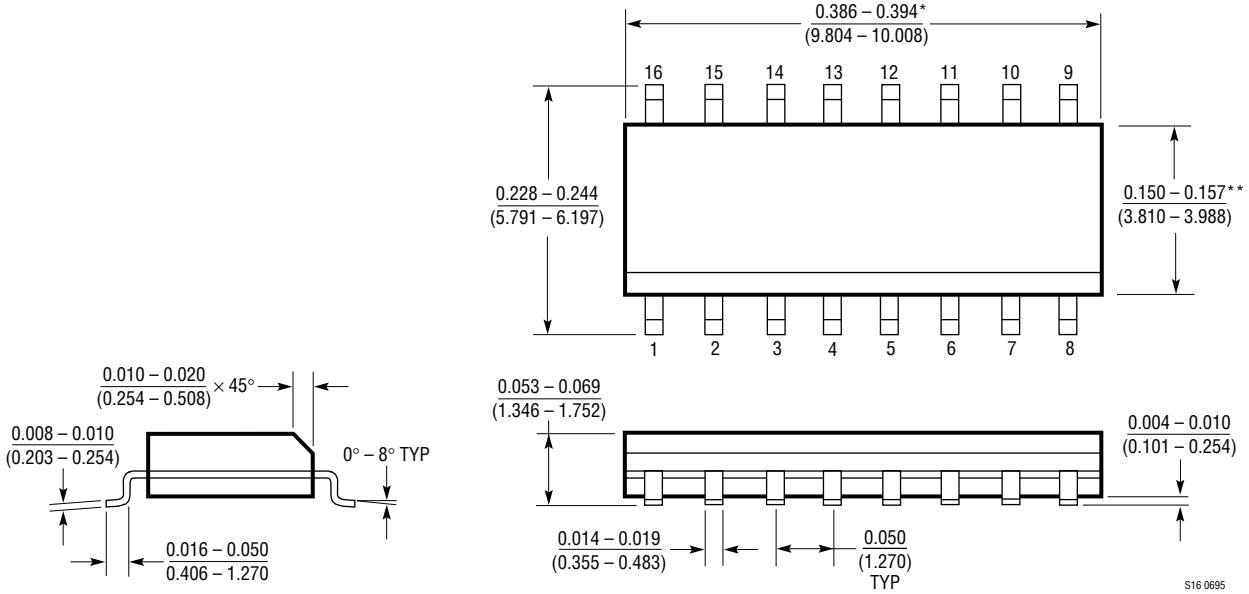
P1, P2: SILICONIX Si9803DY
RSENSE1: IRC 1206-R050F
RSENSE2: IRC 1206-R082F
Z1: MMBZ5231B

Figure 12. Dual 3.3V/5V Buck-Boost Regulator

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

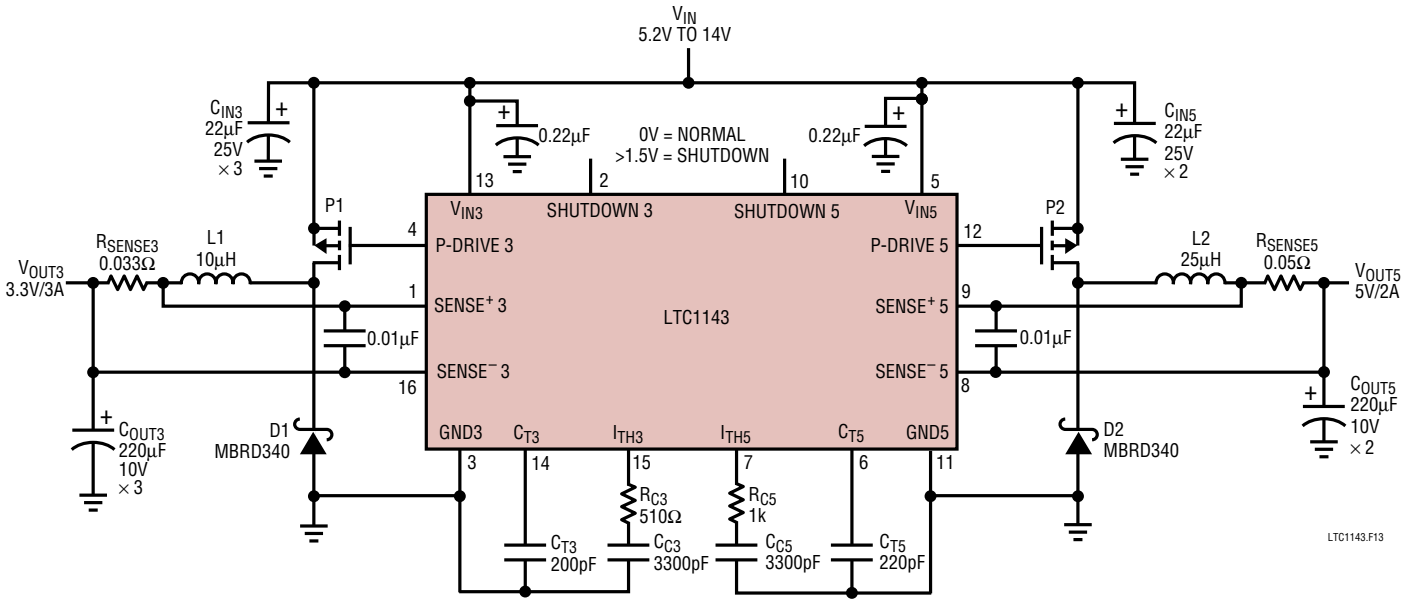
S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION



CIN3, CIN5: AVX TPSD226K025R0200
COUT3, COUT5: AVX TPSE227M010R0080
L1: COILTRONICS CTX10-4
L2: COILTRONICS CTX25-4

P1: SILICONIX Si4431DY
P2: SILICONIX Si9435DY
RSENSE3: KRL SL-1/2-C1-0R033J
RSENSE5: KRL SL-1/2-C1-0R050J

Figure 13. All Surface Mount Dual 5V/2A, 3.3V/3A Converter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1142	Dual High Efficiency Synchronous Step-Down Switching Regulator	Synchronous Equivalent to LTC1143, 4V < V_{IN} < 16V
LTC1142L-ADJ	Dual High Efficiency Synchronous Step-Down Switching Regulator	Synchronous Equivalent to LTC1143L-ADJ, 3.5V < V_{IN} < 16V
LTC1142HV-ADJ	Dual High Efficiency Synchronous Step-Down Switching Regulator	4V < V_{IN} < 20V
LTC1147L	High Efficiency Step-Down Switching Regulator Controller	(1/2) LTC1143L-ADJ in SO-8
LTC1265	1.2A, High Efficiency Step-Down DC/DC Converter	Single Channel with Internal Switch
LTC1438	Dual Synchronous Controller with Power-On Reset and an Extra Comparator	Constant Frequency Current Mode, Drives Synchronous N-Channel MOSFETS
LTC1538-AUX	Dual Synchronous Controller with Auxiliary Linear Regulator Controller and 5V Standby	Up to Four Output Voltages from G28 Package
LTC1539	Dual Synchronous Controller with Phase-Locked Loop and Adaptive Power™ Operation	Full Featured Dual Controller in G36 Package

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