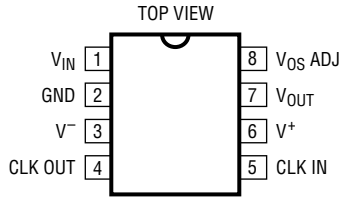
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 400mW
Voltage at Any Input .... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Burn-In Voltage 16V

Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



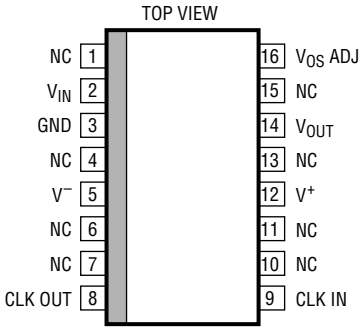
N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 100°C, θ_{JA} = 110°C/W (N)

ORDER PART NUMBER: LTC1063CN8

J8 PACKAGE
8-LEAD CERAMIC DIP
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J)

ORDER PART NUMBER: LTC1063CJ8, LTC1063MJ8

OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source



SW PACKAGE
16-LEAD PLASTIC SO WIDE
T_{JMAX} = 100°C, θ_{JA} = 85°C/W

ORDER PART NUMBER: LTC1063CSW

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz, R_L = 10k, T_A = 25°C, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock-to-Cutoff Frequency Ratio (f_{CLK}/f_C)	±2.375V ≤ V_S ≤ ±7.5V			100±0.5		
Maximum Clock Frequency (Note 2)	V_S = ±7.5V V_S = ±5V V_S = ±2.5V			5 4 3		MHz MHz MHz
Minimum Clock Frequency (Note 3)	±2.5V ≤ V_S ≤ ±7.5V, T_A < 85°C			30		Hz
Input Frequency Range			0		0.9f_{CLK}	
Filter Gain	V_S = ±5V, f_{CLK} = 25kHz, f_C = 250Hz f_{IN} = 250Hz	 ●	 –3.5 –3.6	 –3.0 –3.0	 –2.5 –2.4	 dB dB
	V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz f_{IN} = 100Hz			0		dB
	f_{IN} = 1kHz = 0.2f_C	 ●	–0.06 –0.075	–0.01 –0.01	0.04 0.055	dB dB
	f_{IN} = 2.5kHz = 0.5f_C	 ●	–0.09 –0.14	0.16 0.16	0.41 0.46	dB dB
	f_{IN} = 4kHz = 0.8f_C	 ●	–0.5 –0.6	–0.2 –0.2	0.1 0.2	dB dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz, R_L = 10k, T_A = 25°C, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	f_{IN} = 5kHz = f_C		−3.5	−3.0	−2.5	dB
		●	−3.6	−3.0	−2.4	dB
	f_{IN} = 20kHz = 4f_C		−57.5	−60.0	−62.0	dB
		●	−57.0	−60.0	−62.5	dB
Filter Gain	V_S = ±2.375V, f_{CLK} = 500kHz, f_C = 5kHz f_{IN} = 1kHz		−0.066	0.004	0.074	dB
		●	−0.081	0.004	0.089	dB
	f_{IN} = 2.5kHz		−0.24	0.16	0.56	dB
		●	−0.29	0.16	0.61	dB
	f_{IN} = 4kHz		−0.6	−0.2	0.2	dB
		●	− 0.7	−0.2	0.3	dB
	f_{IN} = 5kHz		−3.5	−3.0	−2.5	dB
		●	−3.6	−3.0	−2.4	dB
Clock Feedthrough	±2.375 ≤ V_S ≤ ±7.5V			50		μV_{RMS}
Wideband Noise (Note 4)	±2.375 ≤ V_S ≤ ±7.5V, 1Hz < f < f_{CLK}			100		μV_{RMS}
THD + Wideband Noise (Note 5)	V_S = ±7.5V, f_C = 20kHz, f_{IN} = 1kHz, $1V_{RMS} \le V_{IN} \le 2.3V_{RMS}$			−80		dB
Filter Output ± DC Swing	V_S = ±2.375V		1.6/−2.0	1.7/−2.2		V
		●	1.4/−1.8			V
	V_S = ±5V		4.0/−4.5	4.3/−4.8		V
		●	3.8/−4.3			V
	V_S = ±7.5V		6.5/−7.0	6.8/−7.3		V
		●	6.3/−6.8			V
Input Bias Current				10		nA
Dynamic Input Impedance				800		MΩ
Output DC Offset (Note 6)	V_S = ±2.375V			2		mV
	V_S = ±5V			0	±5	mV
	V_S = ±7.5V			−4		mV
Output DC Offset Drift	V_S = ±2.375V			10		µV/°C
	V_S = ±5V			20		µV/°C
	V_S = ±7.5V			25		µV/°C
Self-Clocking Frequency (f_{OSC})	R (Pin 4 to 5) = 20k, C (Pin 5 to GND) = 470pF V_S = ±2.375V		99	105	112	kHz
		●	95	103	114	kHz
	V_S = ±5V		102	108	114	kHz
		●	98	106	114	kHz
	V_S = ±7.5V		104	110	116	kHz
		●	101	109	116	kHz
External CLK Pin Logic Thresholds	V_S = ±2.375V Min Logical "1"			1.43		V
	Max Logical "0"			0.47		V
	V_S = ±5V Min Logical "1"			3		V
	Max Logical "0"			1		V
	V_S = ±7.5V Min Logical "1"			4.5		V
	Max Logical "0"			1.5		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz, R_L = 10k, T_A = 25°C, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Current	V_S = ±2.375V, f_{CLK} = 500kHz			2.7	4.0	mA
		●			5.5	mA
	V_S = ±5V, f_{CLK} = 500kHz			5.5	8	mA
		●			11	mA
	V_S = ±7.5V, f_{CLK} = 500kHz			7.0	11	mA
		●			14.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The maximum clock frequency criterion is arbitrarily defined as: The frequency at which the filter AC response exhibits ≥ 1dB of gain peaking.

Note 3: At limited temperature ranges (i.e., $T_A \leq 50°C$) the minimum clock frequency can be as low as 10Hz. The minimum clock frequency is arbitrarily defined as: the clock frequency at which the output DC offset changes by more than 1mV.

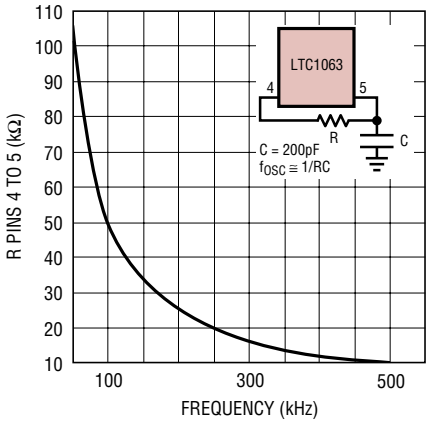
Note 4: The wideband noise specification does not include the clock feedthrough.

Note 5: To properly evaluate the filter's harmonic distortion an inverting output buffer is recommended as shown in the Test Circuit. An output buffer is not necessarily needed when measuring output DC offset or wideband noise.

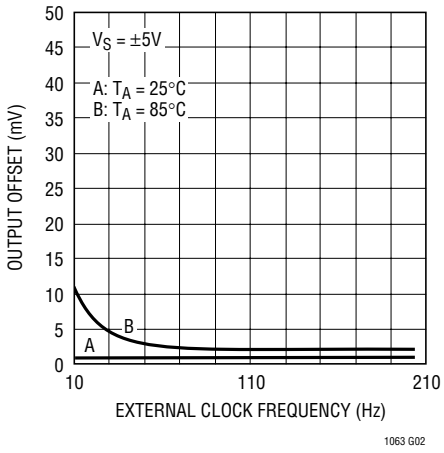
Note 6: The output DC offset is optimized for ±5V supply. The output DC offset shifts when the power supplies change; however this phenomenon is repeatable and predictable.

TYPICAL PERFORMANCE CHARACTERISTICS

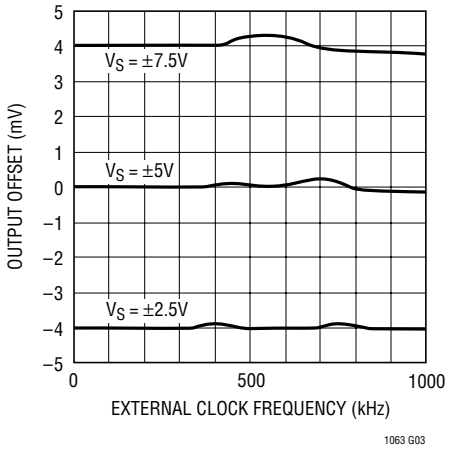
Self-Clocking Frequency vs R



Output Offset vs Clock, Low Clock Rates

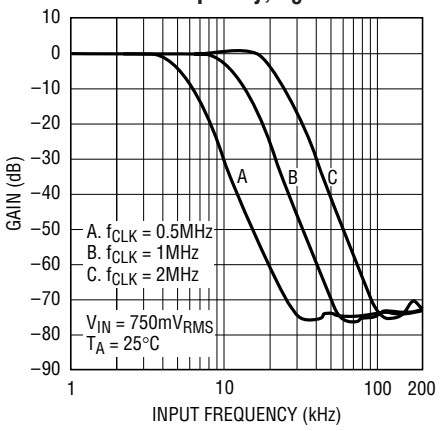


Output Offset vs Clock, Medium Clock Rates

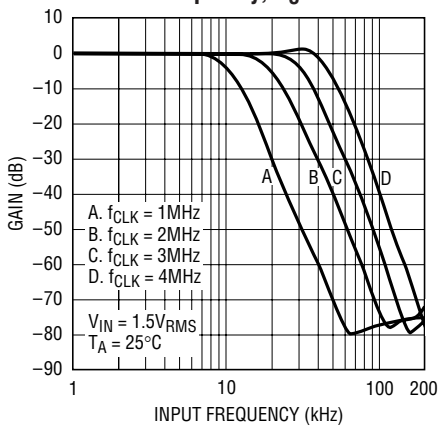


TYPICAL PERFORMANCE CHARACTERISTICS

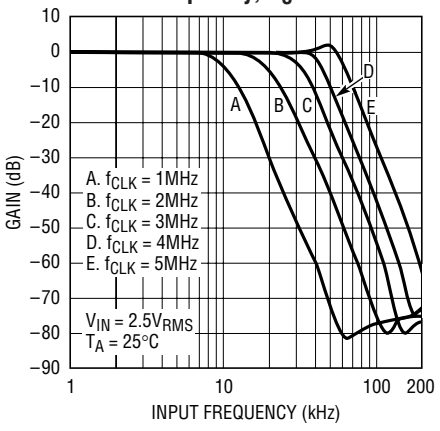
Gain vs Frequency; $V_S = \pm 2.5V$



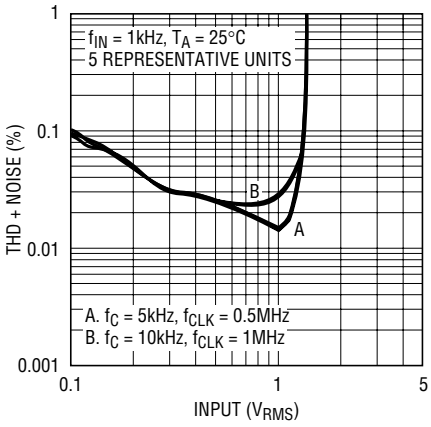
Gain vs Frequency; $V_S = \pm 5V$



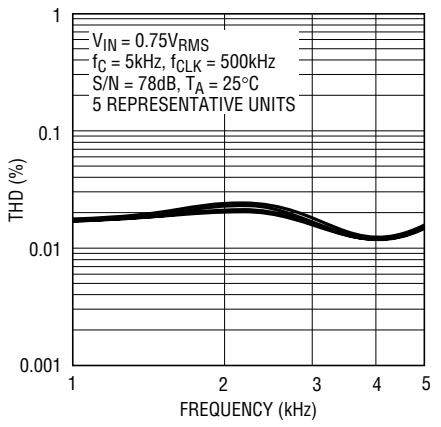
Gain vs Frequency; $V_S = \pm 7.5V$



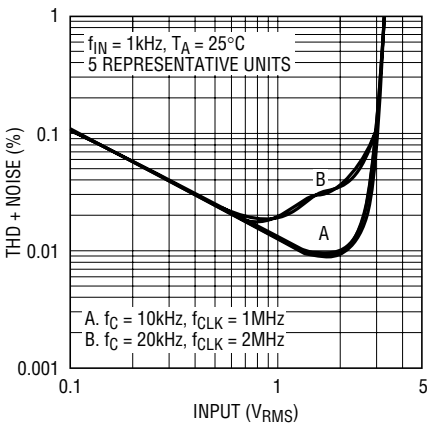
THD + Noise vs Input Voltage; V_S = Single 5V



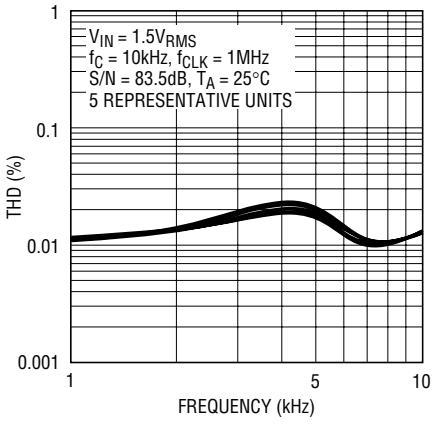
THD vs Frequency; V_S = Single 5V



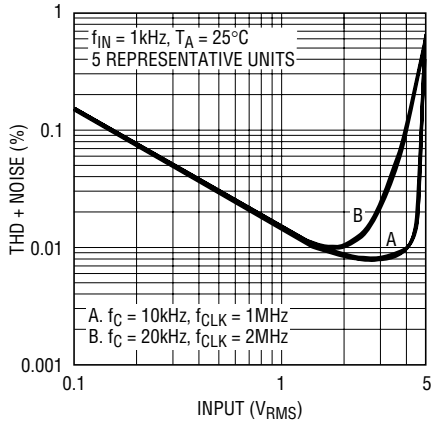
THD + Noise vs Input Voltage; $V_S = \pm 5V$



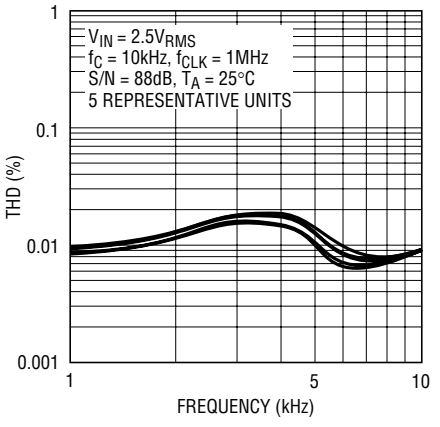
THD vs Frequency; $V_S = \pm 5V$



THD + Noise vs Input Voltage; $V_S = \pm 7.5V$

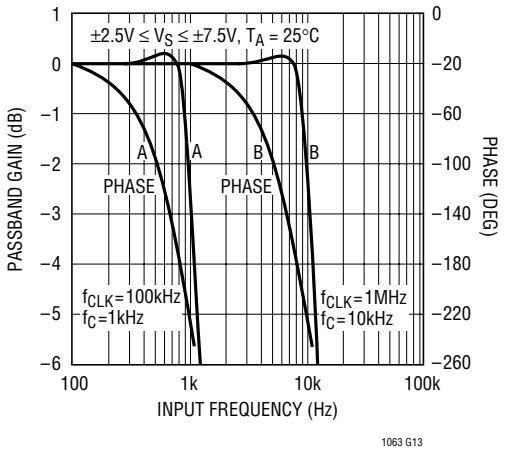


THD vs Frequency; $V_S = \pm 7.5V$



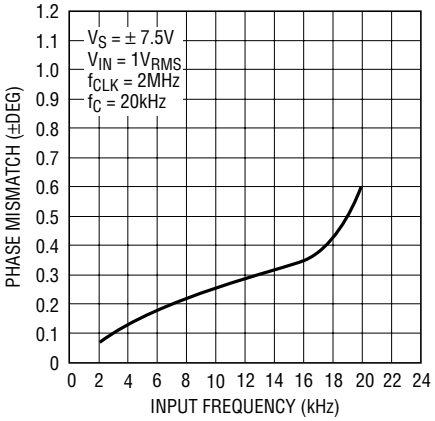
TYPICAL PERFORMANCE CHARACTERISTICS

Passband Gain and Phase vs Input Frequency



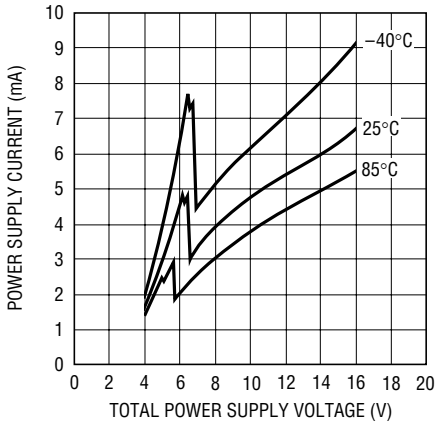
1063 G13

Phase Matching



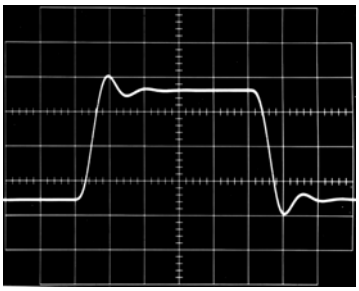
1063 G14

Power Supply Current vs Power Supply Voltage



1063 G15

Transient Response



HORIZONTAL: 0.1ms/DIV, VERTICAL: 2V/DIV
V_S = ±5V, f_C = 10kHz, V_{IN} = 1kHz ±3V_P
SQUARE WAVE

1063 G16

PIN FUNCTIONS

Power Supply Pins (Pins 6, 3, N Package)

The positive and negative supply pin should be bypassed with a high quality 0.1µF ceramic capacitor. In applications where the clock pin (5) is externally swept to provide several cutoff frequencies, the output DC offset variation is minimized by connecting an additional 1µF solid tantalum capacitor in parallel with the 0.1µF disc ceramic. This technique was used to generate the graphs of the output DC offset variation versus clock; they are illustrated in the Typical Performance Characteristics section.

When the power supply voltage exceeds ±7V, and when V^- is applied before V^+, if V^+ is allowed to go below ground, connect a signal diode between the positive supply pin and ground to prevent latch-up (see Typical Applications).

Ground Pin (Pin 2, N Package)

The ground pin merges the internal analog and digital ground paths. The potential of the ground pin is the reference for the internal switched-capacitor resistors, and the reference for the external clock. The positive input of the internal op amp is also tied to the ground pin.

For dual supply operation, the ground pin should be connected to a high quality AC and DC ground. A ground plane, if possible, should be used. A poor ground will degrade DC offset and it will increase clock feedthrough, noise and distortion.

A small amount of AC current flows out of the ground pin whether or not the internal oscillator is used. The frequency of the ground current equals the frequency of the internal or external clock. The average value of this current is approximately 55µA, 110µA, 170µA for ±2.5V, ±5V and ±7.5V supplies respectively.

For single supply operation, the ground pin should be preferably biased at half supply (see Typical Applications).

V_{OS} Adjust Pin (Pin 8, N Package)

The V_{OS} adjust pin can be used to trim any small amount of output DC offset voltage or to introduce a desired output DC level. The DC gain from the V_{OS} adjust pin to the filter output pin equals two.

Any DC voltage applied to this pin will reflect at the output pin of the filter multiplied by two.

If the V_{OS} adjust pin is not used, it should be shorted to the ground pin. The DC bias current flowing into the V_{OS} adjust pin is typically 10pA.

Pin 8 should always be connected to an AC ground; AC signals applied to this pin will degrade the filter response.

Input Pin (Pin 1, N Package)

Pin 1 is the filter input and it is connected to an internal switched-capacitor resistor. If the input pin is left floating, the filter output will saturate. The DC input impedance of pin 1 is very high; with ±5V supplies and 1MHz clock, the DC input impedance is typically 1GΩ. A resistor, R_{IN}, in series, with the input pin will not alter the value of the filter's DC output offset (Figure 1). R_{IN} should, however, be limited to a maximum value (Table 1), otherwise the filter's passband flatness will be affected. Refer to the Applications Information section for more details.

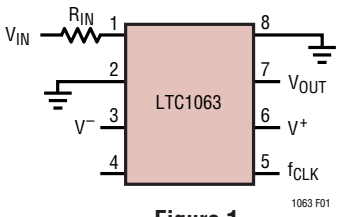


Figure 1.

Table 1. $R_{IN(MAX)}$ vs Clock and Power Supply

	$R_{IN(MAX)}$		
	$V_S = \pm 7.5V$	$V_S = \pm 5V$	$V_S = \pm 2.5V$
f_{CLK} = 4MHz	2.2k	–	–
f_{CLK} = 3MHz	3.4k	2.9k	–
f_{CLK} = 2MHz	5.5k	5k	2.7k
f_{CLK} = 1MHz	11k	11k	9.2k
f_{CLK} = 500kHz	24k	23k	21k
f_{CLK} = 100kHz	120k	120k	110k

PIN FUNCTIONS

Output Pin (Pin 7, N Package)

Pin 7 is the filter output. This pin can typically source over 20mA and sink 2mA. Pin 7 should not drive long coax cables, otherwise the filter's total harmonic distortion will degrade.

Clock Input Pin (Pin 5, N Package)

An external clock when applied to pin 5 tunes the filter cutoff frequency. The clock-to-cutoff frequency ratio is 100:1. The high (V_{HIGH}) and low (V_{LOW}) clock logic threshold levels are illustrated in Table 2. Square wave clocks with duty cycles between 30% and 50% are strongly recommended. Sinewave clocks are not recommended.

Table 2. Clock Pin Threshold Levels

POWER SUPPLY	V_{HIGH}	V_{LOW}
V_S = ±2.5V	1.5V	0.5V
V_S = ±5V	3V	1V
V_S = ±7.5V	4.5V	1.5V
V_S = ±8V	4.8V	1.6V
V_S = 5V, 0V	4V	3V
V_S = 12, 0V	9.6V	7.2V
V_S =15V, 0V	12V	9V

Clock Output Pin (Pin 4, N Package)

Any external clock applied to the clock input pin appears at the clock output pin. The duty cycle of the clock output equals the duty cycle of the external clock applied to the clock input pin. The clock output pin swings to the power supply rails. When the LTC1063 is used in a self-clocking mode, the clock of the internal oscillator appears at the clock output pin with a 30% duty cycle. The clock output pin can be used to drive other LTC1063s or other ICs. The maximum capacitance, $C_{L(MAX)}$, the clock output pin can drive is illustrated in Figure 2.

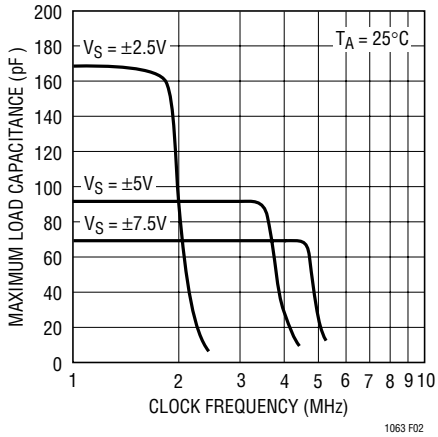


Figure 2. Maximum Load Capacitance at the Clock Output Pin

TEST CIRCUIT

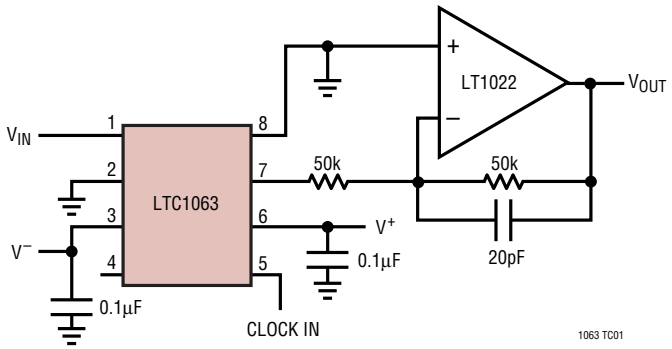


Figure 3. Test Circuit for THD

APPLICATIONS INFORMATION

Self-Clocking Operation

The LTC1063 features an internal oscillator which can be tuned via an external RC. The LTC1063's internal oscillator is primarily intended for generation of clock frequencies below 500kHz. The first curve of the Typical Performance Characteristics section shows how to quickly choose the value of the RC for a given frequency. More precisely, the frequency of the internal oscillator is equal to:

$f_{CLK} = K/RC$

For clock frequencies (f_{CLK}) below 100kHz, K equals 1.07. Figure 4b shows the variation of the parameter K versus clock frequency and power supply. First choose the desired clock frequency, (f_{CLK} < 500kHz), then through Figure 4b pick the right value of K, set C = 200pF and solve for R.

Example 1: f_{CUTOFF} = 2kHz, f_{CLK} = 200kHz, V_S = ±5V, T_A = 25°C, K = 1.0, C = 200pF

then, R = (1.0)/(200kHz × 204pF) = 24.5k.

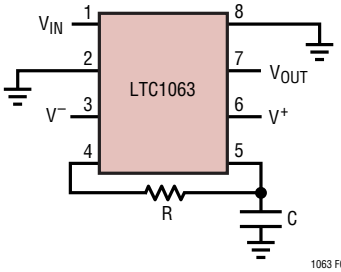


Figure 4a.

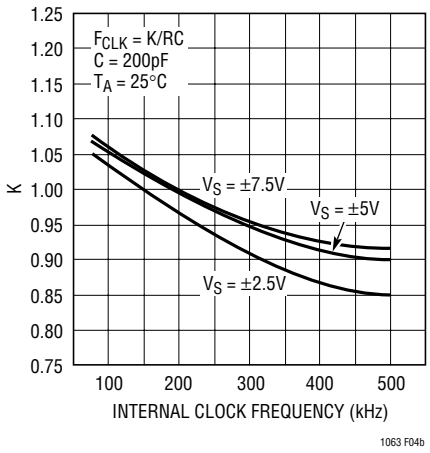


Figure 4b. f_{CLK} vs K

Note a 4pF parasitic capacitance is assumed in parallel with the external 200pF timing capacitor. Figure 5 shows the clock frequency variation from –40°C to 85°C. The 200kHz clock of Example 1 will change by –1.75% at 85°C.

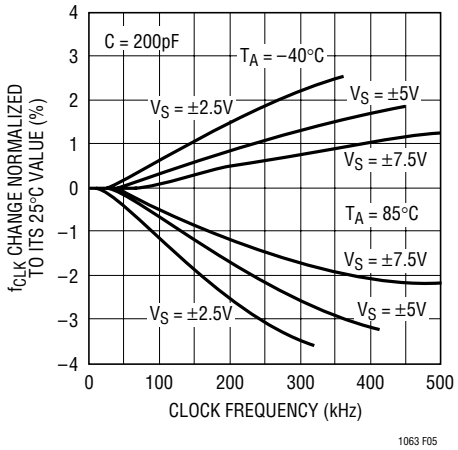


Figure 5. f_{CLK} vs Temperature

For a very limited temperature range, the internal oscillator of the LTC1063 can be used to generate clock frequencies above 500kHz (Figures 6 and 7). The data of Figure 6 is derived from several devices. For a given external (RC) value, the observed device-to-device clock frequency variation was ±1% (V_S = ±5V), and ±1.25% for V_S = ±2.5V.

Example 2: f_{CUTOFF} = 20kHz, f_{CLK} = 2MHz, V_S = ±7.5V, T_A = 25°C, C = 10pF

from Figure 6, K = 0.575,

and, R = (0.575)/(2MHz × 14pF) = 20.5k.

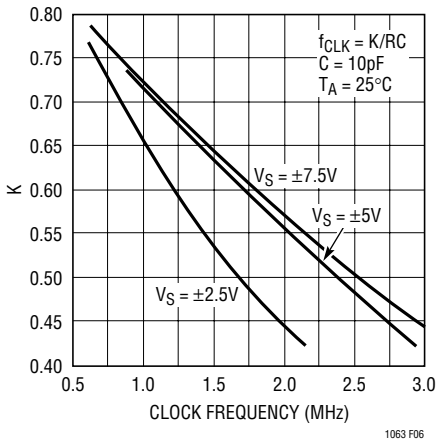


Figure 6. f_{CLK} vs K

APPLICATIONS INFORMATION

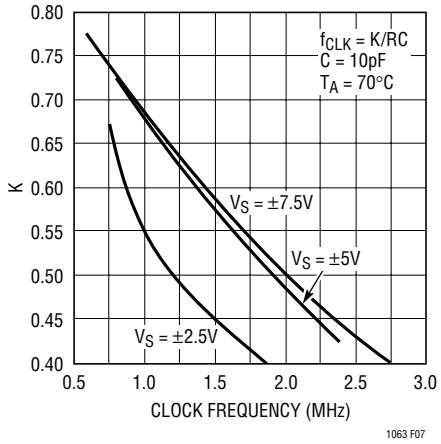


Figure 7. f_{CLK} vs K

A 4pF parasitic capacitance is assumed in parallel with the external 10pF capacitor. A ±1% clock frequency variation from device to device can be expected. The 2MHz clock frequency designed above will typically drift to 1.74MHz at 70°C (Figure 7).

The internal clock of the LTC1063 can be overridden by an external clock provided that the external clock source can drive the timing capacitor, C, which is connected from the clock input pin to ground.

Output Offset

The DC output offset of the LTC1063 is trimmed to typically less than ±1mV . The trimming is done at V_S = ±5V. To obtain optimum DC offset performance, appropriate PC layout techniques should be used and the filter IC should be soldered to the PC board. A socket will degrade the output DC offset by typically 1mV. The output DC offset is sensitive to the coupling of the clock output pin 4 (N package) to the negative power supply pin 3 (N package). The negative supply pin should be well decoupled. When the surface mount package is used, all the unused pins should be grounded.

When the power supplies are fixed, the output DC offset should not change by more than ±100µV over 10Hz to 1MHz clock frequency variation. When the filter clock frequency is fixed, the output DC offset will typically change by –4mV (2mV) when the power supply varies from ±5V to ±7.5V (±2.5V). See Typical Performance Characteristics.

Common Mode Rejection Ratio

The common mode rejection ratio is defined as the change of the output DC offset with respect to the DC change of the input voltage applied to the filter.

$$CMRR = 20\log (\Delta V_{OS\ OUT}/\Delta V_{IN})(dB)$$

Table 3 illustrates the common mode rejection for three power supplies and three temperatures. The common mode rejection improves if the output offset is adjusted to approximately 0V. The output offset can be adjusted via pin 8 (N package) (see Typical Applications).

Table 3. CMRR Data, f_{CLK} = 100kHz

POWER SUPPLY	ΔV_{IN}	–40°C	25°C	85°C	25°C (V_{OS} Nulled)
±2.5V	±1.8V	76dB	78dB	76dB	85dB
±5V	±4V	74dB	79dB	75dB	82dB
±7.5V	±6V	70dB	72dB	74dB	76dB

The above data is valid for clock frequencies up to 800kHz, 900kHz, 1MHz, for V_S = ±2.5V, ±5V, ±7.5V respectively.

Clock Feedthrough

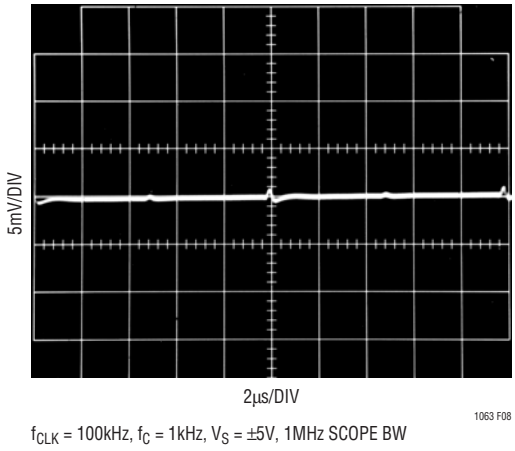
Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics which are present at the filter's output pin. The clock feedthrough is tested with the filter input grounded and it depends on the quality of the PC board layout and power supply decoupling. Any parasitic switching transients, during the rise and fall of the incoming clock, are not part of the clock feedthrough specifications; their amplitude strongly depends on scope probing techniques as well as ground quality and power supply bypassing. For a power supply V_S = ±5V, the clock feedthrough of the LTC1063 is 50µV_{RMS}; for V_S = ±7.5V, the clock feedthrough approaches 75µV_{RMS}. Figure 8 shows a typical scope photo of the LTC1063 output pin when the input pin is grounded. The filter cutoff frequency was 1kHz, while scope bandwidth was chosen to be 1MHz such as switching transients above the 100kHz clock frequency will show.

Wideband Noise

The wideband noise of the filter is the RMS value of the device's output noise spectral density. The wideband noise data is used to determine the operating signal-to-

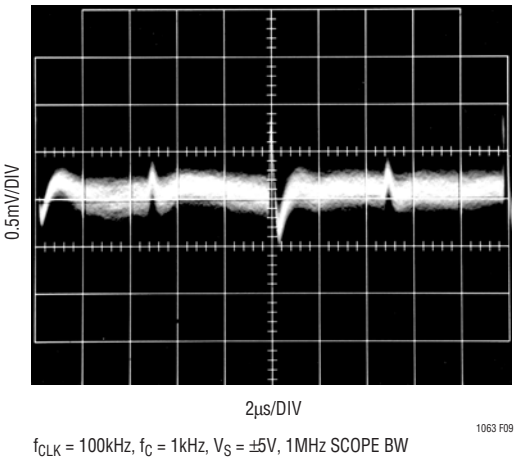
APPLICATIONS INFORMATION

noise ratio at a given distortion level. The wideband noise (μV_{RMS}) is nearly independent of the value of the clock frequency and excludes the clock feedthrough. The LTC1063's typical wideband noise is $95\mu V_{RMS}$. Figure 9 shows the same scope photo as Figure 8 but with a more sensitive vertical scale: The clock feedthrough is imbedded in the filter's wideband noise. The peak-to-peak wideband noise of the filter can be clearly seen; it is approximately $500\mu V_{P-P}$. Note that $500\mu V_{P-P}$ equals the $95\mu V_{RMS}$ wideband noise of the part, multiplied by a crest factor or 5.25.



f_{CLK} = 100kHz, f_C = 1kHz, V_S = ±5V, 1MHz SCOPE BW

Figure 8. LTC1063 Output Clock Feedthrough + Noise



f_{CLK} = 100kHz, f_C = 1kHz, V_S = ±5V, 1MHz SCOPE BW

Figure 9. LTC1063 Output Clock Feedthrough + Noise

Aliasing

Aliasing is an inherent phenomenon of sampled data filters and it primarily occurs when the frequency of an input signal approaches the sampling frequency. For the LTC1063, an input signal whose frequency is in the range of f_{CLK} ±6% will generate an alias signal into the filter's passband and stopband. Table 4 shows details.

Example: LTC1063, f_{CLK} = 20kHz, f_C = 200kHz,
f_{IN} = (19.6kHz, $100mV_{RMS}$)
f_{ALIAS} = (400Hz, $3.16mV_{RMS}$)

An input RC can be used to attenuate incoming signals close to the filter clock frequency (Figure 10). A Butterworth passband response will be maintained if the value of the input resistor follows Table 1.

Table 4. Aliasing Data

INPUT FREQUENCY	OUTPUT FREQUENCY	OUTPUT AMPLITUDE REFERENCED TO INPUT SIGNAL
0.9995 f_{CLK}	0.0005 f_{CLK}	0 dB
0.995 f_{CLK}	0.005 f_{CLK}	0 dB
0.99 f_{CLK}	0.01 f_{CLK}	–3 dB
0.9875 f_{CLK}	0.0125 f_{CLK}	–10.2 dB
0.985 f_{CLK}	0.015 f_{CLK}	–17.7 dB
0.9825 f_{CLK}	0.0175 f_{CLK}	–24.3 dB
0.98 f_{CLK}	0.02 f_{CLK}	–30 dB
0.975 f_{CLK}	0.025 f_{CLK}	–40 dB
0.97 f_{CLK}	0.03 f_{CLK}	–48 dB
0.965 f_{CLK}	0.035 f_{CLK}	–54.5 dB
0.96 f_{CLK}	0.04 f_{CLK}	–60.4 dB
0.955 f_{CLK}	0.045 f_{CLK}	–65.5 dB
0.95 f_{CLK}	0.05 f_{CLK}	–70.16 dB
0.94 f_{CLK}	0.06 f_{CLK}	–78.25 dB
0.93 f_{CLK}	0.07 f_{CLK}	–85.3 dB
0.9 f_{CLK}	0.1 f_{CLK}	–100.3 dB

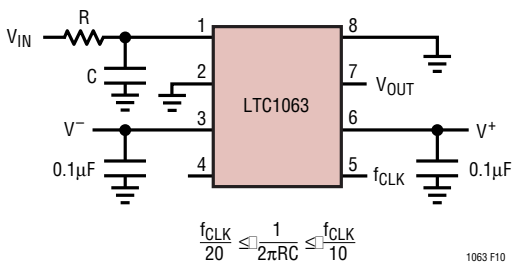


Figure 10. Adding an Input Anti-Aliasing RC

APPLICATIONS INFORMATION

Group Delay

The group delay of the LTC1063 closely approximates the delay of an ideal 5-pole Butterworth lowpass filter (Figure 11, Curve A). To linearize the group delay of the LTC1063 (Figure 11, Curve B), use an input resistor about six times higher than the maximum value of R_{IN}, shown in Table 1. The passband response of the group delay corrected filter approximates a 5-pole Bessel response while its transition band rolls off like a Butterworth.

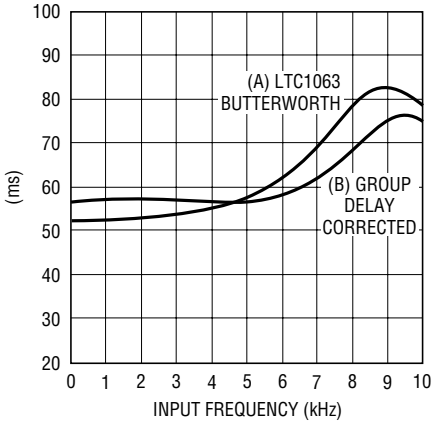
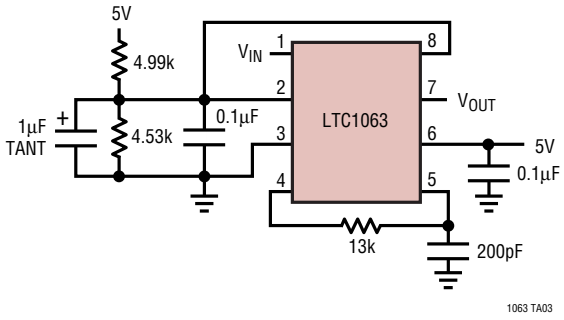


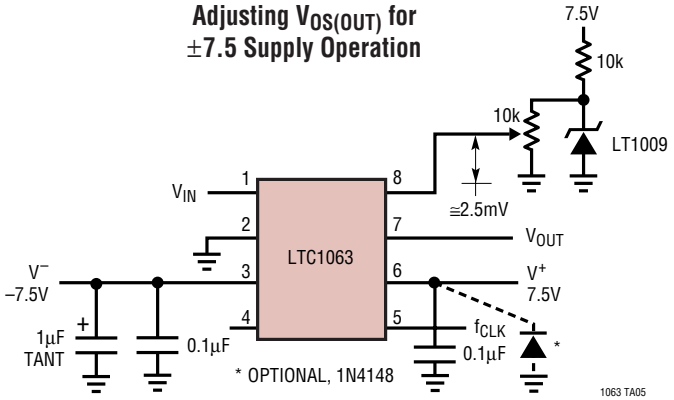
Figure 11. Group Delay

TYPICAL APPLICATIONS

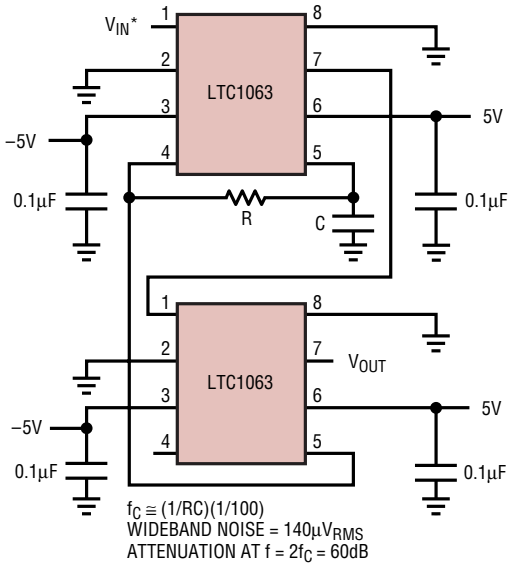
Single 5V Supply Operation (f_C = 3.4kHz)



Adjusting $V_{OS(OUT)}$ for ±7.5 Supply Operation

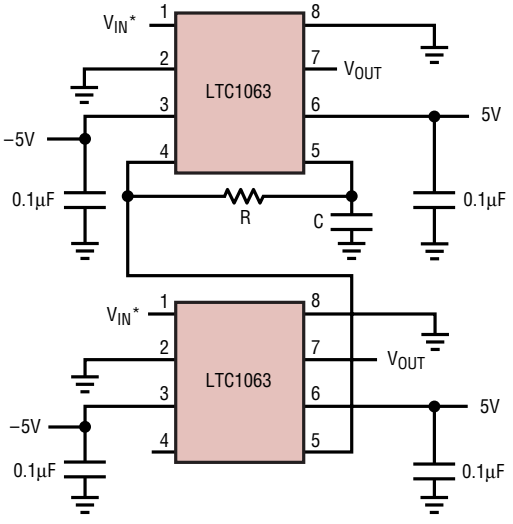


Cascading Two LTC1063s for Steeper Roll-Off



* IF THE INPUT VOLTAGE CAN EXCEED V⁺, CONNECT A SIGNAL DIODE BETWEEN PIN 1 AND V⁺. 1063 TA04

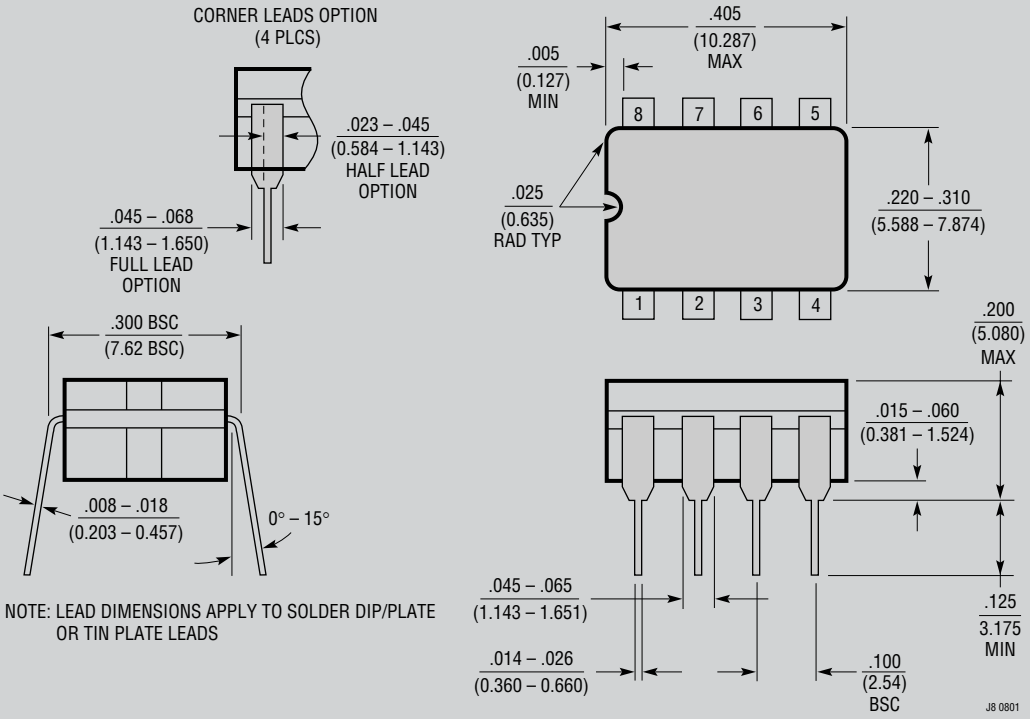
Sharing Clock for Multichannel Applications



* IF THE INPUT VOLTAGE CAN EXCEED V⁺, CONNECT A SIGNAL DIODE BETWEEN PIN 1 AND V⁺. 1063 TA06

PACKAGE DESCRIPTION

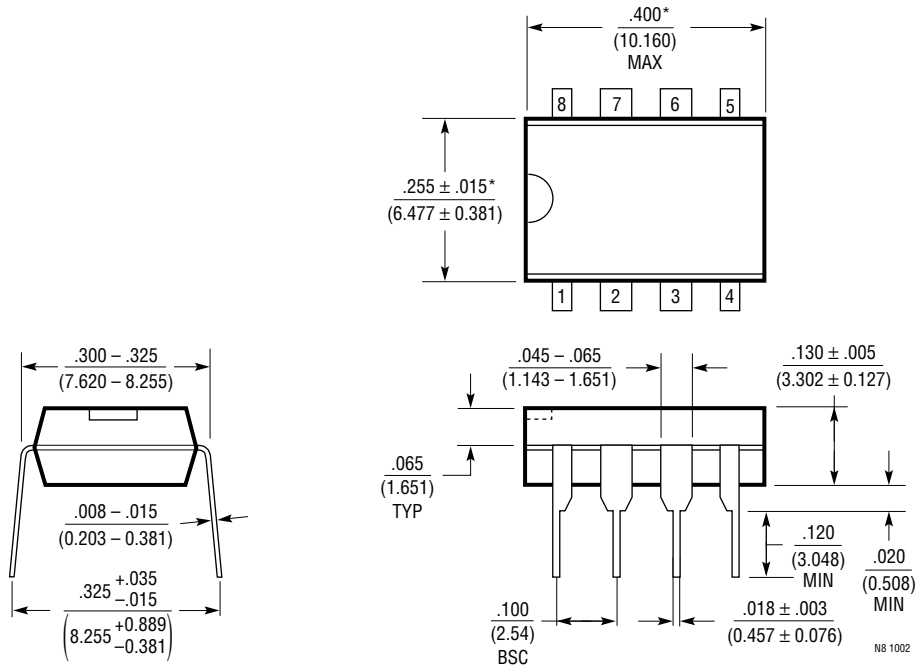
J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

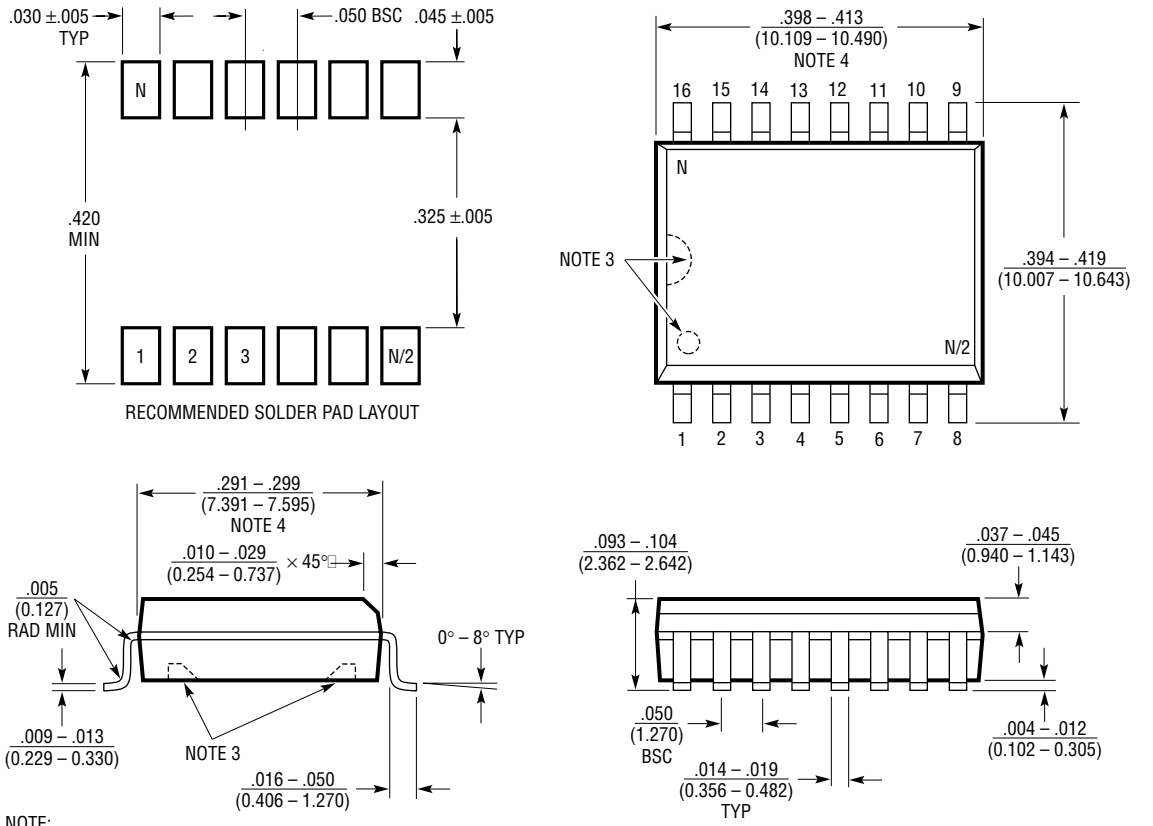


NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

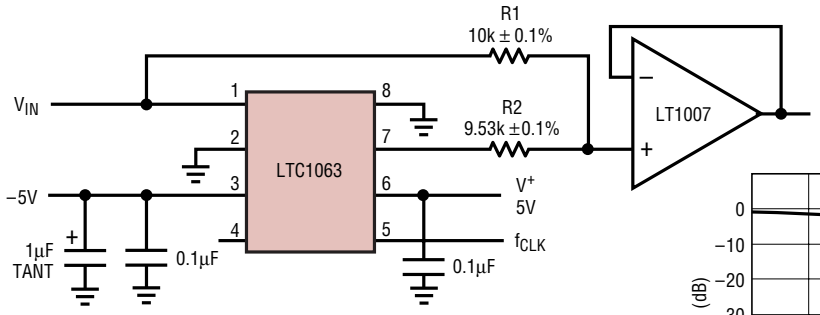
SW Package
16-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



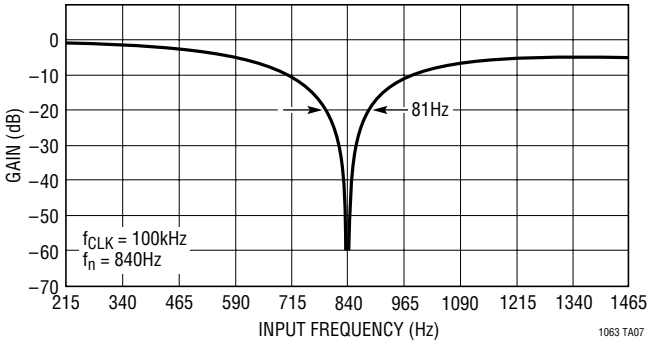
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

TYPICAL APPLICATIONS

Low Noise DC Accurate Clock-Tunable Notch



- $f_{NOTCH} = \frac{f_{CLK}}{119.04}$
- NOTCH DEPTH > 50dB
- OUPUT DC OFFSET = $\frac{(LTC1063)V_{OS}}{2} \cong 500\mu V$
- OUTPUT NOISE = $50\mu V_{RMS}$
- $\frac{f_{NOTCH}}{f(-20dB)BW} = \frac{10.4}{1}$



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1065	Clock-Tunable 5th Order Bessel Lowpass Filter	1mV Offset, 80dB CMR
LTC1565-31	650kHz Linear Phase Lowpass Filter	Continuous Time, Fully Differential In/Out
LTC1566-1	Low Noise, 2.3MHz Lowpass Filter	Continuous Time, Fully Differential In/Out
LT1567	Low Noise Op Amp and Inverter Building Block	Single Ended to Differential Conv
LT1568	Low Noise, 10MHz 4th Order Building Block	Lowpass or Bandpass, Differential Outputs
LTC1569-6	Linear Phase, DC Accurate, 10th Order Lowpass	Resistor Set Clock, F_C < 64kHz
LTC1569-7	Linear Phase, DC Accurate, 10th Order Lowpass	Resistor Set Clock, F_C < 300kHz
LT6600-2.5	Low Noise Differential Amp and 10MHz Lowpass	$55\mu V_{RMS}$ Noise 100kHz-10MHz 3V Supply
LT6600-10	Low Noise Differential Amp and 20MHz Lowpass	$86\mu V_{RMS}$ Noise 100kHz-20MHz 3V Supply

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