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REVISION HISTORY

| | |
|--------------------------|---|
| 11/15—Rev. 0 to Rev. A | |
| Changes to Table 1 | 3 |

9/15—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 3.3\text{ V to }5\text{ V}$, $V_{CTL} = 0\text{ V/V}_{DD}$, $T_A = 25^\circ\text{C}$, $50\ \Omega$ system, unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|--|-------------------------|-----|----------|------------------|
| INSERTION LOSS | 0.1 GHz to 2.0 GHz | | 0.7 | 1.0 | dB |
| | 2.0 GHz to 4.0 GHz | | 0.8 | 1.1 | dB |
| | 4.0 GHz to 6.0 GHz | | 0.9 | 1.3 | dB |
| ISOLATION RFC to RF1/RF2 (Worst Case) | 0.1 GHz to 2.0 GHz | 55 | 70 | | dB |
| | 2.0 GHz to 4.0 GHz | 50 | 60 | | dB |
| | 4.0 GHz to 6.0 GHz | 40 | 51 | | dB |
| RETURN LOSS | On State | | | | |
| | | | 24 | | dB |
| | | | 18 | | dB |
| | Off State | | 18 | | dB |
| | | | 23 | | dB |
| | | | 22 | | dB |
| SWITCHING SPEED | 0.1 GHz to 2.0 GHz | | 16 | | dB |
| | 2.0 GHz to 4.0 GHz | | | | |
| | 4.0 GHz to 6.0 GHz | | | | |
| t_{RISE} , t_{FALL} t_{ON} , t_{OFF} | 10%/90% RF_{OUT} | | 60 | | ns |
| | 50% V_{CTL} to 10%/90% RF_{OUT} | | 150 | | ns |
| RF SETTling TIME | 50% V_{CTL} to 0.1 dB margin of final RF_{OUT} | | 170 | | ns |
| INPUT POWER | 1 dB Compression (P1dB) | $V_{DD} = 3.3\text{ V}$ | 34 | | dB |
| | | $V_{DD} = 5\text{ V}$ | 36 | | dB |
| | 0.1 dB Compression (P0.1dB) | $V_{DD} = 3.3\text{ V}$ | 33 | | dB |
| | | $V_{DD} = 5\text{ V}$ | 35 | | dB |
| INPUT THIRD-ORDER INTERCEPT (IP3) | Two-tone input power = 14 dBm/tone | | 60 | | dBm |
| RECOMMENDED OPERATING CONDITIONS | | | | | |
| Bias Voltage Range (V_{DD}) | | 3.0 | | 5.4 | V |
| Control Voltage Range (V_{CTL} , EN) | | 0 | | V_{DD} | V |
| Maximum RF Input Power ¹ $T_{CASE} = 105^\circ\text{C}$ | Through Path (5 V/3.3 V) | 31/30 | | | dBm |
| | Terminated Path | 24 | | | dBm |
| | Hot Switching | 24 | | | dBm |
| $T_{CASE} = 85^\circ\text{C}$ | Through Path (5 V/3.3 V) | 34/33 | | | dBm |
| | Terminated Path | 27 | | | dBm |
| | Hot Switching | 27 | | | dBm |
| $T_{CASE} = 25^\circ\text{C}$ | Through Path (5 V/3.3 V) | 34/33 | | | dBm |
| | Terminated Path | 29 | | | dBm |
| | Hot Switching | 27 | | | dBm |
| $T_{CASE} = -40^\circ\text{C}$ | Through Path (5 V/3.3 V) | 34/33 | | | dBm |
| | Terminated Path | 29 | | | dBm |
| | Hot Switching | 27 | | | dBm |
| Case Temperature Range (T_{CASE}) | | -40 | | +105 | $^\circ\text{C}$ |

¹ Exposure to levels between the recommended operating conditions and the absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Digital Control Voltages

| State | $V_{DD} = 3.3\text{ V}$ ($\pm 5\% V_{DD}$, $T_{CASE} = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$) | $V_{DD} = 5\text{ V}$ ($\pm 5\% V_{DD}$, $T_{CASE} = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$) |
|-----------------------|---|---|
| Input Control Voltage | | |
| Low (V_{IL}) | 0 V to 0.85 V at $<1\text{ }\mu\text{A}$, typical | 0 V to 1.20 V at $<1\text{ }\mu\text{A}$, typical |
| High (V_{IH}) | 1.15 V to 3.3 V at $<1\text{ }\mu\text{A}$, typical | 1.55 V to 5.0 V at $<1\text{ }\mu\text{A}$, typical |

Table 3. Bias Voltage vs. Supply Current

| Parameter | Symbol | Min | Typ | Max | Unit | Typical I_{DD} (mA) |
|-------------------------|----------|-----|------|-----|------|-----------------------|
| SUPPLY CURRENT | I_{DD} | | | | | |
| $V_{DD} = 3.3\text{ V}$ | | | 0.14 | | mA | 0.14 |
| $V_{DD} = 5\text{ V}$ | | | 0.16 | | mA | 0.16 |

ABSOLUTE MAXIMUM RATINGS

Table 4.

| Parameter | Rating |
|--|-------------------------------|
| Bias Voltage Range (V_{DD}) | −0.3 V to +5.5 V |
| Control Voltage Range (V_{CTL} , EN) | −0.5 V to V_{DD} + (+0.5 V) |
| RF Input Power ¹ (see Figure 2) | |
| Through Path | 35 dBm |
| Terminated Path | 30 dBm |
| Hot Switching | 30 dBm |
| Channel Temperature | 135°C |
| Storage Temperature Range | −65°C to +150°C |
| Thermal Resistance (Channel to Package Bottom) | |
| Through Path | 110°C/W |
| Terminated Path | 100°C/W |
| ESD Sensitivity | |
| HBM | 4 kV (Class 3A) |
| CDM | 1.25 kV |

¹ For recommended operating conditions, see Table 1.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

During the through mode of operation, the supply voltage scales the maximum allowed input power. The power handling vs. frequency for the 3.3 V and 5 V supplies is shown in Figure 2.

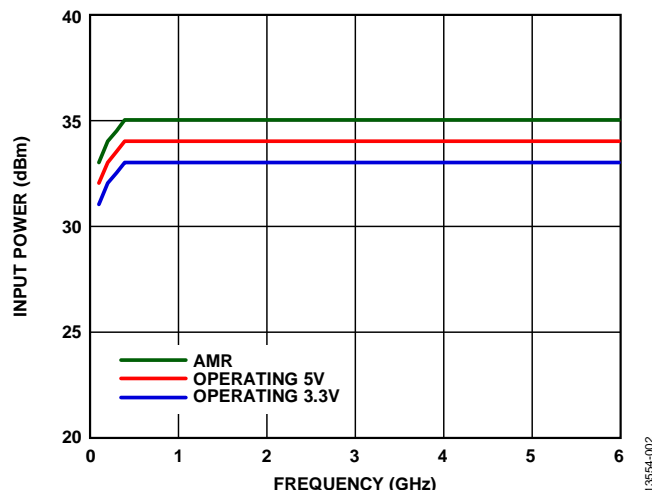


Figure 2. Through Path, Power Handling vs. Frequency

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

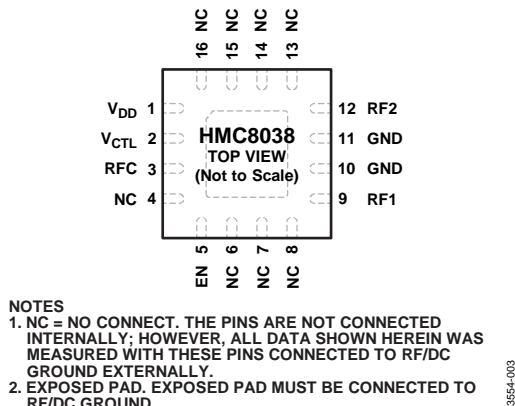


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|------------------------|------------------|--|
| 1 | V _{DD} | Supply Voltage Pin. |
| 2 | V _{CTL} | Control Input Pin. See Figure 5 for the V _{CTL} interface schematic. Refer to Table 6 and the recommended input control voltage range in Table 2. |
| 3 | RFC | RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin. |
| 4, 6 to 8, 13 to 16 | NC | Not Internally Connected. These pins are not internally connected; however, all data shown in this data sheet is measured with the NC pins externally connected to RF/dc ground on the evaluation board. |
| 5 | EN | Enable Input Pin. See Figure 5 for the EN interface schematic. Refer to Table 6 and the recommended input control voltage range in Table 2. |
| 9 | RF1 | RF Port 1. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin. |
| 10, 11 | GND | Ground. The package bottom has an exposed metal pad that must connect to the printed circuit board (PCB) RF ground. See Figure 4 for the GND interface schematic. |
| 12 | RF2 | RF Port 2. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin. |
| | EPAD | Exposed Pad. Exposed pad must be connected to RF/dc ground. |

INTERFACE SCHEMATICS

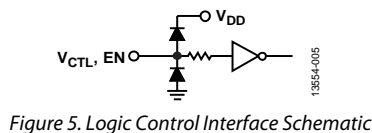
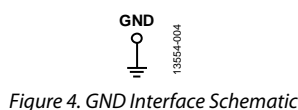
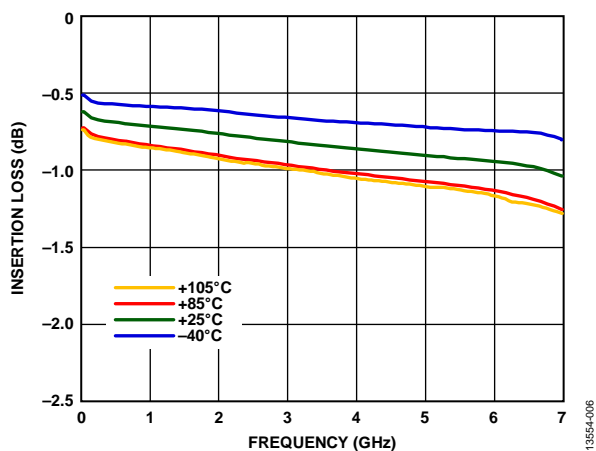
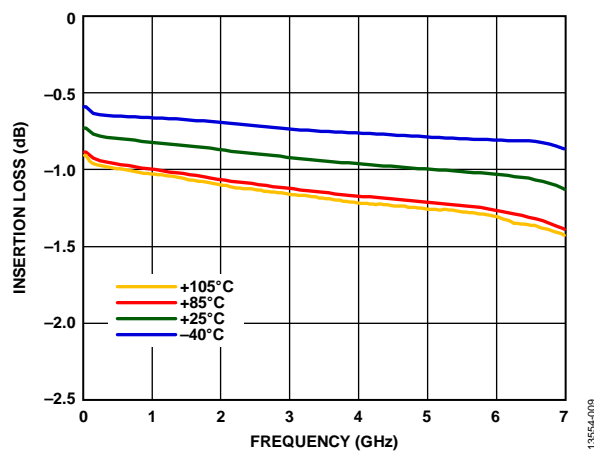
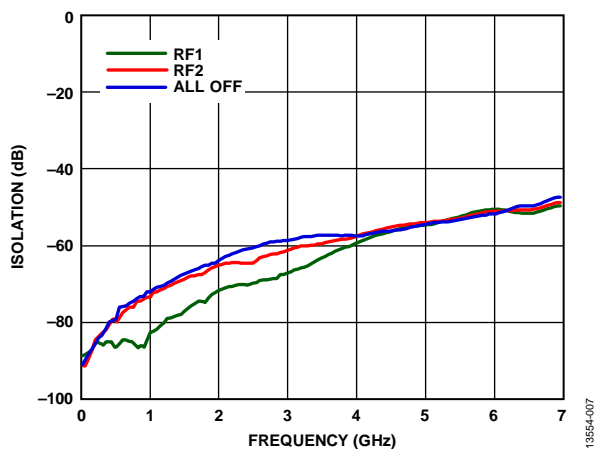
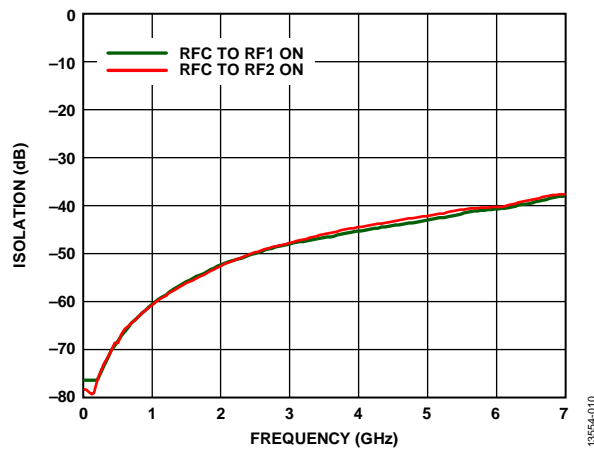
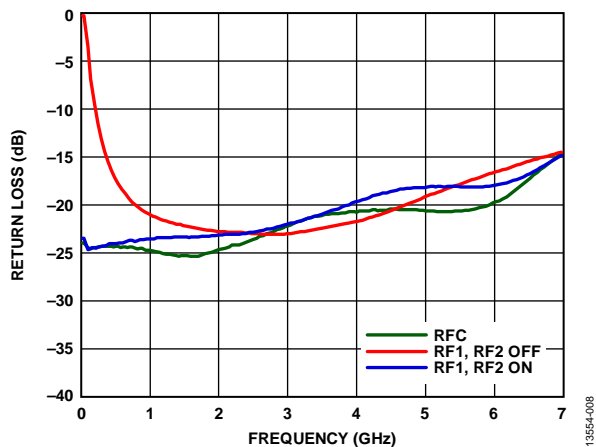


Table 6. Truth Table

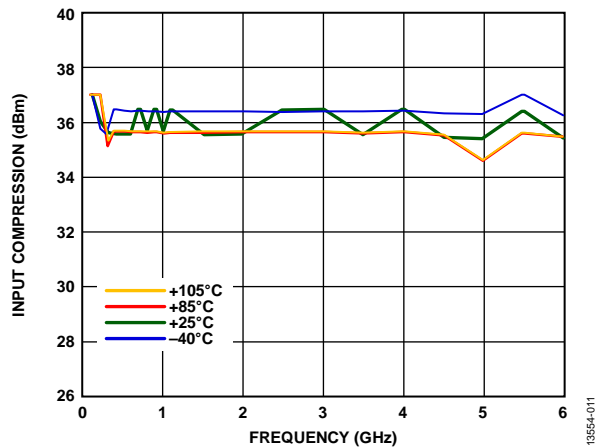
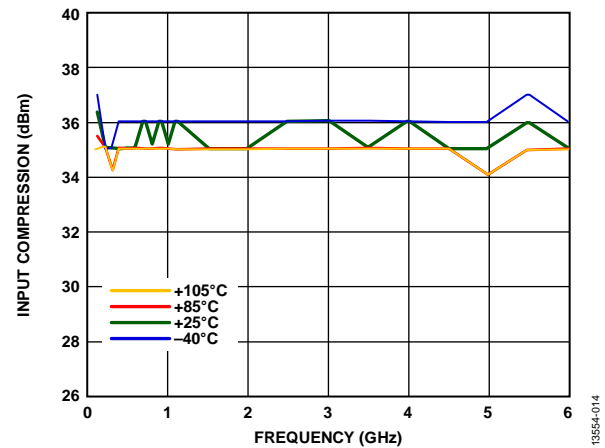
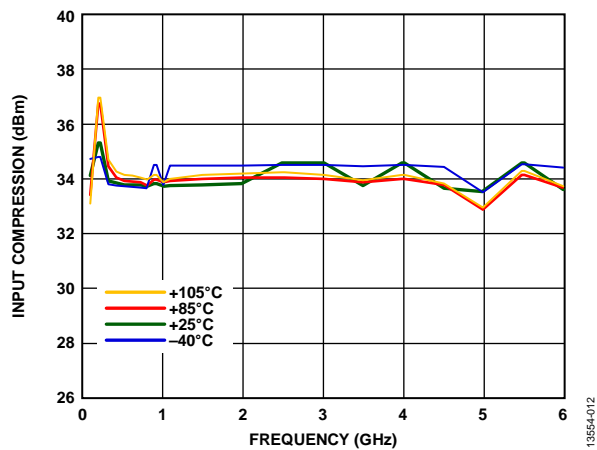
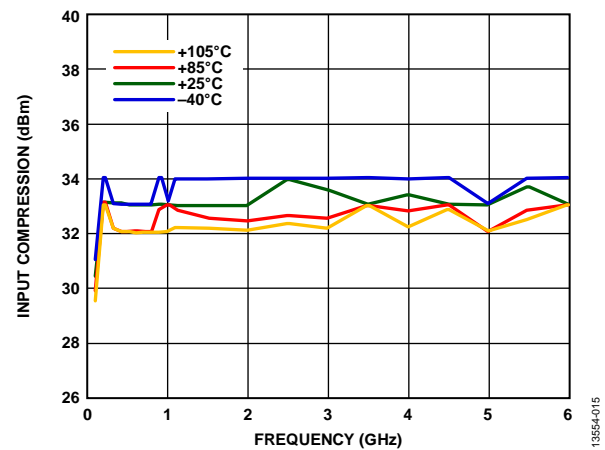
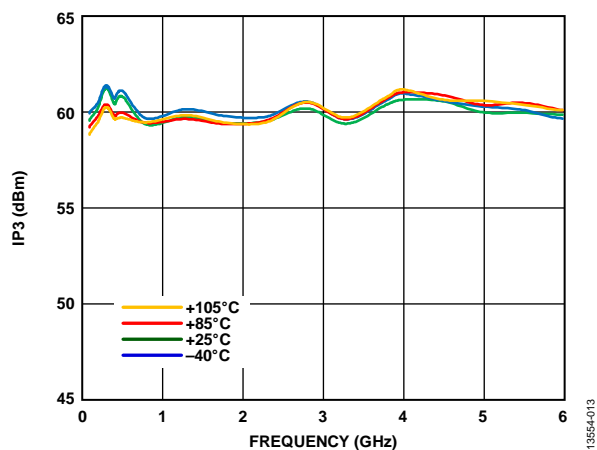
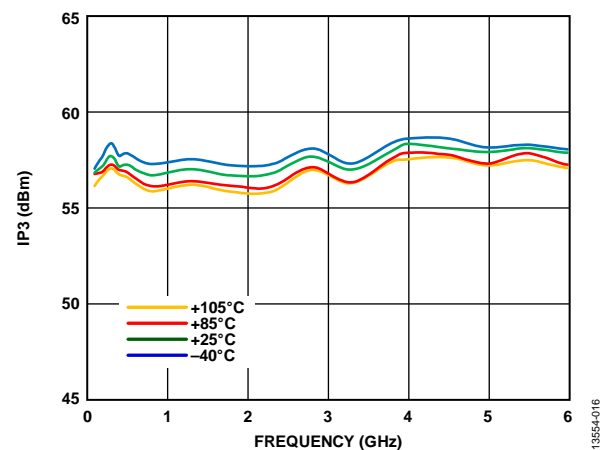
| Control Input | | Signal Path State | |
|------------------------|----------|-------------------|------------|
| V _{CTL} State | EN State | RFC to RF1 | RFC to RF2 |
| Low | Low | Off | On |
| High | Low | On | Off |
| Low | High | Off | Off |
| High | High | Off | Off |

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, ISOLATION, AND RETURN LOSS

Figure 6. Insertion Loss vs. Frequency over Temperatures, $V_{DD} = 5\text{ V}$ Figure 9. Insertion Loss vs. Frequency over Temperatures, $V_{DD} = 3.3\text{ V}$ Figure 7. Isolation Between RFC and RF1/RF2 vs. Frequency at $V_{DD} = 3.3\text{ V}$ to 5 V Figure 10. Isolation Between RF1 and RF2 vs. Frequency at $V_{DD} = 3.3\text{ V}$ to 5 V Figure 8. Return Loss vs. Frequency at $V_{DD} = 3.3\text{ V}$ to 5 V

INPUT COMPRESSION AND INPUT THIRD-ORDER INTERCEPT

Figure 11. Input Compression 1 dB Point vs. Frequency over Temperature, $V_{DD} = 5\text{ V}$ Figure 14. Input Compression 0.1 dB Point vs. Frequency over Temperature, $V_{DD} = 5\text{ V}$ Figure 12. Input Compression 1 dB Point vs. Frequency over Temperature, $V_{DD} = 3.3\text{ V}$ Figure 15. Input Compression 0.1 dB Point vs. Frequency over Temperature, $V_{DD} = 3.3\text{ V}$ Figure 13. Input Third-Order Intercept (IP3) Point vs. Frequency, $V_{DD} = 5\text{ V}$ Figure 16. Input Third-Order Intercept (IP3) Point vs. Frequency, $V_{DD} = 3.3\text{ V}$

THEORY OF OPERATION

The [HMC8038](#) requires a single-supply voltage applied to the V_{DD} pin. Bypassing capacitors are recommended on the supply line to minimize RF coupling.

The [HMC8038](#) is controlled via two digital control voltages applied to the V_{CTL} pin and the EN pin. A small bypassing capacitor is recommended on these digital signal lines to improve the RF signal isolation.

The [HMC8038](#) is internally matched to $50\ \Omega$ at the RF input port (RFC) and the RF output ports (RF1 and RF2); therefore, no external matching components are required. The RFx pins are dc-coupled, and dc blocking capacitors are required on the RF lines. The design is bidirectional; the input and outputs are interchangeable.

The ideal power-up sequence is as follows:

1. Power up GND.
2. Power up V_{DD} .
3. Power up the digital control inputs. The relative order of the logic control inputs are not important. Powering the digital control inputs before the V_{DD} supply can inadvertently forward bias and damage ESD protection structures.
4. Power up the RF input.

With the EN pin is logic low, the [HMC8038](#) has two operation modes: on and off. Depending on the logic level applied to the V_{CTL} pin, one RF output port (for example, RF1) is set to on mode, by which an insertion loss path is provided from the input to the output, as the other RF output port (for example, RF2) is set to off mode, by which the output is isolated from the input. When the RF output port (RF1 or RF2) is in isolation mode, internally terminate it to $50\ \Omega$, and the port absorbs the applied RF signal.

When the EN pin is logic high, the EN pin sets the [HMC8038](#) switch to off mode. In off mode, both output ports are isolated from the input, and the RFC port is open reflective.

Table 7. Switch Operation Mode

| Digital Control Inputs | | Switch Mode | |
|------------------------|----------------|--|--|
| V_{EN} | V_{CTL} | RFC to RF1 | RFC to RF2 |
| 0 | 0 | Off mode. The RF1 port is isolated from the RFC port and is internally terminated to a $50\ \Omega$ load to absorb the applied RF signals. | On mode. A low insertion loss path from the RFC port to the RF2 port. |
| 0 | 1 | On mode. A low insertion loss path from the RFC port to the RF1 port. | Off mode. The RF2 port is isolated from the RFC port and is internally terminated to a $50\ \Omega$ load to absorb the applied RF signals. |
| 1 | X ¹ | All in off mode. Both the RF1 and RF2 ports are isolated from the RFC port, and the RFC port is reflective. | |

¹ X stands for don't care.

APPLICATIONS INFORMATION

Generate the evaluation PCB used in the application shown in Figure 17 with proper RF circuit design techniques. Signal lines at the RF port must have a $50\ \Omega$ impedance, and the package ground leads and backside ground slug must connect directly to the ground plane, as shown in Figure 18. The evaluation board shown in Figure 18 is available from Analog Devices, Inc. upon request.

Table 8. Bill of Materials for Evaluation Board

EV1HMC8038LP4C¹

| Reference Designator | Description |
|----------------------|-------------------------------------|
| J1 to J3 | PCB mount SMA connector |
| C1 to C6 | 100 pF capacitor, 0402 package |
| C7 | 0.1 μ F capacitor, 0402 package |
| R1, R2 | 0 Ω resistor, 0402 package |
| U1 | HMC8038 SPDT switch |
| PCB ² | 600-01267-00 evaluation PCB |

¹ Reference to this evaluation board number when ordering the complete evaluation board.

² Circuit board material: Roger 4350 or Arlon 25FR.

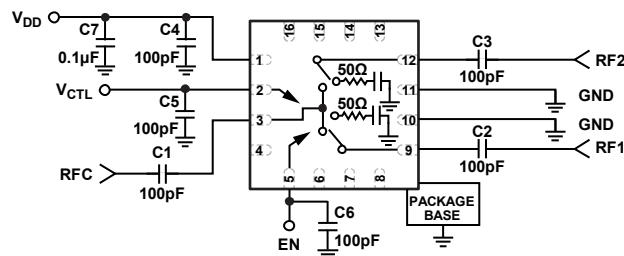


Figure 17. [HMC8038](#) Application Circuit

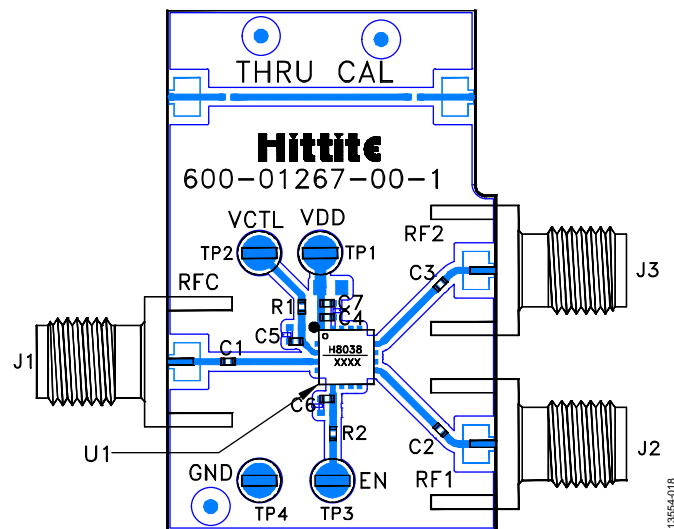
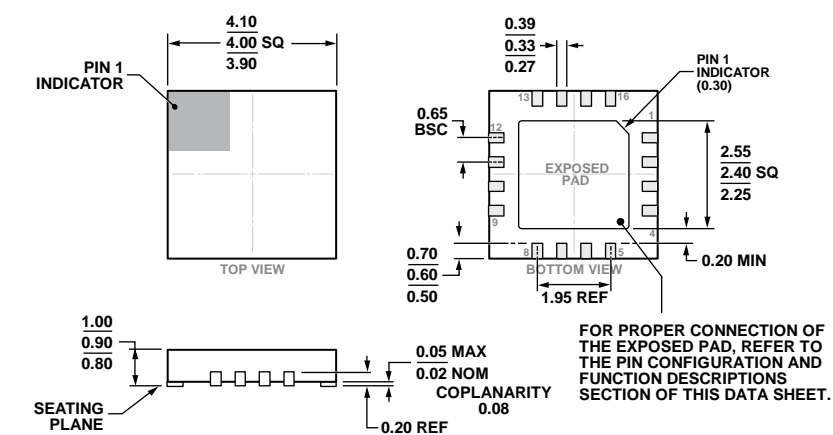


Figure 18. [EV1HMC8038LP4C](#) Evaluation Board

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 19. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.90 mm Package Height
(CP-16-40)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | MSL Rating ² | Package Description | Package Option | Branding ³ |
|--------------------|-------------------|-------------------------|---|----------------|-----------------------|
| HMC8038LP4CE | −40°C to +105°C | MSL3 | 16-lead Lead Frame Chip Scale Package [LFCSP] | CP-16-40 | 8038 XXXX |
| HMC8038LP4CETR | −40°C to +105°C | MSL3 | 16-lead Lead Frame Chip Scale Package [LFCSP] | CP-16-40 | 8038 XXXX |
| EV1HMC8038LP4C | −40°C to +105°C | | Evaluation Board | | |

¹ RoHS-Compliant Part.² The maximum peak reflow temperature is 260°C.³ 4-digit lot number: XXXX.