



December 2014

FODM8071

3.3V/5V Logic Gate Output Optocoupler with High Noise Immunity

Features

- High-noise Immunity Characterized by Common Mode Rejection
 - 20 kV/ μ s Minimum Common Mode Rejection
- High Speed
 - 20 Mbit/s Data Rate (NRZ)
 - 55 ns Maximum Propagation Delay
 - 20 ns Maximum Pulse Width Distortion
 - 30 ns Maximum Propagation Delay Skew
- 3.3 V and 5 V CMOS Compatibility
- Specifications Guaranteed Over 3 V to 5.5 V Supply Voltage and -40°C to +110°C Temperature Range
- Safety and Regulatory Approvals:
 - UL1577, 3750 VAC_{RMS} for 1 Minute
 - DIN EN/IEC60747-5-5

Applications

- Microprocessor System Interface:
 - SPI, I²C
- Industrial Fieldbus Communications:
 - DeviceNet, CAN, RS485
- Programmable Logic Control
- Isolated Data Acquisition System
- Voltage Level Translator

Description

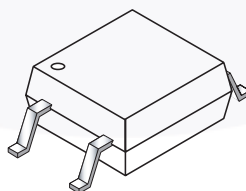
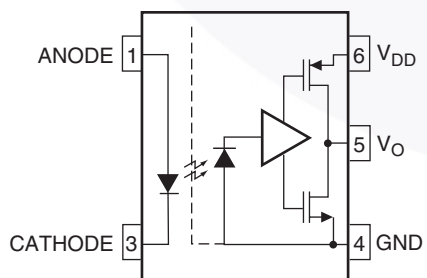
The FODM8071 is a 3.3V/5V high-speed logic gate output optocoupler, which supports isolated communications allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages. It utilizes Fairchild's patented coplanar packaging technology, Optoplanar[®], and optimized IC design to achieve high-immunity, characterized by high common mode rejection specifications.

This high-speed logic gate output optocoupler, housed in a compact 5-pin Mini-Flat package, consists of a high-speed AlGaAs LED at the input coupled to a CMOS detector IC at the output. The detector IC comprises an integrated photodiode, a high-speed transimpedance amplifier and a voltage comparator with an output driver. The CMOS technology coupled with a high-efficiency LED achieves low power consumption as well as very high speed (55 ns propagation delay, 20 ns pulse width distortion).

Related Resources

- [FOD8001 Product Folder](#)
- [FOD0721 Product Folder](#)

Schematic and Package Outline



Truth Table

LED	Output
Off	High
On	Low

Figure 1. Schematic and Package Outline

Safety and Insulation Ratings

As per DIN EN/IEC 60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Parameter		Characteristics
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	< 150 V _{RMS}	I–IV
	< 300 V _{RMS}	I–III
Climatic Classification		40/110/21
Pollution Degree (DIN VDE 0110/1.89)		2
Comparative Tracking Index		175

Symbol	Parameter	Value	Unit
V _{PR}	Input-to-Output Test Voltage, Method A, V _{IORM} × 1.6 = V _{PR} , Type and Sample Test with t _m = 10 s, Partial Discharge < 5 pC	904	V _{peak}
	Input-to-Output Test Voltage, Method B, V _{IORM} × 1.875 = V _{PR} , 100% Production Test with t _m = 1 s, Partial Discharge < 5 pC	1060	V _{peak}
V _{IORM}	Maximum Working Insulation Voltage	565	V _{peak}
V _{IOTM}	Highest Allowable Over-Voltage	4000	V _{peak}
	External Creepage	≥ 5	mm
	External Clearance	≥ 5	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥ 0.4	mm
T _S	Case Temperature ⁽¹⁾	150	°C
I _{S,INPUT}	Input Current ⁽¹⁾	200	mA
P _{S,OUTPUT}	Output Power ⁽¹⁾	300	mW
R _{IO}	Insulation Resistance at T _S , V _{IO} = 500 V ⁽¹⁾	> 10 ⁹	Ω

Note:

1. Safety limit values – maximum values allowed in the event of a failure.

Pin Definitions

Number	Name	Function Description
1	ANODE	Anode
3	CATHODE	Cathode
4	GND	Output Ground
5	V _O	Output Voltage
6	V _{DD}	Output Supply Voltage

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-40 to +125	°C
T _{OPR}	Operating Temperature	-40 to +110	°C
T _J	Junction Temperature	-40 to +125	°C
T _{SOL}	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10 seconds	°C
I _F	Forward Current	20	mA
V _R	Reverse Voltage	5	V
V _{DD}	Supply Voltage	0 to 6.0	V
V _O	Output Voltage	-0.5 to V _{DD} + 0.5	V
I _O	Average Output Current	10	mA
PD _I	Input Power Dissipation ⁽²⁾⁽⁴⁾	40	mW
PD _O	Output Power Dissipation ⁽³⁾⁽⁴⁾	70	mW

Notes:

- Derate linearly from 95°C at a rate of -1.4 mW/°C
- Derate linearly from 100°C at a rate of -3.47 mW/°C.
- Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T _A	Ambient Operating Temperature	-40	+110	°C
V _{DD}	Supply Voltages ⁽⁵⁾	3.0	5.5	V
V _{FL}	Logic Low Input Voltage	0	0.8	V
I _{FH}	Logic High Input Current	5	16	mA
I _{OL}	Logic Low Output Current	0	7	mA

Note:

- 0.1μF bypass capacitor must be connected between 4 and 6.

Electrical Characteristics

Apply over all recommended conditions. $T_A = -40^{\circ}\text{C}$ to $+110^{\circ}\text{C}$, $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, unless otherwise specified. Typical value is measured at $T_A = 25^{\circ}\text{C}$ and $V_{DD} = 3.3\text{ V}$.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INPUT CHARACTERISTICS						
V_F	Forward Voltage	$I_F = 10\text{ mA}$ (Figure 2)	1.05	1.35	1.8	V
BV_R	Input Reverse Breakdown Voltage	$I_R = 10\text{ }\mu\text{A}$	5	15		V
I_{FHL}	Threshold Input Current	(Figure 3)		2.8	5.0	mA
OUTPUT CHARACTERISTICS						
I_{DDL}	Logic Low Output Supply Current	$V_{DD} = 3.3\text{ V}$, $I_F = 10\text{ mA}$ (Figures 4 and 6)		3.3	4.8	mA
		$V_{DD} = 5.0\text{ V}$, $I_F = 10\text{ mA}$ (Figures 4 and 7)		4.0	5.0	mA
I_{DDH}	Logic High Output Supply Current	$V_{DD} = 3.3\text{ V}$, $I_F = 0\text{ mA}$ (Figure 5)		3.3	4.8	mA
		$V_{DD} = 5.0\text{ V}$, $I_F = 0\text{ mA}$ (Figure 5)		4.0	5.0	mA
V_{OH}	Logic High Output Voltage	$V_{DD} = 3.3\text{ V}$, $I_O = -20\text{ }\mu\text{A}$, $I_F = 0\text{ mA}$	$V_{DD} - 0.1\text{ V}$	3.3		V
		$V_{DD} = 3.3\text{ V}$, $I_O = -4\text{ mA}$, $I_F = 0\text{ mA}$	$V_{DD} - 0.5\text{ V}$	3.1		V
		$V_{DD} = 5.0\text{ V}$, $I_O = -20\text{ }\mu\text{A}$, $I_F = 0\text{ mA}$	$V_{DD} - 0.1\text{ V}$	5.0		V
		$V_{DD} = 5.0\text{ V}$, $I_O = -4\text{ mA}$, $I_F = 0\text{ mA}$	$V_{DD} - 0.5\text{ V}$	4.9		V
V_{OL}	Logic Low Output Voltage	$I_O = 20\text{ }\mu\text{A}$, $I_F = 10\text{ mA}$		0.0027	0.01	V
		$I_O = 4\text{ mA}$, $I_F = 10\text{ mA}$		0.27	0.80	V

Electrical Characteristics (Continued)

Apply over all recommended conditions. $T_A = -40^{\circ}\text{C}$ to $+110^{\circ}\text{C}$, $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, unless otherwise specified. Typical value is measured at $T_A = 25^{\circ}\text{C}$ and $V_{DD} = 3.3\text{ V}$.

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Date Rate ⁽⁶⁾					20	Mbps
t_{PW}	Pulse Width		50			ns
t_{PHL}	Propagation Delay Time to Logic Low Output	$C_L = 15\text{ pF}$ (Figures 8, 9, and 13)		31	55	ns
t_{PLH}	Propagation Delay Time to Logic High Output	$C_L = 15\text{ pF}$ (Figures 8, 9, and 13)		25	55	ns
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $	$C_L = 15\text{ pF}$ (Figures 10 and 11)		5.5	20	ns
t_{PSK}	Propagation Delay Skew	$C_L = 15\text{ pF}$ ⁽⁷⁾			30	ns
t_R	Output Rise Time (10% to 90%)	(Figure 12 and 13)		5.8		ns
t_F	Output Fall Time (90% to 10%)	(Figure 12 and 13)		5.3		ns
$ CM_H $	Common Mode Transient Immunity at Output High	$I_F = 0\text{ mA}$, $V_O > 0.8 V_{DD}$, $V_{CM} = 1000\text{ V}$, $T_A = 25^{\circ}\text{C}$, (Figure 14) ⁽⁸⁾	20	40		kV/ μs
$ CM_L $	Common Mode Transient Immunity at Output Low	$I_F = 5\text{ mA}$, $V_O < 0.8\text{ V}$, $V_{CM} = 1000\text{ V}$, $T_A = 25^{\circ}\text{C}$, (Figure 14) ⁽⁸⁾	20	40		kV/ μs
C_{PDO}	Output Dynamic Power Dissipation Capacitance ⁽⁹⁾			4		pF

Notes:

- Data rate is based on 10 MHz, 50% NRZ pattern with a 50 nsec minimum bit time.
- t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between any two units from the same manufacturing date code that are operated at same case temperature ($\pm 5^{\circ}\text{C}$), at the same operating conditions, with equal loads ($R_L = 350\ \Omega$ and $C_L = 15\text{ pF}$), and with an input rise time less than 5 ns.
- Common mode transient immunity at output high is the maximum tolerable positive dV_{cm}/dt on the leading edge of the common mode impulse signal, V_{cm} , to assure that the output will remain high. Common mode transient immunity at output low is the maximum tolerable negative dV_{cm}/dt on the trailing edge of the common pulse signal, V_{cm} , to assure that the output will remain low.
- Unloaded dynamic power dissipation is calculated as follows: $C_{PD} \times V_{DD} \times f + I_{DD} + V_{PD}$ where f is switched time in MHz.

Isolation Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{ISO}	Input-Output Isolation Voltage	$f = 60\text{ Hz}$, $t = 1.0\text{ minute}$, $I_{I-O} \leq 10\ \mu\text{A}$ ⁽¹⁰⁾⁽¹¹⁾	3750			V_{ACRMS}
R_{ISO}	Isolation Resistance	$V_{I-O} = 500\text{ V}$ ⁽¹⁰⁾	10^{11}			Ω
C_{ISO}	Isolation Capacitance	$V_{I-O} = 0\text{ V}$, $f = 1.0\text{ MHz}$ ⁽¹⁰⁾		0.2		pF

Notes:

- Device is considered a two terminal device: pins 1, and 3 are shorted together and pins 4, 5, and 6 are shorted together.
- 11.3,750 V_{ACRMS} for 1 minute duration is equivalent to 4,500 V_{ACRMS} for 1 second duration.

Typical Performance Curves

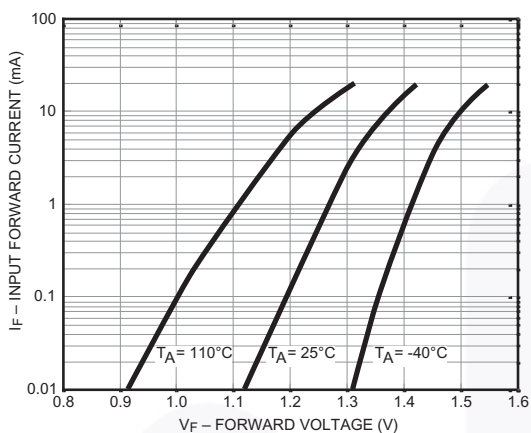


Figure 2. Input Forward Current vs. Forward Voltage

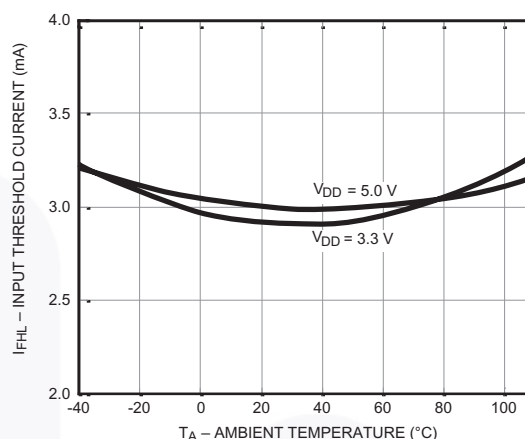


Figure 3. Input Threshold Current vs. Ambient Temperature

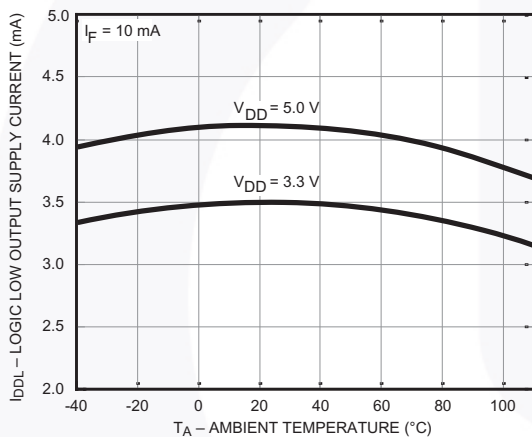


Figure 4. Logic Low Output Supply Current vs. Ambient Temperature

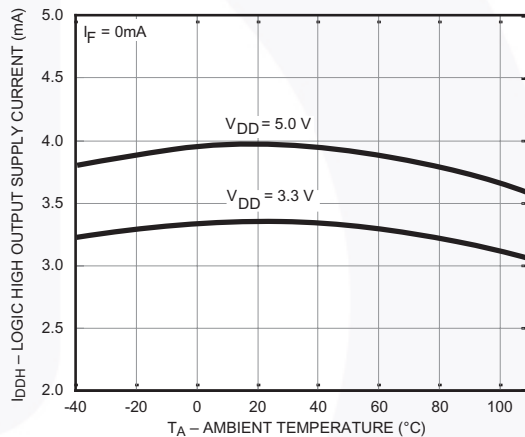


Figure 5. Logic High Output Supply Current vs. Ambient Temperature

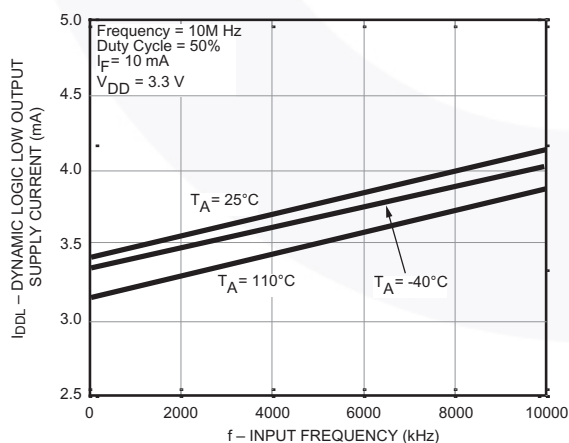


Figure 6. Dynamic Logic Low Output Supply Current vs. Input Frequency ($V_{DD} = 3.3V$)

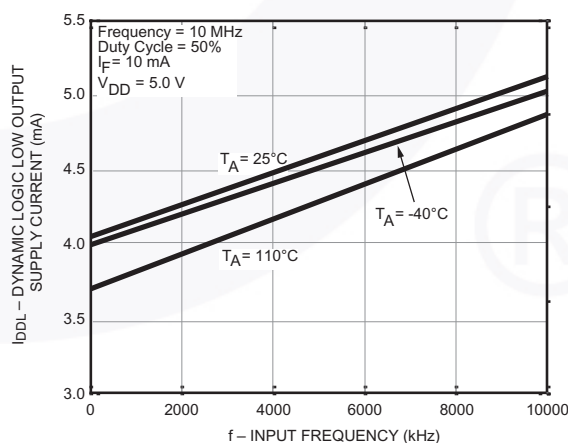


Figure 7. Dynamic Logic Low Output Supply Current vs. Input Frequency ($V_{DD} = 5.0V$)

Typical Performance Curves (Continued)

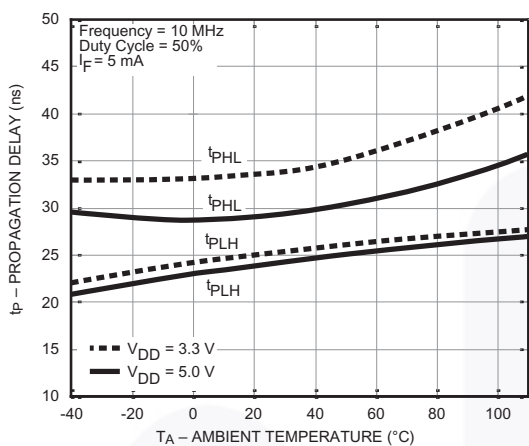


Figure 8. Propagation Delay vs. Ambient Temperature

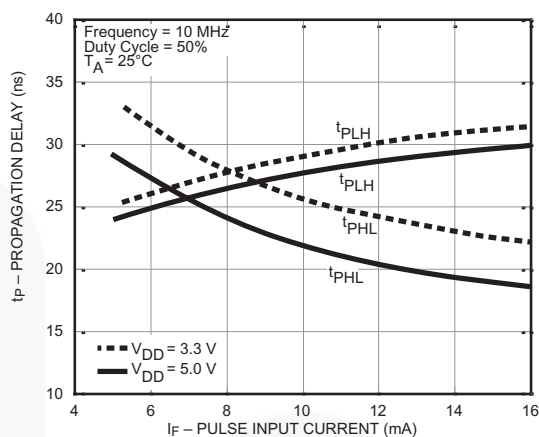


Figure 9. Propagation Delay vs. Pulse Input Current

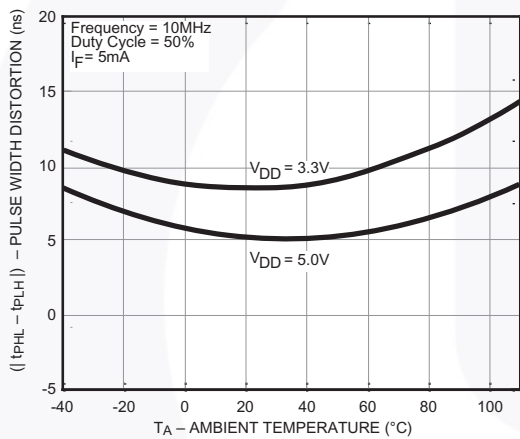


Figure 10. Pulse Width Distortion vs. Ambient Temperature

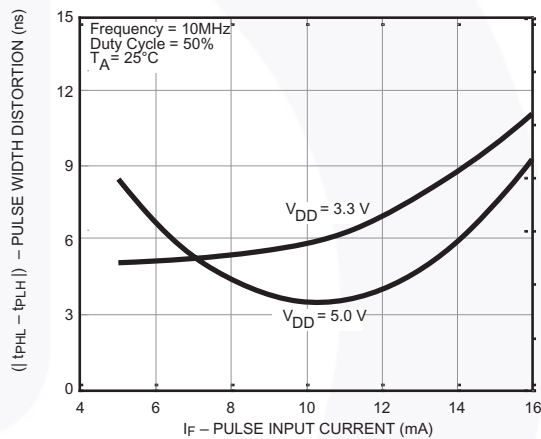


Figure 11. Pulse Width Distortion vs. Pulse Input Current

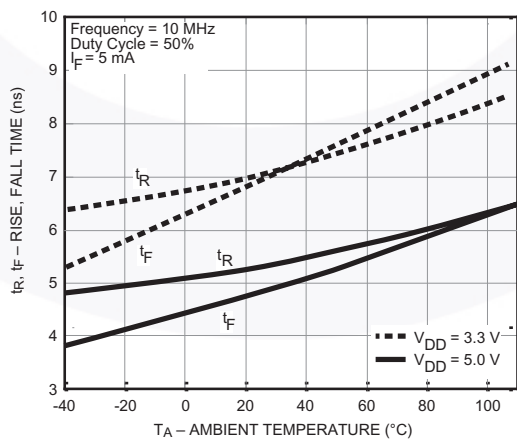


Figure 12. Rise and Fall Time vs. Ambient Temperature

Schematics

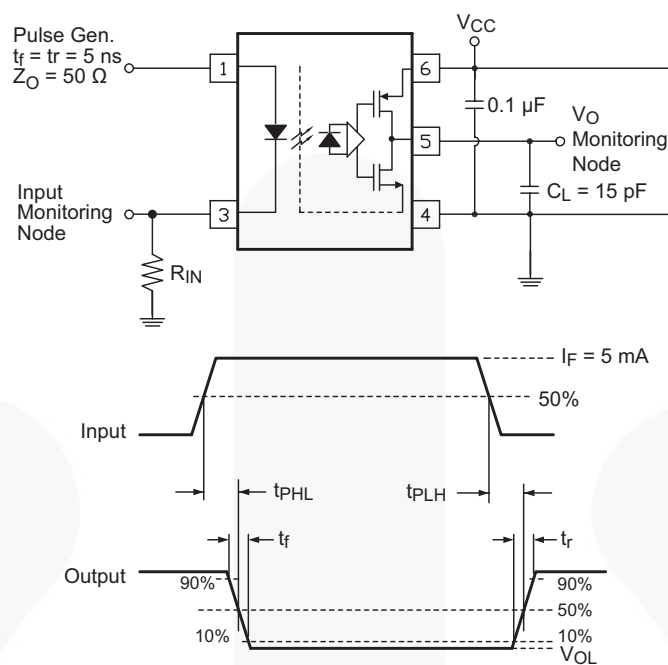


Figure 13. Test Circuit for Propagation Delay Time, Rise Time and Fall Time

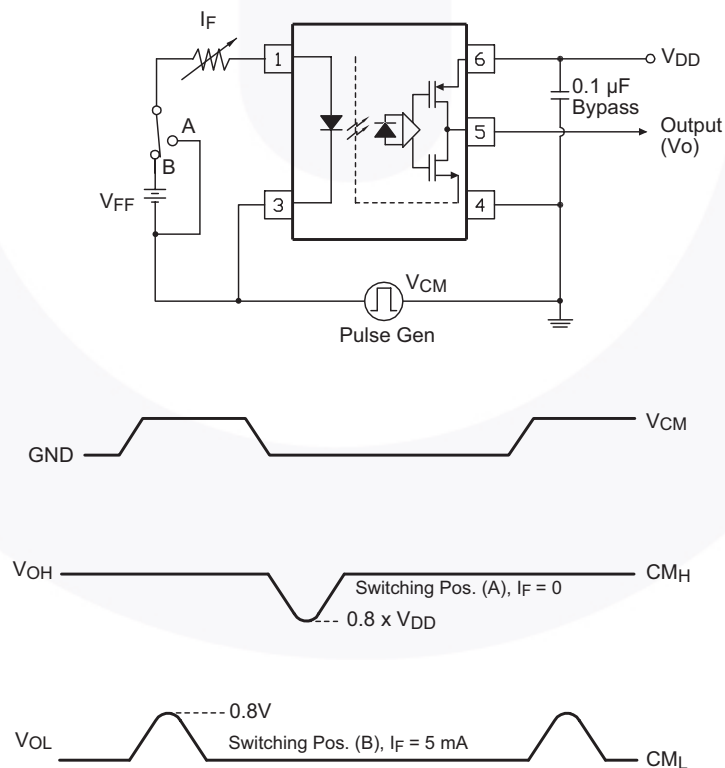


Figure 14. Test Circuit for Instantaneous Common Mode Rejection Voltage

Reflow Profile

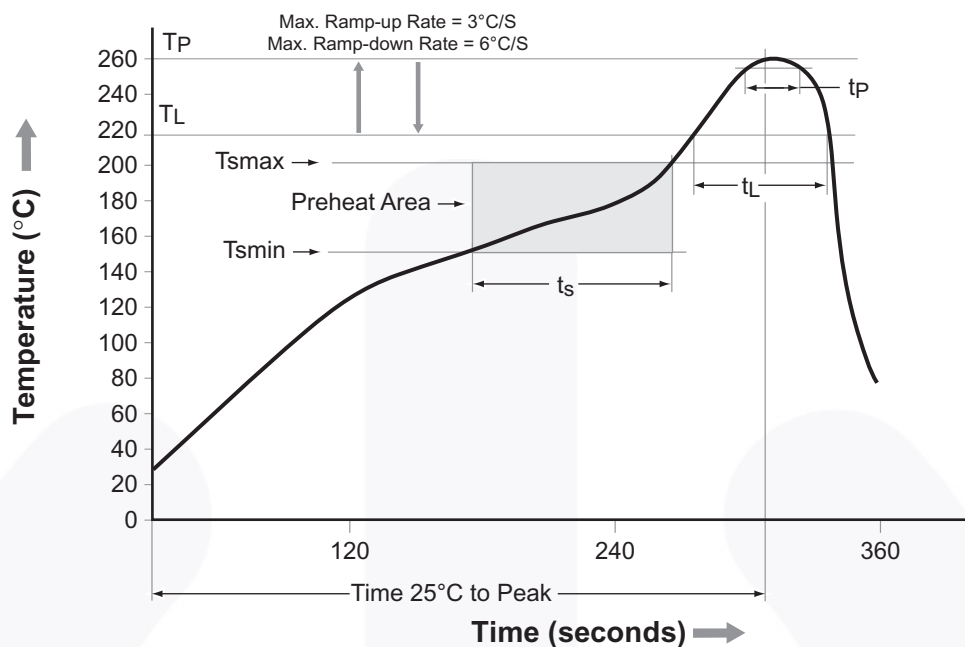



Figure 15. Reflow Profile

Profile Feature	Pb-Free Assembly Profile
Temperature Min. (T_{smin})	150°C
Temperature Max. (T_{smax})	200°C
Time (t_s) from (T_{smin} to T_{smax})	60–120 seconds
Ramp-up Rate (t_L to t_P)	3°C/second maximum
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp-down Rate (T_P to T_L)	6°C/second maximum
Time 25°C to Peak Temperature	8 minutes maximum

Ordering Information

Part Number	Package	Packing Method
FODM8071	Mini-Flat 5-Pin	Tube (100 Units)
FODM8071R2	Mini-Flat 5-Pin	Tape and Reel (2500 Units)
FODM8071V	Mini-Flat 5-Pin, DIN EN/IEC60747-5-5 Option	Tube (100 Units)
FODM8071R2V	Mini-Flat 5-Pin, DIN EN/IEC60747-5-5 Option	Tape and Reel (2500 Units)

 All packages are lead free per JEDEC: J-STD-020B standard.

Marking Information

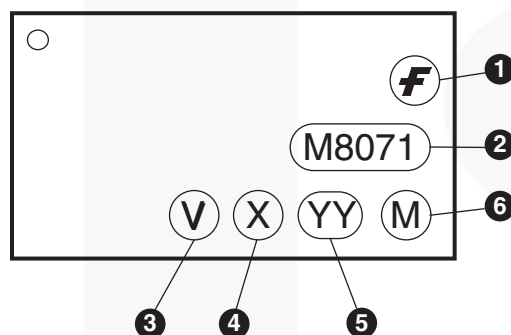


Figure 16. Top Mark

Table 1. Top Mark Definitions

1	Fairchild Logo
2	Device Number
3	DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option)
4	One-Digit Year Code, e.g., "4"
5	Digit Work Week, Ranging from "01" to "53"
6	Assembly Package Code

Package Dimensions

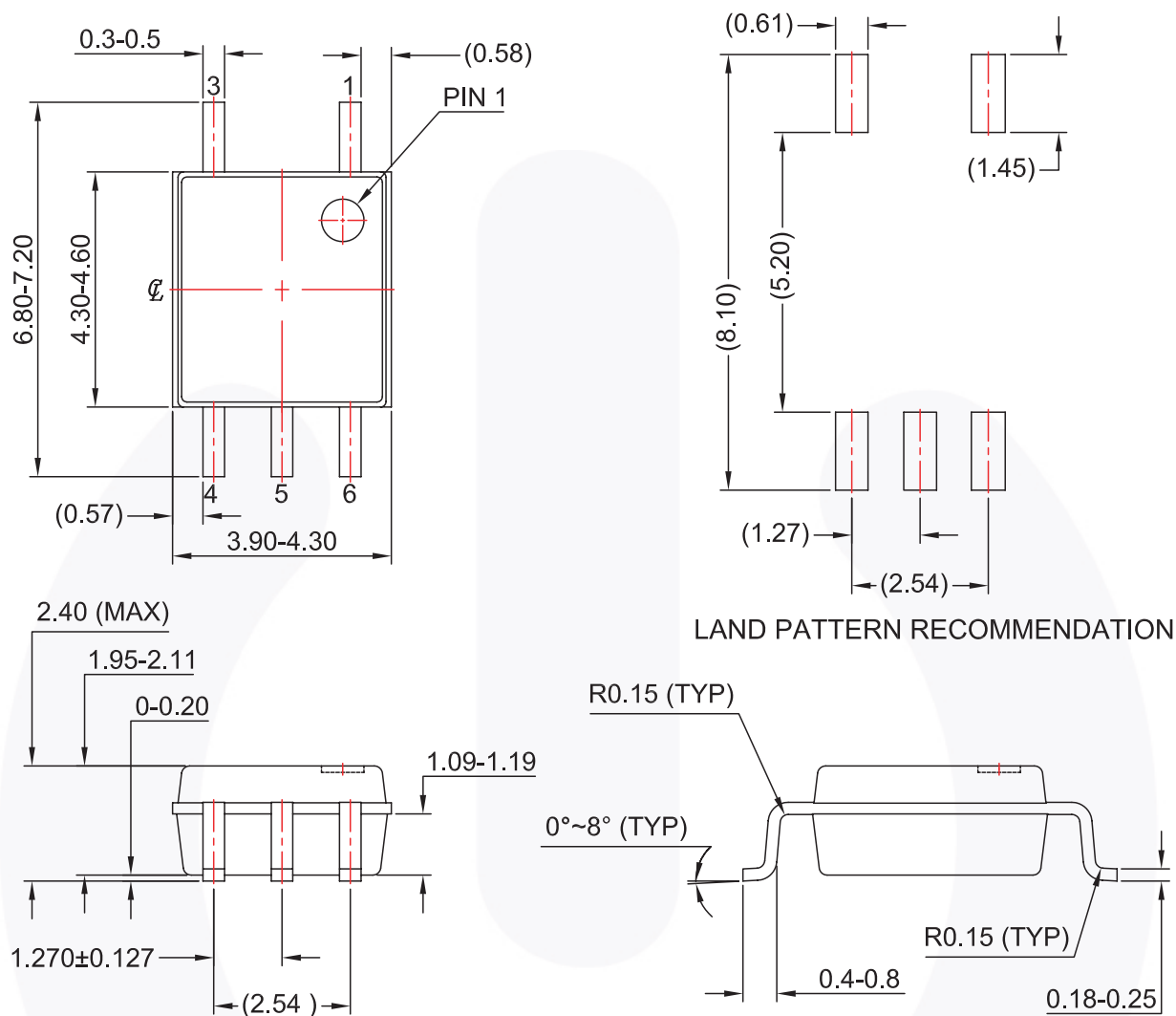


Figure 17. MLP 5L Package





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