

# 256-Kbit (32K × 8) F-RAM Memory

## Features

- 256-Kbit ferroelectric random access memory (F-RAM) logically organized as 32K × 8
  - High-endurance 100 trillion ( $10^{14}$ ) read/writes
  - 151-year data retention (see [Data Retention and Endurance](#) on page 8)
  - NoDelay™ writes
  - Page mode operation
  - Advanced high-reliability ferroelectric process
- SRAM compatible
  - Industry-standard 32K × 8 SRAM pinout
  - 70-ns access time, 140-ns cycle time
- Superior to battery-backed SRAM modules
  - No battery concerns
  - Monolithic reliability
  - True surface mount solution, no rework steps
  - Superior for moisture, shock, and vibration
  - Resistant to negative voltage undershoots
- Low power consumption
  - Active current 5 mA (typ)
  - Standby current 90 μA (typ)
- Low-voltage operation:  $V_{DD} = 2.0\text{ V to }3.6\text{ V}$
- Industrial temperature:  $-40\text{ °C to }+85\text{ °C}$

## Packages:

- 28-pin small outline integrated circuit (SOIC) package
- 28-pin thin small outline package (TSOP) Type I
- 32-pin thin small outline package (TSOP) Type I

## Restriction of hazardous substances (RoHS) compliant

## Functional Description

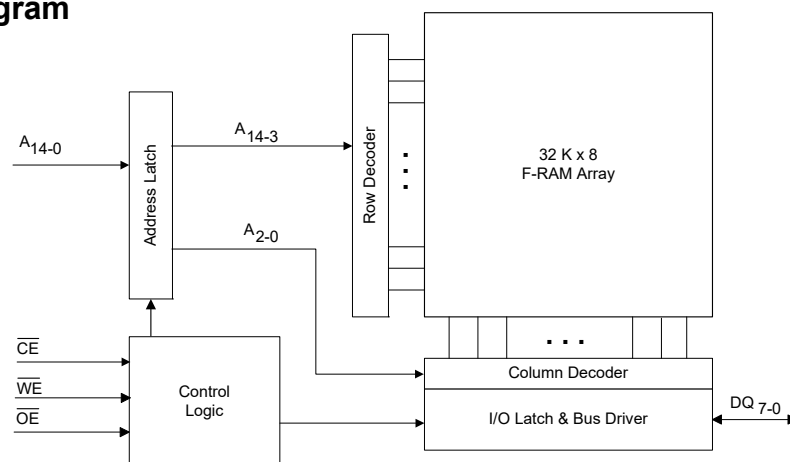
The FM28V020 is a 32K × 8 nonvolatile memory that reads and writes similar to a standard SRAM. A ferroelectric random access memory or F-RAM is nonvolatile, which means that data is retained after power is removed. It provides data retention for over 151 years while eliminating the reliability concerns, functional disadvantages, and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and high write endurance make the F-RAM superior to other types of memory.

The FM28V020 operation is similar to that of other RAM devices and therefore, it can be used as a drop-in replacement for a standard SRAM in a system. Read and write cycles may be triggered by CE or simply by changing the address. The F-RAM memory is nonvolatile due to its unique ferroelectric memory process. These features make the FM28V020 ideal for nonvolatile memory applications requiring frequent or rapid writes.

The device is available in a 28-pin SOIC, 28-pin TSOP I and 32-pin TSOP I surface mount packages. Device specifications are guaranteed over the industrial temperature range  $-40\text{ °C to }+85\text{ °C}$ .

For a complete list of related documentation, click [here](#).

## Logic Block Diagram

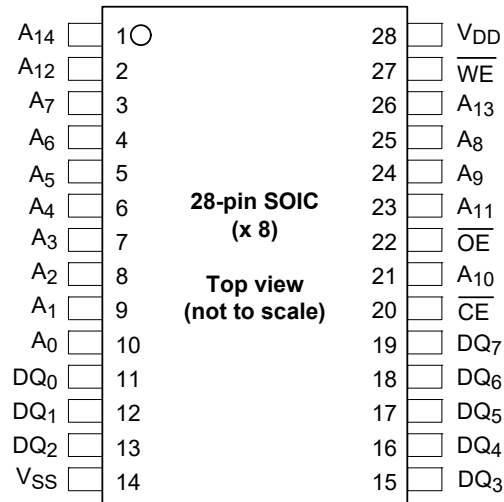


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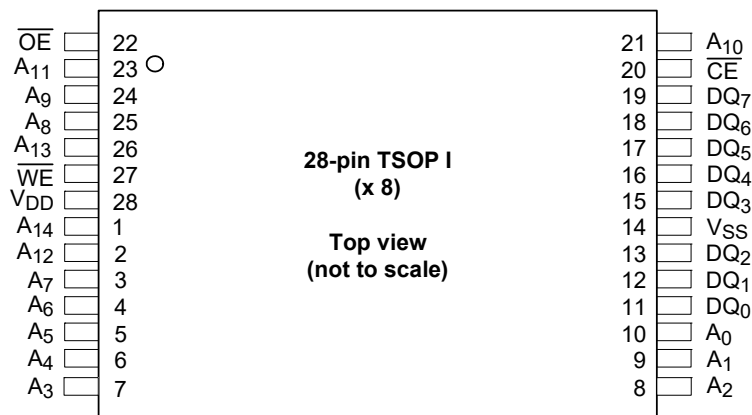
|                                            |          |                                                      |           |
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## Pinouts

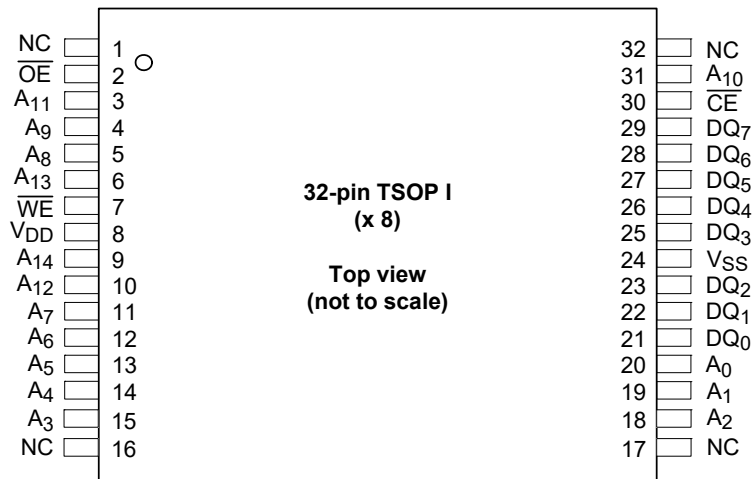
**Figure 1. 28-pin SOIC pinout**



**Figure 2. 28-pin TSOP I pinout**



**Figure 3. 32-pin TSOP I pinout**



## Pin Definitions

| Pin Name                         | I/O Type     | Description                                                                                                                                                                                                                                                                   |
|----------------------------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A <sub>14</sub> –A <sub>0</sub>  | Input        | <b>Address inputs:</b> The 15 address lines select one of 32,768 bytes in the F-RAM array. The lowest two address lines A <sub>2</sub> –A <sub>0</sub> may be used for page mode read and write operations.                                                                   |
| DQ <sub>7</sub> –DQ <sub>0</sub> | Input/Output | <b>Data I/O Lines:</b> 8-bit bidirectional data bus for accessing the F-RAM array.                                                                                                                                                                                            |
| $\overline{WE}$                  | Input        | <b>Write Enable:</b> A write cycle begins when $\overline{WE}$ is asserted. The rising edge causes the FM28V020 to write the data on the DQ bus to the F-RAM array. The falling edge of $\overline{WE}$ latches a new column address for page mode write cycles.              |
| $\overline{CE}$                  | Input        | <b>Chip Enable:</b> The device is selected and a new memory access begins on the falling edge of $\overline{CE}$ . The entire address is latched internally at this point. Subsequent changes to the A <sub>2</sub> –A <sub>0</sub> address inputs allow page mode operation. |
| $\overline{OE}$                  | Input        | <b>Output Enable:</b> When $\overline{OE}$ is LOW, the FM28V020 drives the data bus when the valid read data is available. Deasserting $\overline{OE}$ HIGH tristates the DQ pins.                                                                                            |
| V <sub>SS</sub>                  | Ground       | Ground for the device. Must be connected to the ground of the system.                                                                                                                                                                                                         |
| V <sub>DD</sub>                  | Power supply | Power supply input to the device.                                                                                                                                                                                                                                             |
| NC                               | No connect   | No connect. This pin is not connected to the die.                                                                                                                                                                                                                             |

## Device Operation

The FM28V020 is a byte-wide F-RAM memory logically organized as  $32,768 \times 8$  and accessed using an industry-standard parallel interface. All data written to the part is immediately nonvolatile with no delay. The device offers page mode operation, which provides high-speed access to addresses within a page (row). Access to a different page requires that either  $\overline{CE}$  transitions LOW or the upper address ( $A_{14}-A_3$ ) changes. See the [Functional Truth Table on page 14](#) for a complete description of read and write modes.

## Memory Operation

Users access 32,768 memory locations, each with 8 data bits through a parallel interface. The F-RAM array is organized as eight blocks, each having 512 rows. Each row has eight column locations, which allow fast access in page mode operation. When an initial address is latched by the falling edge of  $\overline{CE}$ , subsequent column locations may be accessed without the need to toggle  $\overline{CE}$ . When  $\overline{CE}$  is deasserted HIGH, a pre-charge operation begins. Writes occur immediately at the end of the access with no delay. The  $\overline{WE}$  pin must be toggled for each write operation. The write data is stored in the nonvolatile memory array immediately, which is a feature unique to F-RAM called NoDelay writes.

## Read Operation

A read operation begins on the falling edge of  $\overline{CE}$ . The falling edge of  $\overline{CE}$  causes the address to be latched and starts a memory read cycle if  $\overline{WE}$  is HIGH. Data becomes available on the bus after the access time is met. When the address is latched and the access completed, a new access to a random location (different row) may begin while  $\overline{CE}$  is still LOW. The minimum cycle time for random addresses is  $t_{RC}$ . Note that unlike SRAMs, the FM28V020's  $\overline{CE}$ -initiated access time is faster than the address access time.

The FM28V020 will drive the data bus when  $\overline{OE}$  is asserted LOW and the memory access time is met. If  $\overline{OE}$  is asserted after the memory access time is met, the data bus will be driven with valid data. If  $\overline{OE}$  is asserted before completing the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven to the bus. When  $\overline{OE}$  is deasserted HIGH, the data bus will remain in a HI-Z state.

## Write Operation

In the FM28V020, writes occur in the same interval as reads. The FM28V020 supports both  $\overline{CE}$  and  $\overline{WE}$  controlled write cycles. In both cases, the address is latched on the falling edge of  $\overline{CE}$ .

In a  $\overline{CE}$ -controlled write, the  $\overline{WE}$  signal is asserted before beginning the memory cycle. That is,  $\overline{WE}$  is LOW when the device is activated with the chip enable. In this case, the device begins the memory cycle as a write. The FM28V020 will not drive the data bus regardless of the state of  $\overline{OE}$  as long as  $\overline{WE}$  is LOW.

Input data must be valid when  $\overline{CE}$  is deasserted HIGH. In a  $\overline{WE}$ -controlled write, the memory cycle begins on the falling edge of  $\overline{CE}$ . The  $\overline{WE}$  signal falls some time later. Therefore, the memory cycle begins as a read. The data bus will be driven if  $\overline{OE}$  is LOW; however, it will be HI-Z when  $\overline{WE}$  is asserted LOW. The  $\overline{CE}$  and  $\overline{WE}$  controlled write timing cases are shown on the [Figure 9 on page 12](#). In [Figure 10 on page 12](#), the data bus is shown as a hi-Z condition while the chip is write-enabled and before the required setup time. Although this is drawn to look like a mid-level voltage, it is recommended that all DQ pins comply with the minimum  $V_{IH}/V_{IL}$  operating levels.

Write access to the array begins on the falling edge of  $\overline{WE}$  after the memory cycle is initiated. The write access terminates on the rising edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever comes first. A valid write operation requires the user to meet the access time specification before deasserting  $\overline{WE}$  or  $\overline{CE}$ . The data setup time indicates the interval during which data cannot change before the end of the write access (rising edge of  $\overline{WE}$  or  $\overline{CE}$ ).

Unlike other nonvolatile memory technologies, there is no write delay with F-RAM. Because the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

## Page Mode Operation

The FM28V020 provides the user fast access to any data within a row element. Each row has eight column-address locations. Address inputs  $A_2-A_0$  define the column address to be accessed. An access can start anywhere within a row and other column locations may be accessed without the need to toggle the  $\overline{CE}$  pin. For fast access reads, after the first data byte is driven to the bus, the column address inputs  $A_2-A_0$  may be changed to a new value. A new data byte is then driven to the DQ pins. For fast access writes, the first write pulse defines the first write access. While  $\overline{CE}$  is LOW, a subsequent write pulse along with a new column address provides a page mode write access.

## Pre-charge Operation

The pre-charge operation is an internal condition in which the memory state is prepared for a new access. Pre-charge is user-initiated by driving the  $\overline{CE}$  signal HIGH. It must remain HIGH for at least the minimum pre-charge time,  $t_{PC}$ .

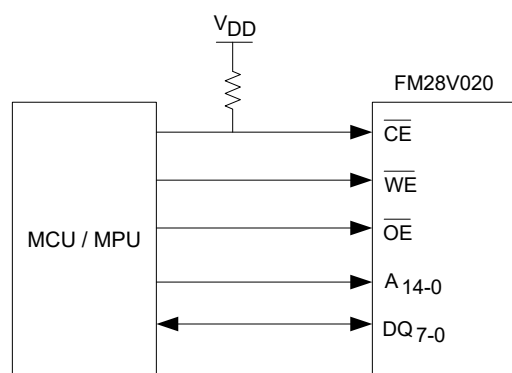
Pre-charge is also activated by changing the upper addresses,  $A_{14}-A_3$ . The current row is first closed before accessing the new row. The device automatically detects an upper order address change, which starts a pre-charge operation. The new address is latched and the new read data is valid within the  $t_{AA}$  address access time; see [Figure 6 on page 11](#). A similar sequence occurs for write cycles; see [Figure 11 on page 12](#). The rate at which random addresses can be issued is  $t_{RC}$  and  $t_{WC}$ , respectively.

## SRAM Drop-In Replacement

The FM28V020 is designed to be a drop-in replacement for standard asynchronous SRAMs. The device does not require  $\overline{CE}$  to toggle for each new address.  $\overline{CE}$  may remain LOW indefinitely while  $V_{DD}$  is applied. While  $\overline{CE}$  is LOW, the device automatically detects address changes and a new access begins. It also allows page mode operation at speeds up to 15 MHz.

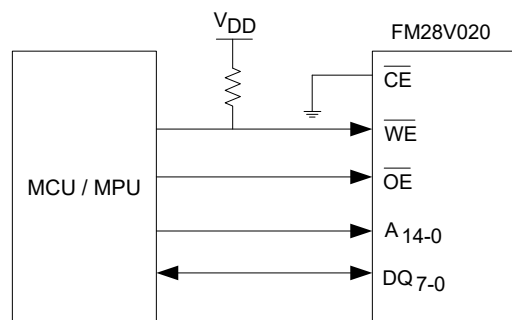
A typical application is shown in Figure 4. It shows a pull-up resistor on  $\overline{CE}$ , which will keep the pin HIGH during power cycles, assuming the MCU / MPU pin tristates during the reset condition. The pull-up resistor value should be chosen to ensure the  $\overline{CE}$  pin tracks  $V_{DD}$  to a high enough value, so that the current drawn when  $\overline{CE}$  is LOW is not an issue. A 10-k $\Omega$  resistor draws 330  $\mu$ A when  $\overline{CE}$  is LOW and  $V_{DD} = 3.3$  V.

**Figure 4. Use of Pull-up Resistor on  $\overline{CE}$**



Note that if  $\overline{CE}$  is tied to ground, the user must be sure  $\overline{WE}$  is not LOW at power-up or power-down events. If  $\overline{CE}$  and  $\overline{WE}$  are both LOW during power cycles, data will be corrupted. Figure 5 shows a pull-up resistor on  $\overline{WE}$ , which will keep the pin HIGH during power cycles, assuming the MCU/MPU pin tristates during the reset condition. The pull-up resistor value should be chosen to ensure the  $\overline{WE}$  pin tracks  $V_{DD}$  to a high enough value, so that the current drawn when  $\overline{WE}$  is LOW is not an issue. A 10-k $\Omega$  resistor draws 330  $\mu$ A when  $\overline{WE}$  is LOW and  $V_{DD} = 3.3$  V.

**Figure 5. Use of Pull-up Resistor on  $\overline{WE}$**



For applications that require the lowest power consumption, the  $\overline{CE}$  signal should be active only during memory accesses. Due to the external pull-up resistor, some supply current will be drawn while  $\overline{CE}$  is LOW. When  $\overline{CE}$  is HIGH, the device draws no more than the maximum standby current  $I_{SB}$ .

$\overline{CE}$  toggling LOW on every address access is perfectly acceptable in FM28V020.

## Endurance

The FM28V020 is capable of being accessed at least  $10^{14}$  times – reads or writes. An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis. The F-RAM architecture is based on an array of rows and columns. Rows are defined by  $A_{14-3}$  and column addresses by  $A_2-A_0$ . The array is organized as 4K rows of eight bytes each. The entire row is internally accessed once whether a single byte or all eight bytes are read or written. Each byte in the row is counted only once in an endurance calculation if the addressing is contiguous in nature.

The user may choose to write CPU instructions and run them from a certain address space. Table 1 shows endurance calculations for a 256-byte repeating loop, which includes a starting address, seven-page mode accesses, and a  $\overline{CE}$  pre-charge. The number of bus clock cycles needed to complete a eight-byte read transaction is 1 + 7 + 1 or 9 clocks. The entire loop causes each byte to experience only one endurance cycle. The F-RAM read and write endurance is virtually unlimited.

**Table 1. Time to Reach 100 Trillion Cycles for Repeating 256-byte Loop**

| Bus Freq (MHz) | Bus Cycle Time (ns) | 256-byte Transaction Time ( $\mu$ s) | Endurance Cycles/sec | Endurance Cycles/yr   | Years to Reach $10^{14}$ Cycles |
|----------------|---------------------|--------------------------------------|----------------------|-----------------------|---------------------------------|
| 10             | 100                 | 28.8                                 | 34,720               | $1.09 \times 10^{12}$ | 91.7                            |
| 5              | 200                 | 57.6                                 | 17,360               | $5.47 \times 10^{11}$ | 182.8                           |

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +125 °C

Maximum accumulated storage time

At 125 °C ambient temperature ..... 1000 h

At 85 °C ambient temperature ..... 10 Years

Ambient temperature

with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{DD}$  relative to  $V_{SS}$  ..... -1.0 V to + 4.5 V

Voltage applied to outputs

in High Z state ..... -0.5 V to  $V_{DD} + 0.5$  V

Input voltage ..... -1.0 V to + 4.5 V and  $V_{IN} < V_{DD} + 1.0$  V

Transient voltage (< 20 ns)

on any pin to ground potential ..... -2.0 V to  $V_{CC} + 2.0$  V

Package power dissipation capability

( $T_A = 25$  °C) ..... 1.0 W

Surface mount Pb soldering temperature

(3 seconds) ..... +260 °C

DC output current

(1 output at a time, 1s duration) ..... 15 mA

Static discharge voltage

Human Body Model (AEC-Q100-002 Rev. E) ..... 2 kV

Charged Device Model (AEC-Q100-011 Rev. B) .. 1.25 kV

Machine Model (AEC-Q100-003 Rev. E) ..... 200 V

Latch-up current ..... > 140 mA

## Operating Range

| Range      | Ambient Temperature ( $T_A$ ) | $V_{DD}$       |
|------------|-------------------------------|----------------|
| Industrial | -40 °C to +85 °C              | 2.0 V to 3.6 V |

## DC Electrical Characteristics

Over the [Operating Range](#)

| Parameter | Description             | Test Conditions                                                                                                                                     | Min                 | Typ <sup>[1]</sup> | Max                 | Unit |
|-----------|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|--------------------|---------------------|------|
| $V_{DD}$  | Power supply voltage    |                                                                                                                                                     | 2.0                 | 3.3                | 3.6                 | V    |
| $I_{DD}$  | $V_{DD}$ supply current | $V_{DD} = 3.6$ V, $\overline{CE}$ cycling at min. cycle time. All inputs toggling at CMOS levels (0.2 V or $V_{DD} - 0.2$ V), all DQ pins unloaded. | –                   | 5                  | 8                   | mA   |
| $I_{SB}$  | Standby current         | $V_{DD} = 3.6$ V, $\overline{CE}$ at $V_{DD}$ , All other pins are static and at CMOS levels (0.2 V or $V_{DD} - 0.2$ V)                            | –                   | 90                 | 150                 | μA   |
| $I_{LI}$  | Input leakage current   | $V_{IN}$ between $V_{DD}$ and $V_{SS}$                                                                                                              | –                   | –                  | ±1                  | μA   |
| $I_{LO}$  | Output leakage current  | $V_{OUT}$ between $V_{DD}$ and $V_{SS}$                                                                                                             | –                   | –                  | ±1                  | μA   |
| $V_{IH}$  | Input HIGH voltage      |                                                                                                                                                     | $0.7 \times V_{DD}$ | –                  | $V_{DD} + 0.3$      | V    |
| $V_{IL}$  | Input LOW voltage       |                                                                                                                                                     | – 0.3               | –                  | $0.3 \times V_{DD}$ | V    |
| $V_{OH1}$ | Output HIGH voltage     | $I_{OH} = -1.0$ mA, $V_{DD} > 2.7$ V                                                                                                                | 2.4                 | –                  | –                   | V    |
| $V_{OH2}$ | Output HIGH voltage     | $I_{OH} = -100$ μA                                                                                                                                  | $V_{DD} - 0.2$      | –                  | –                   | V    |
| $V_{OL1}$ | Output LOW voltage      | $I_{OL} = 1$ mA, $V_{DD} > 2.7$ V                                                                                                                   | –                   | –                  | 0.4                 | V    |
| $V_{OL2}$ | Output LOW voltage      | $I_{OL} = 150$ μA                                                                                                                                   | –                   | –                  | 0.2                 | V    |

### Note

1. Typical values are at 25 °C,  $V_{DD} = V_{DD}(typ)$ . Not 100% tested.

## Data Retention and Endurance

| Parameter       | Description    | Test condition             | Min              | Max | Unit   |
|-----------------|----------------|----------------------------|------------------|-----|--------|
| T <sub>DR</sub> | Data retention | At +85 °C                  | 10               | –   | Years  |
|                 |                | At +75 °C                  | 38               | –   |        |
|                 |                | At +65 °C                  | 151              | –   |        |
| NV <sub>C</sub> | Endurance      | Over operating temperature | 10 <sup>14</sup> | –   | Cycles |

## Capacitance

| Parameter        | Description                   | Test Conditions                                                            | Max | Unit |
|------------------|-------------------------------|----------------------------------------------------------------------------|-----|------|
| C <sub>I/O</sub> | Input/Output capacitance (DQ) | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>DD</sub> = V <sub>DD</sub> (Typ) | 8   | pF   |
| C <sub>IN</sub>  | Input capacitance             |                                                                            | 6   | pF   |

## Thermal Resistance

| Parameter       | Description                              | Test Conditions                                                                                                             | 28-pin SOIC | 28-pin TSOP I | 32-pin TSOP I | Unit |
|-----------------|------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|-------------|---------------|---------------|------|
| Θ <sub>JA</sub> | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 59          | 108           | 84            | °C/W |
| Θ <sub>JC</sub> | Thermal resistance (junction to case)    |                                                                                                                             | 30          | 29            | 26            | °C/W |

## AC Test Conditions

Input pulse levels ..... 0 V to 3 V

Input rise and fall times (10%–90%) ..... ≤ 3 ns

Input and output timing reference levels ..... 1.5 V

Output load capacitance ..... 30 pF

## AC Switching Characteristics

Over the [Operating Range](#)

| Parameters <sup>[2]</sup>          |                   | Description                                            | Min | Max | Unit |
|------------------------------------|-------------------|--------------------------------------------------------|-----|-----|------|
| Cypress Parameter                  | Alt Parameter     |                                                        |     |     |      |
| SRAM Read Cycle                    |                   |                                                        |     |     |      |
| t <sub>CE</sub>                    | t <sub>ACE</sub>  | Chip enable access time                                | –   | 70  | ns   |
| t <sub>RC</sub>                    | –                 | Read cycle time                                        | 140 | –   | ns   |
| t <sub>AA</sub>                    | –                 | Address access time                                    | –   | 140 | ns   |
| t <sub>OH</sub>                    | t <sub>OHA</sub>  | Output hold time                                       | 20  | –   | ns   |
| t <sub>AAP</sub>                   | –                 | Page mode address access time                          | –   | 40  | ns   |
| t <sub>OHP</sub>                   | –                 | Page mode output hold time                             | 3   | –   | ns   |
| t <sub>CA</sub>                    | –                 | Chip enable active time                                | 70  | –   | ns   |
| t <sub>PC</sub>                    | –                 | Pre-charge time                                        | 70  | –   | ns   |
| t <sub>AS</sub>                    | t <sub>SA</sub>   | Address setup time (to $\overline{\text{CE}}$ LOW)     | 0   | –   | ns   |
| t <sub>AH</sub>                    | t <sub>HA</sub>   | Address hold time ( $\overline{\text{CE}}$ Controlled) | 70  | –   | ns   |
| t <sub>OE</sub> <sup>[3]</sup>     | t <sub>DOE</sub>  | Output enable access time                              | –   | 20  | ns   |
| t <sub>HZ</sub> <sup>[4, 5]</sup>  | t <sub>HZCE</sub> | Chip Enable to output HI-Z                             | –   | 10  | ns   |
| t <sub>OHZ</sub> <sup>[4, 5]</sup> | t <sub>HZOE</sub> | Output enable HIGH to output HI-Z                      | –   | 10  | ns   |

### Notes

- Test conditions assume a signal transition time of 3 ns or less, timing reference levels of  $0.5 \times V_{DD}$ , input pulse levels of 0 to 3 V, output loading of the specified  $I_{OL}/I_{OH}$  and load capacitance shown in [AC Test Conditions on page 8](#).
- For  $V_{DD} < 2.7$  V,  $t_{OE}$  max is 25 ns.
- $t_{HZ}$  and  $t_{OHZ}$  are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
- This parameter is characterized but not 100% tested.

## AC Switching Characteristics (continued)

Over the [Operating Range](#)

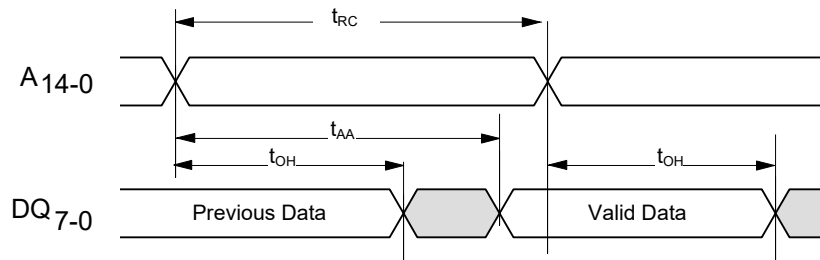
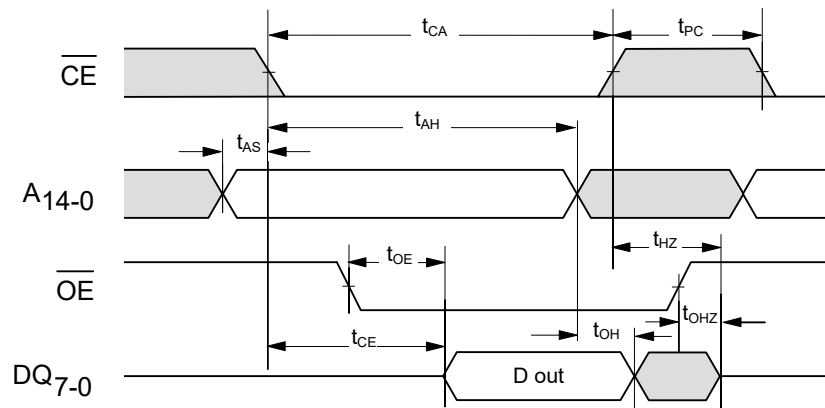
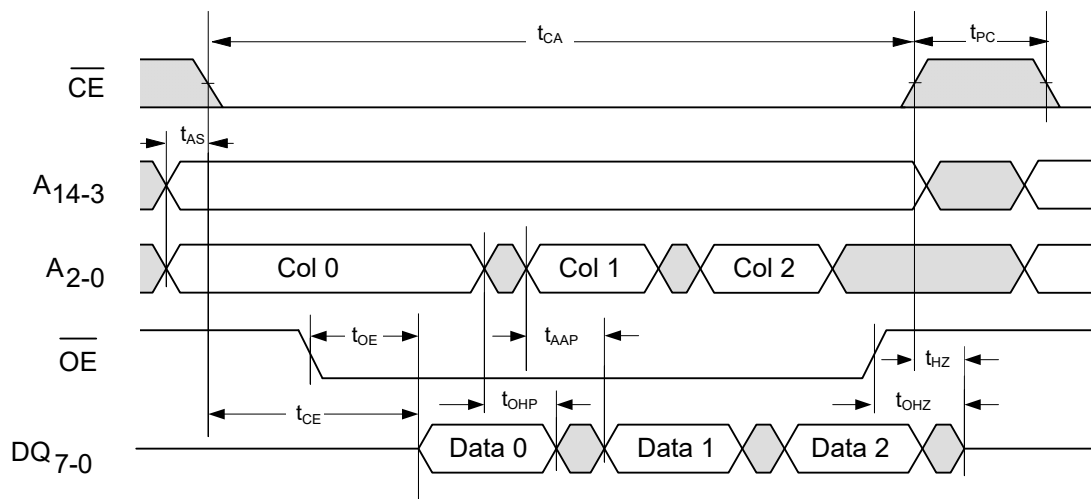
| Parameters <sup>[2]</sup>         |                   | Description                                           | Min | Max | Unit |
|-----------------------------------|-------------------|-------------------------------------------------------|-----|-----|------|
| Cypress Parameter                 | Alt Parameter     |                                                       |     |     |      |
| SRAM Write Cycle                  |                   |                                                       |     |     |      |
| t <sub>WC</sub>                   | t <sub>WC</sub>   | Write cycle time                                      | 140 | –   | ns   |
| t <sub>CA</sub>                   | –                 | Chip enable active time                               | 70  | –   | ns   |
| t <sub>CW</sub>                   | t <sub>SCE</sub>  | Chip enable to write enable HIGH                      | 70  | –   | ns   |
| t <sub>PC</sub>                   | –                 | Pre-charge time                                       | 70  | –   | ns   |
| t <sub>PWC</sub>                  | –                 | Page mode write enable cycle time                     | 35  | –   | ns   |
| t <sub>WP</sub>                   | t <sub>PWE</sub>  | Write enable pulse width                              | 18  | –   | ns   |
| t <sub>AS</sub>                   | t <sub>SA</sub>   | Address setup time (to $\overline{CE}$ LOW)           | 0   | –   | ns   |
| t <sub>AH</sub>                   | t <sub>HA</sub>   | Address hold time ( $\overline{CE}$ Controlled)       | 70  | –   | ns   |
| t <sub>ASP</sub>                  | –                 | Page mode address setup time (to $\overline{WE}$ LOW) | 5   | –   | ns   |
| t <sub>AHP</sub>                  | –                 | Page mode address hold time (to $\overline{WE}$ LOW)  | 20  | –   | ns   |
| t <sub>WLC</sub>                  | t <sub>PWE</sub>  | Write enable LOW to chip disabled                     | 25  | –   | ns   |
| t <sub>WLA</sub>                  | –                 | Write enable LOW to A <sub>14-3</sub> change          | 25  | –   | ns   |
| t <sub>AWH</sub>                  | –                 | A <sub>14-3</sub> change to write enable HIGH         | 140 | –   | ns   |
| t <sub>DS</sub>                   | t <sub>SD</sub>   | Data input setup time                                 | 15  | –   | ns   |
| t <sub>DH</sub>                   | t <sub>HD</sub>   | Data input hold time                                  | 0   | –   | ns   |
| t <sub>WZ</sub> <sup>[6, 7]</sup> | t <sub>HZWE</sub> | Write enable LOW to output HI-Z                       | –   | 10  | ns   |
| t <sub>WX</sub> <sup>[7]</sup>    | –                 | Write enable HIGH to output driven                    | 5   | –   | ns   |
| t <sub>WS</sub> <sup>[7, 8]</sup> | –                 | Write enable to $\overline{CE}$ LOW setup time        | 0   | –   | ns   |
| t <sub>WH</sub> <sup>[7, 8]</sup> | –                 | Write enable to $\overline{CE}$ HIGH hold time        | 0   | –   | ns   |

### Notes

6.  $t_{WZ}$  is specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.

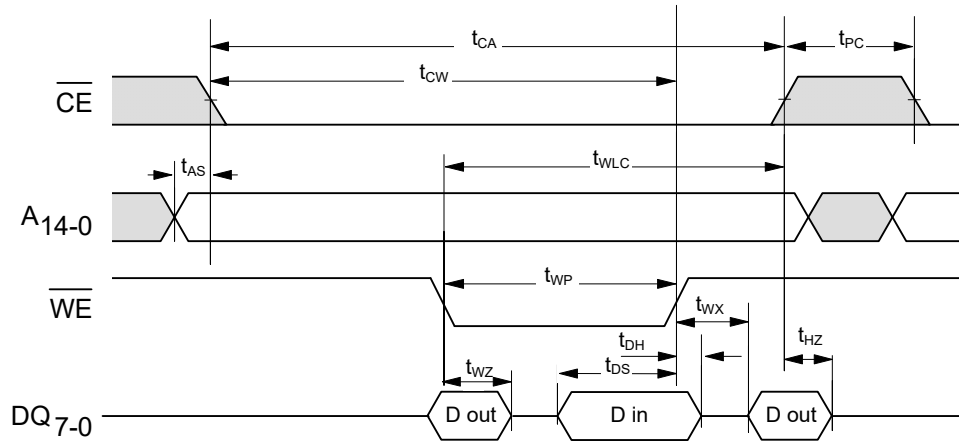
7. This parameter is characterized but not 100% tested.

8. The relationship between  $\overline{CE}$  and  $\overline{WE}$  determines if a  $\overline{CE}$  or  $\overline{WE}$  controlled write occurs.

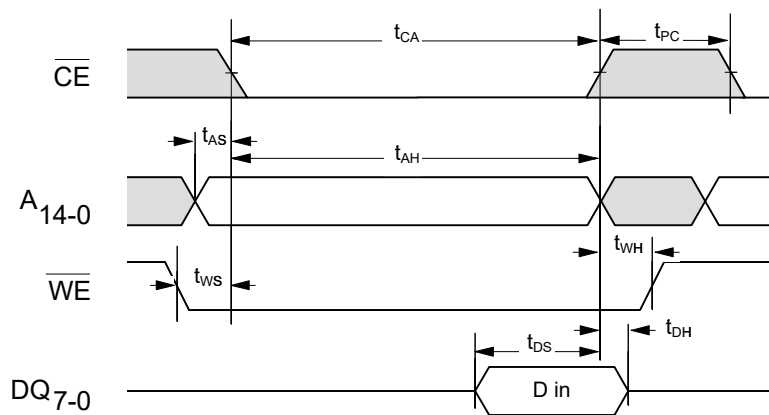
**Figure 6. Read Cycle Timing 1 ( $\overline{CE}$  LOW,  $\overline{OE}$  LOW)**

**Figure 7. Read Cycle Timing 2 ( $\overline{CE}$  Controlled)**

**Figure 8. Page Mode Read Cycle Timing <sup>[9]</sup>**

**Note**

9. Although sequential column addressing is shown, it is not required.

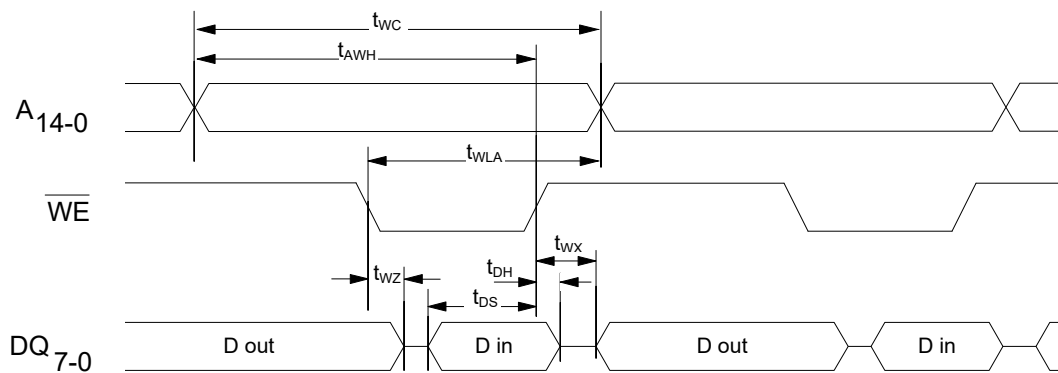
**Figure 9. Write Cycle Timing 1 ( $\overline{\text{WE}}$  Controlled) <sup>[10]</sup>**



**Figure 10. Write Cycle Timing 2 ( $\overline{\text{CE}}$  Controlled)**

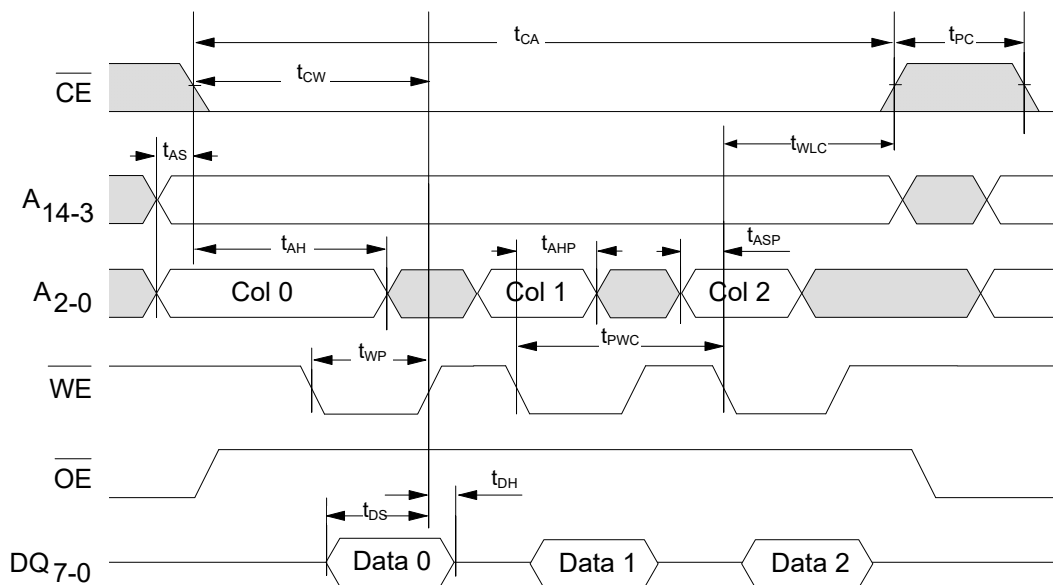


**Figure 11. Write Cycle Timing 3 ( $\overline{\text{CE}}$  LOW) <sup>[10]</sup>**



**Note**

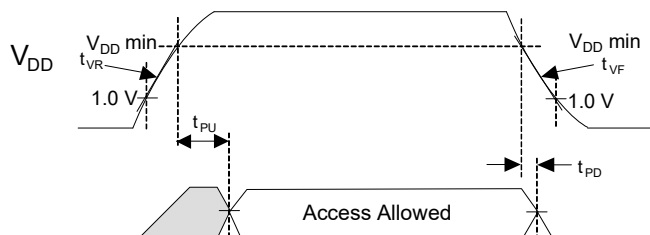
10.  $\overline{\text{OE}}$  (not shown) is LOW only to show the effect of  $\overline{\text{WE}}$  on DQ pins.

**Figure 12. Page Mode Write Cycle Timing**


## Power Cycle Timing

 Over the [Operating Range](#)

| Parameter       | Description                                                    | Min | Max | Unit      |
|-----------------|----------------------------------------------------------------|-----|-----|-----------|
| $t_{PU}$        | Power-up (after $V_{DD}$ min. is reached) to first access time | 250 | —   | $\mu s$   |
| $t_{PD}$        | Last write ( $\overline{WE}$ HIGH) to power down time          | 0   | —   | $\mu s$   |
| $t_{VR}^{[11]}$ | $V_{DD}$ power-up ramp rate                                    | 50  | —   | $\mu s/V$ |
| $t_{VF}^{[11]}$ | $V_{DD}$ power-down ramp rate                                  | 100 | —   | $\mu s/V$ |

**Figure 13. Power Cycle Timing**

**Note**

 11. Slope measured at any point on the  $V_{DD}$  waveform.

## Functional Truth Table

| $\overline{CE}$ | $\overline{WE}$ | $A_{14}-A_3$ | $A_2-A_0$ | Operation <sup>[12, 13]</sup>                         |
|-----------------|-----------------|--------------|-----------|-------------------------------------------------------|
| H               | X               | X            | X         | Standby/Idle                                          |
| ↓<br>L          | H<br>H          | V<br>V       | V<br>V    | Read                                                  |
| L               | H               | No Change    | Change    | Page Mode Read                                        |
| L               | H               | Change       | V         | Random Read                                           |
| ↓<br>L          | L<br>L          | V<br>V       | V<br>V    | $\overline{CE}$ -Controlled Write <sup>[13]</sup>     |
| L               | ↓               | V            | V         | $\overline{WE}$ -Controlled Write <sup>[13, 14]</sup> |
| L               | ↓               | No Change    | V         | Page Mode Write <sup>[15]</sup>                       |
| ↑<br>L          | X<br>X          | X<br>X       | X<br>X    | Starts pre-charge                                     |

### Notes

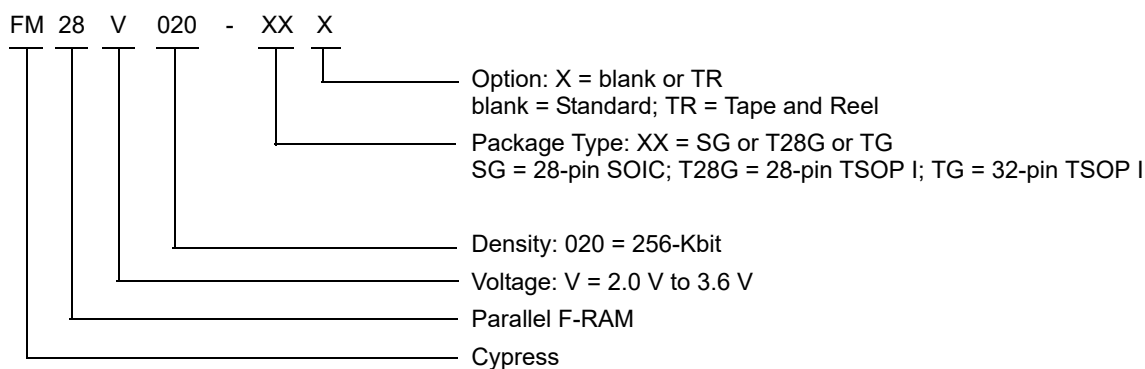
12. H = Logic HIGH, L = Logic LOW, V = Valid Data, X = Don't Care, ↓ = toggle LOW, ↑ = toggle HIGH.  
 13. For write cycles, data-in is latched on the rising edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever comes first.  
 14.  $\overline{WE}$ -controlled write cycle begins as a Read cycle and then  $A_{14}-A_3$  is latched.  
 15. Addresses  $A_2-A_0$  must remain stable for at least 15 ns during page mode operation.

## Ordering Information

| Access time (ns) | Ordering Code   | Package Diagram | Package Type  | Operating Range |
|------------------|-----------------|-----------------|---------------|-----------------|
| 70               | FM28V020-SG     | 51-85026        | 28-pin SOIC   | Industrial      |
|                  | FM28V020-SGTR   | 51-85026        | 28-pin SOIC   |                 |
|                  | FM28V020-T28G   | 001-91155       | 28-pin TSOP I |                 |
|                  | FM28V020-T28GTR | 001-91155       | 28-pin TSOP I |                 |
|                  | FM28V020-TG     | 001-91156       | 32-pin TSOP I |                 |
|                  | FM28V020-TGTR   | 001-91156       | 32-pin TSOP I |                 |

All the above parts are Pb-free.

## Ordering Code Definitions

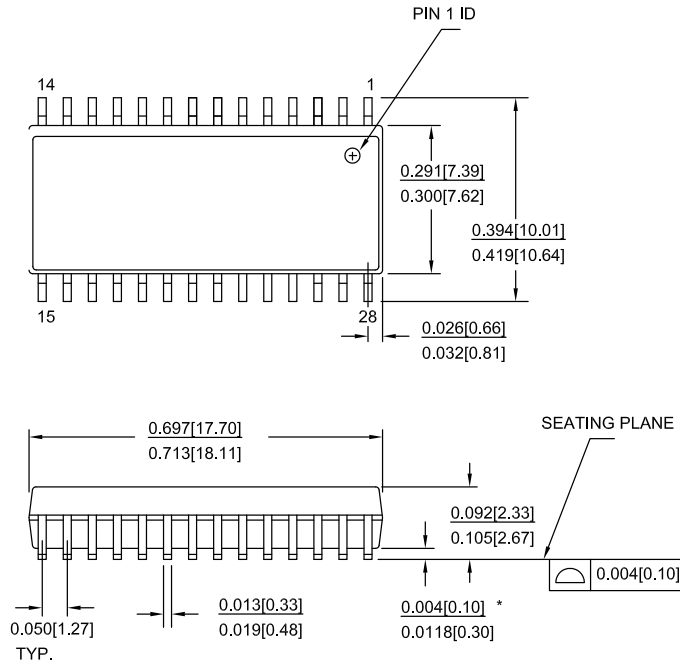


## Package Diagrams

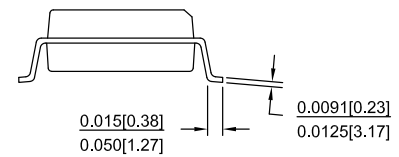
**Figure 14. 28-pin SOIC Package Outline, 51-85026**

NOTE :

1. JEDEC STD REF MO-119
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH,BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.010 in (0.254 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.  
MAX.



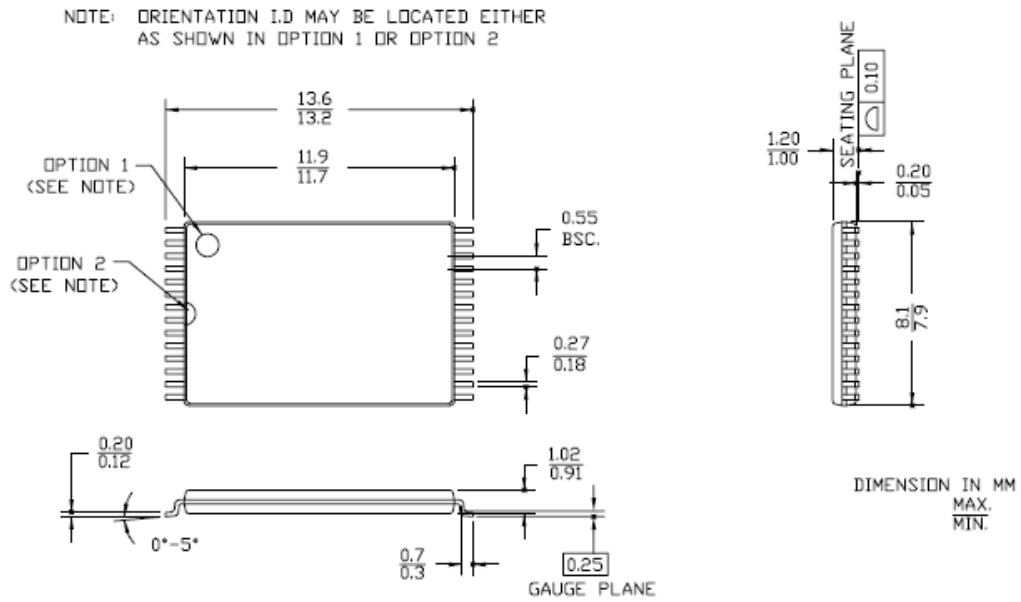
| PART # |                |
|--------|----------------|
| S28.3  | STANDARD PKG.  |
| SZ28.3 | LEAD FREE PKG. |
| SX28.3 | LEAD FREE PKG. |



51-85026 \*H

**Package Diagrams** (continued)

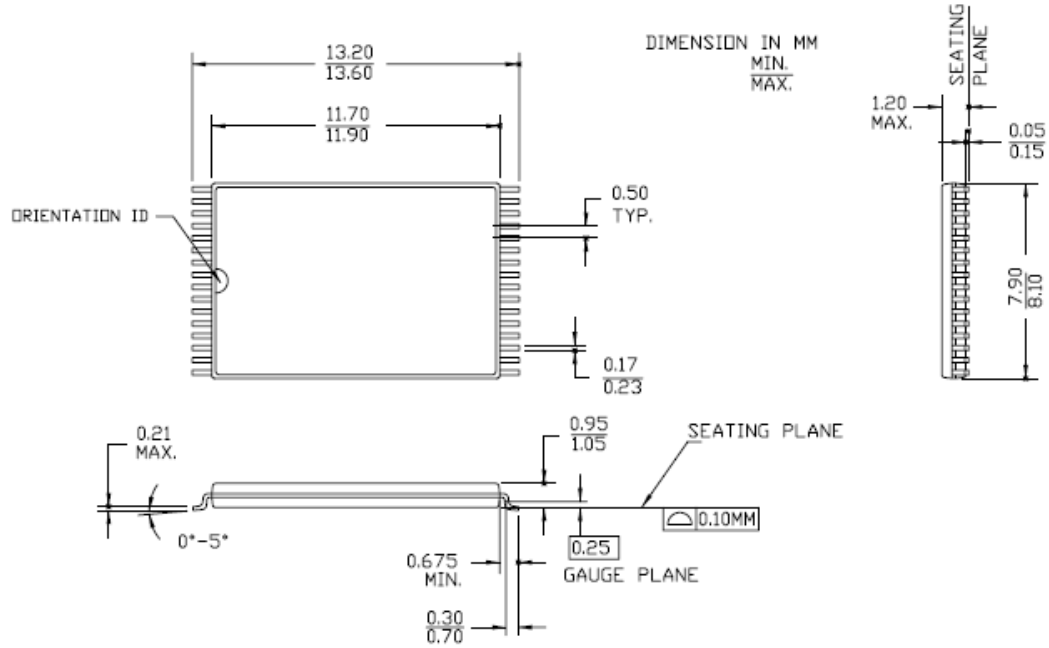
**Figure 15. 28-pin TSOP I Package Outline, 001-91155**



001-91155 \*\*

**Package Diagrams** (continued)

**Figure 16. 32-pin TSOP I Package Outline, 001-91156**



001-91156 \*\*

## Acronyms

| Acronym | Description                                |
|---------|--------------------------------------------|
| CPU     | Central Processing Unit                    |
| CMOS    | Complementary Metal Oxide Semiconductor    |
| JEDEC   | Joint Electron Devices Engineering Council |
| JESD    | JEDEC Standards                            |
| EIA     | Electronic Industries Alliance             |
| F-RAM   | Ferroelectric Random Access Memory         |
| I/O     | Input/Output                               |
| MCU     | Microcontroller Unit                       |
| MPU     | Microprocessor Unit                        |
| RoHS    | Restriction of Hazardous Substances        |
| RW      | Read and Write                             |
| SRAM    | Static Random Access Memory                |
| TSOP    | Thin Small Outline Package                 |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| Hz     | hertz           |
| kHz    | kilohertz       |
| kΩ     | kilohm          |
| MHz    | megahertz       |
| μA     | microampere     |
| μF     | microfarad      |
| μs     | microsecond     |
| mA     | milliampere     |
| ms     | millisecond     |
| MΩ     | megaohm         |
| ns     | nanosecond      |
| Ω      | ohm             |
| %      | percent         |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

## Document History Page

| Document Title: FM28V020, 256-Kbit (32K × 8) F-RAM Memory<br>Document Number: 001-86204 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----------------------------------------------------------------------------------------|---------|-----------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                    | ECN No. | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| **                                                                                      | 3912932 | GVCH            | 02/25/2013      | New spec.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| *A                                                                                      | 3924836 | GVCH            | 03/07/2013      | Changed to Production status<br>Added 28-pin TSOP package related information in all instances across the document.<br>Updated <a href="#">DC Electrical Characteristics</a> :<br>Changed typical value of I <sub>DD</sub> parameter from 7 mA to 5 mA.<br>Changed maximum value of I <sub>DD</sub> parameter from 12 mA to 8 mA.<br>Updated <a href="#">AC Switching Characteristics</a> :<br>SRAM Read Cycle:<br>Changed maximum value of t <sub>AAP</sub> parameter from 60 ns to 40 ns.<br>Changed maximum value of t <sub>OE</sub> parameter from 15 ns to 20 ns.<br>SRAM Write Cycle:<br>Changed minimum value of t <sub>PWC</sub> parameter from 30 ns to 35 ns.<br>Changed minimum value of t <sub>AHP</sub> parameter from 15 ns to 20 ns.<br>Updated <a href="#">Ordering Information</a> :<br>Updated part numbers                                                                                                                                                                                                                                                                                                                                                                                                                     |
| *B                                                                                      | 4000965 | GVCH            | 05/15/2013      | Added Appendix A - Errata for FM28V020.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| *C                                                                                      | 4045491 | GVCH            | 06/30/2013      | All errata items are fixed and the errata is removed.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| *D                                                                                      | 4274812 | GVCH            | 03/11/2014      | Updated <a href="#">Maximum Ratings</a> :<br>Added "Maximum Junction Temperature" and its corresponding details.<br>Added "DC voltage applied to outputs in High-Z state" and its corresponding details.<br>Added "Transient voltage (< 20 ns) on any pin to ground potential" and its corresponding details.<br>Added "Package power dissipation capability (T <sub>A</sub> = 25 °C)" and its corresponding details.<br>Added "DC output current (1 output at a time, 1s duration)" and its corresponding details.<br>Added "Latch-up Current" and its corresponding details.<br>Removed "Package Moisture Sensitivity Level" and its corresponding details.<br>Updated <a href="#">Data Retention and Endurance</a> :<br>Removed existing details of T <sub>DR</sub> parameter.<br>Added details of T <sub>DR</sub> parameter corresponding to "T <sub>A</sub> = 85 °C", "T <sub>A</sub> = 75 °C" and "T <sub>A</sub> = 65 °C".<br>Added NV <sub>C</sub> parameter and its corresponding details.<br>Added <a href="#">Thermal Resistance</a> .<br>Updated <a href="#">Package Diagrams</a> :<br>Removed Package Marking Scheme (top mark).<br>Removed "Ramtron Revision History".<br>Updated to Cypress template.<br>Completing Sunset Review. |

**Document History Page** (continued)

| Document Title: FM28V020, 256-Kbit (32K × 8) F-RAM Memory<br>Document Number: 001-86204 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                             |
|-----------------------------------------------------------------------------------------|---------|-----------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                                    | ECN No. | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                       |
| *E                                                                                      | 4582540 | GVCH            | 11/28/2014      | Updated <a href="#">Functional Description</a> :<br>Added "For a complete list of related documentation, click <a href="#">here</a> ." at the end.<br>Updated <a href="#">Pinouts</a> :<br>Updated <a href="#">Figure 3</a> :<br>Fixed typo (Replaced V <sub>DD</sub> with NC for pin 32).<br>Updated <a href="#">Package Diagrams</a> :<br>spec 51-85026 – Changed revision from *G to *H. |
| *F                                                                                      | 4881722 | ZSK / PSR       | 08/12/2015      | Updated <a href="#">Maximum Ratings</a> :<br>Removed "Maximum junction temperature" and its corresponding details.<br>Added "Maximum accumulated storage time" and its corresponding details.<br>Added "Ambient temperature with power applied" and its corresponding details.<br>Updated to new template.                                                                                  |
| *G                                                                                      | 5718305 | AESATMP7        | 04/28/2017      | Updated Cypress Logo and Copyright.                                                                                                                                                                                                                                                                                                                                                         |
| *H                                                                                      | 6389368 | GVCH            | 11/20/2018      | Updated <a href="#">Maximum Ratings</a> :<br>Replaced "–55 °C to +125 °C" with "–65 °C to +125 °C" in ratings corresponding to "Storage temperature".<br>Updated to new template.                                                                                                                                                                                                           |

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