Contents

1 Block diagram and pins description

Figure 1. Block diagram

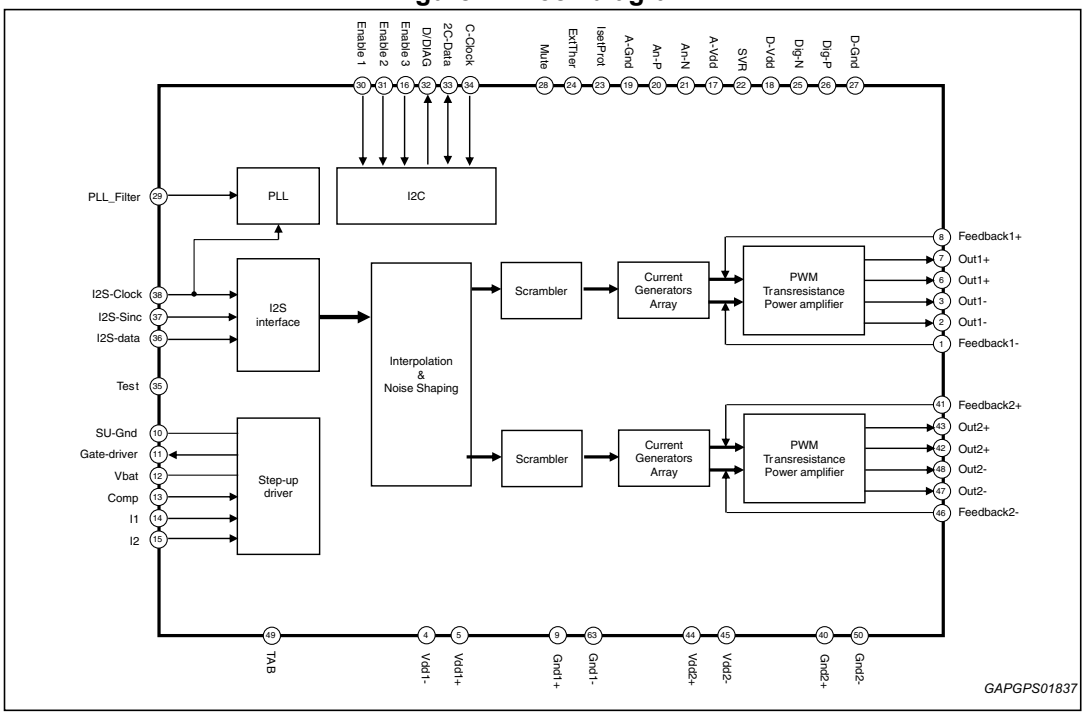


Figure 2. Pins connection diagram (top view)

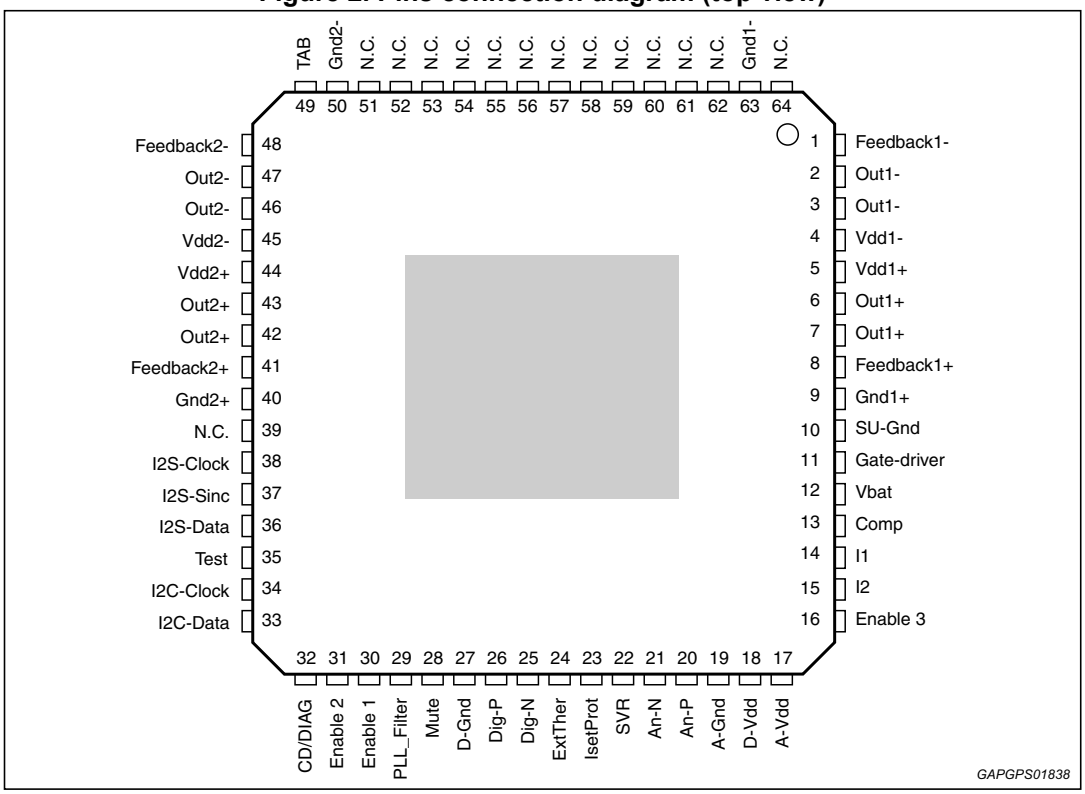


Table 2. Pins list description

Pin #	Pin name	Function
64	N.C.	Not connected
63	Gnd1-	Channel 1, half bridge power ground -
51-62	N.C.	Not connected
50	Gnd2-	Channel 2, half bridge power ground -
49	TAB	TAB connection
48	Feedback2-	Channel 2 half bridge feedback -
47	Out2-	Channel 2 half bridge output -
46	Out2-	Channel 2 half bridge output -
45	Vdd2-	Channel 2 half bridge power supply -
44	Vdd2+	Channel 2 half bridge power supply +
43	Out2+	Channel 2 half bridge output +
42	Out2+	Channel 2 half bridge output +
41	Feedback2+	Channel 2 half bridge feedback +
40	Gnd2+	Channel 2, half bridge power ground +
39	N.C.	Not connected
38	I2S-Clock	I2S/TDM clock Input
37	I2S-Sinc	I2S/TDM sinc Input
36	I2S-Data	I2S/TDM data Input
35	Test	Test pin (do not use)
34	I2C-Clock	I2C data Clock
33	I2C-Data	I2C data input
32	CD/DIAG	Clip detector and diagnostic output: over-current protection, thermal warning, offset detection
31	Enable 2	Chip enable 2
30	Enable 1	Chip enable 1
29	PLL_Filter	PLL filter network
28	Mute	Mute input (6 µA source current)
27	D-Gnd	Digital ground
26	Dig-P	Positive digital supply V(svr)+1.65 (internally generated)
25	Dig-N	Negative digital supply V(svr)-1.65 (internally generated)
24	ExtTher	External thermal protection input
23	IsetProt	Current protection resistor setting
22	SVR	Supply voltage ripple rejection capacitor
21	An-N	Negative analog supply V(svr)-1.65 (internally generated)
20	An-P	Positive analog supply V(svr)+1.65 (internally generated)

Table 2. Pins list description (continued)

Pin #	Pin name	Function
19	A-Gnd	Analog ground
18	D-Vdd	Digital power supply
17	A-Vdd	Analog power supply
16	Enable 3	Chip enable 3
15	I2	Step-up current limiting reference
14	I1	Step-up current limiting input
13	Comp	Step-up compensation input
12	Vbat	Power supply (battery)
11	Gate-driver	External PowerMOS gate drive output
10	SU-Gnd	Step-up power ground
9	Gnd1+	Channel 1, half bridge power ground +
8	Feedback1+	Channel 1 half bridge feedback +
7	Out1+	Channel 1 half bridge output +
6	Out1+	Channel 1 half bridge output +
5	Vdd1+	Channel 1 half bridge power supply +
4	Vdd1-	Channel 1 half bridge power supply -
3	Out1-	Channel 1 half bridge output -
2	Out1-	Channel 1 half bridge output -
1	Feedback1-	Channel 1 half bridge feedback -

2 Device overview

The FDA2100LV is a fully digital single chip class D amplifier with high immunity to the demodulation filter effects, built-in diagnostic functions and step-up driver. The high integration level and the on-board signal processing allow an excellent audio performance to be achieved. Thanks to the digital input and a feedback strategy in the power stage that make the amplifier robust with respect to the output filter non-idealities, the number and size of the external components are minimized.

Differently from the typical PWM switching amplifiers, a new feedback technique is adopted by FDA2100LV. The LC filter is included in the feedback loop making the amplifier highly insensitive to the characteristics of such a demodulator group. This solution optimizes the system performance in terms of THD and frequency response. Regardless of the big phase shifting introduced by the output filter the device shows a great phase margin for any load condition.

A number of features has also been included to reduce EMI, making the system compliant with the stringent limits typical of automotive applications and the fully digital approach provides a strong GSM immunity.

The FDA2100LV includes digital I^2C and I^2S interfaces, internal 20 bits DAC conversion, digital signal processing for interpolation and noise shaping, step-up driver, internal PLL for a pure clock generation and self diagnostic functions and automatic detection of wrong load connections or variation of the load with respect to the expected one.

In particular, considering diagnostic feature, the FDA amplifiers family provides different functions to detect several possible fault conditions. Any warning information will be stored in the I^2C interface and kept until the first I^2C bus reading operation. The main FDA2100LV's diagnostic features are the following ones:

- Load detection
- Under/over voltage evens
- Chip over temperature
- Digital input offset
- Output clipping
- Over temperature of an external component (i.e. step-up DMOS) through a suitable NTC external sensor
- Output current digital acquisition

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

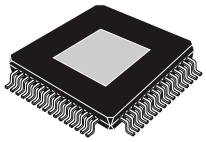
ECOPACK® is an ST trademark.

Figure 3. TQFP64 (exposed pad up) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.090			0.0429
A1	-0.040		0.040	-0.0016		0.0016
A2	0.950	1.000	1.050	0.0374	0.0394	0.0413
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D2(1)	2.000			0.0787		
D3		7.500			0.2953	
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.000	10.200	0.3858	0.3937	0.4016
E2(1)	2.000			0.0787		
E3		7.500			0.2953	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k		3.500	7.000		0.1378	0.2756
ccc			0.080			0.0031
R		1.000			0.0394	
T1-T2		5.250			0.2067	

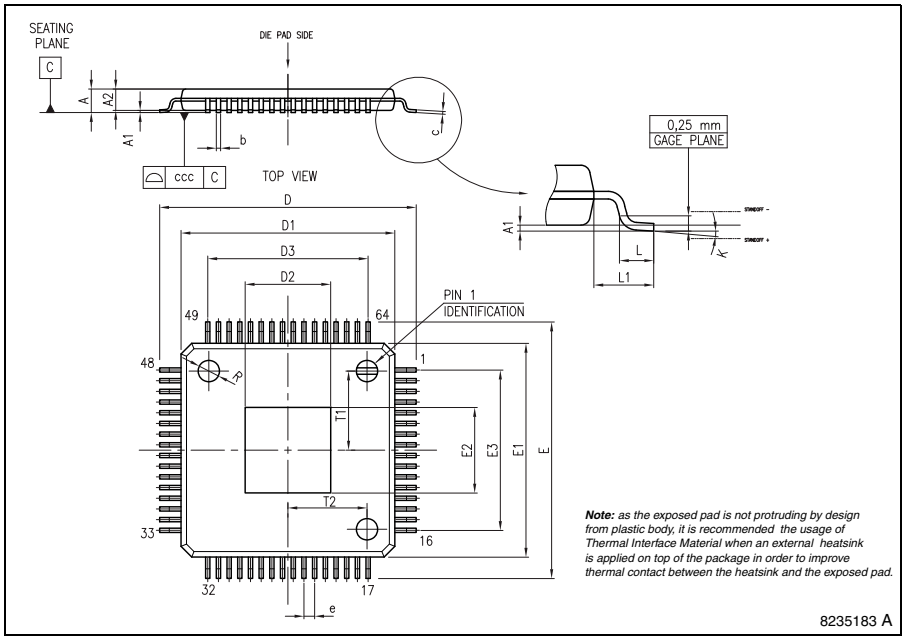
(1) The size of exposed pad is variable depending of leadframe design pad size.
End user should verify “D2” and “E2” dimensions for each device application.

OUTLINE AND MECHANICAL DATA



Body: 10 x 10 x 1mm

TQFP64 (exposed pad up)
Thin **Q**uad **F**lat **P**ackage



4 Revision history

Table 3. Document revision history

Date	Revision	Changes
11-Oct-2013	1	Initial release.

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