ABSOLUTE MAXIMUM RATINGS

Voltage Range on PLS and $\overline{CC}$ Pins, Relative to V_{SS}	-0.3V to +18V
Voltage Range on Any Other Pin, Relative to V_{SS}	-0.3V to +6V
Continuous Internal Sense Resistor Current	±2.5A
Pulsed Internal Sense Resistor Current	±50A for <100µs/s, <1000 pulses
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020A Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.

RECOMMENDED DC OPERATING CONDITIONS

(2.5V ≤ V_{DD} ≤ 5.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 1)	2.5		5.5	V
Voltage Sense Input	V_{IN}	(Note 1)	-0.3		V_{DD} + 0.3	V
Serial Interface Pins	SCL, SDA	(Note 1)	-0.3		+5.5	V

DC ELECTRICAL CHARACTERISTICS

(2.5V ≤ V_{DD} ≤ 5.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Current	I_{ACTIVE}	SCL = SDA = V_{DD}, normal operation		60	90	µA
Sleep Mode Current	I_{SLEEP}	SCL = SDA = 0V, no activity, $\overline{PS}$ floating		1	2	µA
Input Logic High: SCL, SDA	V_{IH}	(Note 1)	1.5			V
Input Logic High: $\overline{PS}$	V_{IH}	(Note 1)	0.7 x V_{DD}			V
Input Logic Low: SCL, SDA	V_{IL}	(Note 1)			0.4	V
Input Logic Low: $\overline{PS}$	V_{IL}	(Note 1)			0.3 x V_{DD}	V
Output Logic High: $\overline{CC}$	V_{OH}	I_{OH} = -0.1mA (Note 1)	V_{PLS} - 0.4			V
Output Logic High: $\overline{DC}$	V_{OH}	I_{OH} = -0.1mA (Note 1)	V_{DD} - 0.4			V
Output Logic Low: $\overline{CC}$	V_{OL_CC}	I_{OL} = 0.1mA (Note 1)			0.4	V
Output Logic Low: $\overline{DC}$	V_{OL_DC}	I_{OL} = 0.5µA (Note 1)			0.4	V
Output Logic Low: SDA	V_{OL}	I_{OL} = 4mA (Note 1)			0.4	V
Pulldown Current: SCL, SDA	I_{PD}			1		µA
Input Resistance: V_{IN}	R_{IN}		5			MΩ
Internal Current-Sense Resistor	R_{SNS}	+25°C	20	25	30	mΩ
Bus Low to Sleep time	t_{SLEEP}		2.1			s

ELECTRICAL CHARACTERISTICS: PROTECTION CIRCUITRY

($2.5V \le V_{DD} \le 5.5V$, T_A = 0°C to +50°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Detect	V_{OV}	(Notes 1, 2)	4.325	4.350	4.375	V
			4.250	4.275	4.300	
Charge Enable	V_{CE}	(Note 1)	4.10	4.15	4.20	V
Undervoltage Detect	V_{UV}	(Note 1)	2.5	2.6	2.7	V
Overcurrent Detect	I_{OC}	(Note 3)	1.8	1.9	2.0	A
Overcurrent Detect	V_{OC}	(Notes 1, 4)	45	47.5	50	mV
Short-Circuit Detect	I_{SC}	(Note 3)	5.0	8.0	11	A
Short-Circuit Detect	V_{SC}	(Notes 1, 4)	150	200	250	mV
Overvoltage Delay	t_{OVD}		0.8	1	1.2	s
Undervoltage Delay	t_{UVD}		90	100	110	ms
Overcurrent Delay	t_{OCD}		5	10	20	ms
Short-Circuit Delay	t_{SCD}		160	200	240	µs
Test Threshold	V_{TP}		0.5	1.0	1.5	V
Test Current	I_{TST}		5	20	40	µA

ELECTRICAL CHARACTERISTICS: TEMPERATURE, VOLTAGE, CURRENT

($2.5V \le V_{DD} \le 5.5V$, T_A = -20°C to +50°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Resolution	T_{LSB}			0.125		°C
Temperature Full-Scale Magnitude	T_{FS}		127			°C
Temperature Error	T_{ERR}	(Note 5)			±3	°C
Voltage Resolution	V_{LSB}			4.88		mV
Voltage Full-Scale Magnitude	V_{FS}		4.75			V
Voltage Gain Error	V_{GERR}				5	%
Current Resolution	I_{LSB}	(Note 3)		0.625		mA
		(Note 4)		15.625		µV
Current Full-Scale Magnitude	I_{FS}	(Notes 3, 6)	1.9	2.56		A
		(Note 4)		64		mV
Current Offset Error	I_{OERR}	(Note 7)			1	LSB
Current Gain Error	I_{GERR}	(Notes 3, 8, 9)			10	%
		(Note 4)			2	
Accumulated Current Resolution	q_{CA}	(Note 3)		0.25		mAh
		(Note 4)		6.25		µVhr
Current Sampling Frequency	f_{SAMP}			1456		Hz
Internal Timebase Accuracy	t_{ERR1}	(Note 10)		±1	±3	%
	t_{ERR2}	(Note 10)			±6.5	%

ELECTRICAL CHARACTERISTICS: 2-WIRE INTERFACE

(2.5V ≤ V_{DD} ≤ 5.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 12)	0		100	KHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		4.7			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 13)	4.0			µs
Low Period of SCL Clock	t_{LOW}		4.7			µs
High Period of SCL Clock	t_{HIGH}		4.0			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		4.7			µs
Data Hold Time	$t_{HD:DAT}$	(Note 14, 15)	0		5.0	µs
Data Setup Time	$t_{SU:DAT}$	(Note 14)	250			ns
Rise Time of both SDA and SCL Signals	t_R				1000	ns
Fall Time of both SDA and SCL Signals	t_F				300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		4.0			µs
Spike pulse widths suppressed by input filter	t_{SP}	(Note 16)	0		50	ns
Capacitive Load for each Bus Line	C_B	(Note 17)			400	pF
SCL, SDA Input Capacitance	C_{BIN}				60	pF

EEPROM RELIABILITY SPECIFICATION

(2.5V ≤ V_{DD} ≤ 5.5V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Copy to EEPROM Time	t_{EEC}			2	10	ms
EEPROM Copy Endurance	N_{EEC}	(Note 11)	25,000			cycles

Note 1: All voltages are referenced to V_{SS}.

Note 2: See the *Selector Guide* section to determine the corresponding part number for each V_{OV} value.

Note 3: Internal current-sense resistor configuration.

Note 4: External current-sense resistor configuration.

Note 5: Self-heating due to output pin loading and sense resistor power dissipation can alter the reading from ambient conditions.

Note 6: Compensation of the internal sense resistor value for initial tolerance and temperature coefficient of -20°C to +70°C can reduce the maximum reportable magnitude to 1.9A.

Note 7: Current offset error null to ±1 LSB typically requires 3.5s in-system calibration by user.

Note 8: Current gain error specification applies to gain error in converting the voltage difference at IS1 and IS2, and excludes any error remaining after the DS2764 compensates for the internal sense resistor's temperature coefficient of 3700ppm/°C to an accuracy of ±500ppm/°C. The DS2764 does not compensate for external sense resistor characteristics, and any error terms arising from the use of an external sense resistor should be taken into account when calculating total current measurement error.

Note 9: Accuracy at time of shipment from Dallas Semiconductor is 3% max. Board mounting processes may cause the current gain error to widen to as much as 10% for devices with the internal sense resistor option. Contact factory for on-board recalibration procedure devices with the internal sense resistor option to improve accuracy.

Note 10: Typical value for t_{ERR1} is specified at 3.6V and +25°C, max value is specified for 0°C to +50°C. Max value for t_{ERR2} is specified for -20°C to +70°C.

Note 11: Four-year data retention at +70°C.

Note 12: Timing must be fast enough to prevent the DS2764 from entering sleep mode due to bus low for period > t_{SLEEP}

Note 13: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

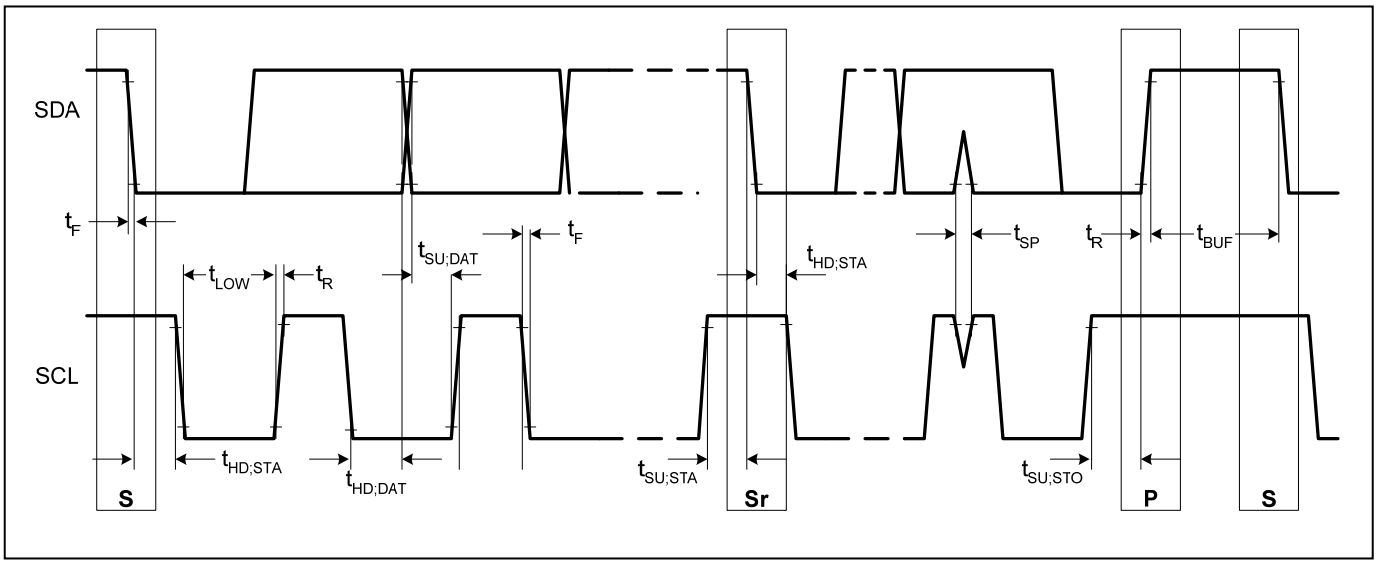
Note 14: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 15: This device internally provides a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 16: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Note 17: C_B— total capacitance of one bus line in pF.

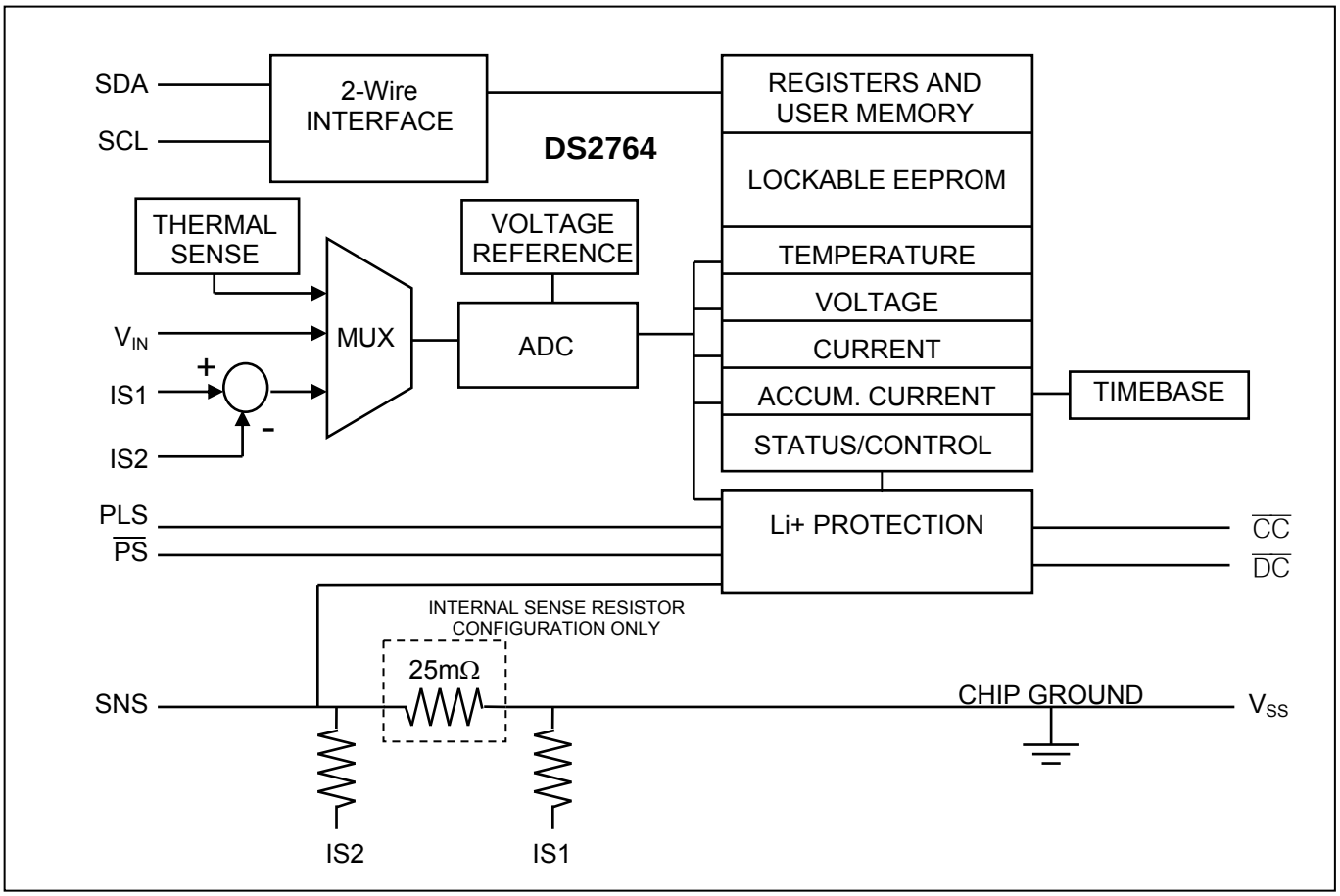
Figure 1. I²C Bus Timing Diagram



PIN DESCRIPTION

PIN		SYMBOL	FUNCTION
TSSOP	FLIP CHIP		
1	C1	$\overline{CC}$	**Charge Protection Control Output.** Controls an external P-channel high-side charge protection FET.
2	B1	PLS	**Battery Pack Positive Terminal Input.** The DS2764 monitors the pack plus terminal through PLS to detect overload and short circuit removal, as well as the presence or removal of a charge source. Additionally, a charge path to recover a deeply depleted cell is provided from PLS to V_{DD}. In sleep mode, any capacitance or voltage source connected to PLS is discharged internally to V_{SS} through 200µA (nominal) to assure reliable detection of a valid charge source. For details of other internal connections to PLS and associated conditions see the *Li+ Protection Circuitry* section.
3	B2	$\overline{DC}$	**Discharge Protection Control Output.** Controls an external P-channel high-side discharge protection FET.
4, 5, 6	A3	SNS	**Sense Resistor Connection.** Connect to the negative terminal of the battery pack. In the internal sense resistor configuration, the sense resistor is connected between V_{SS} and SNS.
7	C4	$\overline{PS}$	**Power Switch Sense Input.** The device wakes up from sleep mode when it senses the closure of a switch to V_{SS} on this pin. Pin has an internal 1µA pull-up to V_{DD}.
8	B4	IS2	**Current-Sense Input.** This pin is internally connected to SNS through a 4.7kΩ resistor.
9	D4	IS1	**Current-Sense Input.** This pin is internally connected to V_{SS} through a 4.7kΩ resistor. Connect a 0.1µF capacitor between IS1 and IS2 to complete a low pass input filter.
10	E4	SDA	**Serial Data Input/Out.** 2-Wire data line. Open-drain output driver. Connect this pin to the DATA terminal of the battery pack. Pin has an internal 1µA pulldown for sensing disconnection.
11, 12, 13	F3	V_{SS}	**Device Ground.** Connect directly to the negative terminal of the Li+ cell. For the external sense resistor configuration, connect the sense resistor between V_{SS} and SNS.
14	E2	SCL	**Serial Clock Input.** 2-Wire clock line. Input only. Connect this pin to the CLOCK terminal of the battery pack. Pin has an internal 1µA pulldown for sensing disconnection.
15	E1	V_{DD}	**Power-Supply Input.** Connect to the positive terminal of the Li+ cell through a decoupling network.
16	D1	V_{IN}	**Voltage Sense Input.** The voltage of the Li+ cell is monitored through this input pin. This pin has a weak pull-up to V_{DD}.
—	C2	SNS Probe	Do not connect.
—	D2	V_{SS} Probe	Do not connect.

Figure 2. Block Diagram



DETAILED DESCRIPTION

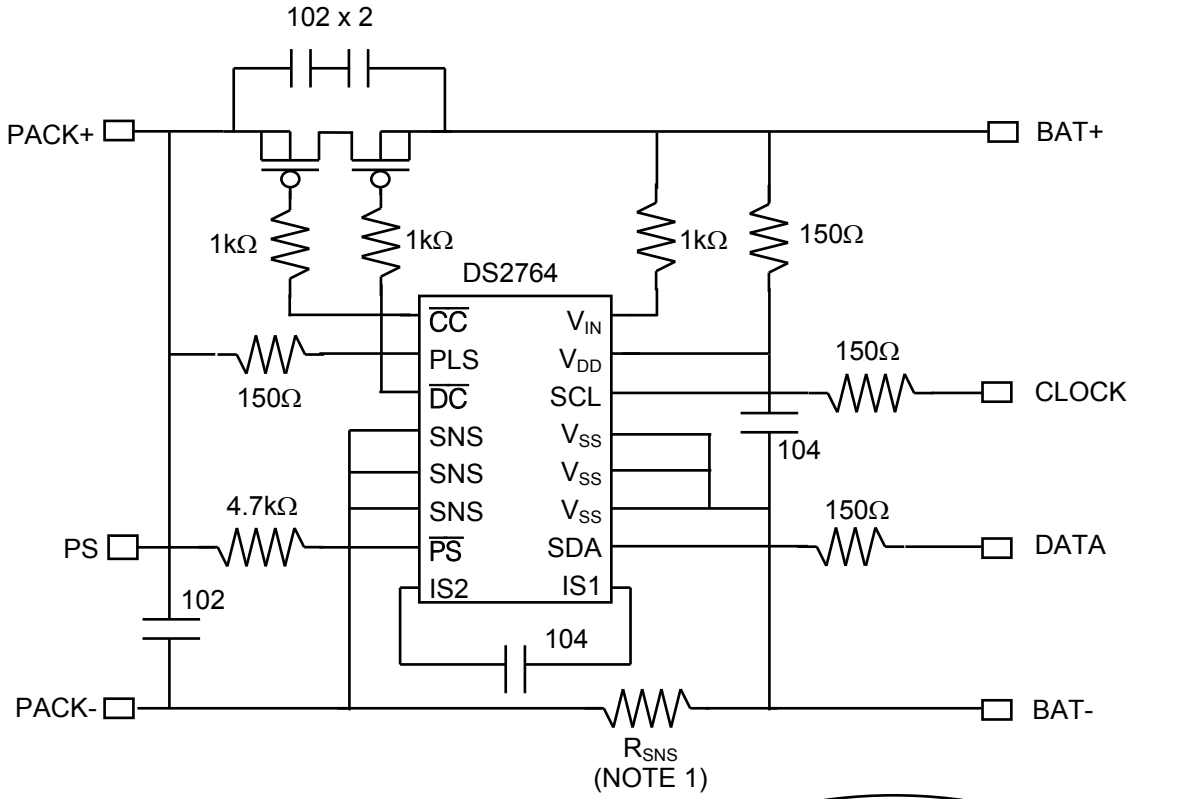
The DS2764 high-precision Li+ battery monitor is a data-acquisition, information-storage, and safety-protection device tailored for cost-sensitive battery pack applications. This low-power device integrates precise temperature, voltage, and current measurement, nonvolatile (NV) data storage, and Li+ protection into the small footprint of either a TSSOP package or flip-chip package. The DS2764 is a key component in applications including remaining capacity estimation, safety monitoring, and battery-specific data storage.

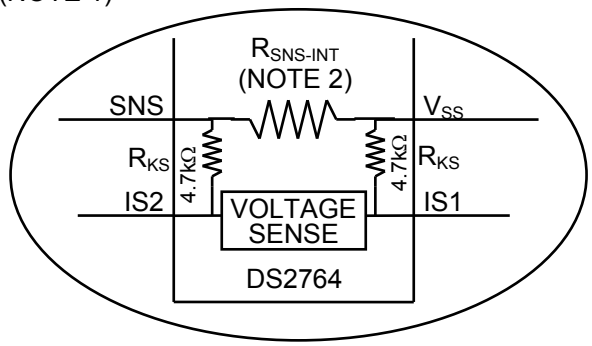
Through its 2-Wire interface, the DS2764 gives the host system read/write access to status and control registers, instrumentation registers, and general-purpose data storage. The 7-bit slave address is field programmable, thus allowing up to 128 devices to be distinctly addressed by the host system.

The DS2764 is capable of performing temperature, voltage, and current measurement to a resolution sufficient to support process monitoring applications such as battery charge control, remaining capacity estimation, and safety monitoring. Temperature is measured using an on-chip sensor, eliminating the need for a separate thermistor. Bidirectional current measurement and accumulation are accomplished using either an internal 25mΩ sense resistor or an external device.

EEPROM memory is provided to save important battery data in true NV memory that is unaffected by severe battery depletion, accidental shorts, or ESD events. 40 bytes are partitioned into two 16-byte blocks and one 8-byte block. Each block can be individually locked or write protected to provide additional security for unchanging battery data. The lock operation is permanent and thus converts rewritable EEPROM to read only memory. Devices ordered with the unique 64-bit ID option do not have access to the 8 byte block, only the two 16 byte blocks of EEPROM are available.

Figure 3. Application Example





NOTE 1: R_{SNS} IS PRESENT FOR EXTERNAL SENSE RESISTOR CONFIGURATIONS ONLY.
NOTE 2: $R_{SNS-INT}$ IS PRESENT FOR INTERNAL SENSE RESISTOR CONFIGURATIONS ONLY.

POWER MODES

The DS2764 has two power modes: active and sleep. While in active mode, the DS2764 continually measures current, voltage, and temperature to provide data to the host system and to support current accumulation and Li+ safety monitoring. In sleep mode, the DS2764 ceases these activities. The DS2764 enters sleep mode when any of the following conditions occurs:

- The PMOD bit in the Status Register has been set to 1 and both SCL and SDA are low for longer than 2.1s (pack disconnection).
- The voltage on V_{IN} drops below undervoltage threshold V_{UV} for t_{UVD} (cell depletion).

The DS2764 returns to active mode when any of the following occurs:

- The PMOD bit has been set to 1 and either the SDA or SCL line is pulled high (pack connection).
- The $\overline{PS}$ pin is pulled low (power switch).
- The voltage on PLS becomes greater than the voltage on V_{DD} (charger connection).

The DS2764 defaults to active mode when power is first applied.

Li+ PROTECTION CIRCUITRY

During active mode, the DS2764 constantly monitors cell voltage and current to protect the battery from overcharge (overvoltage), overdischarge (undervoltage), and excessive charge and discharge currents (overcurrent, short circuit). Conditions and DS2764 responses are described in the following sections and summarized in Table 1 and Figure 4.

Table 1. Li+ Protection Conditions and DS2764 Responses

CONDITION	ACTIVATION			RELEASE THRESHOLD
	THRESHOLD	DELAY	RESPONSE	
Overvoltage	$V_{IN} > V_{OV}$	t_{OVD}	$\overline{CC}$ high	$V_{IN} < V_{CE}$, or $V_{IS} \le -2mV$
Undervoltage	$V_{IN} < V_{UV}$	t_{UVD}	$\overline{CC}$, $\overline{DC}$ high, Sleep Mode	$V_{PLS} > V_{DD}$ (1) (charger connected)
Overcurrent, Charge	$V_{IS} > V_{OC}$ (2)	t_{OCD}	$\overline{CC}$, $\overline{DC}$ high	$V_{PLS} < V_{DD} - V_{TP}$ (3)
Overcurrent, Discharge	$V_{IS} < -V_{OC}$ (2)	t_{OCD}	$\overline{DC}$ high	$V_{PLS} > V_{DD} - V_{TP}$ (4)
Short Circuit	$V_{SNS} > V_{SC}$	t_{SCD}	$\overline{DC}$ high	$V_{PLS} > V_{DD} - V_{TP}$ (4)

$V_{IS} = V_{IS1} - V_{IS2}$. Logic high = V_{PLS} for $\overline{CC}$ and V_{DD} for $\overline{DC}$. All voltages are with respect to V_{SS}. I_{SNS} references current delivered from pin SNS.

Note 1: If $V_{DD} < 2.2V$, release is delayed until the recovery charge current passed from PLS to V_{DD} charges the battery and allows V_{DD} to exceed 2.2V.

Note 2: For the internal sense resistor configuration, the overcurrent thresholds are expressed in terms of current: $I_{SNS} > I_{OC}$ for charge direction and $I_{SNS} < -I_{OC}$ for discharge direction.

Note 3: With test current I_{TST} flowing from PLS to V_{SS} (pulldown on PLS).

Note 4: With test current I_{TST} flowing from V_{DD} to PLS (pullup on PLS).

Overvoltage. If the cell voltage on V_{IN} exceeds the overvoltage threshold, V_{OV}, for a period longer than overvoltage delay, t_{OVD}, the DS2764 shuts off the external charge FET and sets the OV flag in the protection register. When the cell voltage falls below charge enable threshold V_{CE}, the DS2764 turns the charge FET back on (unless another protection condition prevents it). Discharging remains enabled during overvoltage, and the DS2764 re-enables the charge FET before $V_{IN} < V_{CE}$ if a discharge current of -80mA ($V_{IS} \le -2mV$) or less is detected.

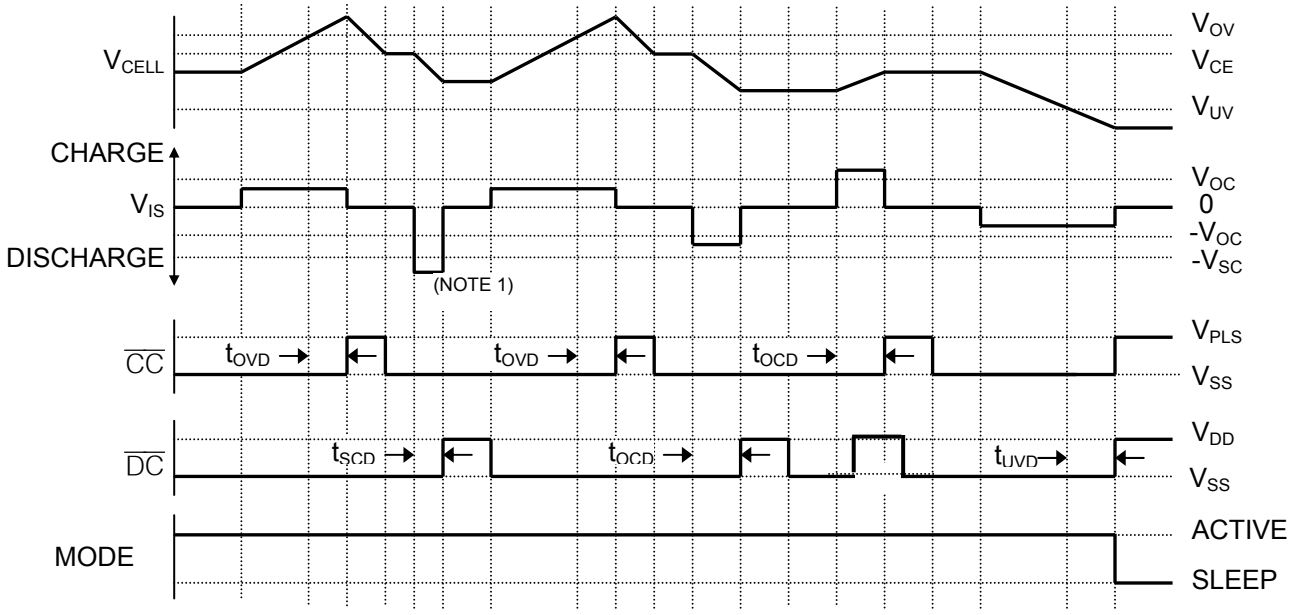
Undervoltage. If the voltage of the cell drops below undervoltage threshold, V_{UV}, for a period longer than undervoltage delay, t_{UVD}, the DS2764 shuts off the charge and discharge FETs, sets the UV flag in the protection register, and enters sleep mode. The DS2764 provides a recovery charge path from PLS to V_{DD} to power the DS2764 by the charger when the cell is severely depleted. Once the DS2764 regains power it will enter active mode of operation and allow full charging of the cell. The recovery charge path is disabled when the cell voltage is above 3.0V to prevent cell overcharge through the PLS pin.

Overcurrent, Charge Direction. The voltage difference between the IS1 pin and the IS2 pin ($V_{IS} = V_{IS1} - V_{IS2}$) is the filtered voltage drop across the current-sense resistor. If V_{IS} exceeds overcurrent threshold V_{OC} for a period longer than overcurrent delay t_{OCD}, the DS2764 shuts off both external FETs and sets the COC flag in the protection register. The charge current path is not re-established until the voltage on the PLS pin drops below $V_{DD} - V_{TP}$. The DS2764 provides a test current of value I_{TST} from PLS to V_{SS} to pull PLS down to detect the removal of the offending charge current source.

Overcurrent, Discharge Direction. If V_{IS} is less than $-V_{OC}$ for a period longer than t_{OCD}, the DS2764 shuts off the external discharge FET and sets the DOC flag in the protection register. The discharge current path is not re-established until the voltage on PLS rises above $V_{DD} - V_{TP}$. The DS2764 provides a test current of value I_{TST} from V_{DD} to PLS to pull PLS up to detect the removal of the offending low-impedance load.

Short Circuit. If the voltage on the SNS pin with respect to V_{SS} exceeds short-circuit threshold V_{SC} for a period longer than short-circuit delay t_{SCD}, the DS2764 shuts off the external discharge FET and sets the DOC flag in the protection register. The discharge current path is not re-established until the voltage on PLS rises above $V_{DD} - V_{TP}$. The DS2764 provides a test current of value I_{TST} from V_{DD} to PLS to pull PLS up to detect the removal of the short circuit.

Figure 4. Li+ Protection Circuitry Example Waveforms



NOTE 1: TO ALLOW THE DEVICE TO REACT QUICKLY TO SHORT CIRCUITS, DETECTION OCCURS ON THE SNS PIN RATHER THAN ON THE FILTERED IS1 AND IS2 PINS. THE ACTUAL SHORT-CIRCUIT DETECT CONDITION IS $V_{SNS} > V_{SC}$.

Summary. All of the protection conditions described above are OR'ed together to affect the $\overline{CC}$ and $\overline{DC}$ outputs.

$\overline{DC}$ = (Undervoltage) or (Overcurrent, Either Direction) or (Short Circuit) or (Protection Register Bit DE = 0) or (Sleep Mode)

$\overline{CC}$ = (Overvoltage and $V_{IS} \geq -2mV$) or (Undervoltage) or (Overcurrent, Charge Direction) or (Protection Register bit CE = 0) or (Sleep Mode)

Soft Startup. The discharge protection FET is turned on slowly when the DS2764 enters Active mode from Sleep. The soft startup reduces the inrush current that normally occurs when a battery pack is inserted into an un-powered host system. Soft Startup does not reduce inrush currents if the DS2764 is already in Active mode when the battery pack is connected to the un-powered system.

CURRENT MEASUREMENT

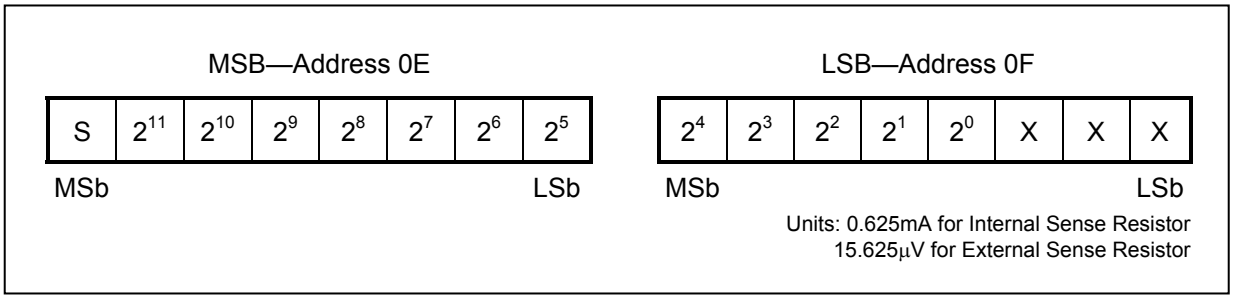
In active mode, the DS2764 continually measures the current flow into and out of the battery by measuring the voltage drop across a current-sense resistor. The DS2764 is available in two configurations: 1) internal 25mΩ current-sense resistor and 2) external user-selectable sense resistor. In either configuration, the DS2764 considers the voltage difference between pins IS1 and IS2 ($V_{IS} = V_{IS1} - V_{IS2}$) to be the filtered voltage drop across the sense resistor. A positive V_{IS} value indicates current is flowing into the battery (charging), while a negative V_{IS} value indicates current is flowing out of the battery (discharging).

V_{IS} is measured with a signed resolution of 12 bits. The current register is updated in two's-complement format every 88ms with an average of 128 readings. Current measurements outside the register range are reported at the range limit. Each measurement is internally compensated for offset on a continual basis minimizing error resulting from variations in device temperature and voltage. Figure 5 shows the format of the current register.

For the internal sense resistor configuration, the DS2764 maintains the current register in units of amps, with a resolution of 0.625mA and full-scale range of no less than ±1.9A (see *Note 7* on I_{FS} spec for more details). The DS2764 automatically compensates for internal sense resistor process variations and temperature effects when reporting current.

For the external sense resistor configuration, the DS2764 writes the measured V_{IS} voltage to the current register, with a 15.625μV resolution and a full-scale ±64mV range.

Figure 5. Current Register Format



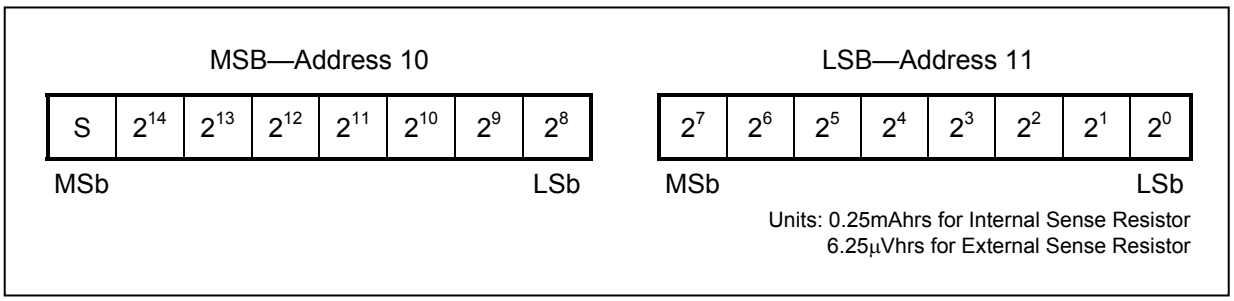
CURRENT ACCUMULATOR

The current accumulator facilitates remaining capacity estimation by tracking the net current flow into and out of the battery. Current flow into the battery increments the current accumulator while current flow out of the battery decrements it. Data is maintained in the current accumulator in two's-complement format. Figure 6 shows the format of the current accumulator.

When the internal sense resistor is used, the DS2764 maintains the current accumulator in units of amp-hours, with a 0.25mAhrs resolution and full-scale ±8.2Ahrs range. When using an external sense resistor, the DS2764 maintains the current accumulator in units of volt-hours, with a 6.25μVhrs resolution and a full-scale ±205mVhrs range.

The current accumulator is a read/write register that can be altered by the host system as needed.

Figure 6. Current Accumulator Format

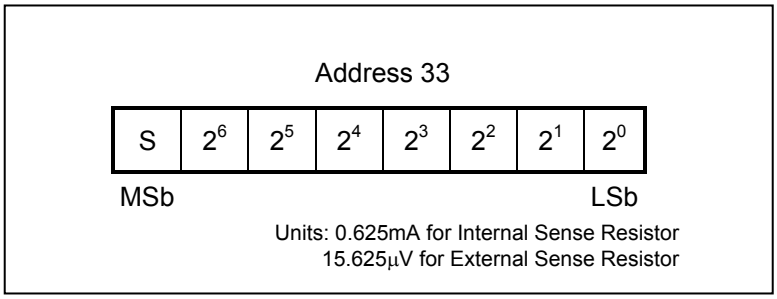


CURRENT OFFSET COMPENSATION

The current measurement and current accumulation are internally compensated for offset on a continual basis minimizing error resulting from variations in device temperature and voltage. Additionally, the Current Offset Bias register is a user programmable constant bias that can be used to alter the offset of the Current and Accumulated current registers. User programmed bias values can be used to correct for offset errors after final assembly of the module or pack. An offset value can be purposely chosen to bias current accumulation in the discharge polarity to ensure a pessimistic accounting of μA level standby currents.

The Current Offset Bias value resides in EEPROM address 33h in two's-complement format and is subtracted from current measurements during the accumulation process. The Current Offset Bias is applied to the internal and external sense resistor configurations. The factory default for EEPROM address 33h is 0.

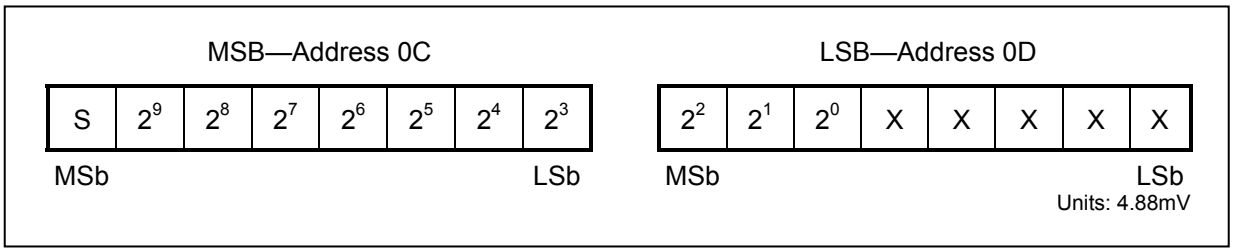
Figure 7. Current Offset Bias



VOLTAGE MEASUREMENT

The DS2764 continually measures the voltage between pins V_{IN} and V_{SS} over a 0 to 4.75V range. The voltage register is updated in two's-complement format every 3.4ms with a 4.88mV resolution. Voltages above the maximum register value are reported as the maximum value. Figure 8 shows the voltage register format.

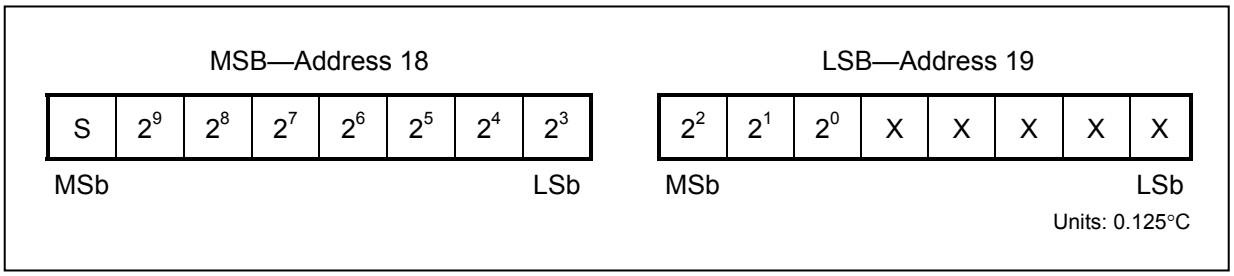
Figure 8. Voltage Register Format



TEMPERATURE MEASUREMENT

The DS2764 uses an integrated temperature sensor to continually measure battery temperature. Temperature measurements are placed in the temperature register every 220ms in two's-complement format with a 0.125°C resolution over a ±127°C range. Figure 9 shows the temperature register format.

Figure 9. Temperature Register Format



POWER SWITCH INPUT

The DS2764 provides a power control function that uses the discharge protection FET to gate battery power to the system. The $\overline{PS}$ pin, internally pulled to V_{DD} through a 1µA current source, is continuously monitored for a low-impedance connection to V_{SS}. If the DS2764 is in sleep mode, the detection of a low on the $\overline{PS}$ pin causes the device to transition into active mode, turning on the discharge FET. If the DS2764 is already in active mode, activity on $\overline{PS}$ has no effect on the FET control.

The host system has the option of monitoring activity on the $\overline{PS}$ pin by reading the $\overline{PS}$ bit in the Special Feature Register. The $\overline{PS}$ bit latches a 0 value when a logic low occurs on the $\overline{PS}$ pin regardless of the operating mode of the DS2764. If the host intends to monitor future $\overline{PS}$ pin events, it must write a 1 to the $\overline{PS}$ bit to ensure that a subsequent low forced on the $\overline{PS}$ pin is latched into the $\overline{PS}$ bit. The $\overline{PS}$ bit value has no effect on operation of the DS2764 and can be ignored if $\overline{PS}$ pin monitoring is not required.

MEMORY

The DS2764 has a 256-byte linear address space. Registers for instrumentation, status, and control are mapped in the lower 32 bytes, with lockable EEPROM blocks and the unique ROM ID occupying portions of the remaining address space. The Function Command Register occupies location FEh. All EEPROM memory is general purpose except byte addresses 31h, 32h and 33h, which should be written with the default values for the Status register, 2-Wire slave address and Current Offset register, respectively. When reading two-byte registers, (Current, ACR, Voltage and Temperature), the MSB should be read first. When the MSB of two-byte registers is read, the MSB and LSB are latched simultaneously and held for the duration of the Read Data transaction. This prevents register updates during the read and ensures synchronization between the MSB and LSB of two byte register values. For consistent results, always read the MSB and the LSB of a two-byte register during the same Read Data transaction.

EEPROM memory is shadowed by RAM to eliminate programming delays between writes and to allow the data to be verified by the host system before being copied to EEPROM. The Read Data and Write Data protocols to/from EEPROM memory addresses access the shadow RAM. The Recall Data function command transfers data from the EEPROM to the shadow RAM. The Copy Data function command transfers data from the shadow RAM to the EEPROM and requires t_{EEC} to complete programming of the EEPROM cells. In unlocked EEPROM blocks, writing data updates shadow RAM. In locked EEPROM blocks, attempts to write data are ignored. The Copy Data function command copies the contents of shadow RAM to EEPROM in an unlocked block of EEPROM but has no effect on locked blocks. The Recall Data function command copies the contents of a block of EEPROM to shadow RAM regardless of whether the block is locked or not.

Figure 10. EEPROM Access via Shadow RAM

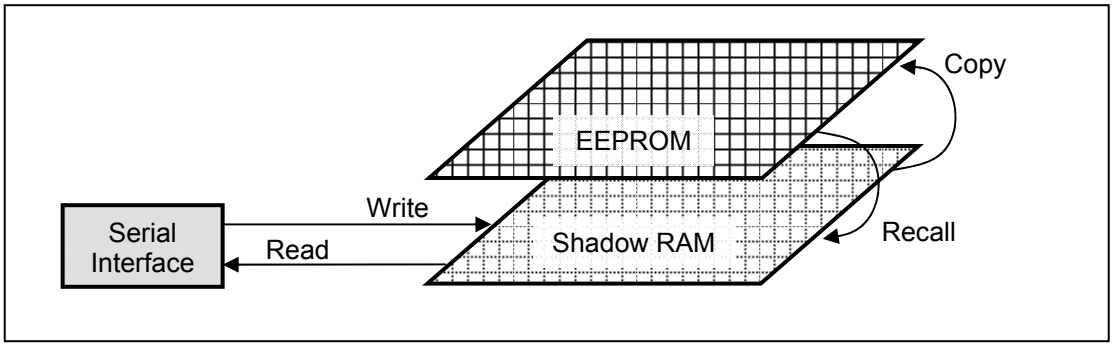


Table 2. Memory Map

ADDRESS (HEX)	DESCRIPTION	READ/WRITE
00	Protection Register	R/W
01	Status Register	R
02–06	Reserved	
07	EEPROM Register	R/W
08	Special Feature Register	R/W
09–0B	Reserved	
0C	Voltage Register MSB	R
0D	Voltage Register LSB	R
0E	Current Register MSB	R
0F	Current Register LSB	R
10	Accumulated Current Register MSB	R/W
11	Accumulated Current Register LSB	R/W
12–17	Reserved	
18	Temperature Register MSB	R
19	Temperature Register LSB	R
1A–1F	Reserved	
20–2F	EEPROM, block 0	R/W*
30–3F	EEPROM, block 1	R/W*
40–47	EEPROM, block 2	R/W*
50–EF	Reserved	
F0–F7	Unique ID	R+
F8–FD	Reserved	
FE	Function Command Register	W
FF	Reserved	

** Each EEPROM block is read/write until locked by the LOCK command, after which it is read-only.*

+ Unique 64 bit ID is a factory option available by special order. Units with IDs do not allow access to block 2 of user EEPROM

PROTECTION REGISTER

The protection register consists of flags that indicate protection circuit status and switches that give conditional control over the charging and discharging paths. Bits OV, UV, COC, and DOC are set when corresponding protection conditions occur and remain set until cleared by the host system. The default values of the CE and DE bits of the protection register are stored in lockable EEPROM in the corresponding bits in address 30h. A recall data command for EEPROM block 1 recalls the default values into CE and DE. Figure 11 shows the format of the protection register. The function of each bit is described in detail in the following paragraphs.

Figure 11. Protection Register Format

ADDRESS 00

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OV	UV	COC	DOC	$\overline{CC}$	$\overline{DC}$	CE	DE

OV—Overvoltage Flag. When set to 1, this bit indicates the battery pack has experienced an overvoltage condition. This bit must be reset by the host system.

UV—Undervoltage Flag. When set to 1, this bit indicates the battery pack has experienced an undervoltage condition. This bit must be reset by the host system.

COC—Charge Overcurrent Flag. When set to 1, this bit indicates the battery pack has experienced a charge-direction overcurrent condition. This bit must be reset by the host system.

DOC—Discharge Overcurrent Flag. When set to 1, this bit indicates the battery pack has experienced a discharge-direction overcurrent condition. This bit must be reset by the host system.

$\overline{CC}$—$\overline{CC}$ Pin Mirror. This read-only bit mirrors the state of the $\overline{CC}$ output pin.

$\overline{DC}$—$\overline{DC}$ Pin Mirror. This read-only bit mirrors the state of the $\overline{DC}$ output pin.

CE—Charge Enable. Writing a 0 to this bit disables charging ($\overline{CC}$ output high, external charge FET off) regardless of cell or pack conditions. Writing a 1 to this bit enables charging, subject to override by the presence of any protection conditions. The DS2764 automatically sets this bit to 1 when it transitions from sleep mode to active mode.

DE—Discharge Enable. Writing a 0 to this bit disables discharging ($\overline{DC}$ output high, external discharge FET off) regardless of cell or pack conditions. Writing a 1 to this bit enables discharging, subject to override by the presence of any protection conditions. The DS2764 automatically sets this bit to 1 when it transitions from sleep mode to active mode.

STATUS REGISTER

The read-only Status register shows the status of bits which enable or disable selected functions of the DS2764. Functions are enabled or disabled by programming a default value for the corresponding bits in lockable EEPROM address 31h. After writing the desired value to 31h, the Copy Data and Recall Data commands for EEPROM block 1 are required to transfer the default values into the status register bits and activate the selected functions. The selected functions become the default mode of the DS2764 since a recall from block 1 occurs on power-up. The format of the Status register is shown in Figure 12.

Figure 12. Status Register Format

ADDRESS 01

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	PMOD	X	X	X	X	X

X—Reserved Bits.

PMOD—Sleep Mode Enable. A value of 1 in this bit enables the DS2764 to enter sleep mode when the bus is low for greater than 2s and to leave sleep mode when the SCL OR SDA line goes high. A value of 0 disables bus-related transitions into and out of sleep mode. This bit is read-only. The desired default value should be set in bit 5 of address 31h. The factory default is 0.

EEPROM REGISTER

The format of the EEPROM register is shown in Figure 13. The function of each bit is described in detail in the following paragraphs.

Figure 13. EEPROM Register Format

ADDRESS 07

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EEC	LOCK	X	X	X	BL2	BL1	BL0

EEC—EEPROM Copy Flag. A 1 in this read-only bit indicates that a Copy Data or Lock function command is in progress. While this bit is high, writes to EEPROM addresses are ignored and Copy Data and Lock function commands cannot be issued. A 0 in this bit indicates that data may be written to unlocked EEPROM blocks.

LOCK—EEPROM Lock Enable. When this bit is 0, the Lock function command is ignored. Writing a 1 to this bit enables the Lock function command. After the Lock function command is executed, the LOCK bit is reset to 0. The factory default is 0.

BL2—EEPROM Block 2 Lock Flag. A 1 in this read-only bit indicates that EEPROM block 2 (addresses 40 to 47) is locked (read-only) while a 0 indicates block 2 is unlocked (read/write). The special order unique 64-bit ID device does not support EEPROM Block 2.

BL1—EEPROM Block 1 Lock Flag. A 1 in this read-only bit indicates that EEPROM block 1 (addresses 30 to 3F) is locked (read-only) while a 0 indicates block 1 is unlocked (read/write).

BL0—EEPROM Block 0 Lock Flag. A 1 in this read-only bit indicates that EEPROM block 0 (addresses 20 to 2F) is locked (read-only) while a 0 indicates block 0 is unlocked (read/write).

X—Reserved Bits.

SPECIAL FEATURE REGISTER

The format of the special feature register is shown in Figure 14. The function of each bit is described in detail in the following paragraphs.

Figure 14. Special Feature Register Format

ADDRESS 08

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{PS}$	X	X	X	X	X	SAWE	X

$\overline{PS}$—$\overline{PS}$ Pin Latch. This bit latches a low state on the $\overline{PS}$ pin with a 0 value. The bit is cleared only by writing a 1 to this location. See the Power Switch Input section.

SAWE—Slave Address Write Enable. This bit must be set to 1 before the 2-wire slave address in location 0x32 can be modified. SAWE should be written back to 0 after writing the slave address. Power up default is 0.

X—Reserved Bits.

PROGRAMMABLE SLAVE ADDRESS

The 2-Wire slave address of the DS2764 is stored in lockable EEPROM block 1, address 32h. Programming the slave address requires a write to set the SAWE bit in the Special Feature register, followed by a write to 32h with the desired slave address. The new slave address value is effective following the write to 32h, and must be used to address the DS2764 on subsequent bus transactions. The slave address value is not stored to EEPROM until a Copy EEPROM block 1 command is executed. Prior to executing the Copy command, power cycling the DS2764 restores the original slave address value. The data format of the slave address value in address 32h is shown in Figure 15.

Figure 15. Slave Address Format

ADDRESS 32

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
A6	A5	A4	A3	A2	A1	A0	X

A6 to A0—Slave Address. A6-A0 contains the 7-bit slave address of the DS2764. The factory default is 0110100b.

X—Reserved Bits.

2-WIRE BUS SYSTEM

The 2-Wire bus system supports operation as a slave only device in a single or multi-slave, and single or multi-master system. Up to 128 slave devices may share the bus by uniquely setting the 7-bit slave address. The 2-wire interface consists of a serial data line (SDA) and serial clock line (SCL). SDA and SCL provide bidirectional communication between the DS2764 slave device and a master device at speeds up to 100kHz. The DS2764's SDA pin operates bi-directionally, that is, when the DS2764 receives data, SDA operates as an input, and when the DS2764 returns data, SDA operates as an open drain output, with the host system providing a resistive pull-up. The DS2764 always operates as a slave device, receiving and transmitting data under the control of a master device. The master initiates all transactions on the bus and generates the SCL signal as well as the START and STOP bits which begin and end each transaction.

Bit Transfer

One data bit is transferred during each SCL clock cycle, with the cycle defined by SCL transitioning low-to-high and then high-to-low. The SDA logic level must remain stable during the high period of the SCL clock pulse. Any change in SDA when SCL is high is interpreted as a START or STOP control signal.

Bus Idle

The bus is defined to be idle, or not busy, when no master device has control. Both SDA and SCL remain high when the bus is idle. The STOP condition is the proper method to return the bus to the idle state.

START and STOP Conditions

The master initiates transactions with a START condition (S), by forcing a high-to-low transition on SDA while SCL is high. The master terminates a transaction with a STOP condition (P), a low-to-high transition on SDA while SCL is high. A Repeated START condition (Sr) can be used in place of a STOP then START sequence to terminate one transaction and begin another without returning the bus to the idle state. In multi-master systems, a Repeated START allows the master to retain control of the bus. The START and STOP conditions are the only bus activities in which the SDA transitions when SCL is high.

Acknowledge Bits

Each byte of a data transfer is acknowledged with an Acknowledge bit (A) or a No Acknowledge bit (N). Both the master and the DS2764 slave generate acknowledge bits. To generate an Acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low until SCL returns low. To generate a No Acknowledge (also called NAK), the receiver releases SDA before the rising edge of the acknowledge-related clock pulse and leaves SDA high until SCL returns low. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer can occur if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should re-attempt communication.

Data Order

A byte of data consists of 8 bits ordered most significant bit (msb) first. The least significant bit (lsb) of each byte is followed by the Acknowledge bit. DS2764 registers composed of multi-byte values are ordered most significant byte (MSB) first. The MSB of multi-byte registers is stored on even data memory addresses.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by a Slave Address (SAddr) and the read/write (R/W) bit. When the bus is idle, the DS2764 continuously monitors for a START condition followed by its slave address. When the DS2764 receives a slave address that matches the value in its Programmable Slave Address register, it responds with an Acknowledge bit during the clock period following the R/W bit. The 7-bit Programmable Slave Address register is factory programmed to 0110100. The slave address can be re-programmed, refer to the Programmable Slave Address section for details.

Read/Write Bit

The R/W bit following the slave address determines the data direction of subsequent bytes in the transfer. R/W = 0 selects a write transaction, with the following bytes being written by the master to the slave. R/W = 1 selects a read transaction, with the following bytes being read from the stave by the master.

Bus Timing
The DS2764 is compatible with any bus timing up to 100kHz. No special configuration is required to operate at any speed.

2-Wire Command Protocols
The command protocols involve several transaction formats. The simplest format consists of the master writing the START bit, slave address, R/W bit, and then monitoring the acknowledge bit for presence of the DS2764. More complex formats such as the Write Data, Read Data and Function command protocols write data, read data and execute device specific operations. All bytes in each command format require the slave or host to return an Acknowledge bit before continuing with the next byte. Each function command definition outlines the required transaction format. The following key applies to the transaction formats.

Table 3. 2-Wire Protocol Key

KEY	DESCRIPTION	KEY	DESCRIPTION
S	START bit	Sr	Repeated START
SAddr	Slave Address (7-bit)	W	R/W bit = 0
FCmd	Function Command byte	R	R/W bit = 1
MAddr	Memory Address byte	P	STOP bit
Data	Data byte written by master	Data	Data byte returned by slave
A	Acknowledge bit - Master	A	Acknowledge bit—Slave
N	No Acknowledge - Master	N	No Acknowledge—Slave

Basic Transaction Formats

Write: S SAddr W A MAddr A Data0 A P

A write transaction transfers one or more data bytes *to* the DS2764. The data transfer begins at the memory address supplied in the MAddr byte. Control of the SDA signal is retained by the master throughout the transaction, except for the Acknowledge cycles.

Read: S SAddr W A MAddr A Sr SAddr R A Data0 N P

Write Portion Read Portion

A read transaction transfers one or more bytes *from* the DS2764. Read transactions are composed of two parts, a write portion followed by a read portion, and is therefore inherently longer than a write transaction. The write portion communicates the starting point for the read operation. The read portion follows immediately, beginning with a Repeated START, Slave Address with R/W set to a 1. Control of SDA is assumed by the DS2764 beginning with the Slave Address Acknowledge cycle. Control of the SDA signal is retained by the DS2764 throughout the transaction, except for the Acknowledge cycles. The master indicates the end of a read transaction by responding to the last byte it requires with a No Acknowledge. This signals the DS2764 that control of SDA is to remain with the master following the Acknowledge clock.

Write Data Protocol
The write data protocol is used to write to register and shadow RAM data to the DS2764 starting at memory address MAddr. Data0 represents the data written to MAddr, Data1 represents the data written to MAddr + 1 and DataN represents the last data byte, written to MAddr + N. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit.

S SAddr W A MAddr A Data0 A Data1 A … DataN A P

The msb of the data to be stored at address MAddr can be written immediately after the MAddr byte is acknowledged. Because the address is automatically incremented after the least significant bit (lsb) of each byte is received by the DS2764, the msb of the data at address MAddr + 1 is can be written immediately after the acknowledgement of the data at address MAddr. If the bus master continues an auto-incremented write transaction beyond address 4Fh, the DS2764 ignores the data. Data is also ignored on writes to read-only addresses and reserved addresses, locked EEPROM blocks as well as a write that auto increments to the Function Command register (address FEh). Incomplete bytes and bytes that are Not Acknowledged by the DS2764 are not written to memory. As noted in the Memory Section, writes to unlocked EEPROM blocks modify the shadow RAM only.

Read Data Protocol

The Read Data protocol is used to read register and shadow RAM data from the DS2764 starting at memory address specified by MAddr. Data0 represents the data byte in memory location MAddr, Data1 represents the data from MAddr + 1 and DataN represents the last byte read by the master.

S SAddr W A MAddr A Sr SAddr R A Data0 A Data1 A … DataN N P

Data is returned beginning with the most significant bit (msb) of the data in MAddr. Because the address is automatically incremented after the least significant bit (lsb) of each byte is returned, the msb of the data at address MAddr + 1 is available to the host immediately after the acknowledgement of the data at address MAddr. If the bus master continues to read beyond address FFh, the DS2764 outputs data values of FFh. Addresses labeled "Reserved" in the memory map return undefined data. The bus master terminates the read transaction at any byte boundary by issuing a No Acknowledge followed by a STOP or Repeated START.

Function Command Protocol

The Function Command protocol executes a device specific operation by writing one of the function command values (FCmd) to memory address FEh. Table 4 lists the DS2764 FCmd values and describes the actions taken by each. A one byte write protocol is used to transmit the function command, with the MAddr set to FEh and the data byte set to the desired FCmd value. Additional data bytes are ignored. Data read from memory address FEh is undefined.

S SAddr W A MAddr=0FEh A FCmd A P

Table 4. Function Commands

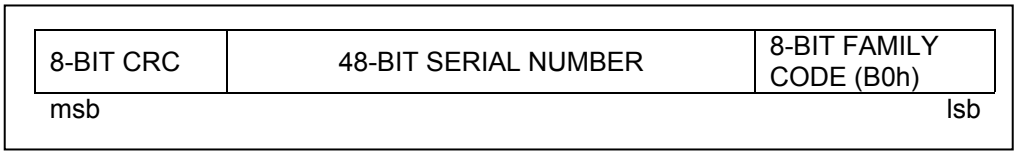
FUNCTION COMMAND	TARGET EEPROM BLOCK	FCMD VALUE	DESCRIPTION
Copy Data	0	42h	This command copies the shadow RAM to the target EEPROM block. Copy Data commands that target locked blocks are ignored. While the Copy Data command is executing, the EEC bit in the EEPROM register is set to 1, and Write Data commands with MAddr set to any address within the target block are ignored. Read Data and Write Data commands with MAddr set outside the target block are processed while the copy is in progress. The Copy Data command execution time, t_{EEC}, is 2ms typical and starts after the FCMD byte is acknowledged. Subsequent Copy or Lock commands must be delayed until the EEPROM programming cycle completes.
	1	44h	
	2	48h	
Recall Data	0	B2h	This command recalls the contents of the targeted EEPROM block to its shadow RAM.
	1	B4h	
	2	B8h	
Lock	0	63h	This command locks (write-protects) the targeted EEPROM block. The LOCK bit in the EEPROM register must be set to 1 before the lock command is executed. If the LOCK bit is 0, the lock command has no effect. The lock command is permanent; a locked block can never be written again. The Lock command execution time, t_{EEC}, is 2ms typical and starts after the FCMD byte is acknowledged. Subsequent Copy or Lock commands must be delayed until the EEPROM programming cycle completes.
	1	66h	
	2	6Ah	

Note: EEPROM block 2 is not supported on special order devices with unique IDs.

64-BIT UNIQUE ID

The DS2764 can be special ordered with a unique, factory-programmed ID that is 64 bits in length. The first eight bits are the product family code (B0h for DS2764). The next 48 bits are a unique 40-bit serial number followed by 0x64h. The last eight bits are a cyclic redundancy check (CRC) of the first 56 bits (see Figure 16). The 64-bit ID can be read as 8 bytes starting at memory address F0h. The 64-bit ID is read only.

Figure 16. 64-BIT ID FORMAT



SELECTOR GUIDE

PART	MARKING	PACKAGE INFORMATION
DS2764AE+	DS2764A	TSSOP, External Sense Resistor, 4.275V V_{OV}
DS2764BE+	DS2764B	TSSOP, External Sense Resistor, 4.35V V_{OV}
DS2764AE+T&R	DS2764A	DS2764AE+ on Tape-and-Reel
DS2764BE+T&R	DS2764B	DS2764BE+ on Tape-and-Reel
DS2764AE+025*	2764A25	TSSOP, 25mΩ Sense Resistor, 4.275V V_{OV}
DS2764BE+025*	2764B25	TSSOP, 25mΩ Sense Resistor, 4.35V V_{OV}
DS2764AE+025/T&R*	2764A25	DS2764AE+025 in Tape-and-Reel
DS2764BE+025/T&R*	2764B25	DS2764BE+025 in Tape-and-Reel
DS2764AX-025/T&R*	DS2764AR	Flip-Chip, 25mΩ Sense Resistor, Tape-and-Reel, 4.275V V_{OV}
DS2764BX-025/T&R*	DS2764BR	Flip-Chip, 25mΩ Sense Resistor, Tape-and-Reel, 4.35V V_{OV}
DS2764AX/T&R*	DS2764A	Flip-Chip, External Sense Resistor, Tape-and-Reel, 4.275V V_{OV}
DS2764BX/T&R*	DS2764B	Flip-Chip, External Sense Resistor, Tape-and-Reel, 4.35V V_{OV}

**Denotes option available at a future date; contact factory for availability.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.

Note 1: Additional V_{OV} options are available, contact the factory.
Note 2: To order devices with the unique 64-bit ID option, contact the factory.

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600