The second function the DS1832 performs is pushbutton reset control. The DS1832 debounces the pushbutton input and guarantees an active reset pulse width of 250 ms minimum. The third function is a watchdog timer. The DS1832 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to timeout. The watchdog timer function can be set to operate on timeout settings of approximately 150 ms, 600 ms, or 1.2 seconds.

OPERATION - POWER MONITOR

The DS1832 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL, the V_{CC} comparator outputs the signals RST and $\overline{RST}$. When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 2.98 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 2.64 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

OPERATION - PUSHBUTTON RESET

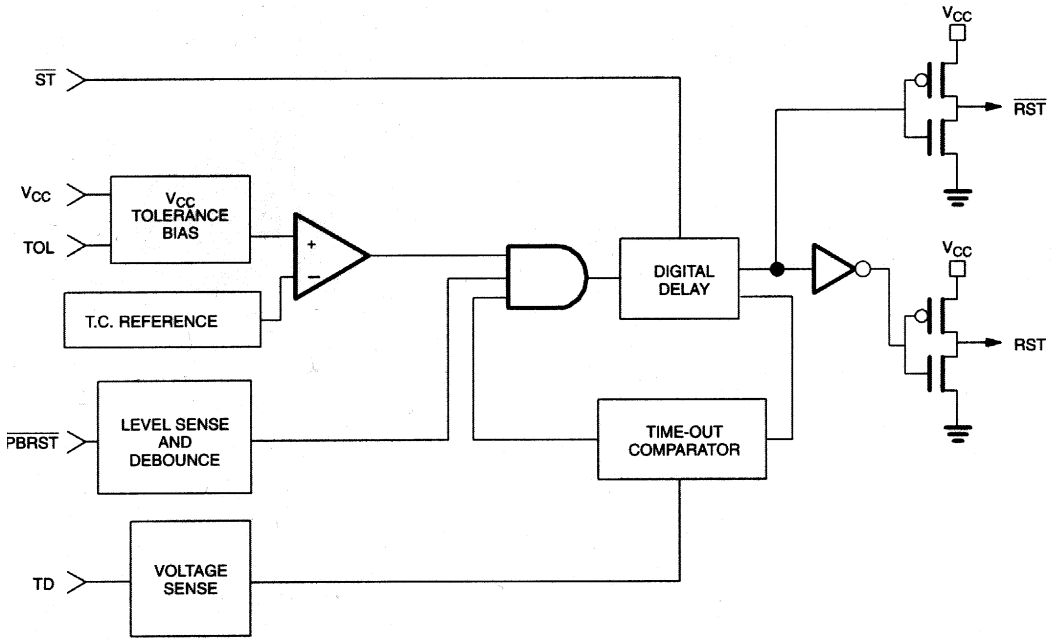
The DS1832 provides an input pin for direct connection to a pushbutton reset (see Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 250 ms minimum are generated. The 250 ms delay commences as the pushbutton reset input is released from the low level.

OPERATION - WATCHDOG TIMER

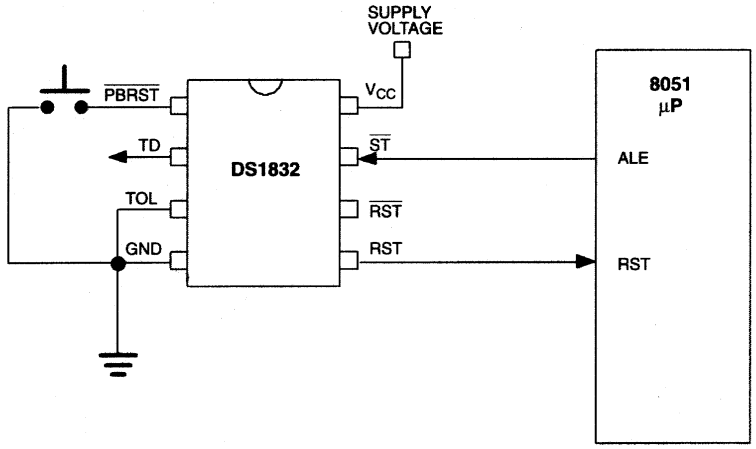
The watchdog timer function forces RST and $\overline{RST}$ signals active when the $\overline{ST}$ input is not clocked within the predetermined time period. The timeout period is determined by the condition of the TD pin. If TD is connected to ground the minimum watchdog timeout would be 62.5 ms, TD floating would yield a minimum timeout of 250 ms, and TD connected to V_{CC} would provide a timeout of 500 ms minimum. Timeout of the watchdog starts when RST and $\overline{RST}$ become inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to timeout, the watchdog timer is reset and begins to timeout again. If the watchdog timer is allowed to timeout, then the RST and $\overline{RST}$ signals are driven active for a minimum of 250 ms. The $\overline{ST}$ input can be derived from many microprocessor outputs. The most typical signals used are the microprocessor address signals, data signals or control signals. When the microprocessor functions normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to timeout. To guarantee that the watchdog timer does not timeout, a high-to-low transition must occur at or less than the minimum times shown in Table 1. A typical circuit example is shown in Figure 4.

The DS1832 watchdog function cannot be disabled. The watchdog strobe input must be strobed to avoid a watchdog timeout and reset.

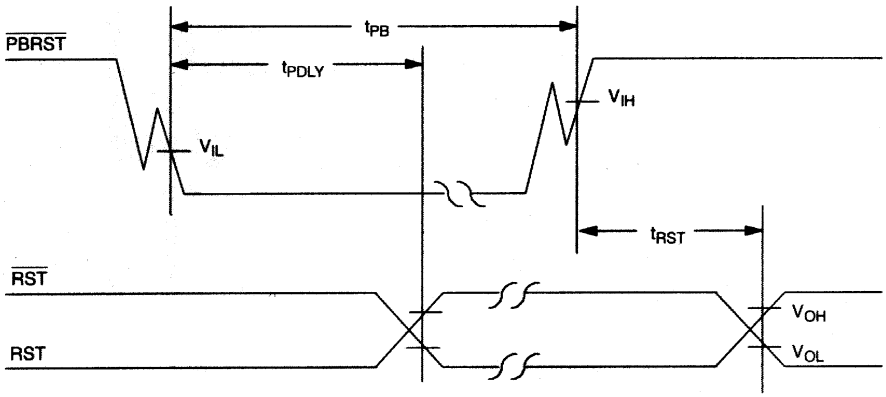
MICROMONITOR BLOCK DIAGRAM Figure 1



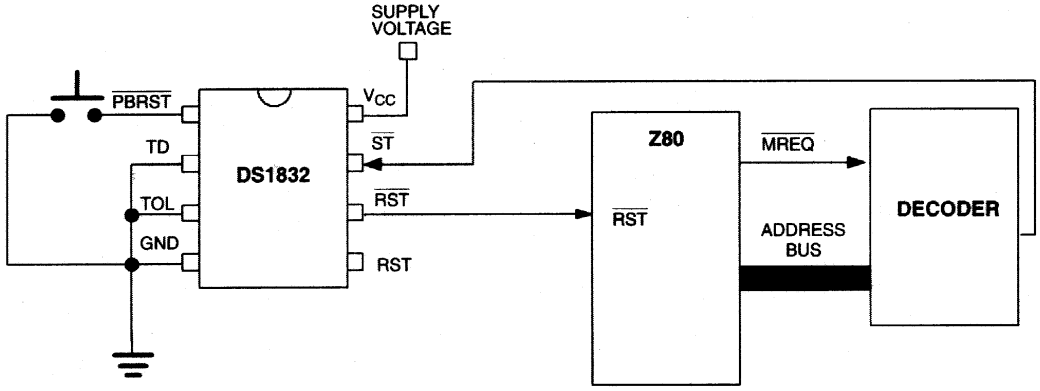
PUSHBUTTON RESET Figure 2



TIMING DIAGRAM: PUSHBUTTON RESET Figure 3



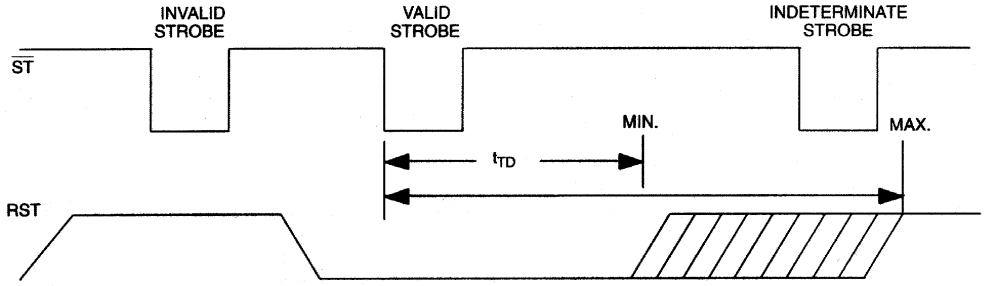
WATCHDOG TIMER Figure 4



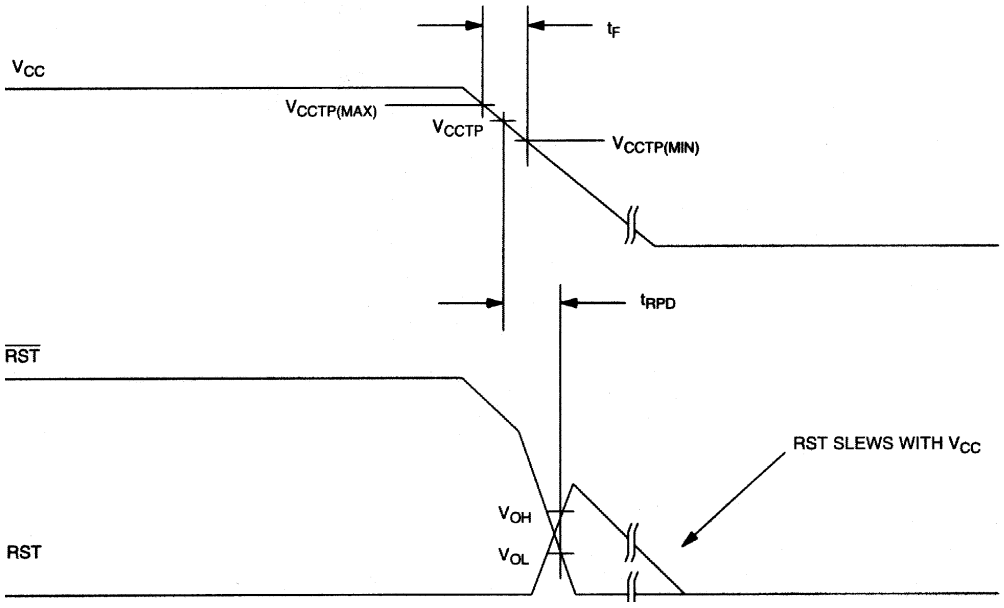
WATCHDOG TIMEOUTS Table 1

TD	TIMEOUT		
	MIN	**TYP**	**MAX**
GND	62.5 ms	150 ms	250 ms
Float	250 ms	600 ms	1000 ms
V_{CC}	500 ms	1200 ms	2000 ms

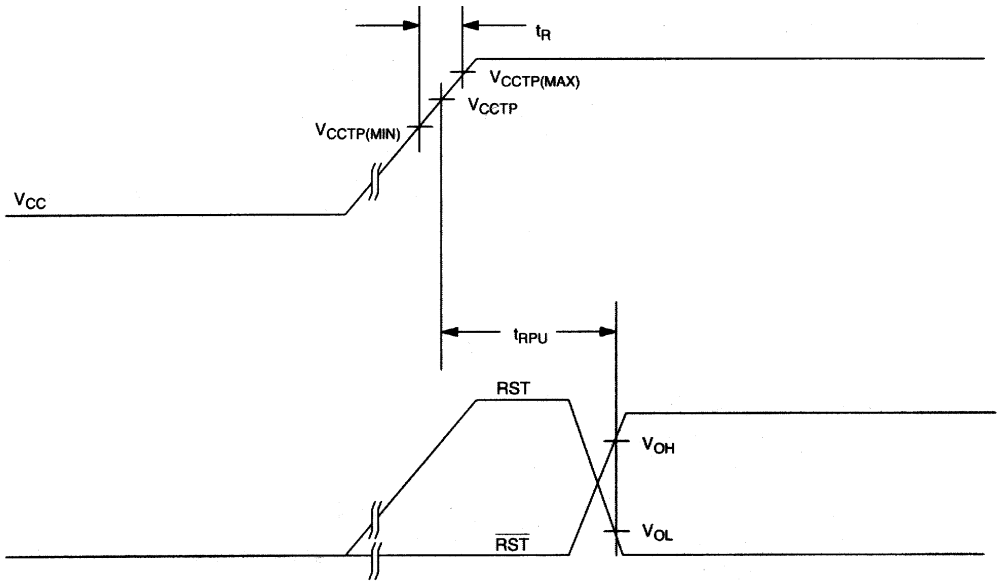
TIMING DIAGRAM: STROBE INPUT Figure 5



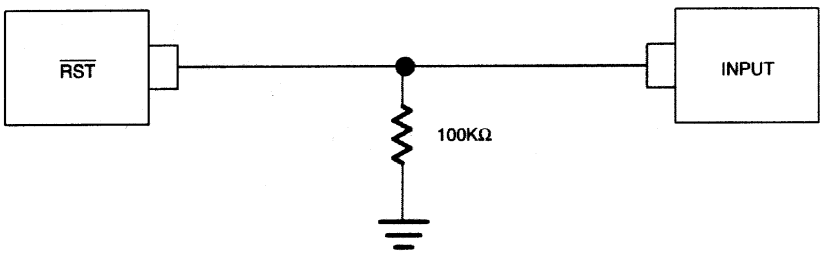
TIMING DIAGRAM: POWER DOWN Figure 6



TIMING DIAGRAM: POWER-UP Figure 7



$\overline{RST}$ VALID TO 0 VOLTS V_{CC} Figure 8



OUTPUT VALID CONDITIONS

The $\overline{RST}$ output uses a push-pull output which can maintain a valid output down to 0.8 volts V_{CC}. To sink current below 0.8 volts a resistor can be connected from $\overline{RST}$ to Ground (see Figure 8). This arrangement will maintain a valid value on $\overline{RST}$ during both power-up and power-down but will draw current when $\overline{RST}$ is in the high state. A value of about 100 kΩ should be adequate in most situations. The output with a resistor pull-down can maintain a valid reset down to V_{CC} equal to 0 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground	-0.5V to V_{CC} +0.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	1.0		5.5	V	1
$\overline{ST}$ and $\overline{PBRST}$ Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1, 3
		V_{CC} -0.4				1, 4
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}	-0.3		0.5	V	1

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC}=1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Trip Point (TOL = GND)	V_{CCTP}	2.80	2.88	2.97	V	1
V_{CC} Trip Point (TOL = V_{CC})	V_{CCTP}	2.47	2.55	2.64	V	1
Input Leakage	I_{IL}	-1.0		+1.0	µA	2
Output Current @ 2.4V	I_{OH}		350		µA	3
Output Current @ 0.4V	I_{OL}	10			mA	3
Output Voltage @ -500 uA	V_{OH}	V_{CC} -0.3V	V_{CC} -0.1V		V	4
Operating Current	I_{CC}			35	µA	5

CAPACITANCE (t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC}=1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	20			ms	
RESET Active Time	t_{RST}	250	610	1000	ms	
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	6, 7
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}		5	8	µs	8
V_{CC} Slew Rate	t_F	20			µs	
V_{CC} Detect to RST and $\overline{RST}$	t_{RPU}	250	610	1000	ms	9
V_{CC} Slew Rate	t_R	0			ns	
$\overline{PBRST}$ Stable Low to $\overline{RST}$ and RST	t_{PDLY}			20	ms	

NOTES:

1. All voltages referenced to ground.
2. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 40 kΩ typical.
3. Measured with $V_{CC} \geq 2.7V$.
4. Measured with $V_{CC} < 2.7V$.
5. Measured with outputs open, $V_{CC} \leq 3.6$ volts, and all inputs at V_{CC} or Ground.
6. Must not exceed t_{TD} minimum.
7. The Watchdog cannot be disabled it must be strobed to avoid resets.
8. Noise immunity - Pulses < 2 µs at V_{CCTP} minimum will not cause a reset.
9. t_R = 5 µs.

MARKING INFORMATION:

8-pin DIP - “DS1832”
8-pin SOIC - “DS1832”
8-pin - µ-SOP - “1832”