ORDERING INFORMATION

Temp Range	Package	Part Number
DG467/DG468		
- 40 °C to 85 °C	6-Pin TSOP	DG467DV-T1-E3
		DG468DV-T1-E3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter Referenced To V-		Symbol	Limit	Unit
V+			44	V
GND			25	
Digital Inputs[a], $V_{NO/NC}$, V_{COM}			(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Current, (Any Terminal) Continuous			30	mA
Current (NO or NC or COM) Pulsed at 1 ms, 10 % duty cycle			100	
Storage Temperature			- 65 to 150	°C
Power Dissipation (Package)[b]	6-Pin TSOP[c]		570	mW

Notes:
a. Signals on NO, NC, COM, or IN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 7 mW/°C above 70 °C.

For technical questions, contact: analogswitchtechsuoort@vishay.com
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SPECIFICATIONS[a] (V ± = ± 15 V)							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 15 V, V- = - 15 V V_{IN} = 2.4 V, 0.8 V[f]	**Temp.**[b]	**D Suffix** - 40 °C to 85 °C **Min.**[d]	**Typ.**[c]	**Max.**[d]	**Unit**
Analog Switch							
Analog Signal Range[eron]	V_{ANALOG}		Full	- 15		15	V
Drain-Source On-Resistance	R_{ON}	$I_{NO/NC}$ = 10 mA, V_{COM} = 10 V V+ = 13.5 V, V- = - 13.5 V	Room Full		7	9 10	Ω
On-Resistance Flatness	R_{ON} Flatness	$I_{NO/NC}$ = 10 mA, V_{COM} = ± 5 V, 0 V V+ = 13.5 V, V- = - 13.5 V	Room Full		0.7	1 2	Ω
Switch Off Leakage Current	$I_{NO/NC(off)}$	V+ = 16.5, V- = - 16.5 V V_{COM} = ± 15.5 V $V_{NO/NC}$ = -/+ 15.5 V	Room Full	- 1 - 10	- 0.1	1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10	- 0.1	1 10	
Channel On Leakage Current	$I_{COM(on)}$	V+ = 16.5 V, V- = - 16.5 V_{COM} = $V_{NO/NC}$ = ± 15.5 V	Room Full	- 1 - 10	- 0.1	1 10	
Digital Control							
Input, High Voltage	V_{INH}		Full	2.4			V
Input, Low Voltage	V_{INL}		Full			0.8	
Input Capacitance[e]	C_{IN}		Room		5		pF
Input Current	I_{IN}	V_{IN} = 0 or 5 V		- 1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF $V_{NO/NC}$ = ± 10 V	Room Full		100	140 160	ns
Turn-Off Time	t_{OFF}		Room Full		50	80 100	
Charge Injection[e]	Q	C_L = 1 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		21		pC
Off-Isolation[e]	OIRR	C_L= 5 pF, R_L = 50 Ω, f = 1 MHz	Room		- 61		dB
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room		30		pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room		15		
Channel On Capacitance[e]	$C_{D(on)}$	f = 1 MHz	Room		76		
Power Supplies							
Positive Supply Current	I+	V+ = 16.5 V, V- = - 16.5 V V_{IN} = 0 or 5 V	Room Full		5	15 20	µA
Negative Supply Current	I-		Room Full	- 1 - 10	- 0.02		

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SPECIFICATIONS[a] (V+ = 12 V)							
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** V+ = 12 V, V- = 0 V V_{IN} = 2.4 V, 0.8 V[f]	**Temp.**[b]	**D Suffix** - 40 °C to 85 °C **Min.**[d]	**Typ.**[c]	**Max.**[d]	**Unit**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	0		12	V
Drain-Source On-Resistance	R_{ON}	$I_{NO/NC}$ = –10 mA, V_{COM} = 8 V V+ = 10.8 V	Room Full		12	16 20	Ω
On-Resistance Flatness	R_{ON} Flatness	$I_{NO/NC}$ = 10 mA, V_{COM} = 2, 6, 8 V V+ = 10.8 V	Room Full		1.5	3 4	Ω
Dynamic Characteristics							
Turn-On Time	t_{ON}	$V_{NO, NC}$ = ± 10 V, R_L = 300 Ω, C_L = 35 pF	Room Full		130	160 200	nS
Turn-Off Time	t_{OFF}		Room Full		50	80 100	
Charge Injection[e]	Q	C_L = 1 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		8		pC
Power Supplies							
Positive Supply Current	I+	V+ = 13.2 V, V_{IN} = 0 V, 5 V	Room Full		3	7 10	µA

Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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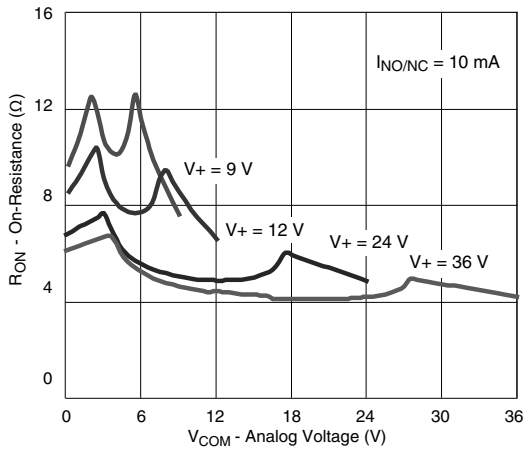
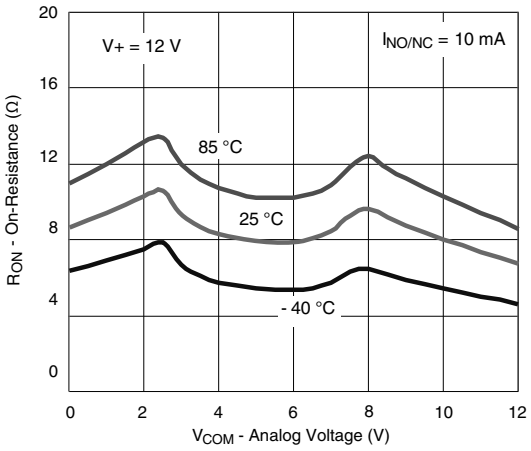
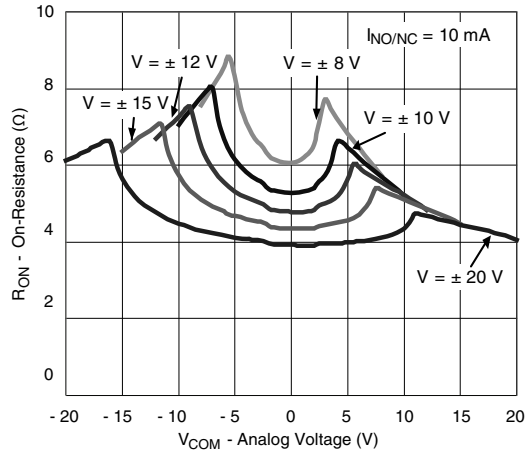


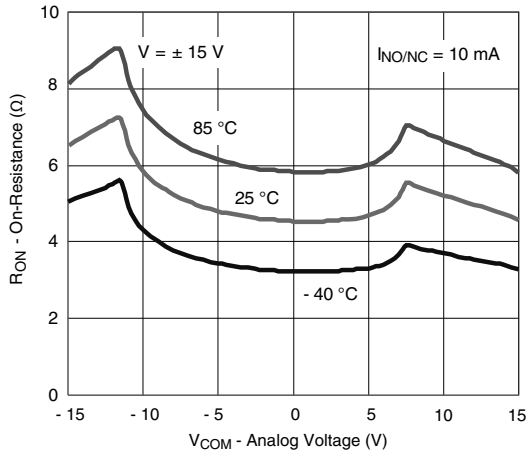
R_{ON} vs. V_{COM} and Single Supply Voltage



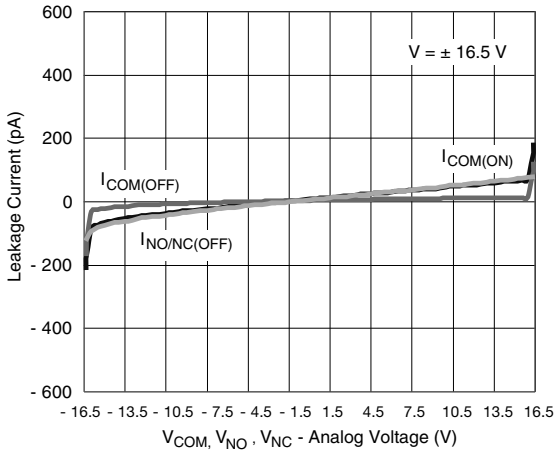
R_{ON} vs. Analog Voltage and Temperature



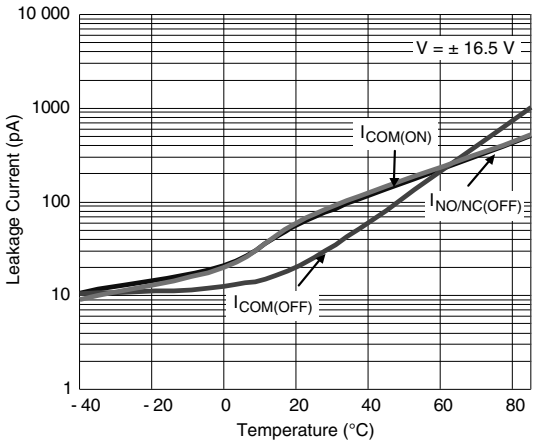
R_{ON} vs. V_{COM} and Dual Supply Voltage



R_{ON} vs. Analog Voltage and Temperature



Leakage vs. Analog Voltage



Leakage Current vs. Temperature

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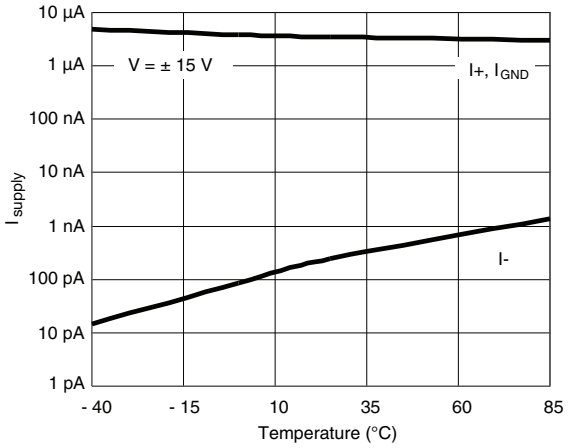
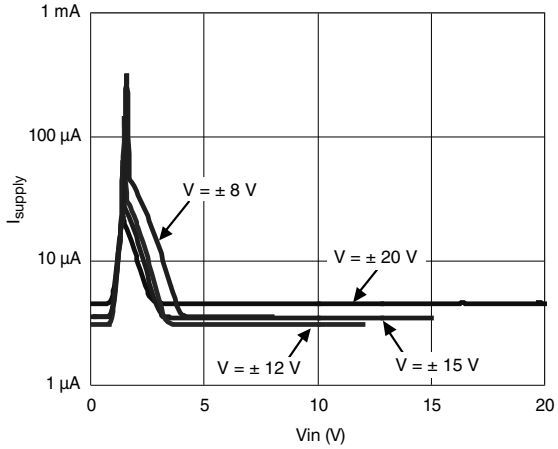
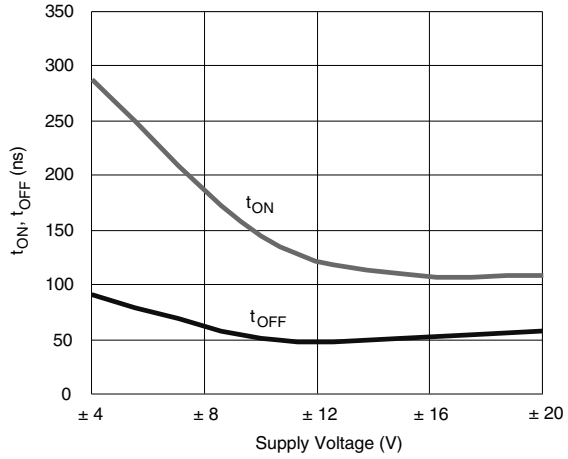


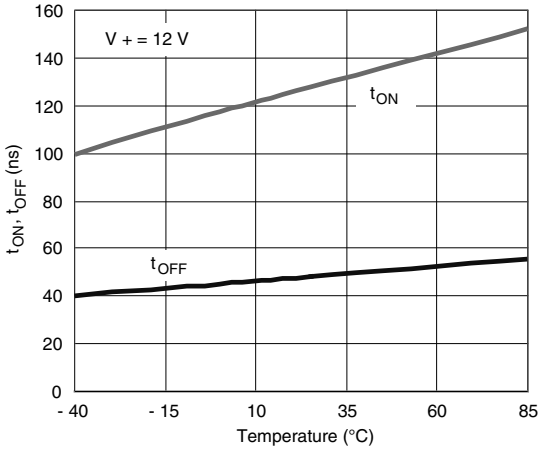
Supply Current vs. Temperature



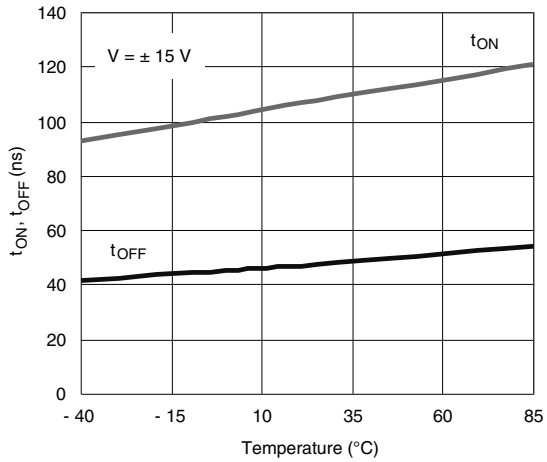
Supply Current vs. V_{IN}



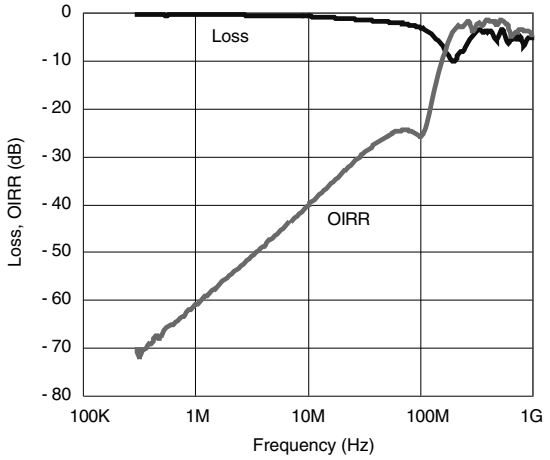
Switching Time vs. Supply Voltages



Switching Time vs. Temperature



Switching Time vs. Temperature



Off Isolation and Insertion Loss vs. Frequency

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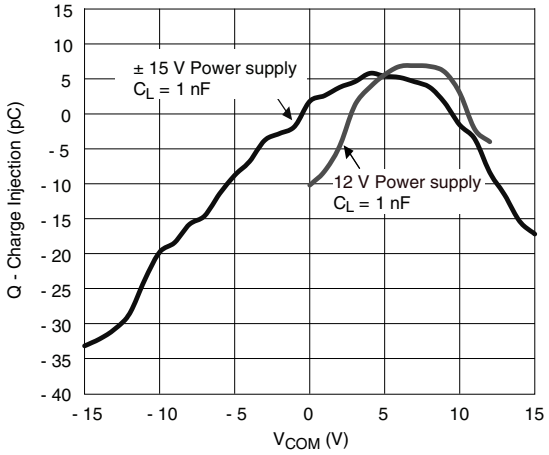
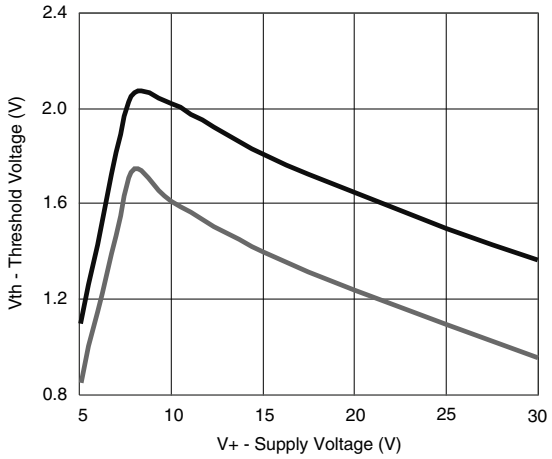


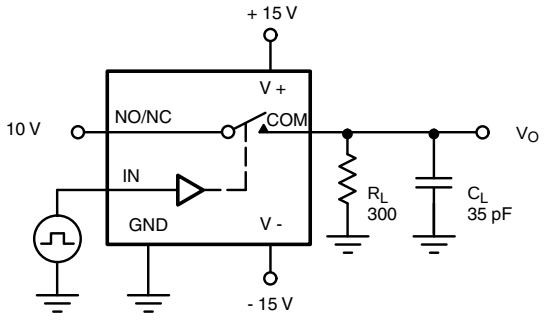
Charge Injection vs. Analog Voltage



Input Switching Threshold vs. Supply Voltage

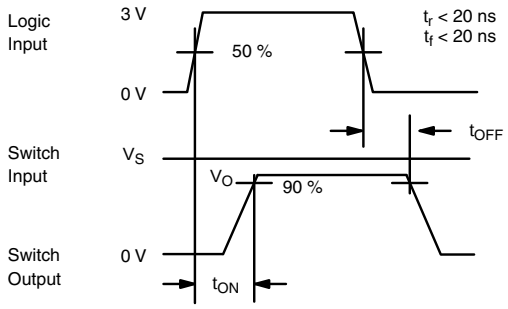
TEST CIRCUITS

V_O is the steady state output with the switch on.



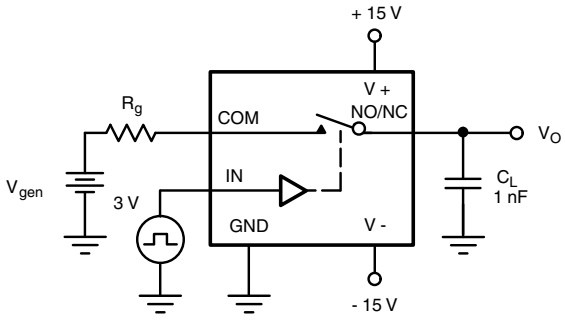
C_L (includes fixture and stray capacitance)

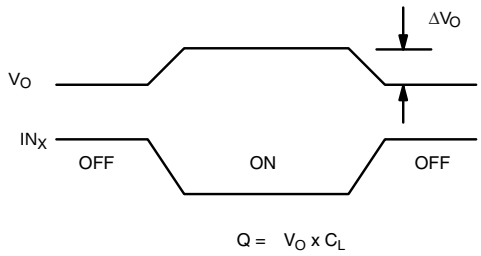
$$V_O = V_S \frac{R_L}{R_L + r_{ON}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 1. Switching Time





$$Q = V_O \times C_L$$

Figure 2. Charge Injection

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TEST CIRCUITS

V_O is the steady state output with the switch on.

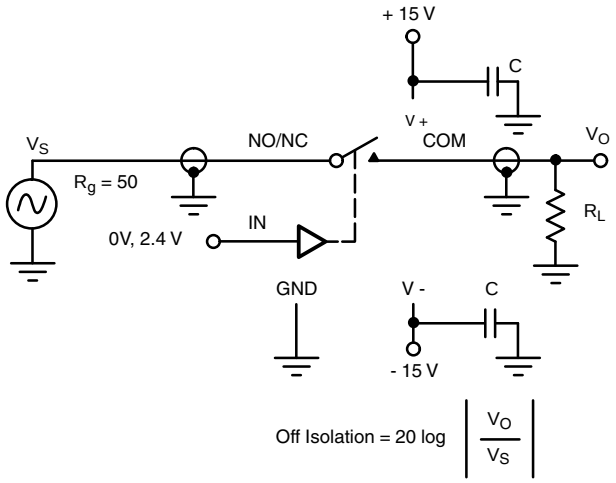

Figure 3. Off Isolation

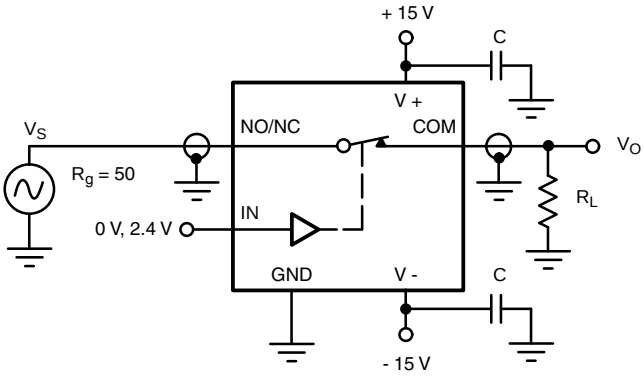

Figure 4. Insertion Loss

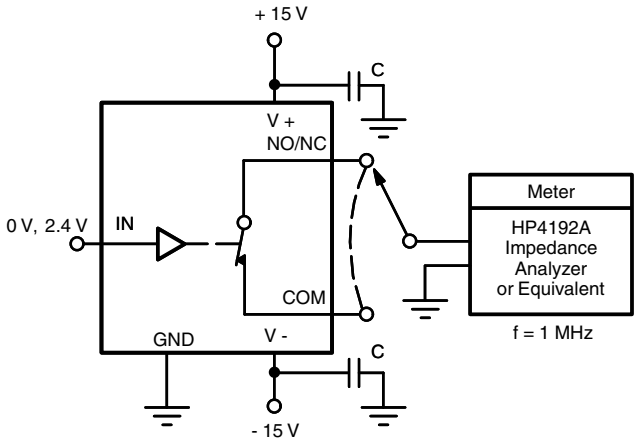

Figure 5. Source/Drain Capacitances

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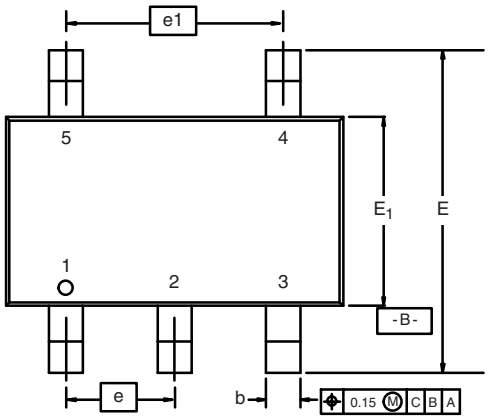
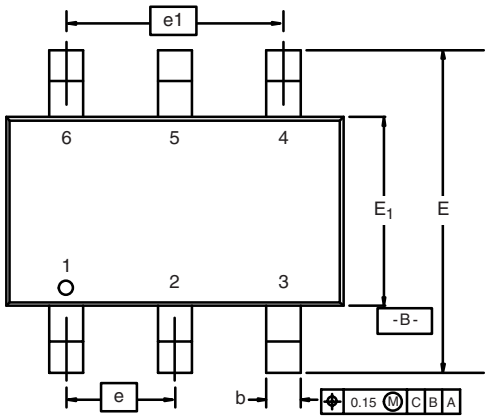
TSOP: 5/6–LEAD

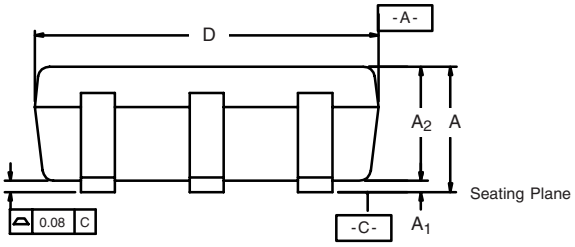
JEDEC Part Number: MO-193C

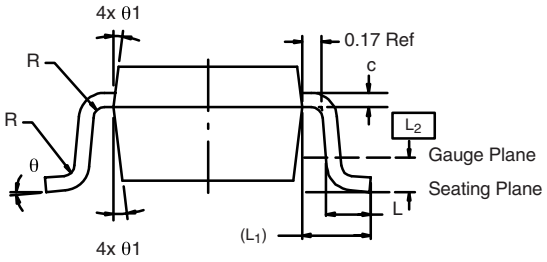


5-LEAD TSOP



6-LEAD TSOP





Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A_1	0.01	-	0.10	0.0004	-	0.004
A_2	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e_1	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L_1	0.60 Ref			0.024 Ref		
L_2	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
$θ_1$	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06 DWG: 5540						

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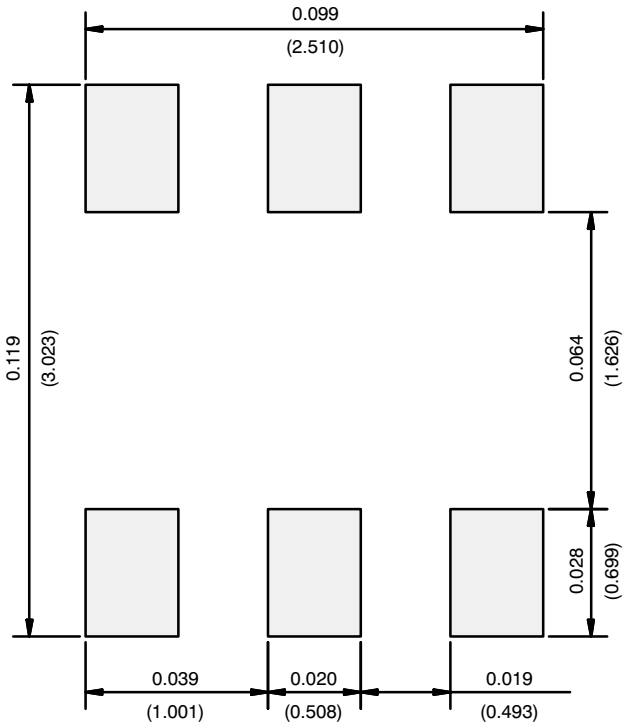
RECOMMENDED MINIMUM PADS FOR TSOP-6



Recommended Minimum Pads
Dimensions in Inches/(mm)

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