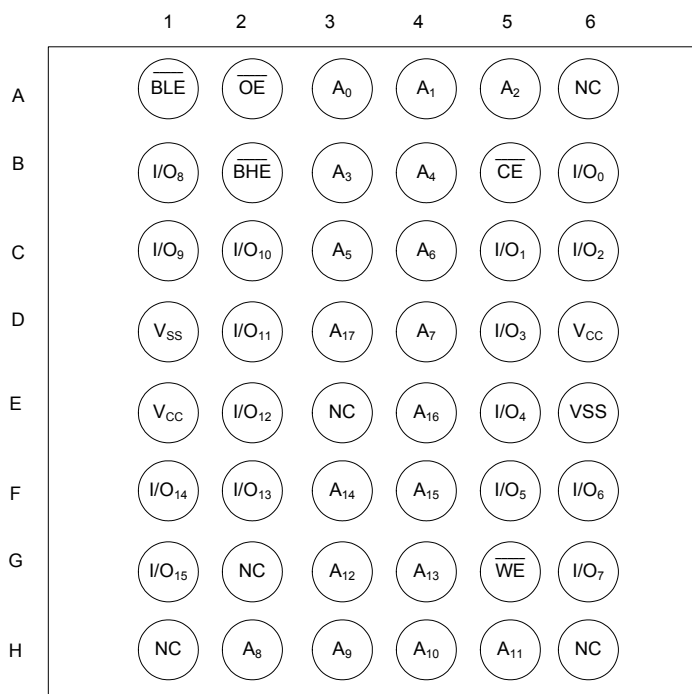


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## Pin Configuration

**Figure 1. 48 ball BGA pinout** <sup>[1]</sup>



## Selection Guide

Description		-10	Unit
Maximum access time		10	ns
Maximum operating current	Automotive-E	130	mA
Maximum CMOS standby current	Automotive-E	15	mA

### Note

1. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  relative to GND <sup>[2]</sup> ..... -0.5 V to +4.6 V

DC voltage applied to outputs in High Z state <sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage <sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... > 2001 V

Latch up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature ( $T_A$ )	$V_{CC}$
Automotive-E	-40 °C to +125 °C	3.3 V $\pm$ 10%

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		Unit
				Min	Max	
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = −4.0 mA		2.4	–	V
V <sub>OL</sub>	Output LOW voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA		–	0.4	V
V <sub>IH</sub>	Input HIGH voltage			2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW voltage <sup>[2]</sup>			−0.3	0.8	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Automotive-E	−20	+20	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output disabled	Automotive-E	−20	+20	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Automotive-E	–	130	mA
I <sub>SB1</sub>	Automatic CE power down current – TTL Inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Automotive-E	–	45	mA
I <sub>SB2</sub>	Automatic CE power down current – CMOS inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0	Automotive-E	–	15	mA

### Note

2.  $V_{IL}(\text{min}) = -2.0 \text{ V}$  for pulse durations of less than 20 ns.

## Capacitance

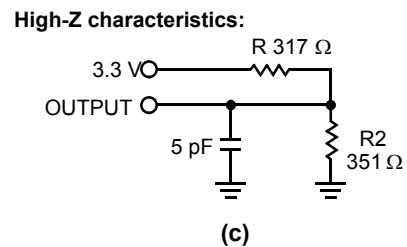
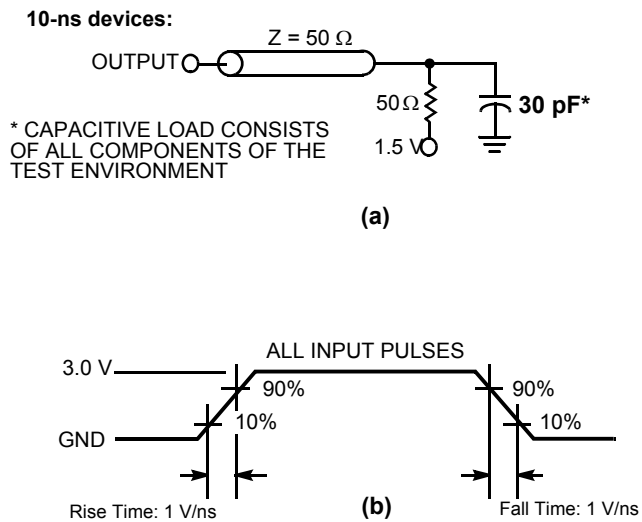
Parameter <sup>[3]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V	8	pF
C <sub>OUT</sub>	Output capacitance		8	pF

## Thermal Resistance

Parameter <sup>[3]</sup>	Description	Test Conditions	48-ball BGA	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	38.15	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		9.15	°C/W

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms <sup>[4]</sup>



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) for 10-ns parts are tested using the load conditions shown in Figure 2 (a). High Z characteristics are tested using the test load shown in Figure 2 (c).

## Switching Characteristics

Over the Operating Range

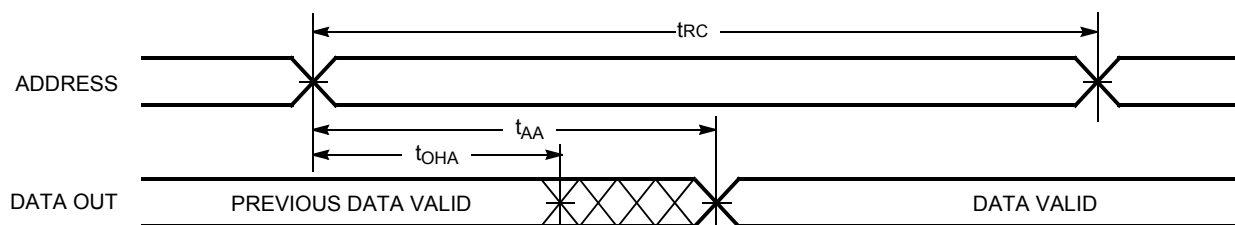
Parameter <sup>[5]</sup>	Description	-10		Unit
		Min	Max	
Read Cycle				
t <sub>power</sub> <sup>[6]</sup>	V <sub>CC</sub> (typical) to the first access	100	–	μs
t <sub>RC</sub>	Read cycle time	10	–	ns
t <sub>AA</sub>	Address to data valid	–	10	ns
t <sub>OHA</sub>	Data hold from address change	3	–	ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to data valid	–	10	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to data valid	–	6	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to Low Z <sup>[7]</sup>	0	–	ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High Z <sup>[7, 8]</sup>	–	5	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to Low Z <sup>[7]</sup>	3	–	ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to High Z <sup>[7, 8]</sup>	–	5	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ LOW to power up	0	–	ns
t <sub>PD</sub>	$\overline{\text{CE}}$ HIGH to power down	–	10	ns
t <sub>DBE</sub>	Byte enable to data valid	–	6	ns
t <sub>LZBE</sub>	Byte enable to Low Z	0	–	ns
t <sub>HZBE</sub>	Byte disable to High Z	–	6	ns
Write Cycle <sup>[9, 10]</sup>				
t <sub>WC</sub>	Write cycle time	10	–	ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to write end	7	–	ns
t <sub>AW</sub>	Address setup to write end	7	–	ns
t <sub>HA</sub>	Address hold from write end	0	–	ns
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ pulse width	7	–	ns
t <sub>SD</sub>	Data setup to write end	5	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low Z <sup>[7]</sup>	3	–	ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High Z <sup>[7, 8]</sup>	–	5	ns
t <sub>BW</sub>	Byte enable to end of write	7	–	ns

### Notes

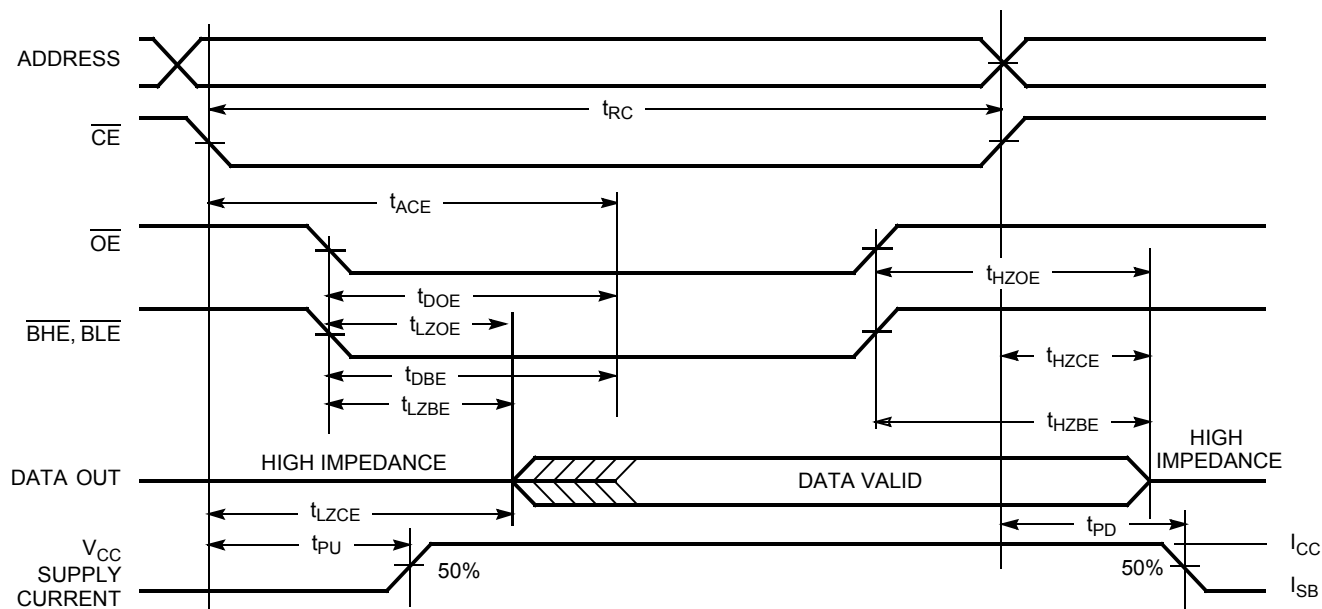
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V.
- $t_{\text{POWER}}$  gives the minimum amount of time that the power supply is at typical  $V_{\text{CC}}$  values until the first memory access is performed.
- At any temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any device.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZBE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (c) of [Figure 2 on page 5](#). Transition is measured  $\pm 500$  mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW,  $\overline{\text{WE}}$  LOW, and  $\overline{\text{BHE/BLE}}$  LOW.  $\overline{\text{CE}}$ ,  $\overline{\text{WE}}$ , and  $\overline{\text{BHE/BLE}}$  must be LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Switching Waveforms

**Figure 3. Read Cycle No. 1 (Address Transition Controlled)** [11, 12]

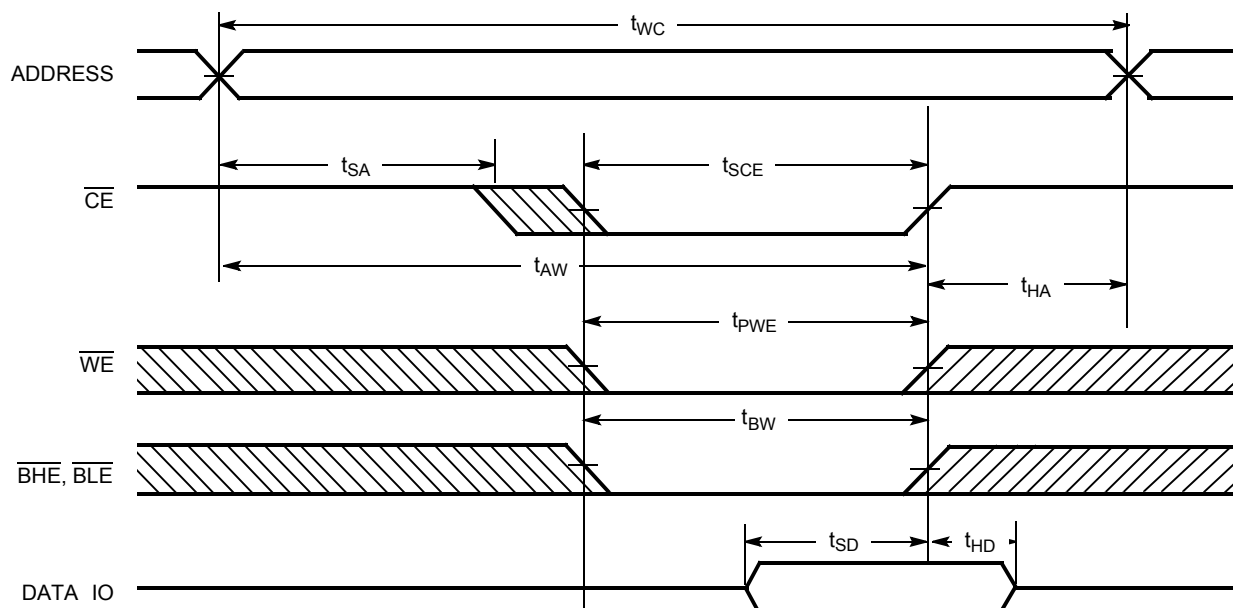
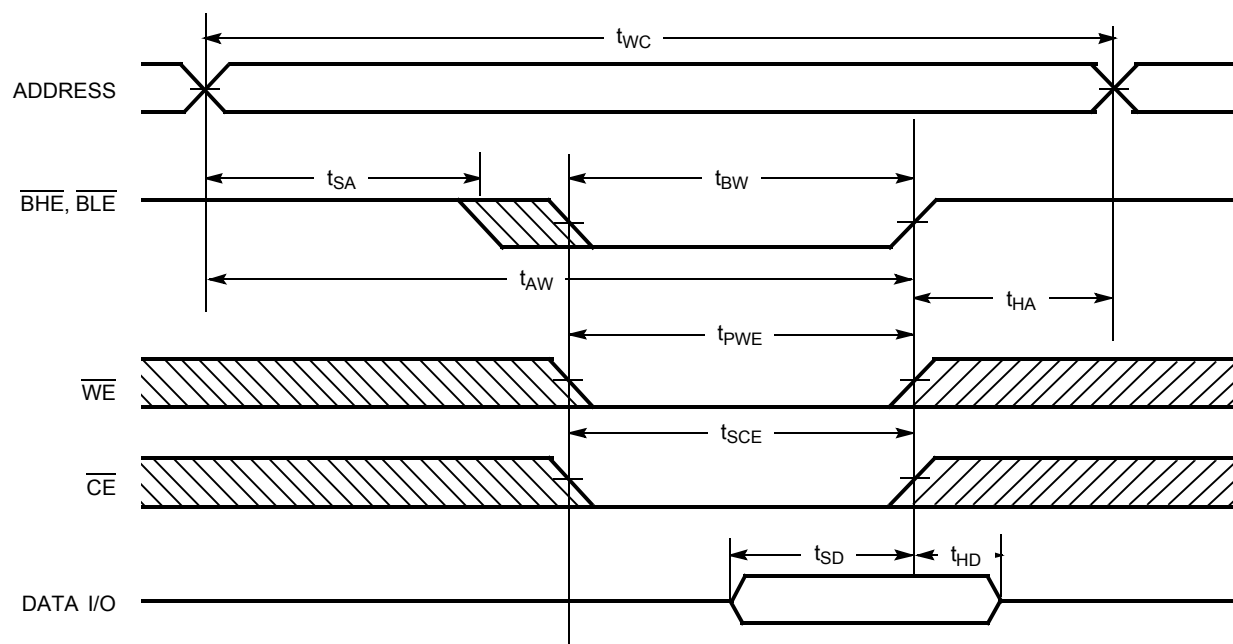


**Figure 4. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)** [12, 13]



### Notes

11. Device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}$ ,  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}} = V_{\text{IL}}$ .
12.  $\overline{\text{WE}}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.

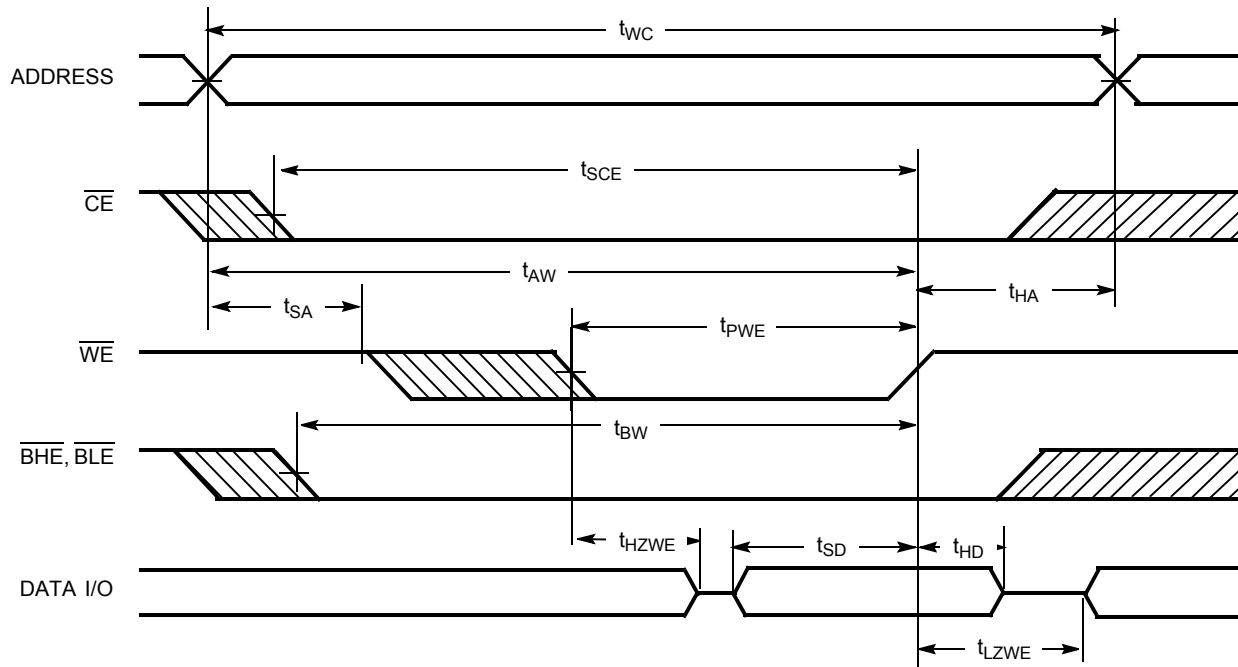
**Switching Waveforms (continued)**
**Figure 5. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [14, 15]**

**Figure 6. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

**Notes**

 14. Data I/O is high impedance if  $\overline{\text{OE}}$ ,  $\overline{\text{BHE}}$ , and/or  $\overline{\text{BLE}}$  =  $V_{IH}$ .

 15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high impedance state.

**Switching Waveforms** (continued)

**Figure 7. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled, LOW)**





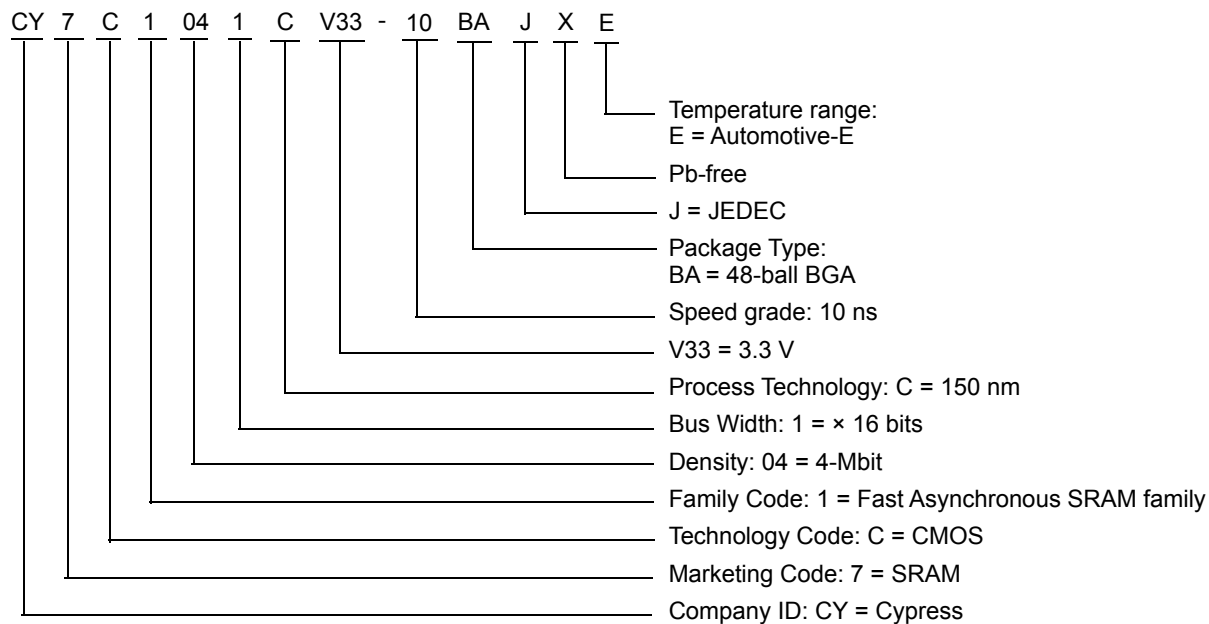
**Truth Table**

CE	OE	WE	BLE	BHE	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read – all bits	Active ( $I_{CC}$ )
L	L	H	L	H	Data Out	High Z	Read – lower bits only	Active ( $I_{CC}$ )
L	L	H	H	L	High Z	Data Out	Read – upper bits only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write – all bits	Active ( $I_{CC}$ )
L	X	L	L	H	Data In	High Z	Write – lower bits only	Active ( $I_{CC}$ )
L	X	L	H	L	High Z	Data In	Write – upper bits only	Active ( $I_{CC}$ )
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active ( $I_{CC}$ )

## Ordering Information

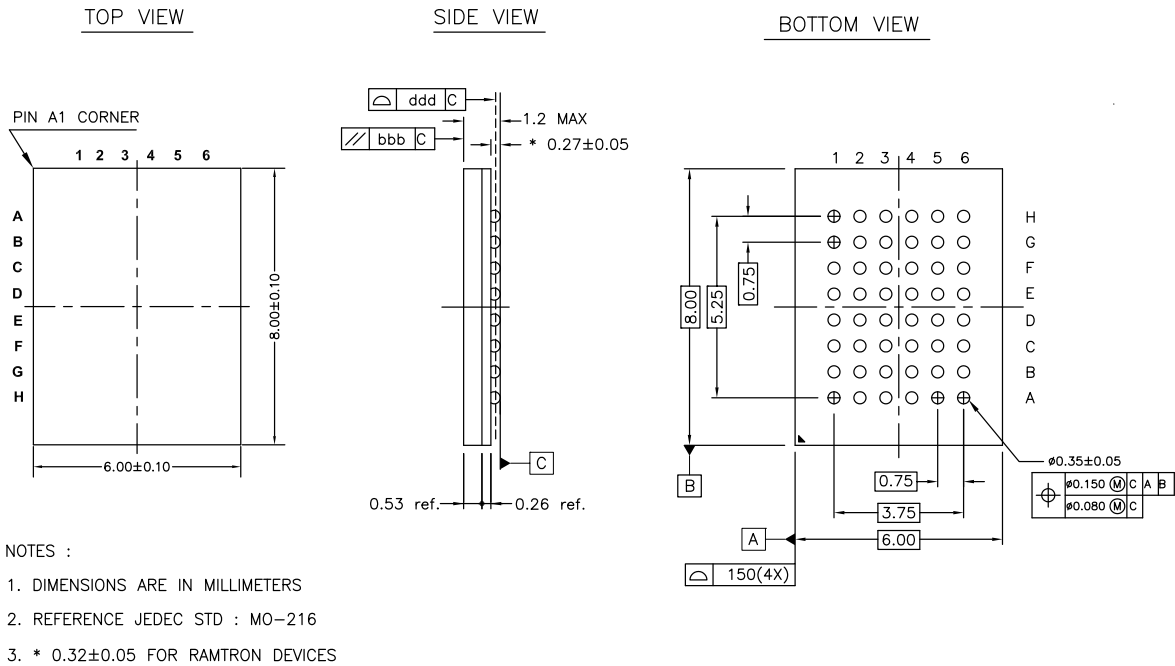
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1041CV33-10BAJXE	001-85259	48-ball BGA (Pb-free)	Automotive-E

## Ordering Code Definitions



## Package Diagrams

**Figure 8. 48-ball FBGA (6 × 8 × 1.2 mm) BA48M/BK48M (0.35 mm Ball Diameter) Package Outline, 001-85259**



001-85259 \*A

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
mW	milliwatt
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1041CV33 Automotive, 4-Mbit (256 K × 16) Static RAM Document Number: 001-86495				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3925192	TAVA	04/04/2013	New data sheet.
*A	4103029	MEMJ	08/23/2013	Changed status from Preliminary to Final.  Updated <a href="#">Ordering Information</a> : No change in part numbers. Replaced "51-85087" with "001-85259" in "Package Diagram" column.  Updated <a href="#">Package Diagrams</a> : spec 001-85259 – Changed revision from ** to *A.  Updated in new template.
*B	4396000	VINI	06/02/2014	No technical updates.  Completing Sunset Review.
*C	4724503	PSR	04/14/2015	Updated <a href="#">Functional Description</a> : Added "For a complete list of related resources, <a href="#">click here</a> ." at the end. Updated to new template. Completing Sunset Review.
*D	6003585	AESATP12	12/22/2017	Updated logo and copyright.

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